Vertex Tracker Detector

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On behalf of the study group

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CEPC Physics and Detector CDR International Review

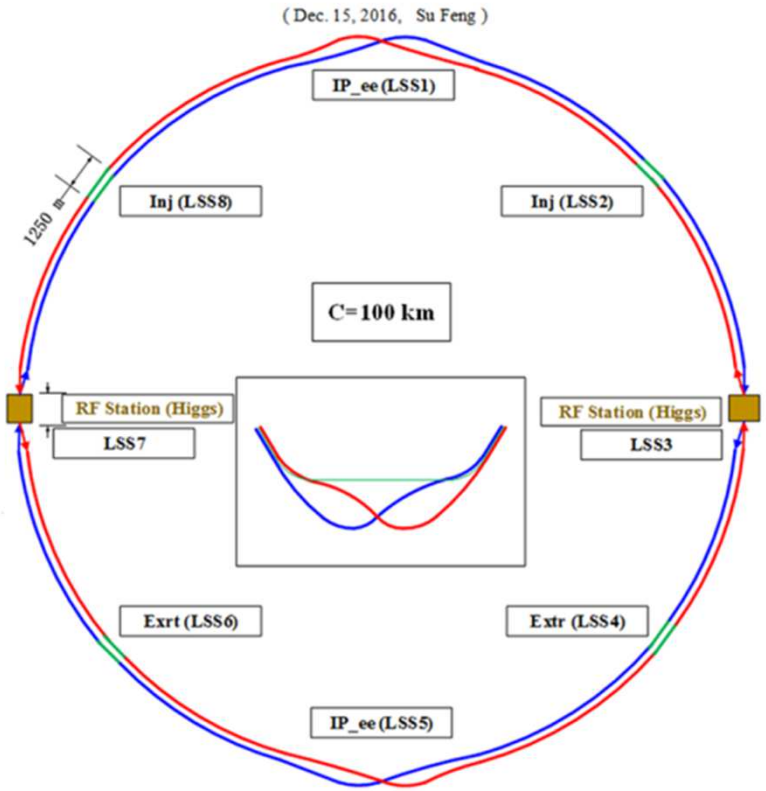
Outline:

- *Requirements and challenges*
- *Baseline design and performance studies*
- *Sensor technology options*
- *Mechanics and Integration*
- *R&D activities*
- *Summary*

Reminder: CEPC Beam Timing

Circular e^+e^- Higgs (Z) factory **two detectors, 1M ZH events in 10yrs**

E_{cm}≈240GeV, luminosity ~2×10^{34} $cm^{-2}s^{-1}$, (1.6×10^{35} $cm^{-2}s^{-1}$ at the Z-pole)



Bunch spacing 0.68 μs @ H(240)

0.21 μs @ W(160)

25 ns @ Z(91)

Fully Partial Double Ring - 100Km

Vertex Detector Requirements

- Efficient tagging of heavy quarks (b/c) and τ leptons

  ⟶ impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\,(\mu m)$$

- Detector system requirements:
  - σ_{SP} near the interaction point: *<3 μm* ⟶ ~16μm pixel pitch
  - material budget: *≤ 0.15%X $_0$/layer* ⟶ power consumption < 50mW/cm^2 , if air cooling used
  - first layer located at a radius: *~1.6 cm*
  - pixel occupancy: *≤ 1 %* ⟶ ~ μs level readout

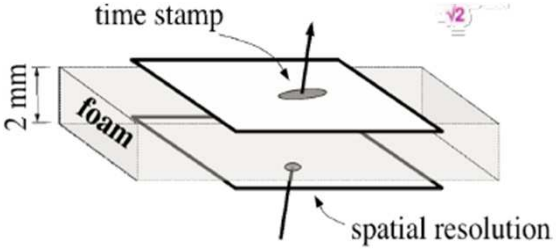
* Radiation tolerance: see slide 8

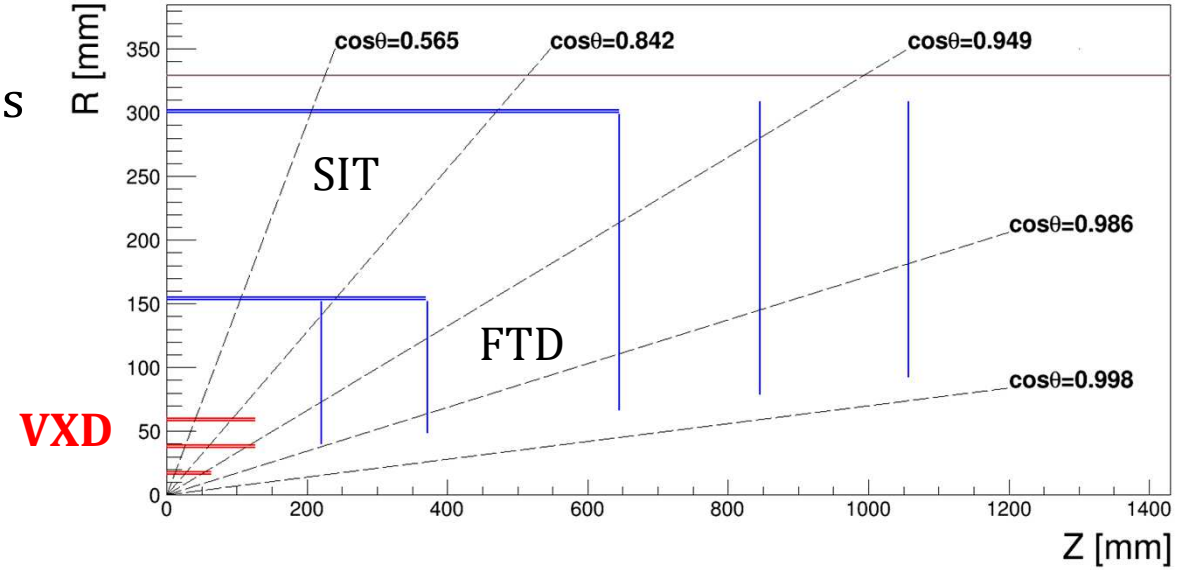
* Time stamp: needed for short bunch spacing

Baseline Vertex Detector Layout

VXD: *B=3T*

- 3 layers of double-sided pixels
- σ_{SP}=2.8μm in L1
- Faster pixel sensor in L2, to provide time-stamp
- Polar angle θ~15 degrees



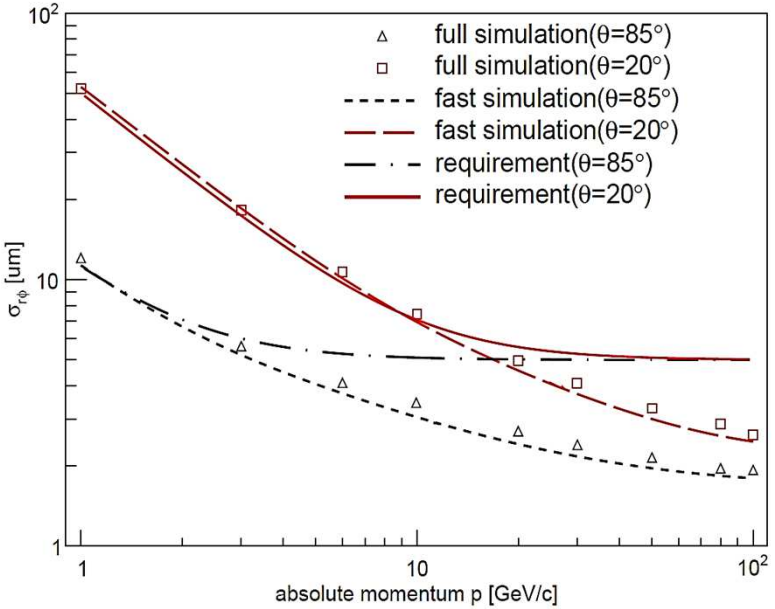


VXD parameters

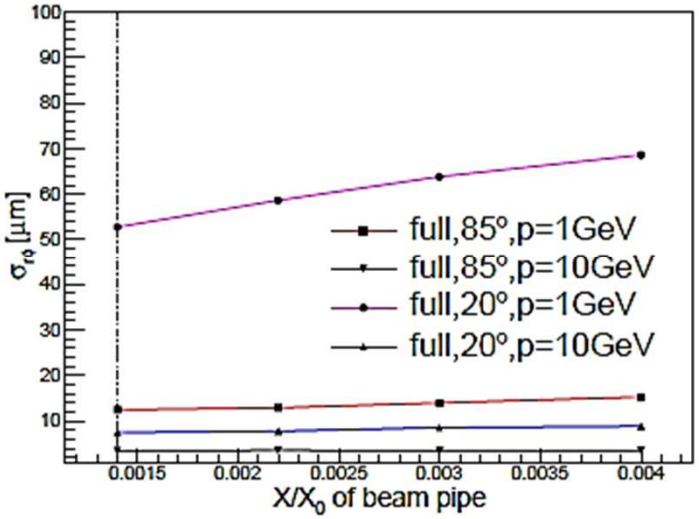
	R (mm)	|z| (mm)	|cos θ|	σ_{sp} (μm)
Layer 1	**16**	**62.5**	**0.97**	**2.8**
Layer 2	**18**	**62.5**	**0.96**	**6**
Layer 3	**37**	**125.0**	**0.96**	**4**
Layer 4	**39**	**125.0**	**0.95**	**4**
Layer 5	**58**	**125.0**	**0.91**	**4**
Layer 6	**60**	**125.0**	**0.90**	**4**

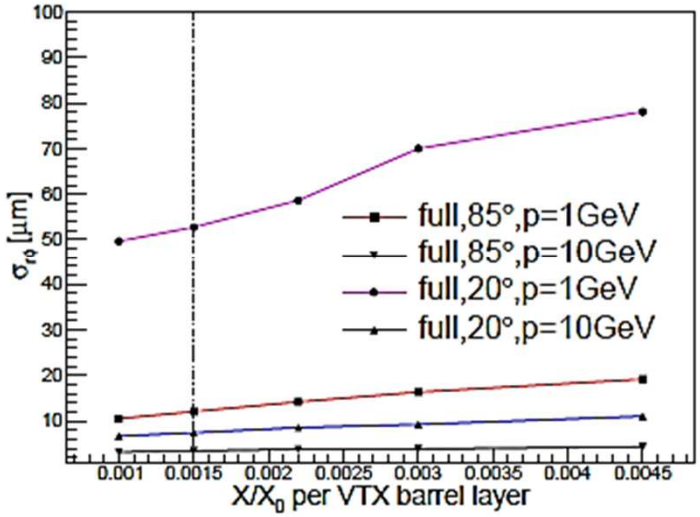
Performance Studies – IP Resolution

Performance of the baseline configurations with fast and full simulation

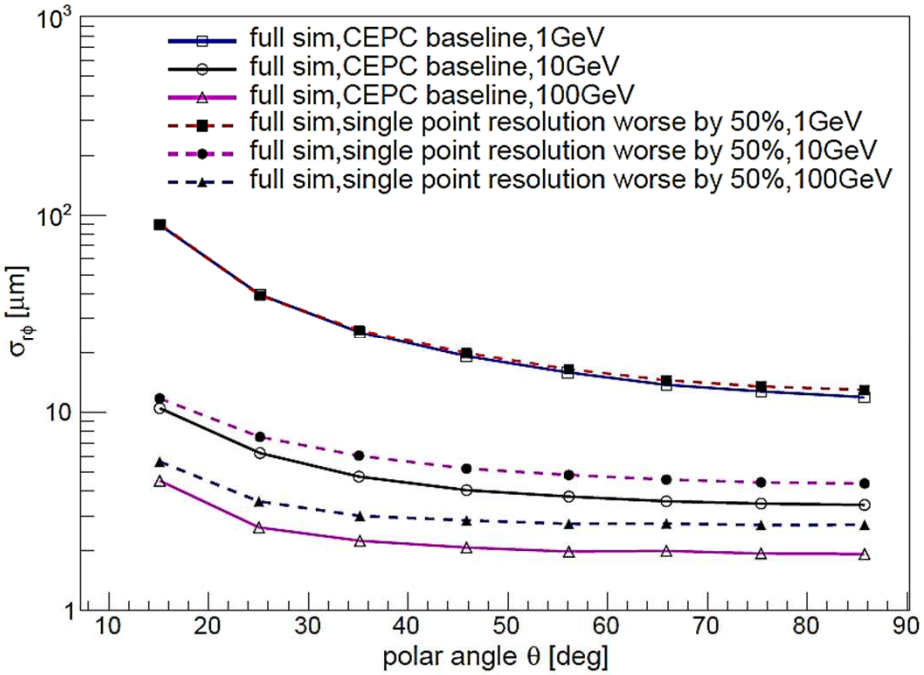


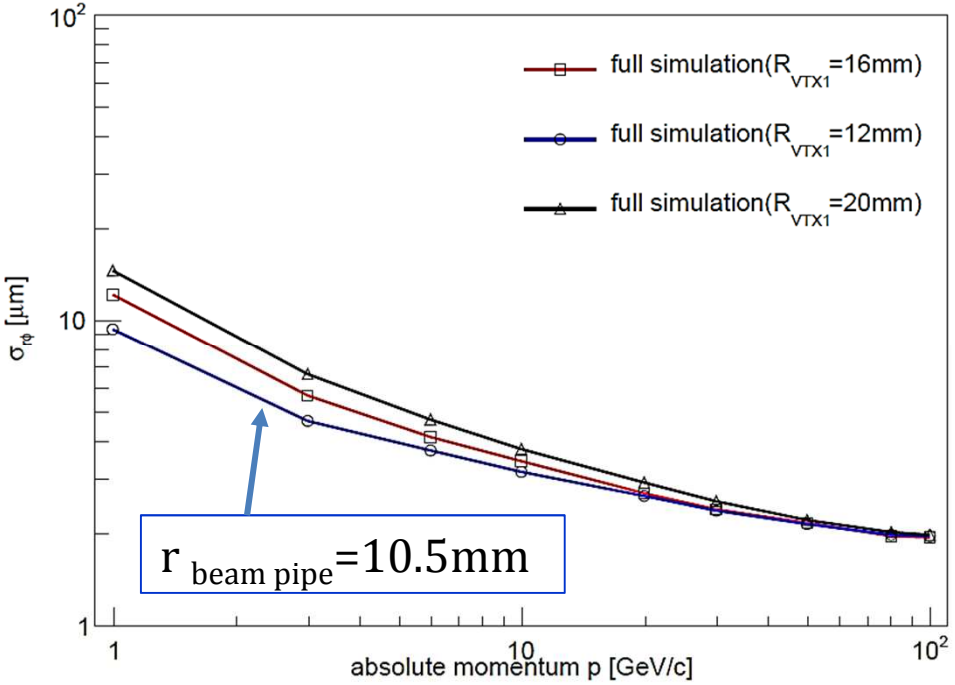
Sensitivity to material budget with full simulation





Performance Studies – IP Resolution





Sensitivity to single-point resolution and innermost radius with full simulation

Beam-Induced Radiation Backgrounds

	H (240)	W (160)	Z (91)
Hit Density [hits/cm^2·BX]	2.4	2.3	0.25
TID [MRad/year]	0.93	2.9	3.4
NIEL [10^{12} 1 MeV n_{eq}/cm^2·year]	2.1	5.5	6.2

Radiation level

Table 9.4: Summary of hit density, total ionizing dose (TID) and non-ionizing energy loss (NIEL) with combined contributions from pair production and off-energy beam particles, at the first vertex detector layer ($r = 1.6$ cm) at different machine operation energies of $\sqrt{s} = 240$, 160 and 91 GeV, respectively.

	H(240)	W(160)	Z(91)
Hit density (hits · cm^{-2} · BX^{-1})	2.4	2.3	0.25
Bunching spacing (μs)	0.68	0.21	0.025
Occupancy (%)	0.08	0.25	0.23

Table 4.2: Occupancies of the first vertex detector layer at different machine operation energies: 240 GeV for ZH production, 160 GeV near W-pair threshold and 91 GeV for Z-pole.

detector occupancy <1%, assuming 10 μs of readout time for the silicon pixel sensor and an average cluster size of 9 pixels per hit.

Sensor Technology Options

Technology	Examples	Small pixels	Low mass	Low power	Fast timing
Monolithic CMOS MAPS	Mimosa CPS	++	++	**++**	-
Integrated sensor/amplif. + separate r/o	DEPFET, FPCCD	+/++	o	+	-
Monolithic CMOS with depletion	HV-CMOS, HR-CMOS	+	++	**o**	**+**
3D integrated	Tezzaron, SOI	++	+	o	++
Hybrid	CLICpix+planar sensor, HV-CMOS hybrid	+	o	+	++

Ref: Recent developments in LC vertex and tracking R&D，Dominik Dannheim，LCWS 2015

Many technologies from ILC/CLIC could be referred.
BUT, unlike the ILD/CLIC, the CEPC detector will operate in continuous mode. → **without power-pulsing**

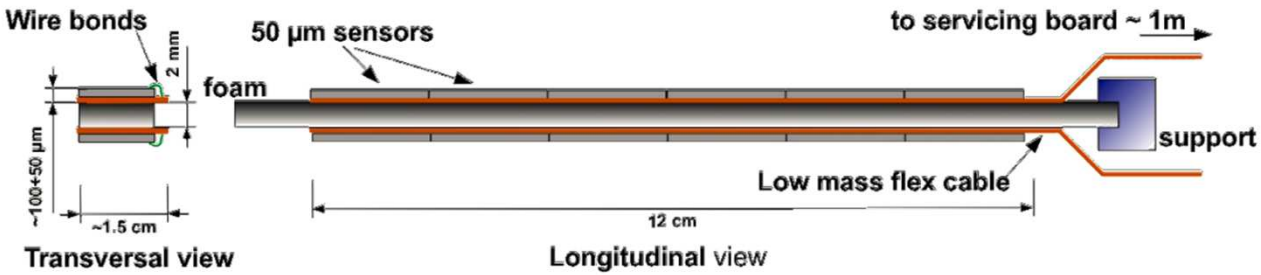
Sensor Technology Options

Possible technologies for CEPC vertex

- HR-CMOS sensor with a novel readout structure (ALPIDE @ ALICE-ITS upgrade)
  - relatively mature technology
  - <50mW/cm^2 expected
  - Capable of readout every ~4μs
- SOI sensor with similar readout structure
  - Fully depleted HR substrate, potential of 16μm pixel size design
  - Full CMOS circuit
- DEPFET: possible application for inner most vertex layer
  - small material budget, low power consumption in sensitive area
- 3D-IC: ultimate detector, but not mature enough

Mechanics and Integration

- Double-sided ladder
  - PLUME design concept
- Cooling
  - to be considered



Vertex detector	Power dissipation	Cooling method	Material budget requirement/layer
Alice ITS	300 mW/cm^2	water	0.3%
STAR PXL	170 mW/cm^2	air	0.39%
ILD vertex	< 120 mW/cm^2 (CPS and DEPFET)	air or N_2	0.15%
	35 W inside cryostat (FPCCD)	two-phase CO_2	
BELLE-II PXD	20 W for sensor and SWITCHER	Air	0.2%
	180 W on each end	CO_2	

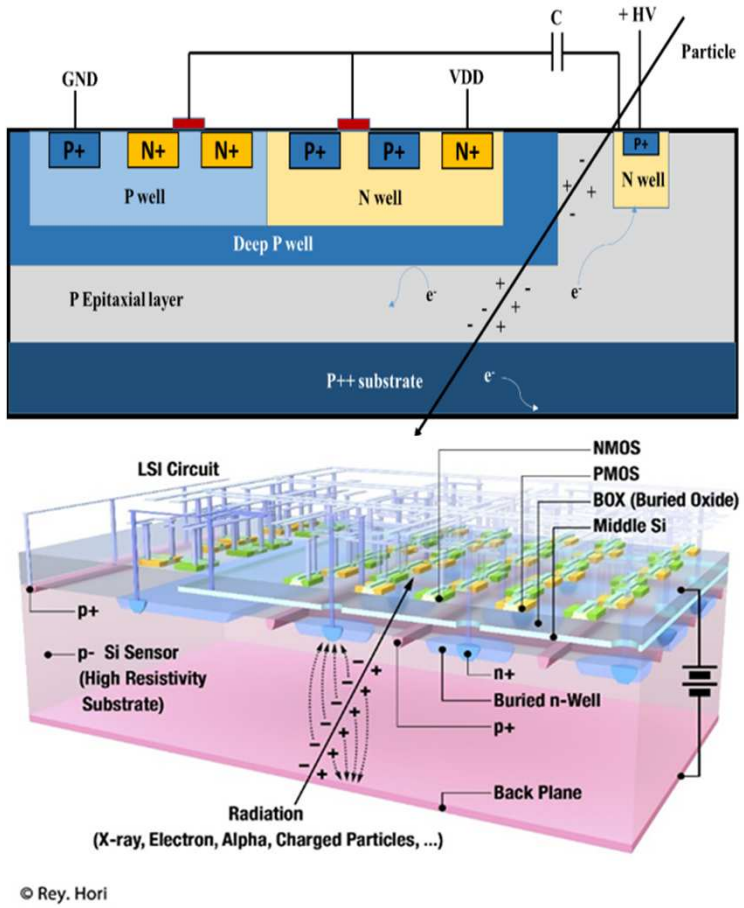
Table 4.3: Cooling methods for several vertex detector designs. The chip power dissipation, coolant type and corresponding material budget requirement per sensor layer are indicated. The active CO_2 cooling adds additional material in the forward region, outside the sensitive area. For the ILD FPCCD option, this additional material budget is 0.3% X_0 averaged over the end-plate region, while for the BELLE-II PXD, it is $\sim 0.1 - 0.2\%\, X_0$ per layer.

R&D Activities in China

Initial sensor R&D targeting on

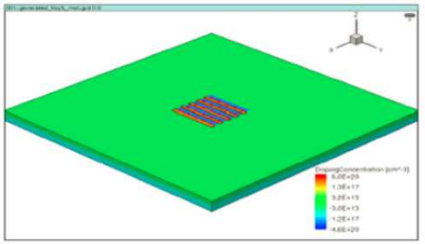
- *Pixel single point resolution <3 - 5μm*
- *Power consumption at the current level <100mW/cm²*
- *Integration time 10-100μs*

- Two monolithic pixel technologies
- CMOS pixel sensor (CPS)
  - *TowerJazz CIS 0.18 μm process*
  - *Quadruple well process*
  - *Thick (~20 μm) epitaxial layer*
  - *with high resistivity (≥1 kΩ•cm)*
- SOI pixel sensor
  - *LAPIS 0.2 μm process*
  - High resistive substrate (≥1 kΩ•cm)
  - Double SOI layers available
  - Thinning and backside process



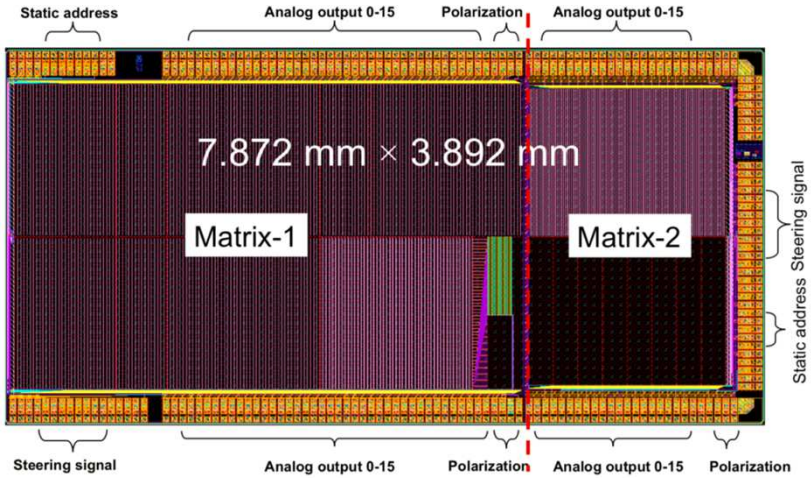
CMOS Pixel Sensor – 1st Design

- **Sensor design & TCAD simulation** Y.Zhang, et al, NIMA 831(2016)99-104
  - Different sensor diode geometries, epitaxial-layer properties and radiation damage



- **JadePix1 submission in Nov. 2015** Y. Zhang, Y.Zhou, et al (IHEP, SDU)
  - Exploratory prototype, analog pixel, rolling shutter readout mode
  - Sensor optimization and radiation tolerance study
  - sensing node AC-coupled to increase biased voltage

- **Sensor characterization**
  - Noise level
  - Charge collection efficiency
  - Irradiation with Neutron
  - Test beam in Aug. 2018



CMOS Pixel Sensor – 2nd Design

Design goal: digital readout pixel sensor with

- *Single point resolution better than 5μm*
- *Power consumption <80 mW/cm²*
- *Integration time < 100μs*

Technology: *TowerJazz CIS 0.18 μm process*

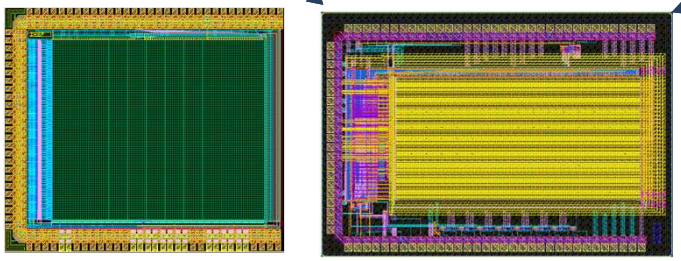
Joint effort of CCNU and IHEP

Design submission in May 2017

- Tow prototypes with digital pixels (in-pixel discriminator)
- Tow different readout schemes: rolling shutter & asynchronous

JadePix2: Y.Zhou (IHEP)

- Pixel size: 22μm×22μm
- Two different pixel version with higher biased voltage
- Test in lab ongoing



MIC4: P.Yang(CCNU)
Y.Zhou (IHEP)

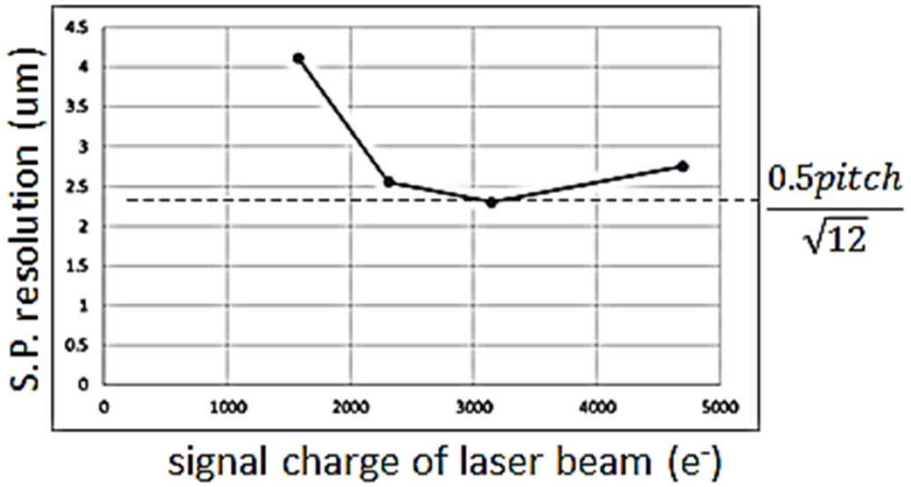
- Pixel size: 25μm×25μm
- Two different pixel front-end with Matrix readout architecture
- Test in lab ongoing

R&D Activities - SOI Pixel Sensor

- **First submission (CPV1) in June 2015** — Y. Lu (IHEP)
  - 16*16 μm with in-pixel-discrimination
  - Double-SOI process for shielding and radiation enhancement
- **Second submission (CPV2) in June 2016** — Y. Lu, Y.Zhou (IHEP)
  - In-pixel CDS stage inserted
  - To improve RTC and FPN noise
  - To replace the charge injection threshold

CPV2 performance

- *Thinned down to 75um thick*
- *Temporal noise ~6e$^-$*
- *Threshold dispersion (FPN) ~114e$^-$*
- *Single point resolution measurement under infrared laser beam*



Future Plan on R&D

- Further optimization study of vertex system
- Novel readout scheme exploration
- Large area pixel array design
- Radiation hardness and time-stamp sensor design
- Prototype development
- Small (16μm×16μm) pixel, targeting on 3μm single point resolution
  - To explore 3D connection technology by designing the in-pixel digital logic in a separated tier
  - Or to look for any new process

Summary

- CDR finished with baseline design
- Critical technologies listed
- R&D project started along the baseline design specifications
  - *in-pixel electronics, small pixel size*
  - *new asynchronous readout architecture*
- Collaboration with international teams
- Going to TDR for next step
- Expertise demanding

Many thanks to all members of CEPC Physics and Detector working group who made significant efforts to prepare the CDR !

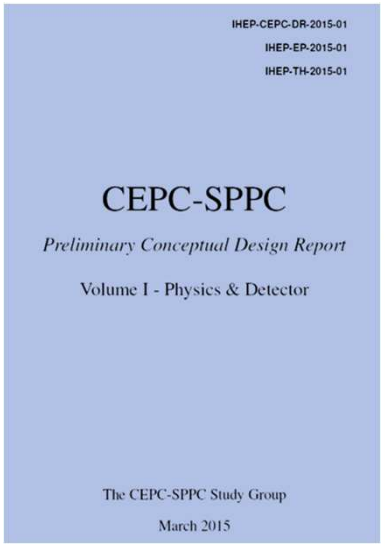
Thank you for your attention!

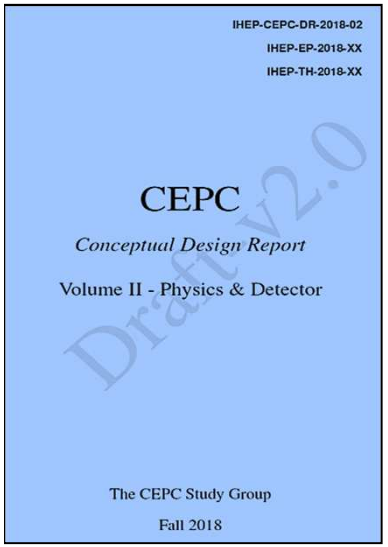
CEPC CDR Parameters

D. Wang

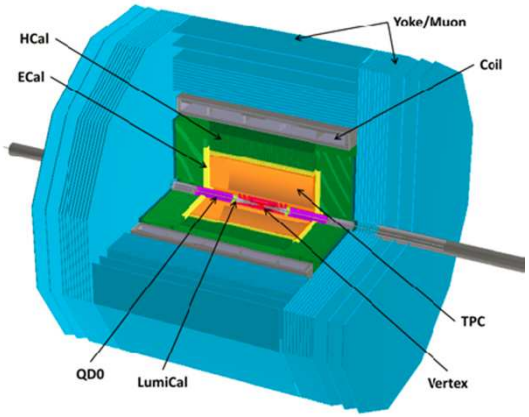
	Higgs	*W*	*Z（3T）*	*Z（2T）*
Number of IPs	2			
Beam energy (GeV)	120	80	45.5	
Circumference (km)	100			
Synchrotron radiation loss/turn (GeV)	1.73	0.34	0.036	
Crossing angle at IP (mrad)	16.5×2			
Piwinski angle	2.58	7.0	23.8	
Number of particles/bunch N_e (10^{10})	15.0	12.0	8.0	
Bunch number (bunch spacing)	242 (0.68μs)	1524 (0.21μs)	12000 (25ns+10%gap)	
Beam current (mA)	17.4	87.9	461.0	
Synchrotron radiation power /beam (MW)	30	30	16.5	
Bending radius (km)	10.7			
Momentum compact (10^{-5})	1.11			
β function at IP β_x^* / β_y^* (m)	0.36/0.0015	0.36/0.0015	0.2/0.0015	0.2/0.001
Emittance $\varepsilon_x/\varepsilon_y$ (nm)	1.21/0.0031	0.54/0.0016	0.18/0.004	0.18/0.0016
Beam size at IP σ_x/σ_y (μm)	20.9/0.068	13.9/0.049	6.0/0.078	6.0/0.04
Beam-beam parameters ξ_x/ξ_y	0.031/0.109	0.013/0.106	0.0041/0.056	0.0041/0.072
RF voltage V_{RF} (GV)	2.17	0.47	0.10	
RF frequency f_{RF} (MHz) (harmonic)	650 (216816)			
Natural bunch length σ_z (mm)	2.72	2.98	2.42	
Bunch length σ_z (mm)	3.26	5.9	8.5	
Betatron tune ν_x/ν_y	363.10 / 365.22			
Synchrotron tune ν_z	0.065	0.0395	0.028	
HOM power/cavity (2 cell) (kw)	0.54	0.75	1.94	
Natural energy spread (%)	0.1	0.066	0.038	
Energy acceptance requirement (%)	1.35	0.4	0.23	
Energy acceptance by RF (%)	2.06	1.47	1.7	
Photon number due to beamstrahlung	0.29	0.35	0.55	
Lifetime _simulation (min)	100			
Lifetime (hour)	0.67	1.4	4.0	2.1
F (hour glass)	0.89	0.94	0.99	
Luminosity/IP L ($10^{34}cm^{-2}s^{-1}$)	2.93	10.1	16.6	32.1

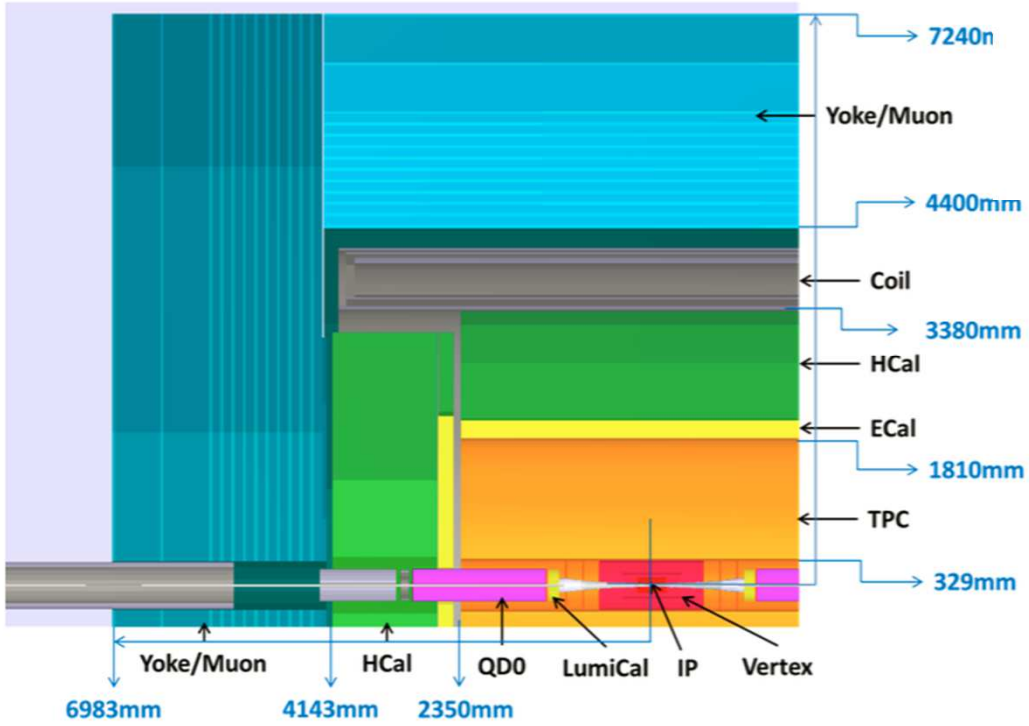
Physics & Detector CDR





- Pre-CDR published in March 2015
- CDR to be published in Oct. 2018





*** Baseline detector** - 3 Tesla— changed from pre-CDR
- L* increased to 2.2 m)

*** ILD-like (similar to pre-CDR)**

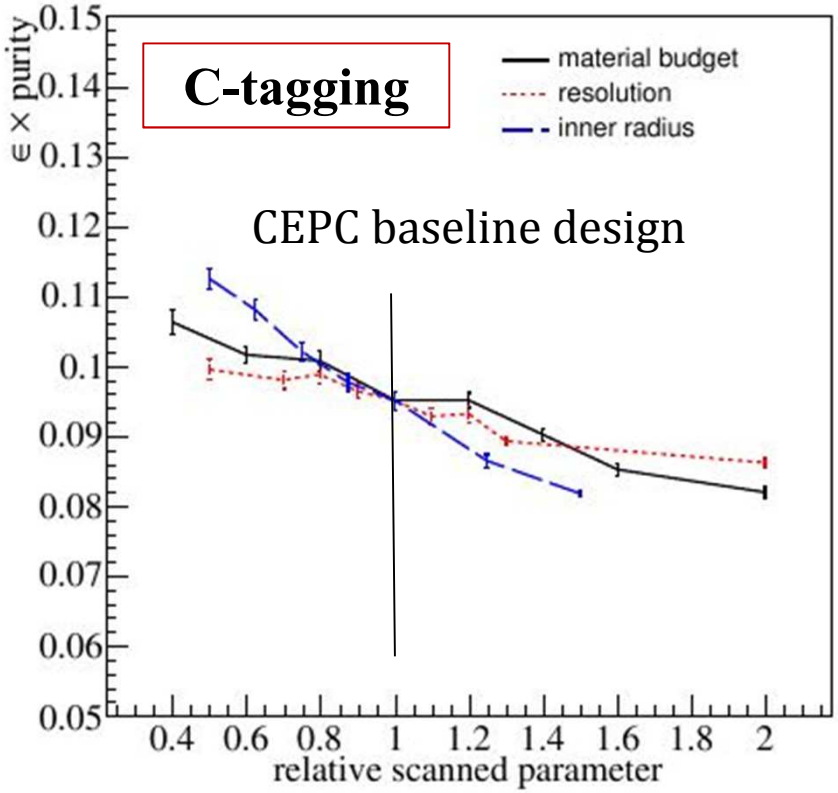
Performance Studies – Flavour Tagging

b-tagging

situations	best	baseline	worst
$\epsilon \cdot$ purity	0.925±0.001	0.914±0.001	0.900±0.001

c-tagging

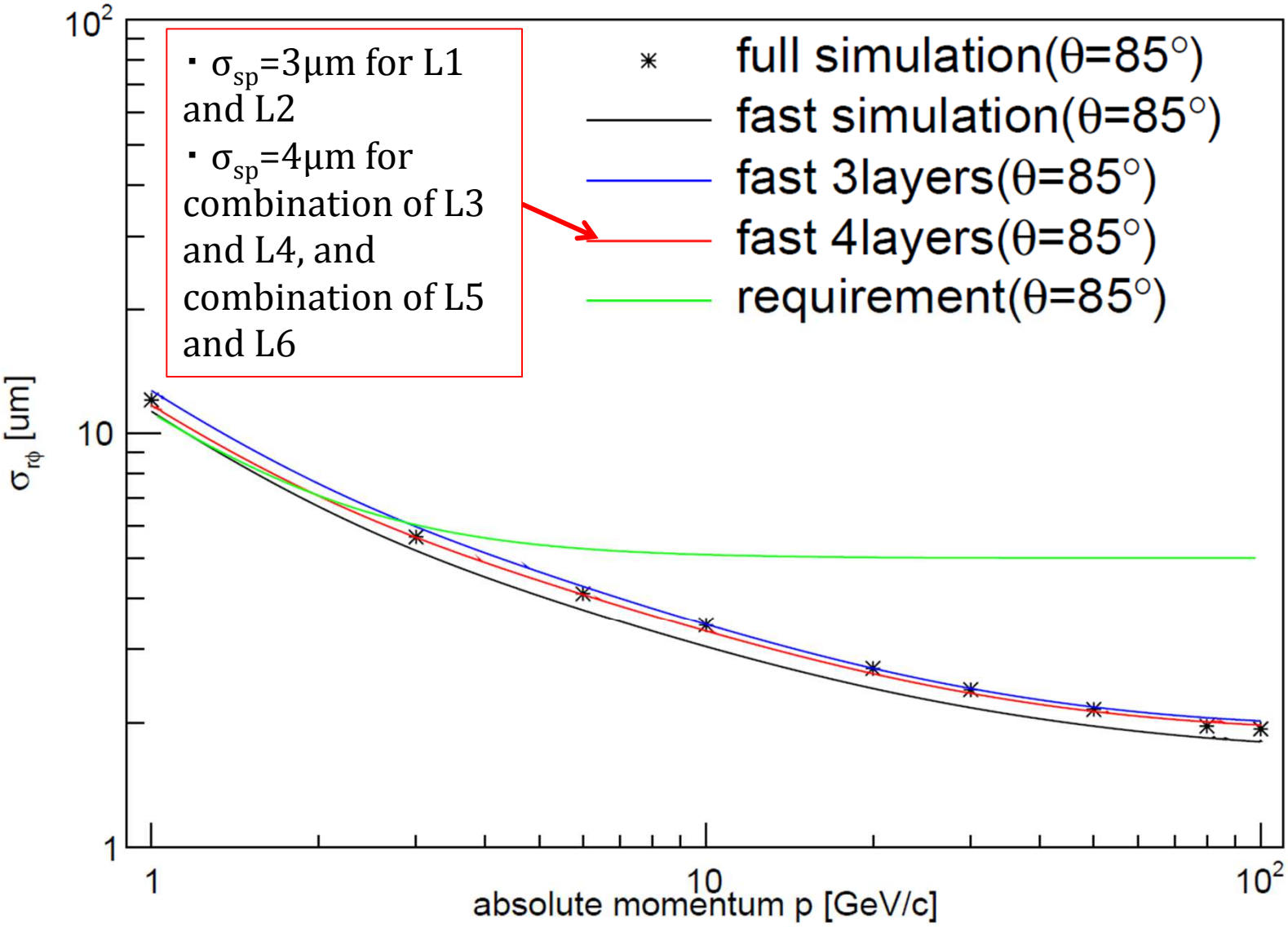
$\epsilon \cdot$ purity	best	baseline	worst
simulation	0.133±0.002	0.095±0.001	0.078±0.001



worst case: with parameters of ALICE ITS upgrade

- material budget： 0.3% X_0/layer
- resolution： 5 μm
- inner radius： 23 mm

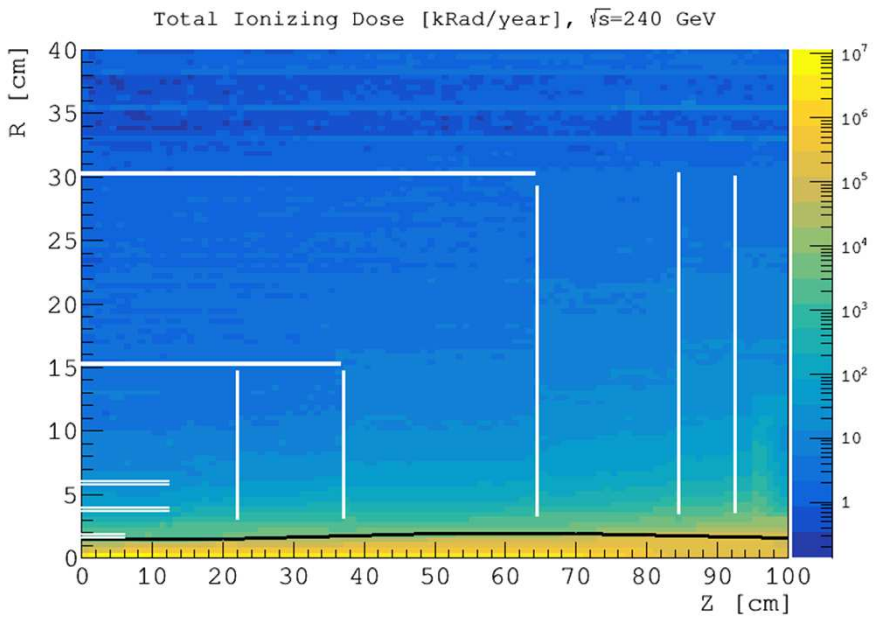
Performance Studies – IP Resolution

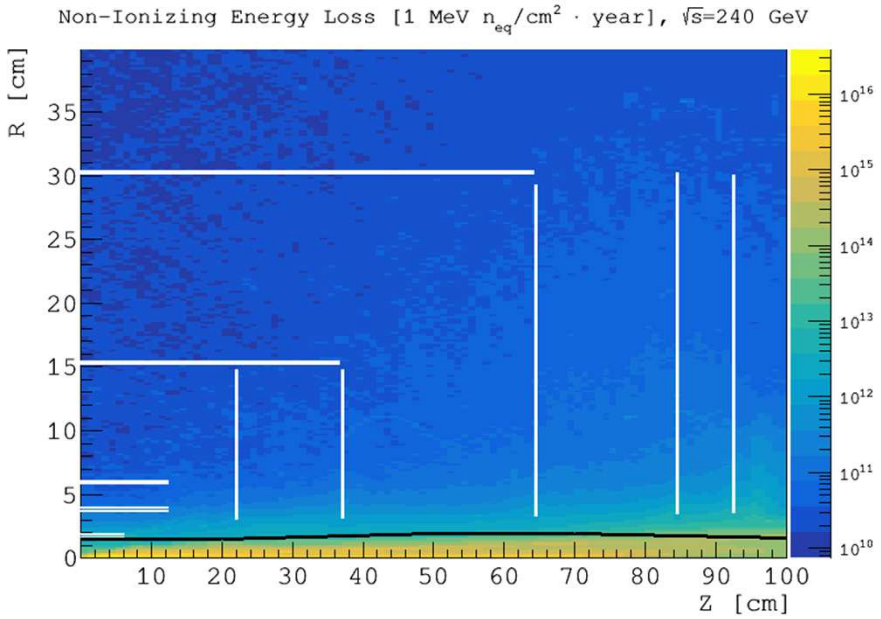


Radiation Background Levels

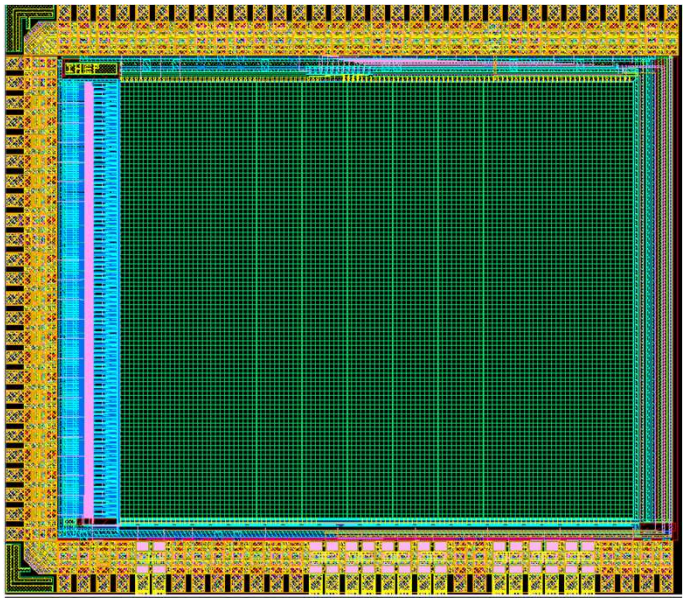
H. Zhu, CEPC Workshop Rome May 24-26 2018

- Using hit density, total ionizing dose (TID) and non-ionizing energy loss (NIEL) to quantify the radiation background levels
- Adopted the calculation method used for the ATLAS background estimation (ATL-GEN-2005-001), safety factor of ×10 applied

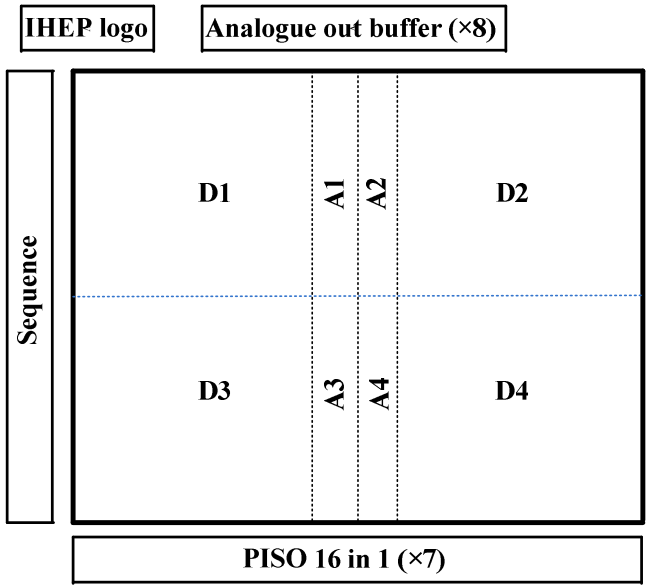




JadePix2: Rolling - shutter Mode



Details in Yang Zhou's presentation



Two different pixel versions:

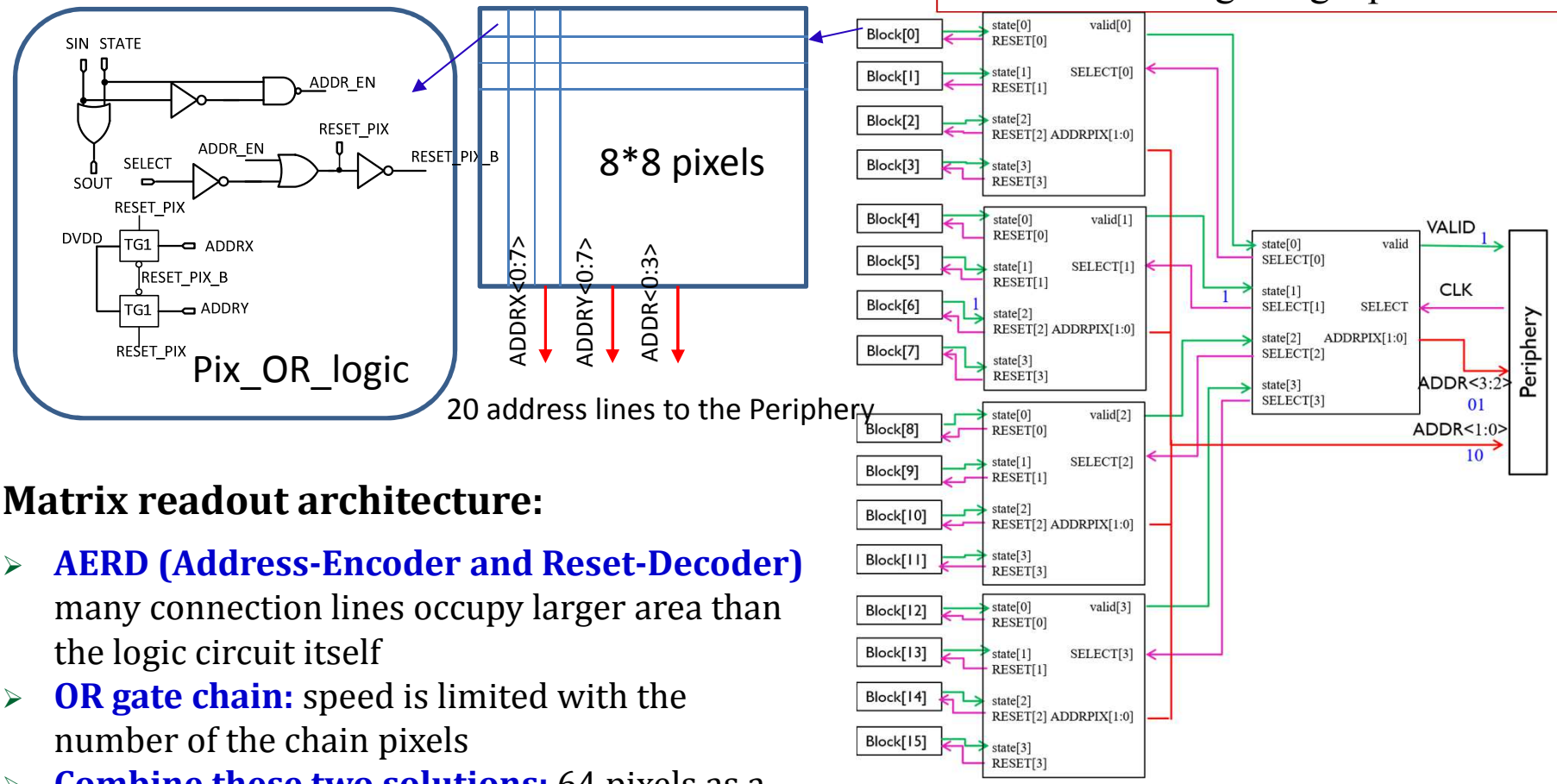
- Pixel size: 22μm×22μm
- Same amount of transistors;
- Offset cancellation technique;
- Version 2 has higher signal gain, but suffers "more" from "Latch" input voltage distortion.

Chip features:

- 3×3.3 mm^2
- 96×112 pixels with 8 sub-matrix
- Processing speed: 11.2μs/frame with 100 ns/row
- Output data speed: 160 MHz
- Power: 3.7μA/pixel (14.4 mW/cm^2 @pixel matrix)

MIC4 Design: Asynchronous Mode

Details in Ping Yang's presentation



Matrix readout architecture:

- **AERD (Address-Encoder and Reset-Decoder)** many connection lines occupy larger area than the logic circuit itself
- **OR gate chain:** speed is limited with the number of the chain pixels
- **Combine these two solutions:** 64 pixels as a group using OR gate chain, groups using AERD structure to readout

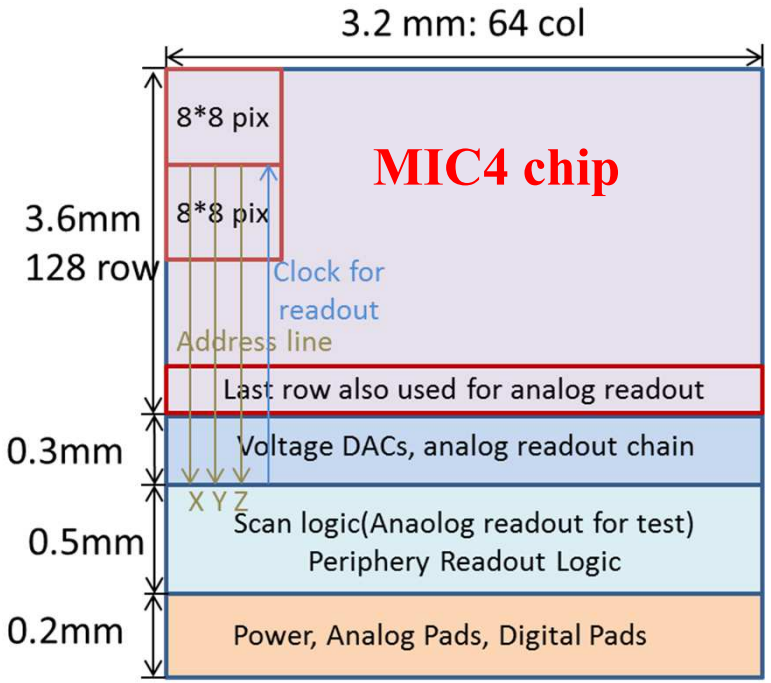
front-end I: ALPIDE structure P. Yang (CCNU)
front-end II: CSA based front-end circuit Y. Zhang (IHEP)

MIC4 Submission: Asynchronous Mode

Y. Zhang (IHEP) & P.Yang (CCNU)

front-end I: Same structure as ALPIDE chip

- ENC: 8 e^-
- Power cons.: 61 nA/pixel
- Threshold: 140 e^-
- Peaking time < 1 us
- Pulse duration < 3 μs



front-end II: CSA based front-end circuit

- Pixel size: 25×25 μm^2
- ENC: 24 e^-
- Power cons.: 50 nW/pixel (8 mW/cm^2 @pixel matrix)
- Threshold: 170 e^-
- Peaking time < 500 ns @ Qin < 1.5 ke^-
- Pulse duration < 9.4 μs @ Qin < 1.5 ke^-

- 3.2 × 3.7 mm^2
- 128 × 64 pixels
- Integration time: < 5 μs/10 μs
- Power consumption: < 80 mW/cm^2
- Chip periphery
  - Band gap
  - Voltage DAC
  - Current DAC
  - Matrix configuration
  - LVDS
  - Custom designed PADs