Silicon Tracker

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Introduction

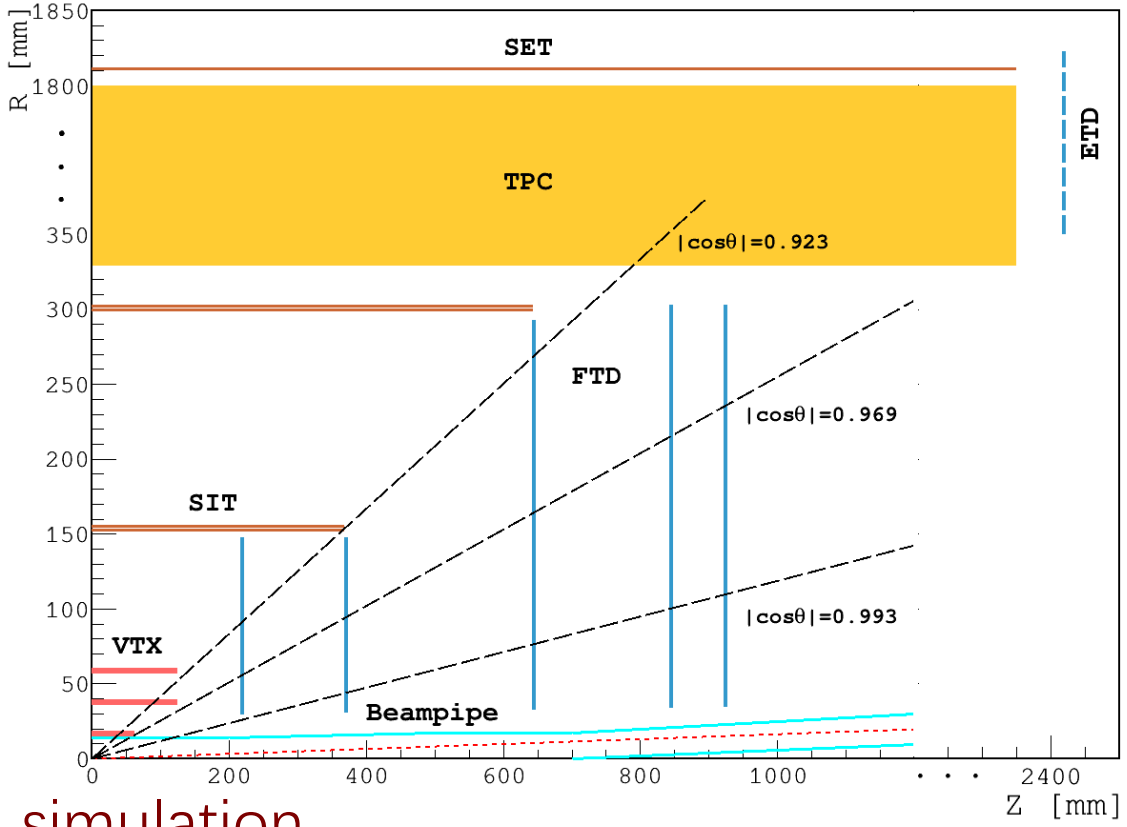
- baseline tracking system: VTX + Silicon Tracker + TPC
- physics requirements on momentum resolution

$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}] \qquad a \sim 2 \times 10^{-5}\,\mathrm{GeV}^{-1} \quad \text{and} \quad b \sim 1 \times 10^{-3}$$

- functionalities
  - monitoring possible field distortion in TPC
  - detector alignment
  - time-stamping to separate events between bunch crossings
  - dE/dx measurement, potentially
- key constraint: material budget

Baseline design – layout

- 4 components
  - SIT – Silicon Inner Tracker
  - SET – Silicon External Tracker
  - ETD – Endcap Tracking Detector
  - FTD – Forward Tracking Detector
- silicon envelope
  - SIT + SET + ETD
- notes
  - ETD not included in the current full simulation.
  - FTD being essential for tracking down to very small/large polar angles.



Baseline design – main parameters

Detector		Radius R [mm]		z [mm]	Material budget [X_0]
SIT	Layer 1:	153		371.3	0.65%
	Layer 2:	300		664.9	0.65%
SET	Layer 3:	1811		2350	0.65%
FTD	Disk 1:	$R_{in} = 39$	$R_{out} = 151.9$	220	0.50%
	Disk 2:	$R_{in} = 49.6$	$R_{out} = 151.9$	371.3	0.50%
	Disk 3:	$R_{in} = 70.1$	$R_{out} = 298.9$	644.9	0.65%
	Disk 4:	$R_{in} = 79.3$	$R_{out} = 309$	846	0.65%
	Disk 5:	$R_{in} = 92.7$	$R_{out} = 309$	1057.5	0.65%
ETD	Disk:	$R_{in} = 419.3$	$R_{out} = 1822.7$	2420	0.65%

Table 4.5: Main parameters of the CEPC silicon tracker.

Sensor technologies – baseline

- requirements of the single point resolution
  - vary with positions of tracker components
  - generally required $\sigma_{SP} < 7$ μm
- the basic sensor technology: silicon microstrips
  - for all components except two innermost FTD disks.
  - baseline features
    - a large detection area of 10 x 10 cm^2
    - a fine pitch of 50 μm
    - thichness < 200 μm

Sensor technologies – alternative

- a fully pixelated silicon tracker
- choice of pixel technologies is open
- CMOS pixel sensors (CPS) is under investigation for two main performance advantages compared to the microstrip sensors:
  - granularity, significantly reducing the ambiguity of multiple-hits
  - material budget, can be thinned to less than 50 μm
- CPS based on standard CMOS procedure in industry
  - production cost could be significantly reduced for large area detectors

data acquisition requirements

- estimated with the pixelated alternative (Table 4.6)
  - pixel dimension 50 x 350 μm^2
  - track multiplicities inferred from hit densities at the 1st vertex detector layer
  - readout time of pixel sensors 10 μs, the same as that of VTX
  - conservatively assumed 9 hits per track

operation mode	H (240)	W (160)	Z (91)
track multiplicity (BX^{-1})	310	300	32
bunching spacing (ns)	680	210	25
SIT-L1 occupancy (%)	0.19	0.58	0.52
FTD-D1 occupancy (%)	0.17	0.54	0.48

Front-End electronics

- FE chips will depend on the choice of sensors
  - microstrips: ASICs with deep sub-micron CMOS technology
  - pixels: in-pixel electronics
- common requirements
  - low noise, low power consumption and high radiation tolerance
  - high degree digitization to relax pressure on downstream electronics
- common functions
  - ADC, zero suppression, sparsification
  - possibly time stamping
  - control curcuitry

Powering & cooling

- fully open, novel techniques to be investigated
  - BUT, a chosen technique will have to provide sufficient powering or cooling without compromising the detector performance.
- powering
  - DC-DC converters?
- cooling
  - forced cooled gas flow
  - silicon micro-channel cooling

Mechanics & integration

- fully open, novel techniques to be investigated
- lightweight but stiff support structure
  - carbon fiber reinforced plastic material?
- concerns
  - design of support structure, cable routing and electronics common to other sub-detectors have to minimize overall material budget.
  - easy construction and integration
  - precise and quick system alignment

Critical R&D

- to be pursued in the R&D phase of CEPC
  - alternative pixelated strip sensors with CMOS technologies
  - p^+-on-n silicon microstrip sensors with slim-edgy structure
  - FE electronics with low power consumption and low noise, fabricated with CMOS technologies of small feature size
  - efficient powering and cooling techniques with low material budget
  - lightweight but robust support structure and related mechanics
  - detector layout optimization, particularly in the end regions
- also important, to exploit synergies with existing R&D from other experiments to share expertise.

Tracking performance

- based on the vertex detector and the silicon tracker (Figure 4.22)