中国科学院高能物理研究所
Institute of High Energy Physics
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Analog front-end design

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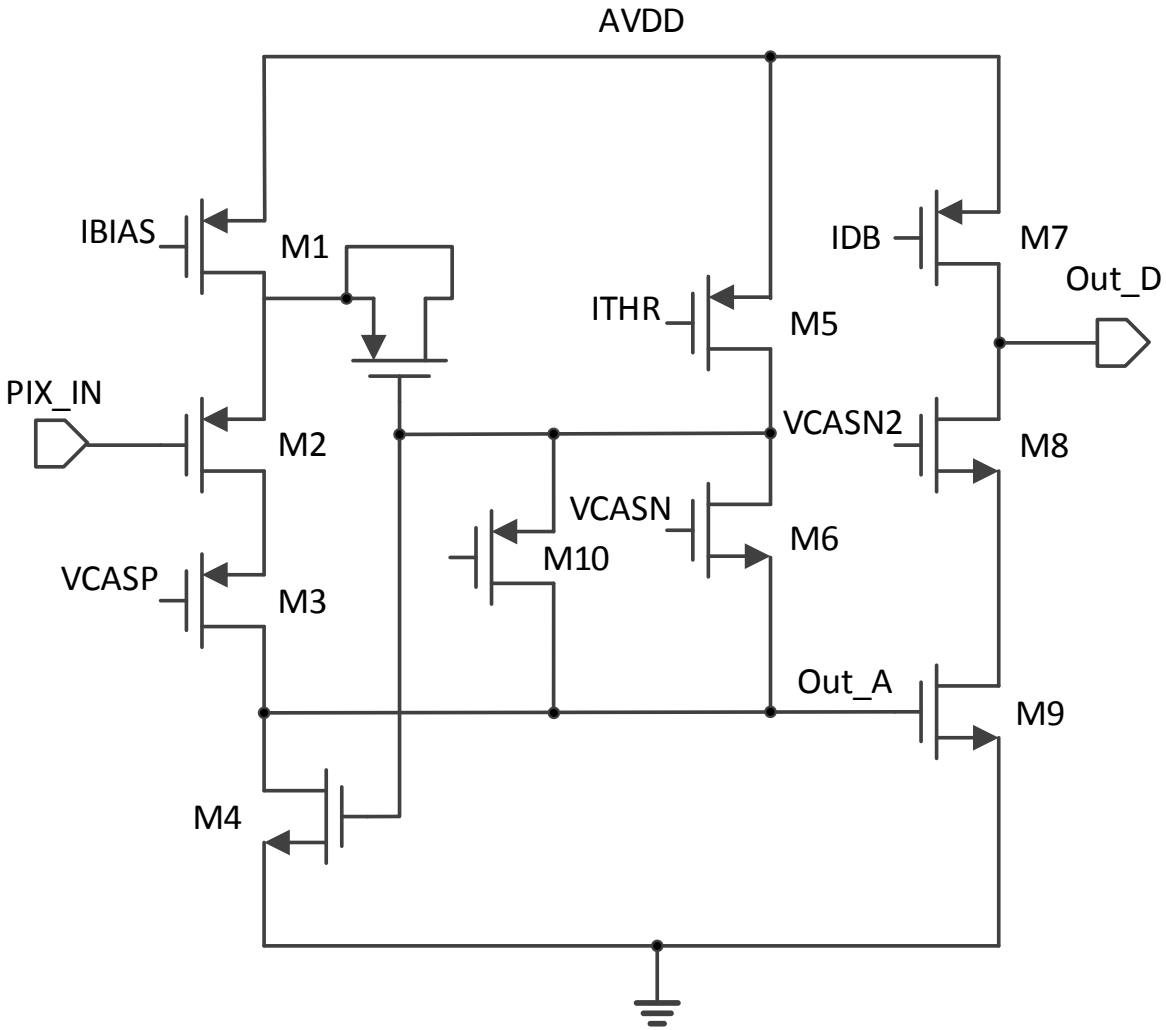
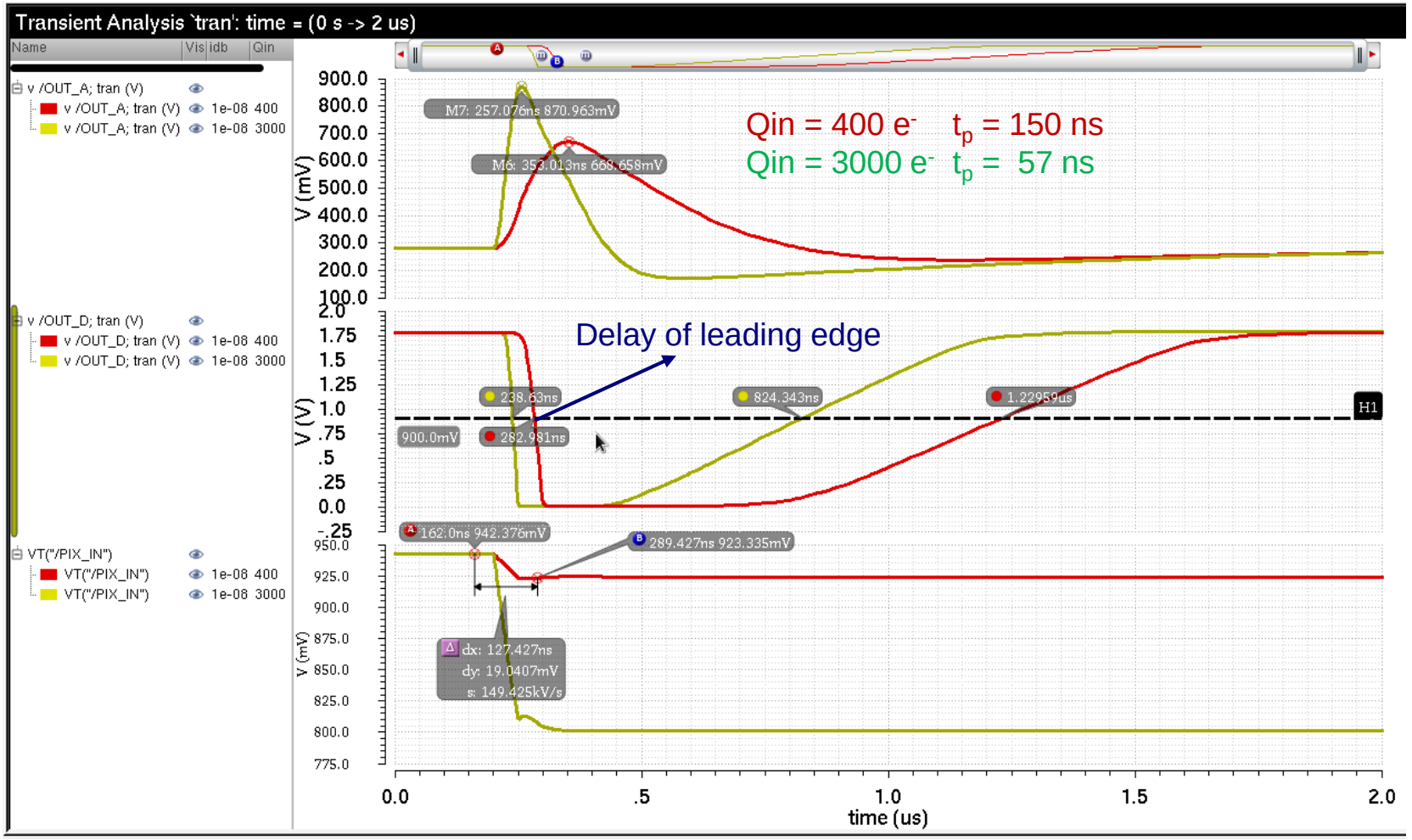
Front-end design



Front-end simulation

Simulation condition: Cd = 2.5 fF, IBIAS = 440 nA



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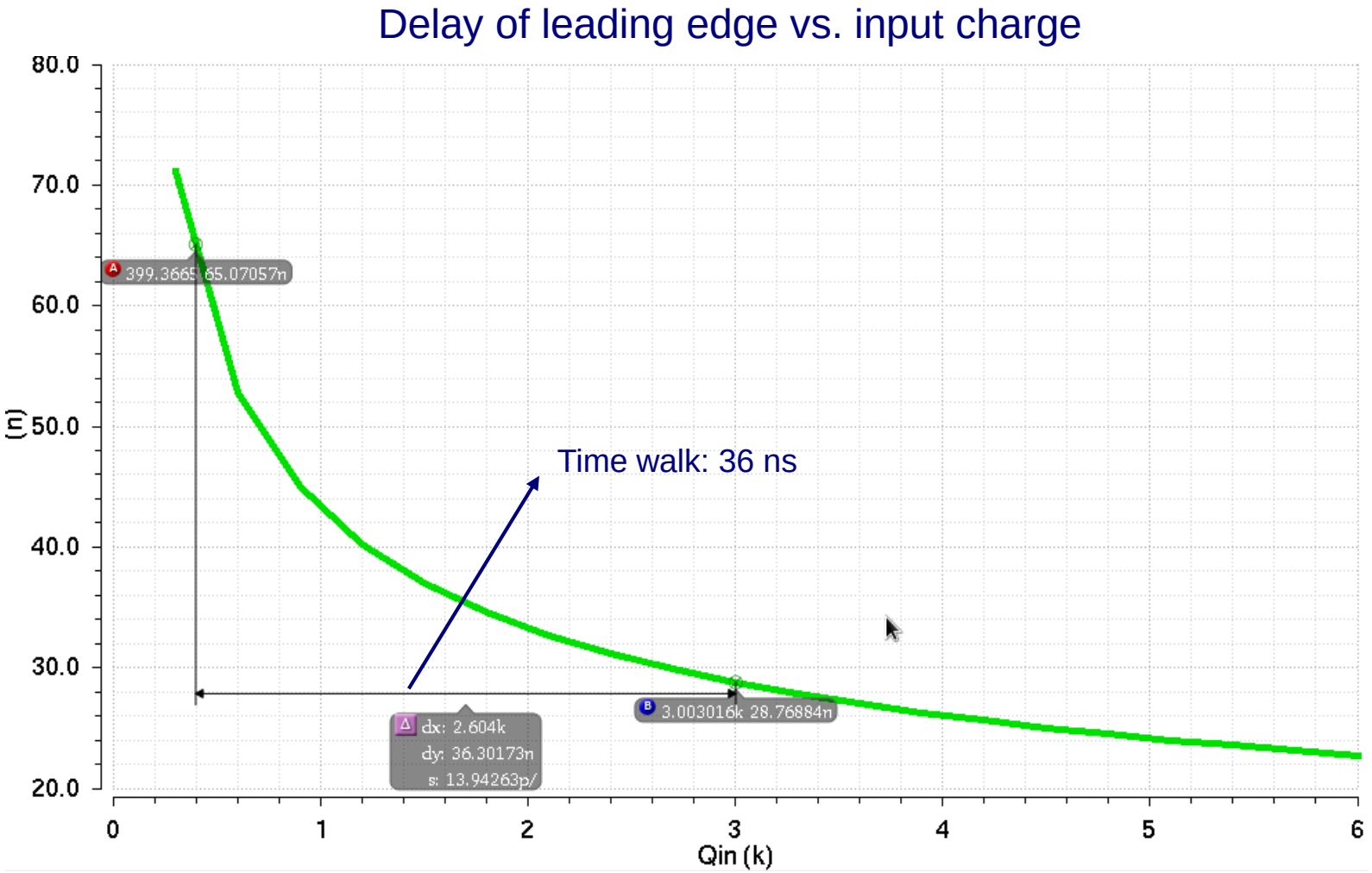
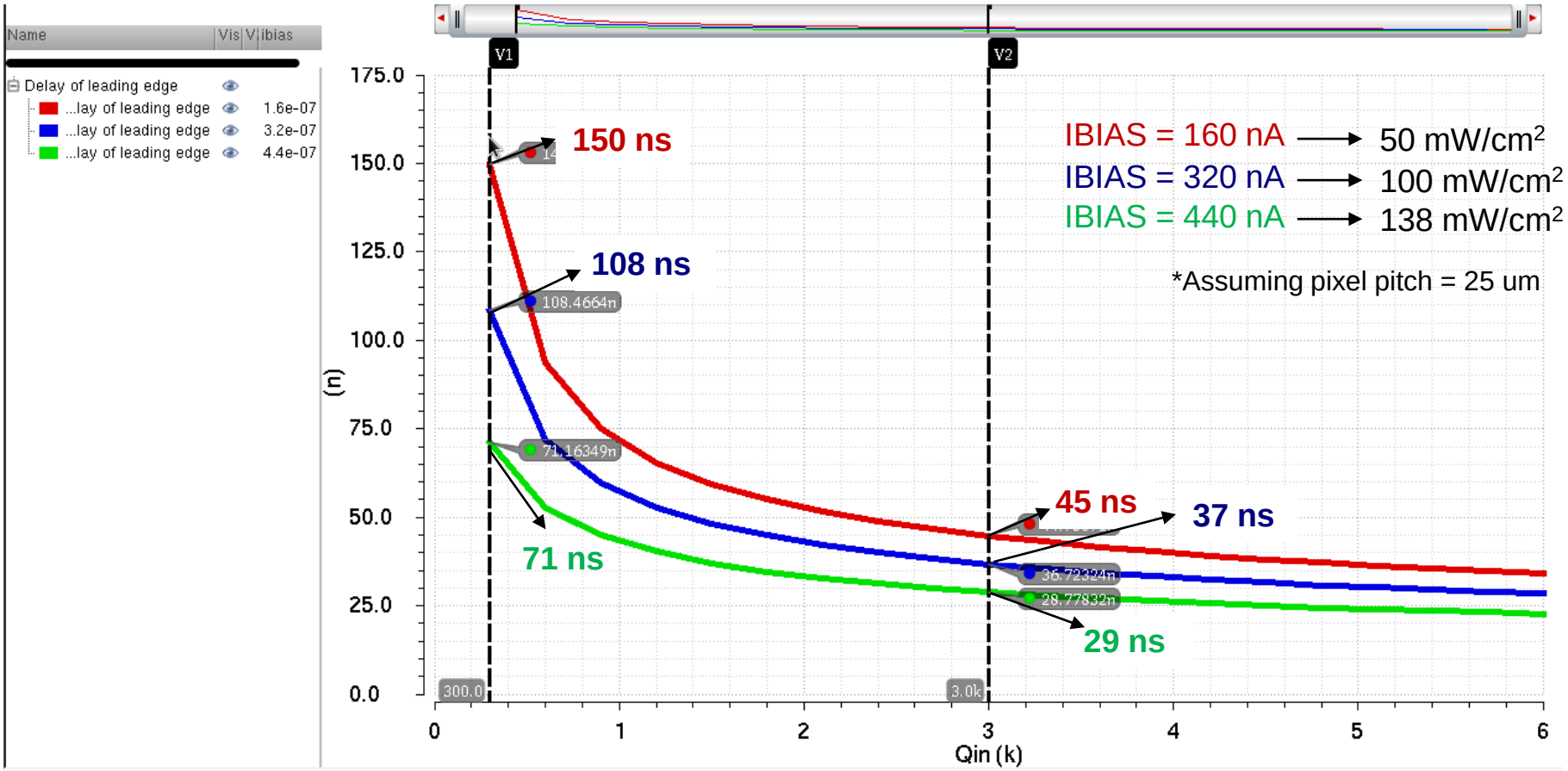


Front-end simulation

Simulation condition: Cd = 2.5 fF, Qin = 50 e^- – 6k e^-, 3 different IBIAS

Delay of leading edge vs. input charge



300 e^- 3000 e^-

Discussion and next step

- **How fast do we need?**
  - Peaking time? Time walk?
  - Compromise between time performance and power consumption

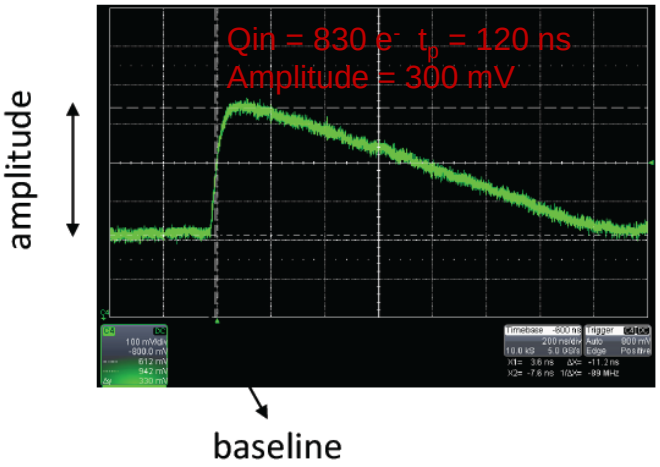
- **Next step: noise and mismatch need to be verified and optimisation**

Backup

MALTA chip for ATLAS

Analog Performance

- Measured analog output signal (OUT_A) of the front-end on monitoring pixels in sector 0 (diode reset) after test pulse injection
- V_{SUB}= - 6 V, pulsing with V_{HIGH}= 1.78 V and V_{LOW}= 1.2 V (≈ 830 e- equiv ½ MIP))



W4R7

P-well bias (V)	Analogue output baseline (mV)	Analogue output amplitude (mV)
0	320	170
-1	440	275
-2	510	290
-3	555	290
-4	580	295
-5	600	300
-6	615	305

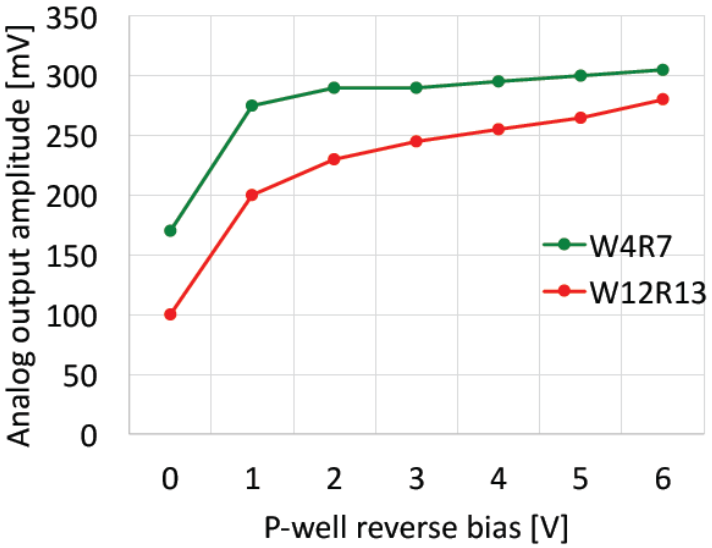
- + 10% increase in signal when going in V_{SUB} from -6 to -20 V

MALTA chip for ATLAS

Analog Performance

W12R13

P-well bias (V)	Analog output baseline (mV)	Analog output amplitude (mV)
0	310	100
-1	420	200
-2	485	230
-3	530	245
-4	550	255
-5	570	265
-6	585	280



- Chip from wafer 4 has slightly higher gain than wafer 12 (consistent with previous measurements on the TJ Investigator chip)
- All subsequent tests performed at V_{SUB}= -6 V and V_{PWELL}= -6 V