Status of Digital Pixel

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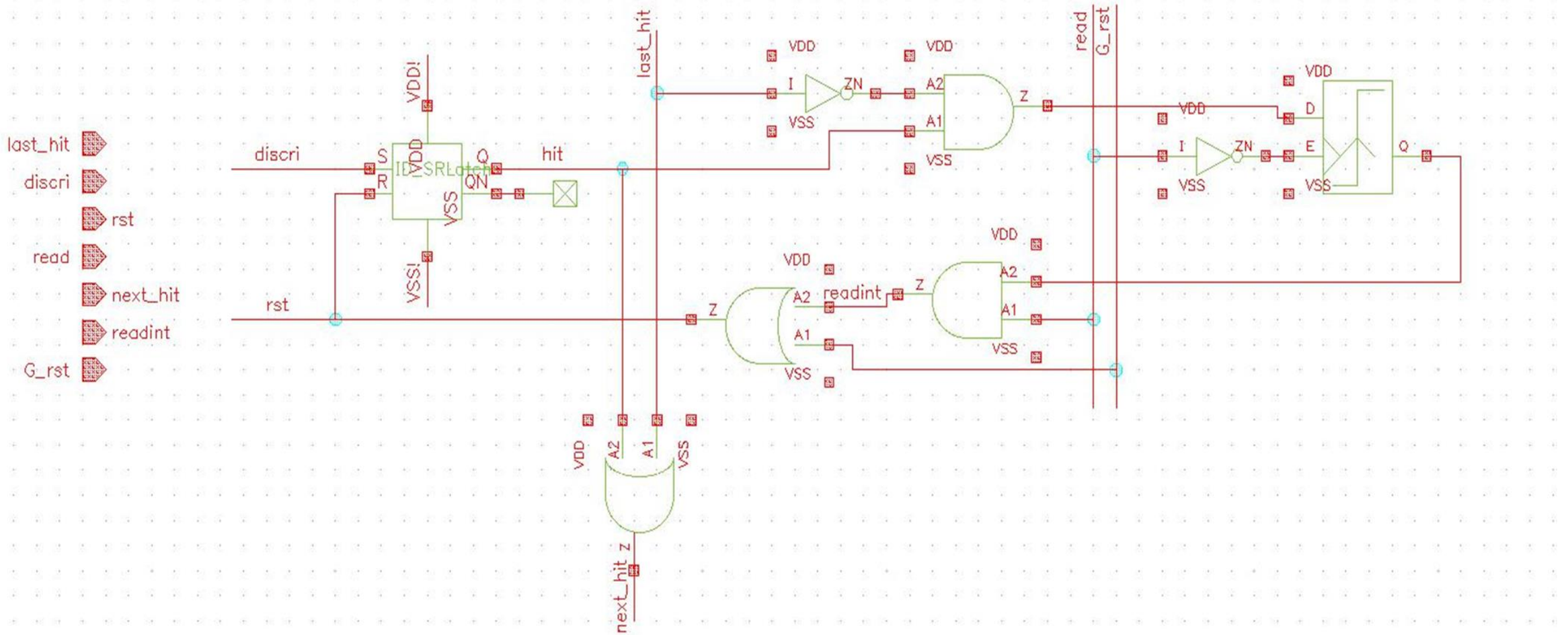
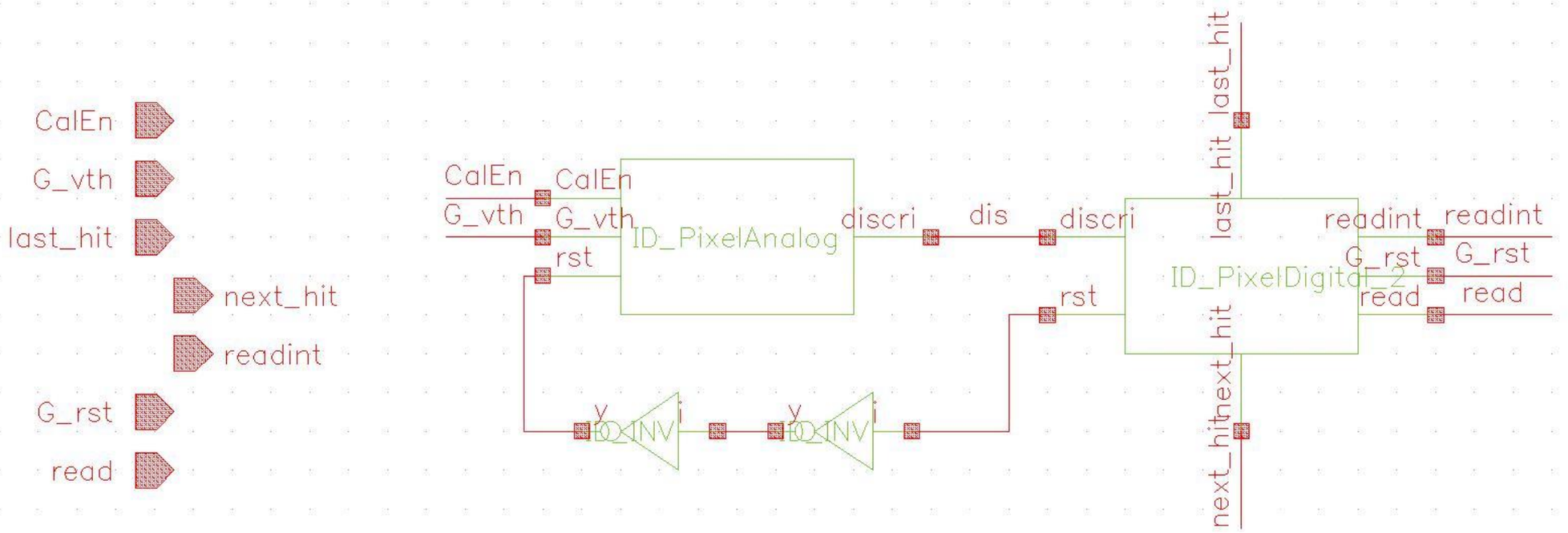
Logic scheme of Digital Pixel



Logic scheme of Pixel Cell

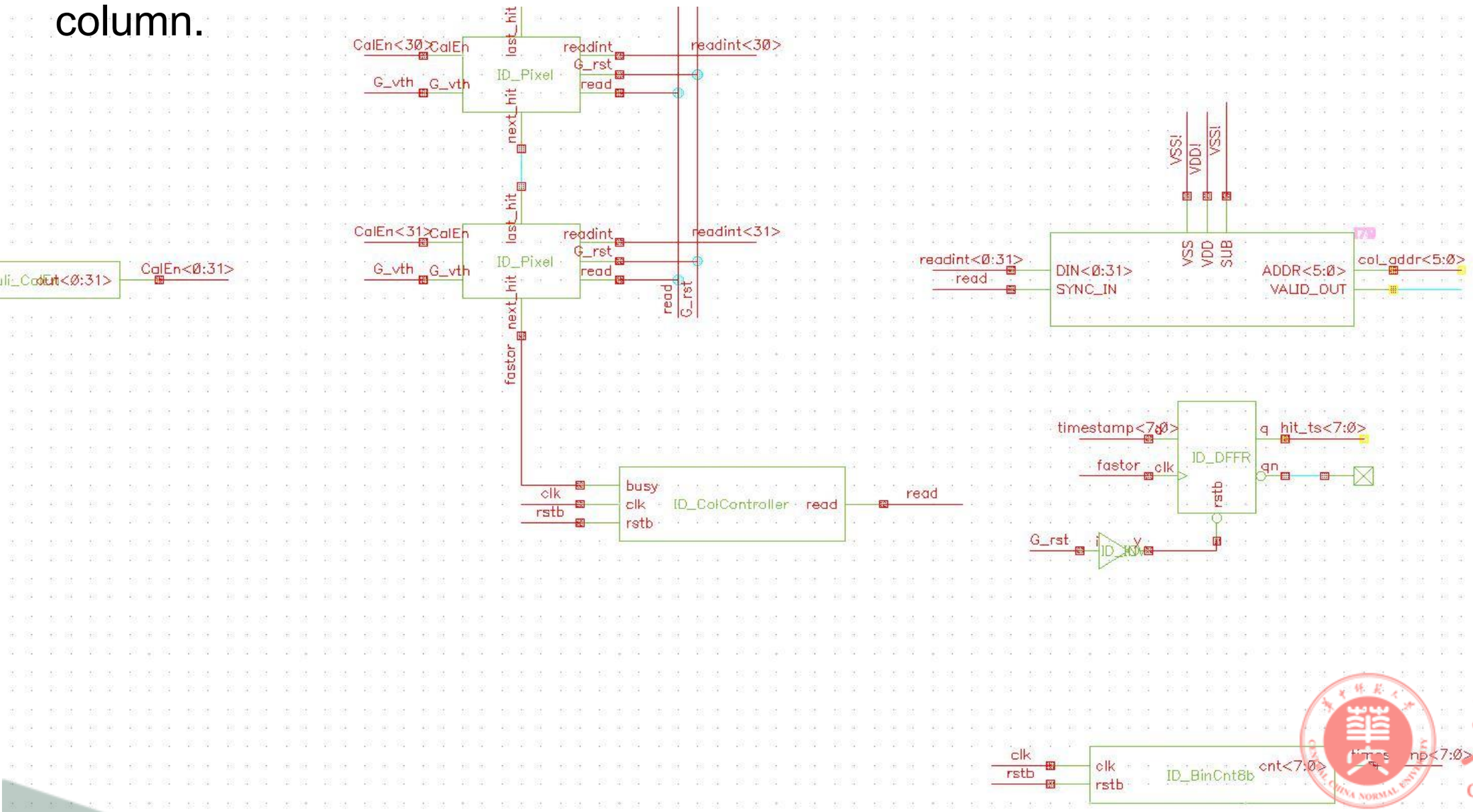
The rst signal can’t work unless adding a buffer.

There probably existed a delay in real circuits.



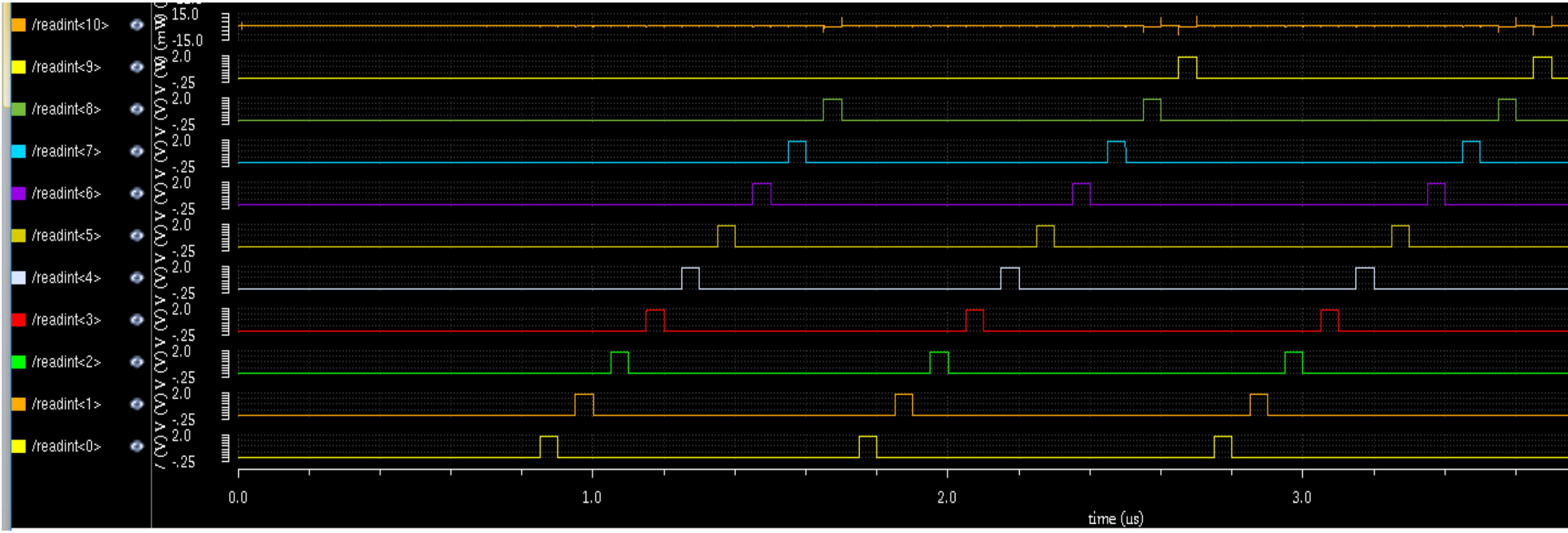
Address decoding circuit

I changed the address decode circuits with the structure in MOST1(but only 32bit used for simulation). From the simulation result, it works fine in the column.



Column simulation

From the plot, we can see the digital pixel (from cell 0 to cell 9)produce the stable pulse per 1us, and the width of pulse is 50ns.



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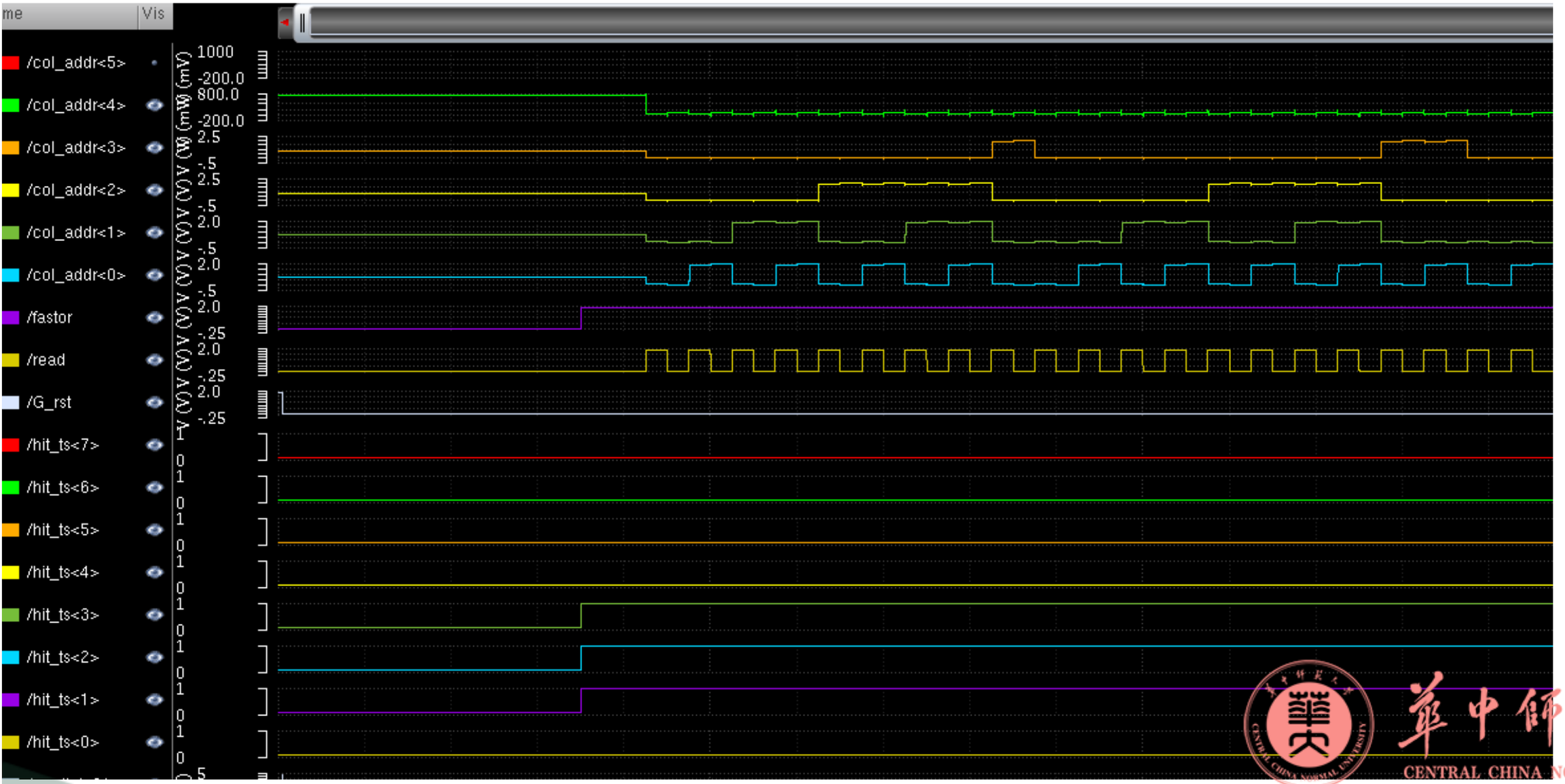
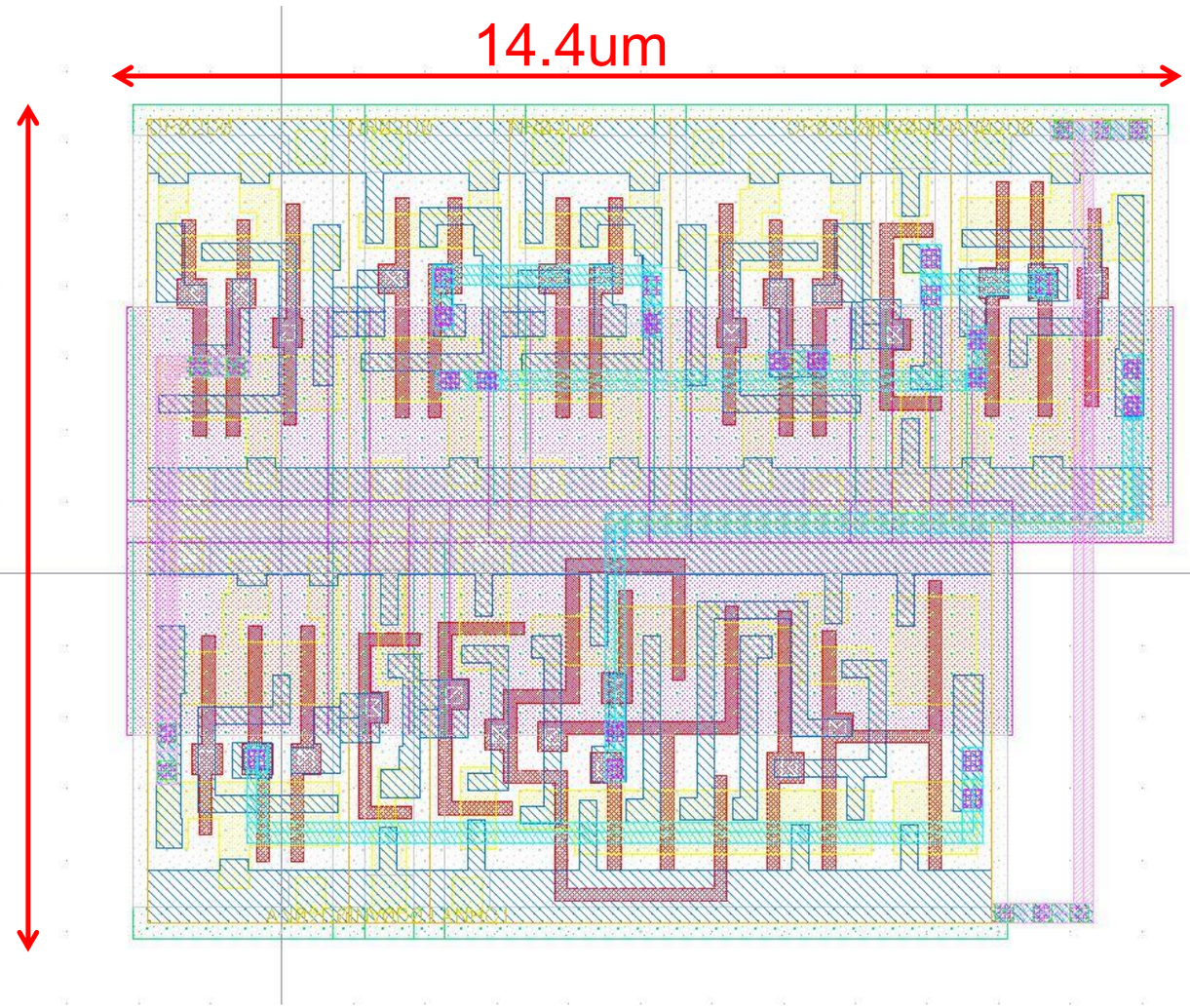
Column simulation

We can see that the decoding circuits address output in order during one clock cycle of “read” .



First version layout of digital pixel

This is the minimum size I did at present, with DRC and LVS clean.



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Next Step

- Simulate one column with 512 pixels, and give a solution of 512bit address decoding circuits.
- Seek for a possibility of reducing the size further.
- Evaluate the power consumption of the pixels.

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Thanks for your attention.

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