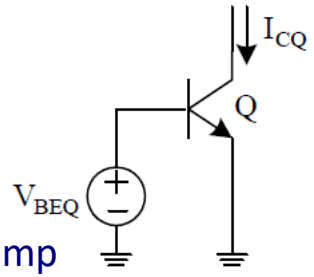
Concept of Bandgap Reference

- **Concept of V_{REF}**
  - V_{BE} decreases slight non-linearly with temperature
  - V_T （~kT/q） increases linearly with temperature
  - $\Delta V_{BE} = V_T \cdot \ln(N) = V(T)$
  - Weighted sum of V_{BE} and V_T results in low-temp dependence reference voltage
  - $V_{REF} = V_{BE} + V(T) \approx 1.205V@27°C$ ($V_T \approx 26$ mV)

    a small and temp-dependent voltage



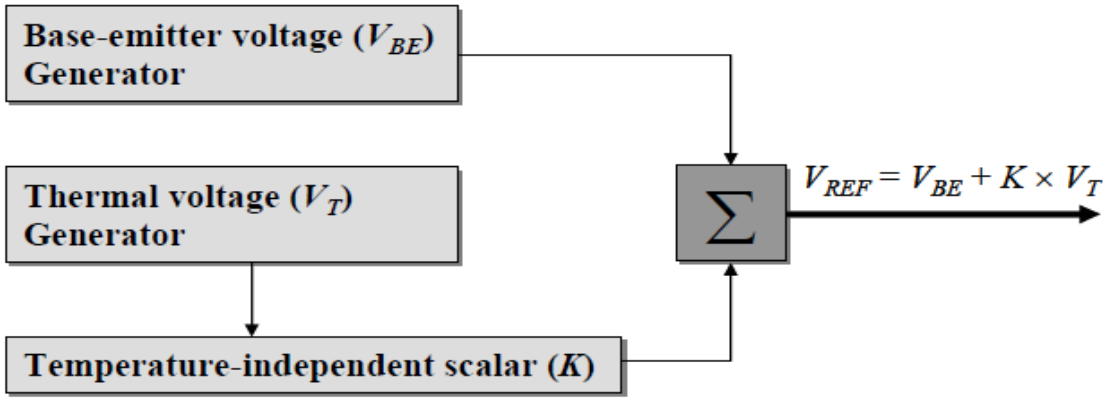
$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \quad (1)$$

$$V_{BE} = \frac{KT}{q}\ln\left(\frac{I_C}{I_S}\right) \quad (2)$$

$$V_{BE} \cong \frac{kT}{q} ln\left(\frac{I_C}{I_0} e^{V_{G0}/(kT/q)}\right)$$

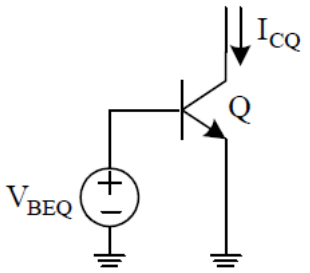
$$\cong V_{G0} - \frac{kT}{q} ln\left(\frac{I_0}{I_C}\right) \quad (3)$$

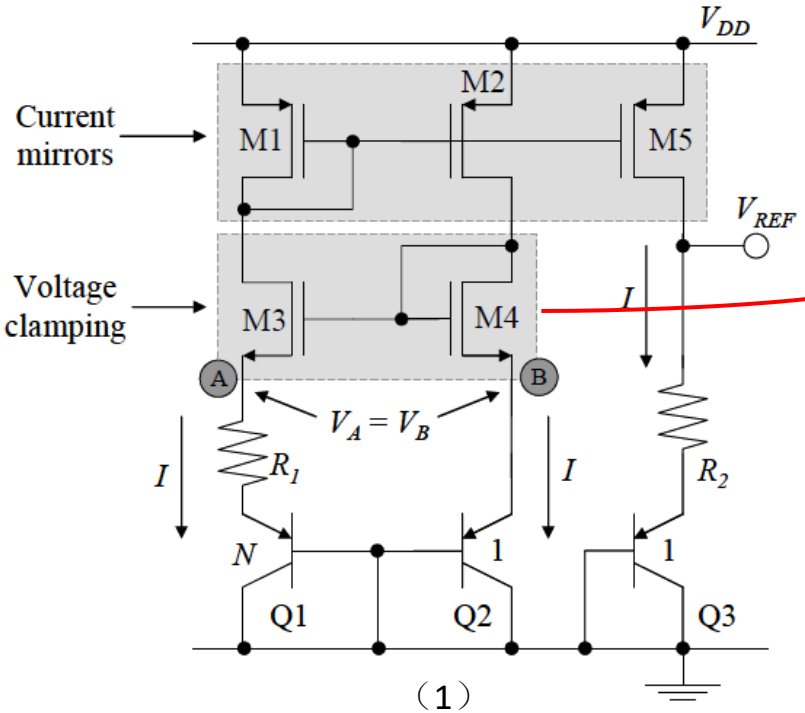
$$V_{G0} = \frac{1.205eV}{q} = 1.205V$$



Simple Implementation

- **Simple implementation of bandgap reference**
  - Current mirror enforces equal current at M1, M2 and M5
  - Voltage clamping to enforce V_A=V_B
  - PTAT loop formed by Q1,Q2 and R1
  - $I = V_T \cdot \ln(N)/R_1 \qquad V_{REF} = V_{EB3} + (R_2/R_1) \cdot \ln(N) \cdot V_T$
  - Cascode current mirror for better current matching at high power supply





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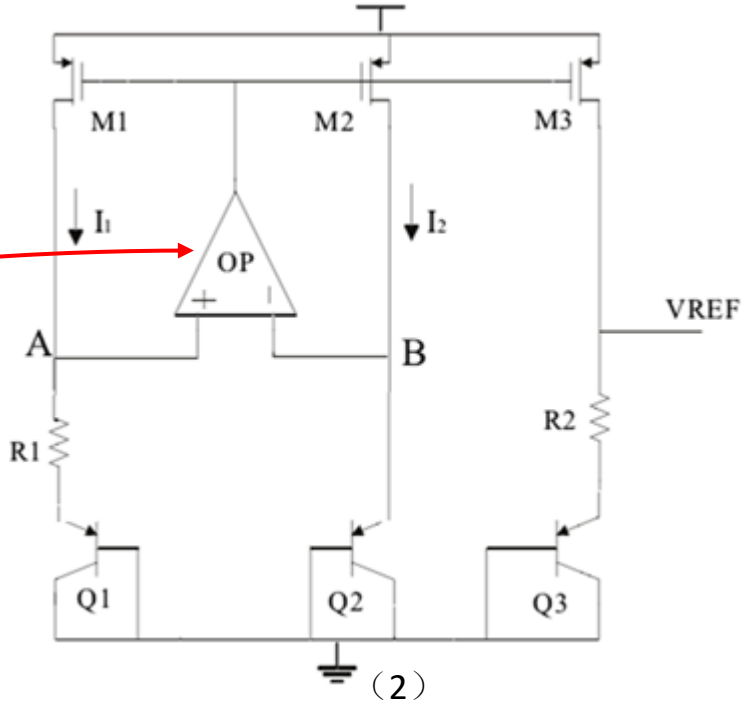

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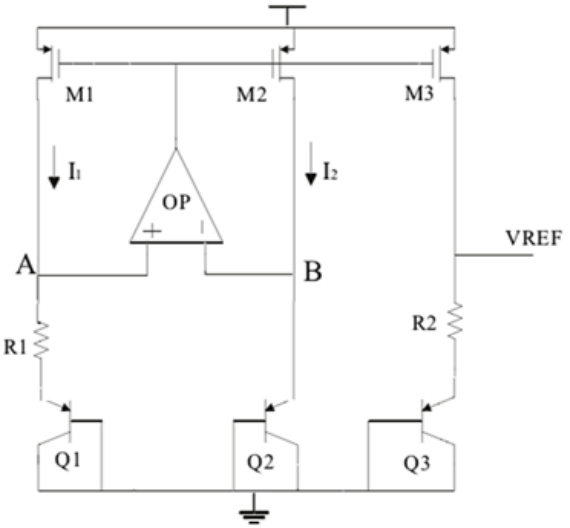
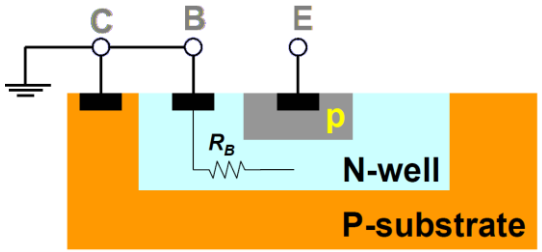
Error Sources

- **Error Sources in Voltage-Reference Design**
  - Current mirror
  - Voltage-clamping circuit (Error Amplifier offset)
  - BJT emitter area ratio (BJT matching)
  - Resistor ratio (resistor matching)
  - Systematic offset at different supply voltages
  - Random offset of devices
- **Design Considerations: Current mirror**
  - Large size of MOSFET(larger length)
  - Cascode current mirror with 3.3 V power supply
- **Design Considerations: Error Amplifier offset**
  - Large size of MOSFET (input pair)
  - Reasonable placement of layout
  - Matching is important
- **Design Considerations: BJTs**
  - Diode-connected BJT ≠ V_{EB}
  - Reduce voltage across R_B
  - Guarantee V_{EB} >> V_B, more N-well contacts to reduce R_B





Structure Research

- **Structure concept**
  - Voltage-mode references generate a temperature-independent voltage by summing PTAT currents multiply resistor with V_{BE}
  - Cascode current mirror
  - R1, R2, R3 & R4 of same material
  - Good matching R1 and R4 for optimizing tempco
  - $I = V_T \cdot \ln(N)/R_1 \qquad V_{REF} = V_{EB3} + R_4/R_1 \cdot \ln(N) \cdot V_T$
  - V_{REF}=1.2V