MIMOSA32TER LVDS TEST STRUCTURE

TEST REPORT

VERSION 130319

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1 Introduction

This test report concludes preliminary results of device characterizations of auxiliary Low-Voltage Differential Signaling (LVDS) Test Structure designed by Zhan Shi for a MIMOSA-32TER device. This LVDS test structure consists of a common LVDS receiver with two different output driver implementations: a standard LVDS output driver and an advanced output driver based on Reduced Swing Differential Signaling (RSDS) standard.
A block diagram of the test structure is shown in Figure below. The implementation of the LVDS driver and the RSDS driver are labeled as LVDS_TX and RSDS_TX, respectively. The common LVDS receiver is labeled as LVDS_RX. The LVDS Test Structure includes single-ended CMOS pads for injecting a test signal for Output drivers or extracting the output signal of the LVDS receiver. The CMOS input signal for the differential output drivers is labeled as IN_TX and the CMOS output for the LVDS receiver is labeled as OUT_RX.
For the reason of limited number of I/O pad available for the test structure, there are only 3 digital input signals to select test configuration mode: SEL_RX, SEL_TX and SEL_RXO.

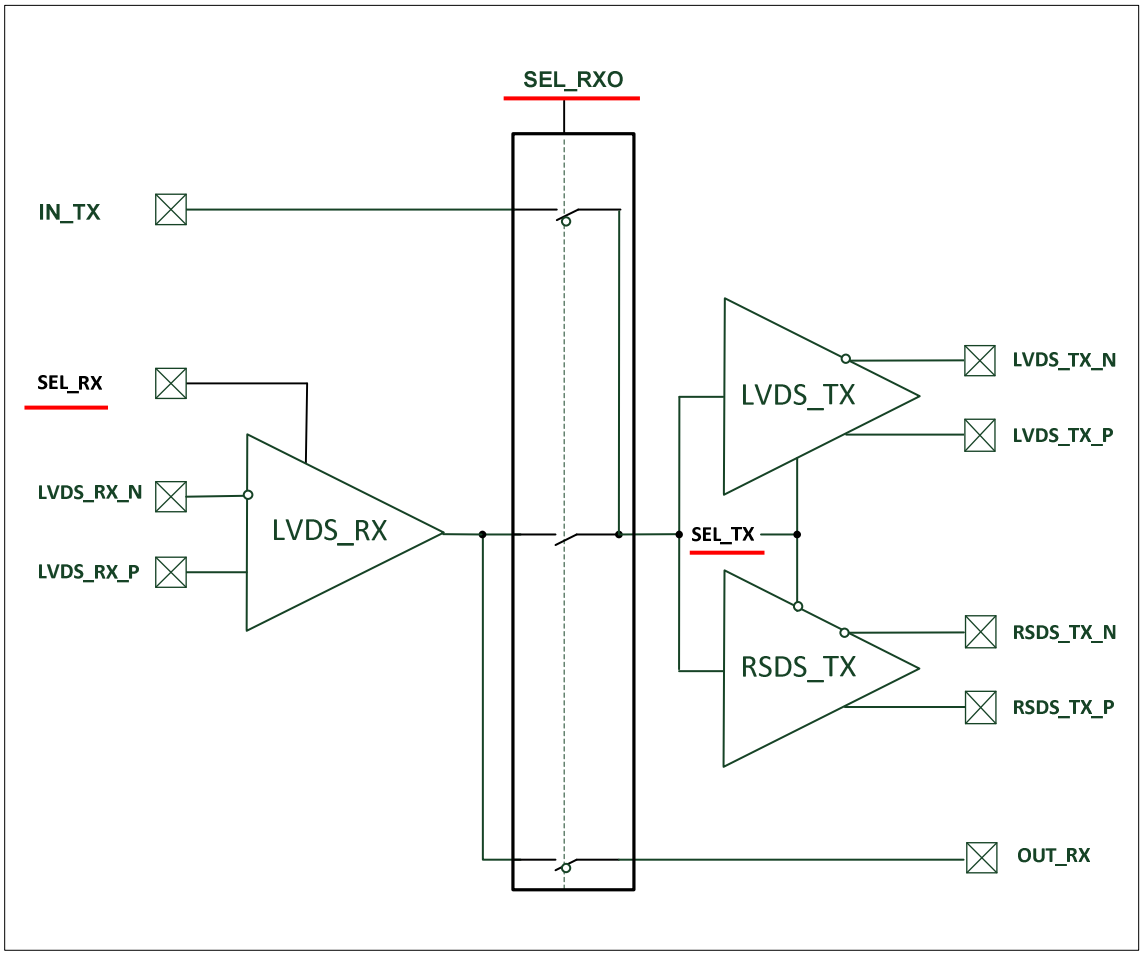


Figure 1. A block diagram of MIMOSA-32TER LVDS Test Structure

In a Table 1 is presented configuration settings. The receiver input can be the CMOS input pad IN_TX or the LVDS receiver input LVDS_RX. Output signal is available on the CMOS output pad OUT_RX or on the LVDS driver pads LVDS_TX or on the RSDS driver pads RSDS_TX.

SEL_RX	SEL_TX	SEL_RX0	MODE	
			RECEIVER	DRIVER
0	0	0	IN_TX	RSDS_TX
			LVDS_RX	-
0	0	1	IN_TX	-
			LVDS_RX	-
0	1	0	IN_TX	LVDS_TX
			LVDS_RX	-
0	1	1	IN_TX	-
			LVDS_RX	-
1	0	0	IN_TX	RSDS_TX
			LVDS_RX	OUT_RX
1	0	1	IN_TX	-
			LVDS_RX	RSDS_TX
1	1	0	IN_TX	LVDS_TX
			LVDS_RX	OUT_RX
1	1	1	IN_TX	-
			LVDS_RX	LVDS_TX

Table 1. Configuration settings by SEL_RX, SEL_TX and SEL_RXO pads.

2 LVDS Receiver and LVDS Driver Bias current

2.1 LVDS Driver Output Differential Voltage versus ILVDS_TX current

This measurement is done with the constant input value and the CMOS input IN_TX is selected as input (SEL_RX=1, SEL_TX=1 and SEL_RXO=0).

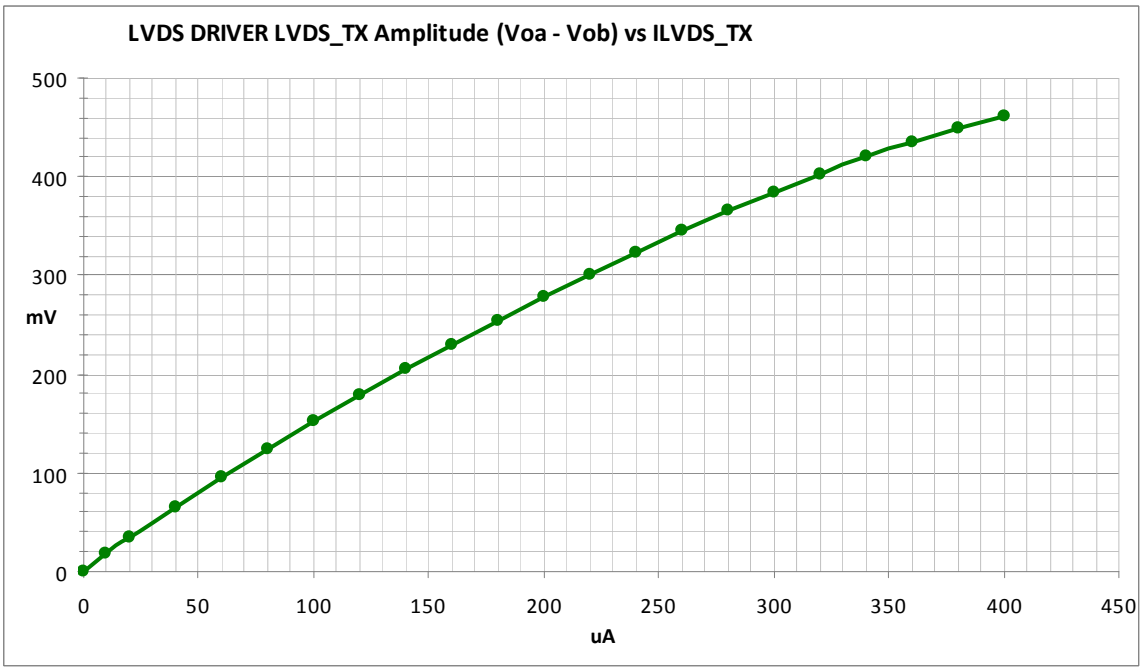


Figure 2. LVDS_TX Driver Output amplitude vs. bias current ILVDS_TX

2.2 RSDS Driver Output Differential Voltage versus ILVDS_TX current

This measurement is done with the constant input value and the CMOS input IN_TX is selected as input (SEL_RX=1, SEL_TX=0 and SEL_RXO=0).

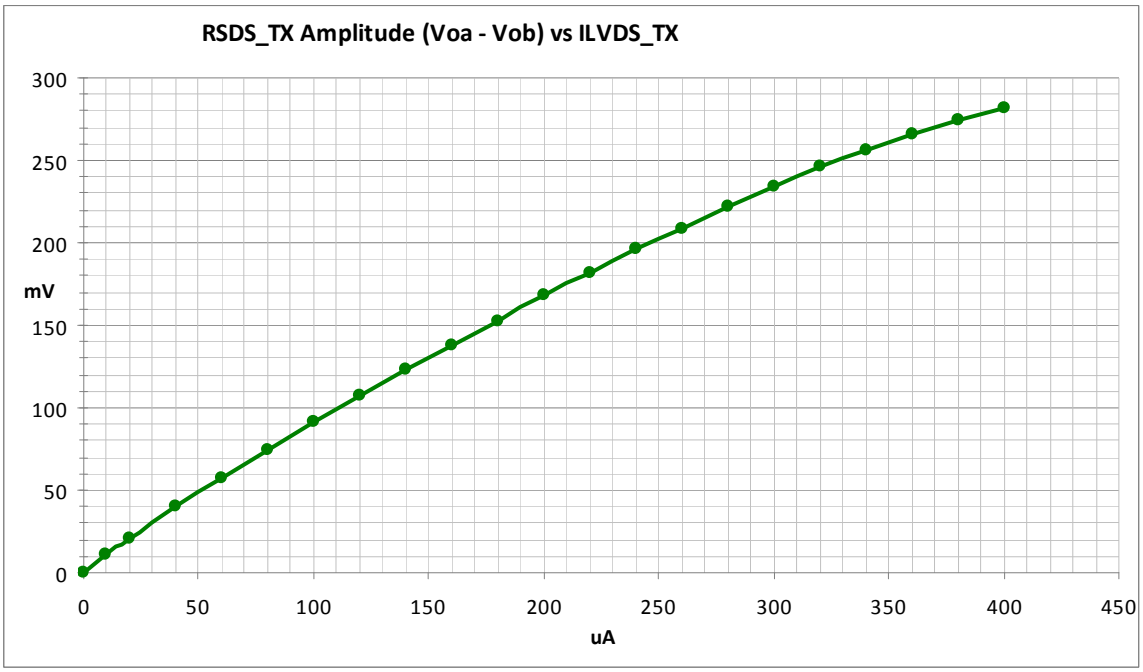


Figure 3. RSDS_TX Driver Output amplitude vs. bias current ILVDS_TX

On following measurements the common ILVDS_TX bias current for LVDS_TX and RSDS_TX Driver is fixed to 220 µA.

2.3 Driver Output Jitter versus ILVDS_RX current

In Figure 4 is shown the LVDS_TX output driver Total Jitter (TIE Mode with BER=10^{-12}). The ILVDS_TX bias current is fixed to 220 µA. The LVDS receiver LVDS_RX is selected as an input for the LVDS driver LVDS_TX (SEL_RX=1, SEL_TX=1 and SEL_RXO=1). The reference clock signal frequency is 250 MHz.

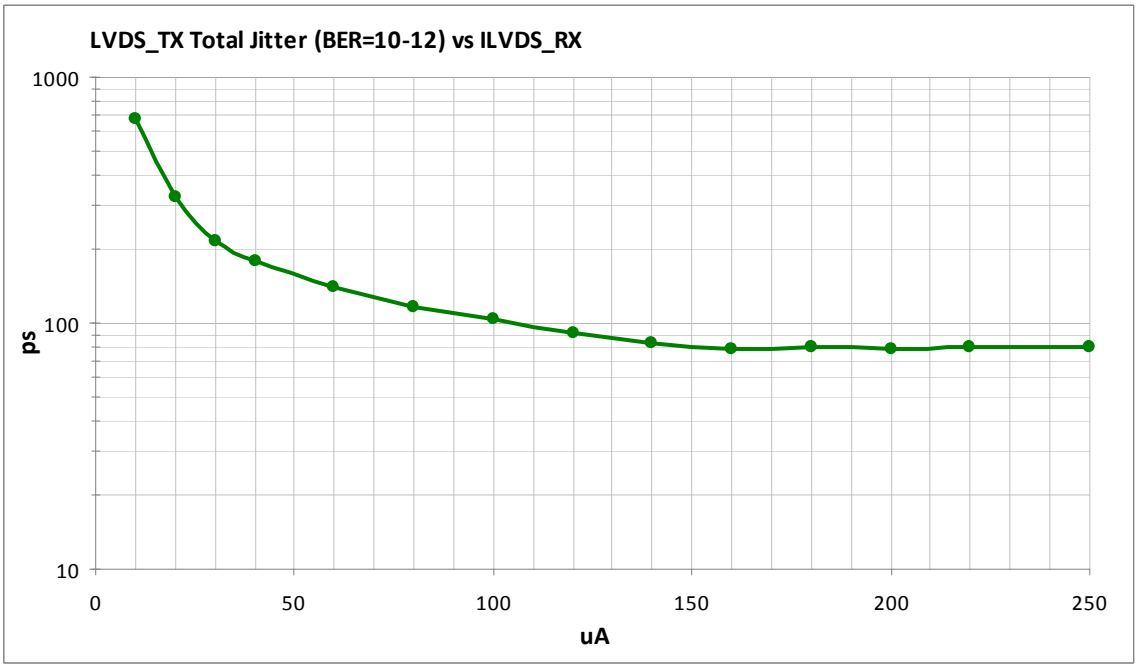


Figure 4. LVDS_TX Driver Output Total Jitter vs. bias current ILVDS_TX

On following measurements the ILVDS_RX bias current is fixed to 180 µA.

3 LVDS Driver LVDS_TX measurement

In following measurements, a Double Termination configuration is always used for LVDS_TX driver, because the LVDS_TX driver has an internal on-chip termination of 100 ohm (Figure 5). The measured value of the internal termination resistance is 111 ohm.

Double Termination (DT)
In this Configuration, the transmission line is terminated twice to a differential load of 100 ohm, firstly at output of the LVDS Driver and secondly, at the end of PCB traces with a single-ended to differential termination board. The signal captured at the single-ended to differential termination board with a differential probe.

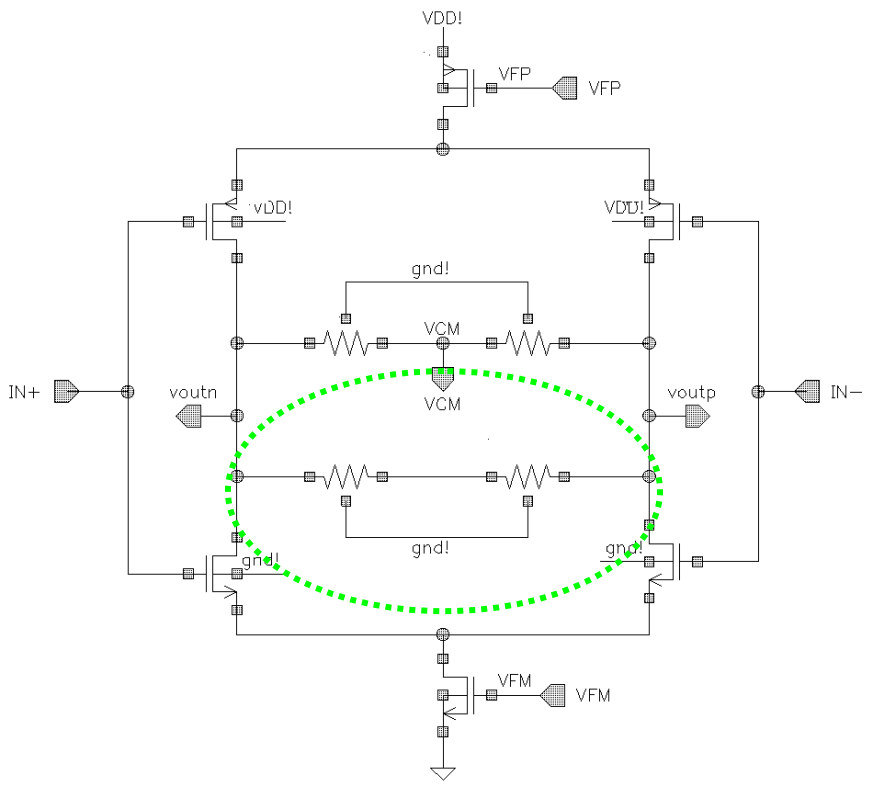


Figure 5. The LVDS_TX Driver with the internal termination resistances.

ICore:Ifb2:Icmfb_p=40:2:1

Ilvds_dc=6(1+1/20 +2*1/40)=6*1.1=6.6mA

3.1 LVDS Driver DC parameter

Please see the document IEEE Std 1596.3-1996 for more details of parameters presented in this Chapter. The ILVDS_RX and ILVDS_TX bias currents are 180 µA and 220 µA, respectively.

I_TX_LVDS_Core=6 mA

Symbol	Parameter	units	min	max	Condition	Measured Value	
						V_{oa}	V_{ob}
V_{oh}	Output Voltage High	mV		1475	IN_TX= 3.3V	1352	1352
V_{ol}	Output Voltage Low	mV	925		IN_TX= 0V	1049	1050
$\|V_{od}\|$	Output Differential voltage	mV	250	400	IN_TX= 3.3V	302	
					IN_TX= 0V	303	
V_{os}	Output Offset Voltage	mV	1125	1275	IN_TX= 3.3V	1201	
					IN_TX= 0V	1201	
$\|\Delta V_{od}\|$	Change in V_{os} between "0" and "1"	mV		25		11	
ΔV_{os}	Change in V_{os} between "0" and "1"	mV		25		1	
I_{sa}, I_{sb}	Output current, driver shorted to GND	mA		40	IN_TX= 3.3V	12.8	12.6
					IN_TX= 0V	12.6	12.8
I_{sab}	Output current, driver shorted together	mA		12	IN_TX= 3.3V	4.9	
					IN_TX= 0V	4.9	

3.2 LVDS Driver AC parameter

Symbol	Parameter	units	min	max	Condition	Measured Value	
						V_{oa}	V_{ob}
Clock	Clock signal duty cycle At 250 MHz	%	45	55	LVDS receiver LVDS_RX is selected	49.3	
T_{HLT}	Differential High to Low Transition Time, Clock pattern of alternating 1 and 0 at 500 Mbps, V_{od} fall time 20-80%	ps	300	500		153	
T_{LHT}	Differential Low to High Transition Time, Clock pattern of alternating 1 and 0 at 500 Mbps, V_{od} rise time 20-80%	ps	300	500		149	
t_{ON}	LVDS Driver Output Enable Time	ns		-	Enable by SEL_TX signal	54	
t_{OFF}	LVDS Driver Output Disable Time	ns		-	Disable by SEL_TX signal	3	
t_{PD}	Differential Propagation Delay from LVDS_RX to LVDS_TX	ns		-		0.3	
t_{PSE}	Single-ended Propagation Delay from IN_TX to LVDS_TX	ns		-		2	

4 RSDS Driver RSDS_TX measurement

Simple Termination (ST)

In this Configuration, the transmission line is terminated only once to a differential load of 100 ohm at the end of the PCB traces with a single-ended to differential termination board. The signal captured at the single-ended to differential termination board with a differential probe.

The RSDS Driver RSDS_TX is not furnished with an internal termination resistance. For the reason of reduced output signal swing, the Simple Termination configuration is used in following measurements.

ICore:Ifb2:Icmfb_p=20:1:1

Irsds_dc=1.84(1+1/20 +2*1/20)=1.84*1.15=2.12mA

4.1 RSDS Driver DC parameter

Please see the document IEEE Std 1596.3-1996 for more details of parameters presented in this Chapter. The ILVDS_RX and ILVDS_TX bias currents are 180 µA and 220 µA, respectively. The RSDS is considered as a Reduced Range Link.

I_TX_RSDS_Core=1.8 mA

wrong mesurement method

Symbol	Parameter	units	min	max	Condition	Measured Value	
						V_{oa}	V_{ob}
V_{oh}	Output Voltage High	mV		1375	IN_TX= 3.3V	1280	1280
V_{ol}	Output Voltage Low	mV	1025		IN_TX= 0V	1096	1096
$\|V_{od}\|$	Output Differential voltage	mV	150	250	IN_TX= 3.3V	184	
					IN_TX= 0V	184	
V_{os}	Output Offset Voltage	mV	1150	1250	IN_TX= 3.3V	1188	
					IN_TX= 0V	1188	
R_o	Output impedance, Single-ended (V_{oahi} - V_{oalo}) or (V_{obhi} - V_{oblo})	mV	40 ohm corresponds to 178 mV	140 ohm corresponds to 295 mV	IN_TX= 3.3V, V_{cm} = 1V, V_{oahi} - V_{oalo}	311	
					IN_TX= 0V, V_{cm} = 1V, V_{oahi} - V_{oalo}	299	
					IN_TX= 3.3V, V_{cm} = 1.4V, V_{obhi} - V_{oblo}	299	
					IN_TX= 0V, V_{cm} = 1.4V, V_{obhi} - V_{oblo}	311	
ΔR_o	R_o mismatch between A & B	%		10		0	
	$\|(V_{oahi} - V_{obhi}) - (V_{oalo} - V_{oblo})\|$	mV		20	IN_TX= 3.3V	12	
	$\|(V_{oahi} - V_{obhi}) - (V_{oalo} - V_{oblo})\|$				IN_TX= 0V	12	
$\|\Delta V_{od}\|$	Change in V_{od} between "0" and "1"	mV		25		0	
ΔV_{os}	Change in V_{os} between "0" and "1"	mV		25		0	
I_{sa},I_{sb}	Output current, driver shorted to GND	mA		40	IN_TX= 3.3V	3.57	0.01
					IN_TX= 0V	0.01	3.57
I_{sab}	Output current, driver shorted together	mA		12	IN_TX= 3.3V	1.87	
					IN_TX= 0V	1.87	

4.2 RSDS Driver AC parameter

Symbol	Parameter	units	min	max	Condition	Measured Value	
						V_{oa}	V_{ob}
Clock	Clock signal duty cycle At 250 MHz	%	45	55	LVDS receiver LVDS_RX is selected	50.3	
T_{HLT}	Differential High to Low Transition Time, Clock pattern of alternating 1 and 0 at 500 Mbps, V_{od} fall time 20-80%	ps	300	500		186	
T_{LHT}	Differential Low to High Transition Time, Clock pattern of alternating 1 and 0 at 500 Mbps, V_{od} rise time 20-80%	ps	300	500		182	
t_{ON}	LVDS Driver Output Enable Time	ns		-	Enable by SEL_TX signal	38	
t_{OFF}	LVDS Driver Output Disable Time	ns		-	Disable by SEL_TX signal	8	
t_{PD}	Differential Propagation Delay from LVDS_RX to LVDS_TX	ns		-		1.3	
t_{PSE}	Single-ended Propagation Delay from IN_TX to LVDS_TX	ns		-		2.1	

5 LVDS Receiver LVDS_RX measurement

5.1 Receiver DC parameter

Symbol	Parameter	units	min	max	Condition	Measured Value	
						V_{ia}	V_{ib}
V_i	Input voltage range, V_{ia} or V_{ib}, $\|V_{gpd}\| < 50$ mV, measured $\|V_{gpd}\| = 0.3$ mV	mV	825	1575	V_{ia}	790	1670
					V_{ib}	770	1460
V_{ith}	Input differential threshold , $\|V_{gpd}\| < 50$ mV, measured $\|V_{gpd}\| = 0.3$ mV	mV	-100	100	1)	35	
V_{hyst}	Input differential hysteresis, V_{idthh} - V_{idthl}	mV	25		V_{ia} variable, V_{ib} fixed, V_{idthh} - V_{idthl} = 13 – (-15) mV	28	

1) The output of LVDS_TX Driver (Device1) of LVDS Driver is injected in LVDS_RX Receiver (Device2) input. The output signal amplitude of LVDS_TX Driver (Device1) is varied by changing the current ILVDS_TX (Device1) from 0 µA to 50 µA by step of 1 µA. A clock signal is used as input for the LVDS_TX Driver (Device1) and the output of LVDS_TX Driver (Device2) is monitored to define a differential threshold voltage level for LVDS_RX Receiver (Device2).

6 Power Consumption

6.1 Power Consumption with LVDS_TX Driver

Symbol	Parameters, Conditions	units	Measured Value
$I_{VDD\_LVDS\_STATIC}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, LVDS_TX Driver Enable, Static Condition, ILVDS_RX = 180 µA, ILVDS_TX = 220 µA	mA	7.5
$I_{VDD\_LVDS\_500Mbps}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, LVDS_TX Driver Enable, Clock Pattern at 500 Mbps ILVDS_RX = 180 µA, ILVDS_TX = 220 µA	mA	10.9
$I_{VDD\_LVDS\_1000Mbps}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, LVDS_TX Driver Enable, Clock Pattern at 1000 Mbps ILVDS_RX = 180 µA, ILVDS_TX = 220 µA	mA	12.0
$I_{VDD\_LVDS\_STATIC\ ,ILVDS\_TX=0}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, LVDS_TX Driver Enable, Static Condition, ILVDS_RX = 180 µA, ILVDS_TX = 0 µA	mA	0.8
$I_{VDD\_LVDS\_500Mbps,ILVDS\_TX=0}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, LVDS_TX Driver Enable, Clock Pattern at 500 Mbps ILVDS_RX = 180 µA, ILVDS_TX = 0 µA	mA	4.7
$I_{VDD\_LVDS\ 1000Mbps,ILVDS\_TX=0}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, LVDS_TX Driver Enable, Clock Pattern at 1000 Mbps ILVDS_RX = 180 µA, ILVDS_TX = 0 µA	mA	6.0
$I_{VDD\_LVDS\_STATIC\ ,\ ILVDS\_RX=0}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, LVDS_TX Driver Enable, Static Condition, ILVDS_RX = 0 µA, ILVDS_TX = 220 µA	mA	7.1

In Figure 6 is shown the 1.8V power supply (VDD18) current of the LVDS test structure versus the input data clock frequency. The measurements are performed in two different ILVDS_TX bias current conditions: ILVDS_TX = 0 µA and ILVDS_TX = 220 µA. The LVDS Receiver bias current ILVDS_RX is 180 µA.

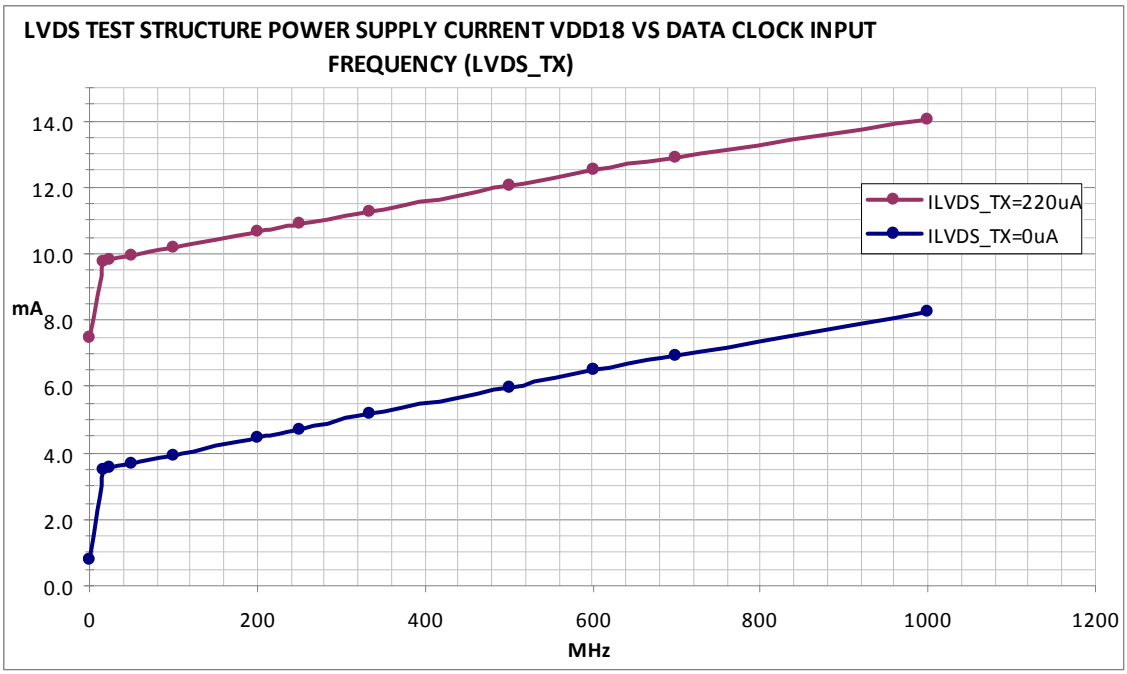


Figure 6. Power supply (VDD18) current of the LVDS test structure (LVDS_TX selected) vs. data input clock frequency

In Figure 7 is shown the 1.8V power supply (VDD18) current of the LVDS test structure versus the bias current ILVDS_TX. The measurements are performed in two different ILVDS_RX bias current conditions: ILVDS_RX = 0 µA (Static Condition) and ILVDS_RX = 180 µA. The input data clock frequency is 250 MHz.

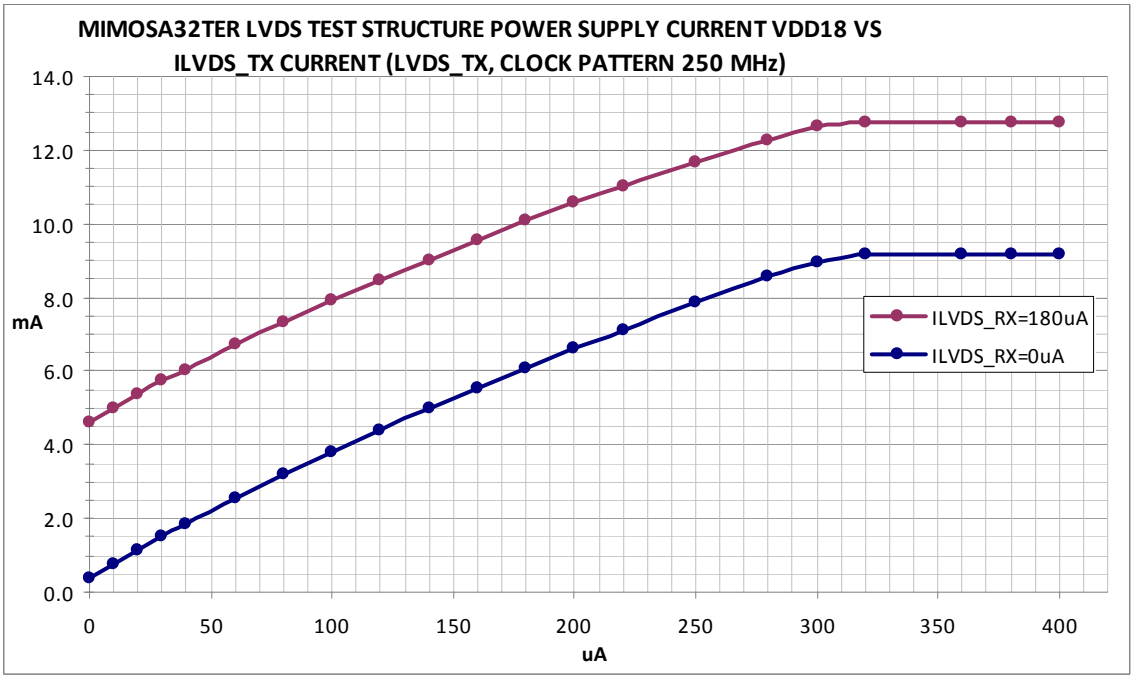


Figure 7. Power supply (VDD18) current of the LVDS test structure (LVDS_TX selected) vs. bias current ILVDS_TX

6.2 Power Consumption with RSDS_TX Driver

Symbol	Parameters, Conditions	units	Measured Value
$I_{VDD\_RSDS\ STATIC}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, RSDS_TX Driver Enable, Static Condition, ILVDS_RX = 180 µA, ILVDS_TX = 220 µA	mA	3.4
$I_{VDD\_RSDS\ 500Mbps}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, RSDS_TX Driver Enable, Clock Pattern at 500 Mbps ILVDS_RX = 180 µA, ILVDS_TX = 220 µA	mA	7.2
$I_{VDD\_RSDS\ 1000\ Mbps}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, RSDS_TX Driver Enable, Clock Pattern at 1000 Mbps ILVDS_RX = 180 µA, ILVDS_TX = 220 µA	mA	8.4
$I_{VDD\_RSDS\ STATIC\ ,ILVDS\_TX=0}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, RSDS_TX Driver Enable, Static Condition, ILVDS_RX = 180 µA, ILVDS_TX = 0 µA	mA	0.8
$I_{VDD\_RSDS\ 500Mbps,ILVDS\_TX=0}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, RSDS_TX Driver Enable, Clock Pattern at 500 Mbps ILVDS_RX = 180 µA, ILVDS_TX = 0 µA	mA	4.8
$I_{VDD\_RSDS\ 1000Mbps,ILVDS\_TX=0}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, RSDS_TX Driver Enable, Clock Pattern at 1000 Mbps ILVDS_RX = 180 µA, ILVDS_TX = 0 µA	mA	6.1
$I_{VDD\_RSDS\ STATIC\ ,\ ILVDS\_RX=0}$	VDD= 1.8 V supply current, LVDS_RX Receiver Enable, RSDS_TX Driver Enable, Static Condition, ILVDS_RX = 0 µA, ILVDS_TX = 220 µA	mA	2.8

In Figure 8 is shown the 1.8V power supply (VDD18) current of the LVDS test structure versus the input data clock frequency. The measurements are performed in two different ILVDS_TX bias current conditions: ILVDS_TX = 0 µA and ILVDS_TX = 220 µA. The LVDS Receiver bias current is 180 µA.

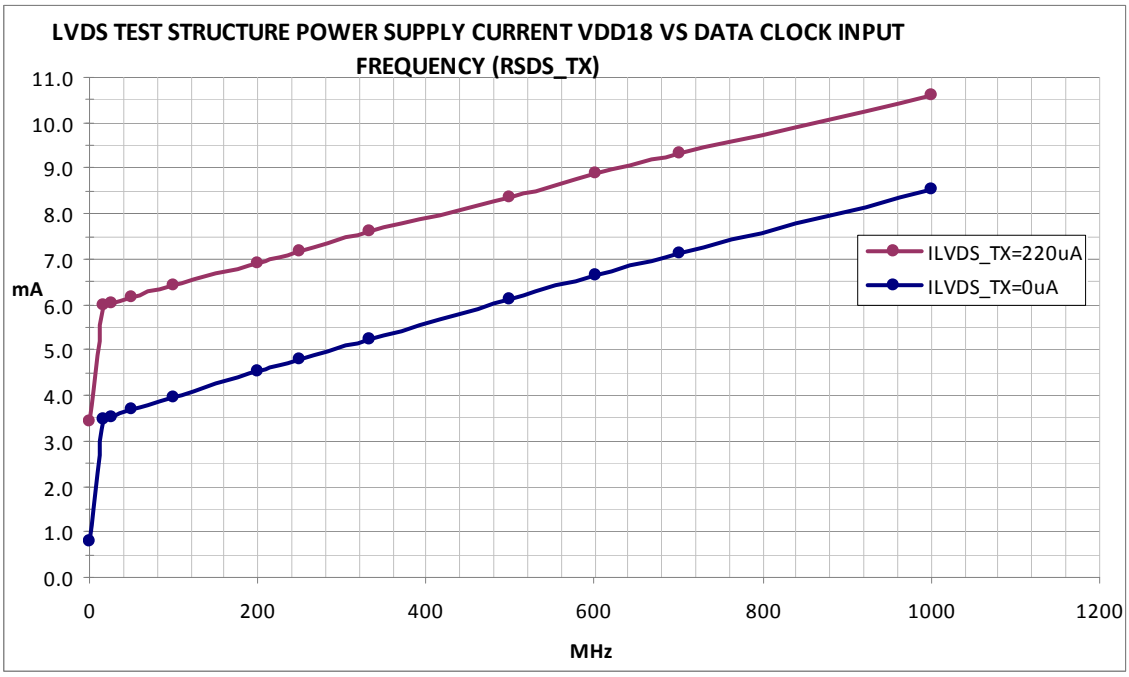


Figure 8. Power supply (VDD18) current of the LVDS test structure (RSDS_TX selected) vs. data input clock frequency

In Figure 9 is shown the 1.8V power supply (VDD18) current of the LVDS test structure versus the bias current ILVDS_TX. The measurements are performed in two different ILVDS_RX bias current conditions: ILVDS_RX = 0 µA (Static Condition) and ILVDS_RX = 180 µA. The input data clock frequency is 250 MHz.

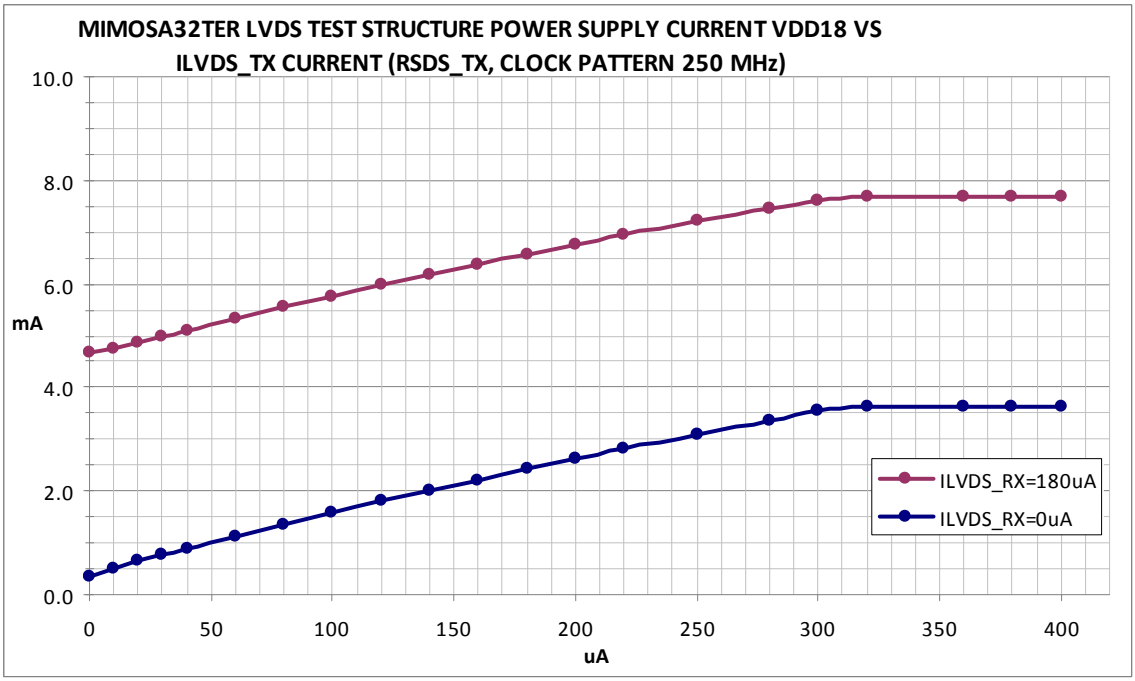


Figure 9. Power supply (VDD18) current of the LVDS test structure (RSDS_TX selected) vs. bias current ILVDS_TX

7 LVDS Receiver and LVDS Driver Jitter Performance

The LVDS Receiver and Driver jitter performances are measured ensemble. An evaluation board for Xilinx Kintex-7 is used as a data pattern generator. A block diagram of the data pattern generator configurations can be found in Appendix A and Appendix B.

7.1 Direct output Measurement

In Figure 10 is presented a block diagram of a direct output measurement configuration for the LVDS Driver. In this configuration the output signal of the LVDS Driver is measured with a short connection to the differential probe.

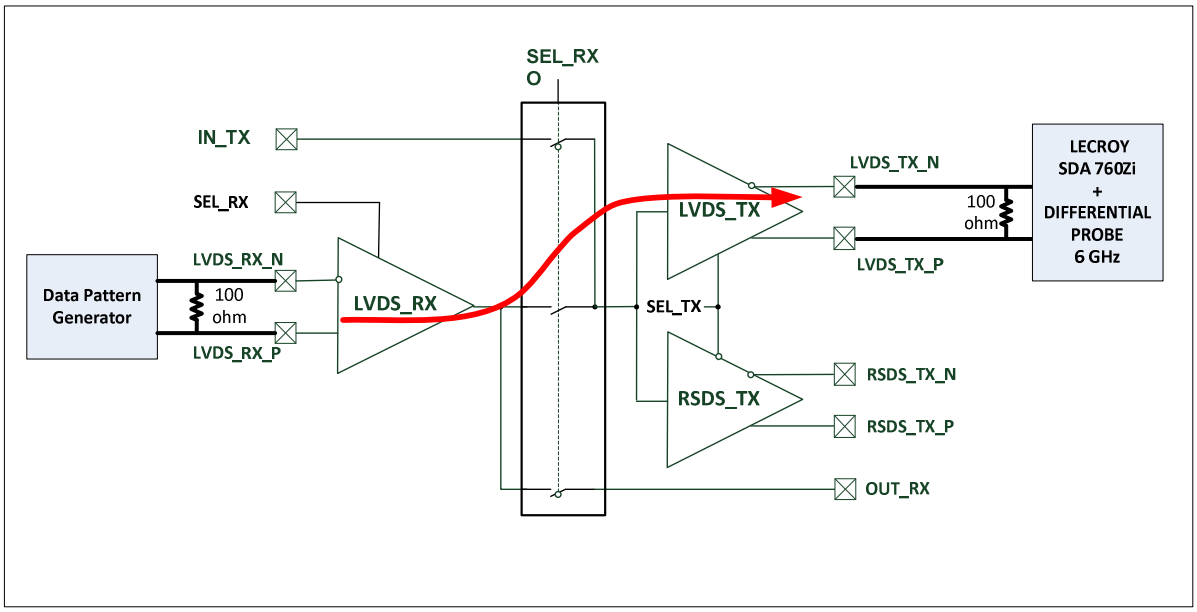


Figure 10. Direct Measurement Configuration for the LVDS Driver

7.2 Differential Transmission Line Measurement

In Figure 11 is presented a block diagram of a differential transmission line measurement configuration for the LVDS Driver. The length of the differential transmission line is 30 cm or 60 cm.

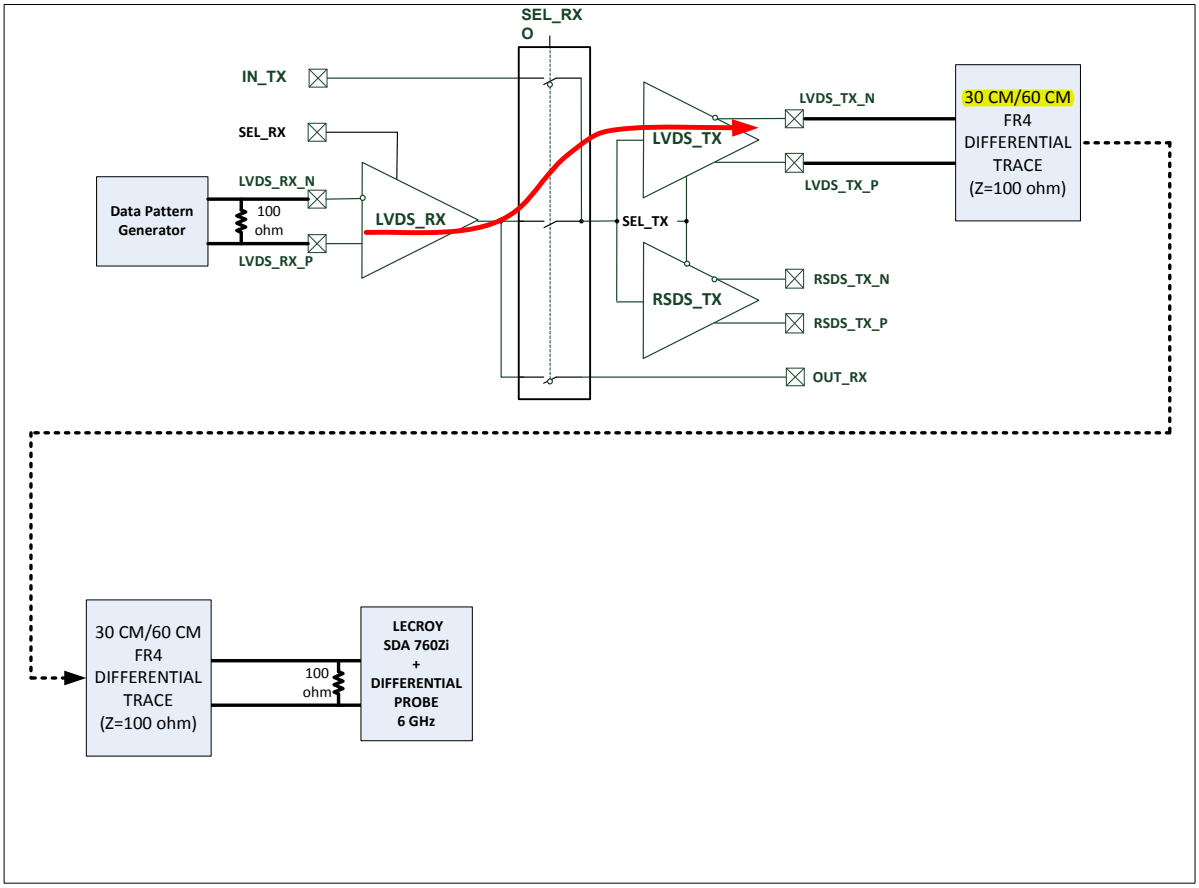


Figure 11. Differential Transmission Line Measurement Configuration for the LVDS Driver

7.3 Differential Transmission Line Measurement with the LVDS Receiver

In Figure 12 is presented a block diagram of a differential transmission line with the LVDS Receiver measurement configuration for the LVDS Driver. The length of the differential transmission line is 30 cm or 60 cm.

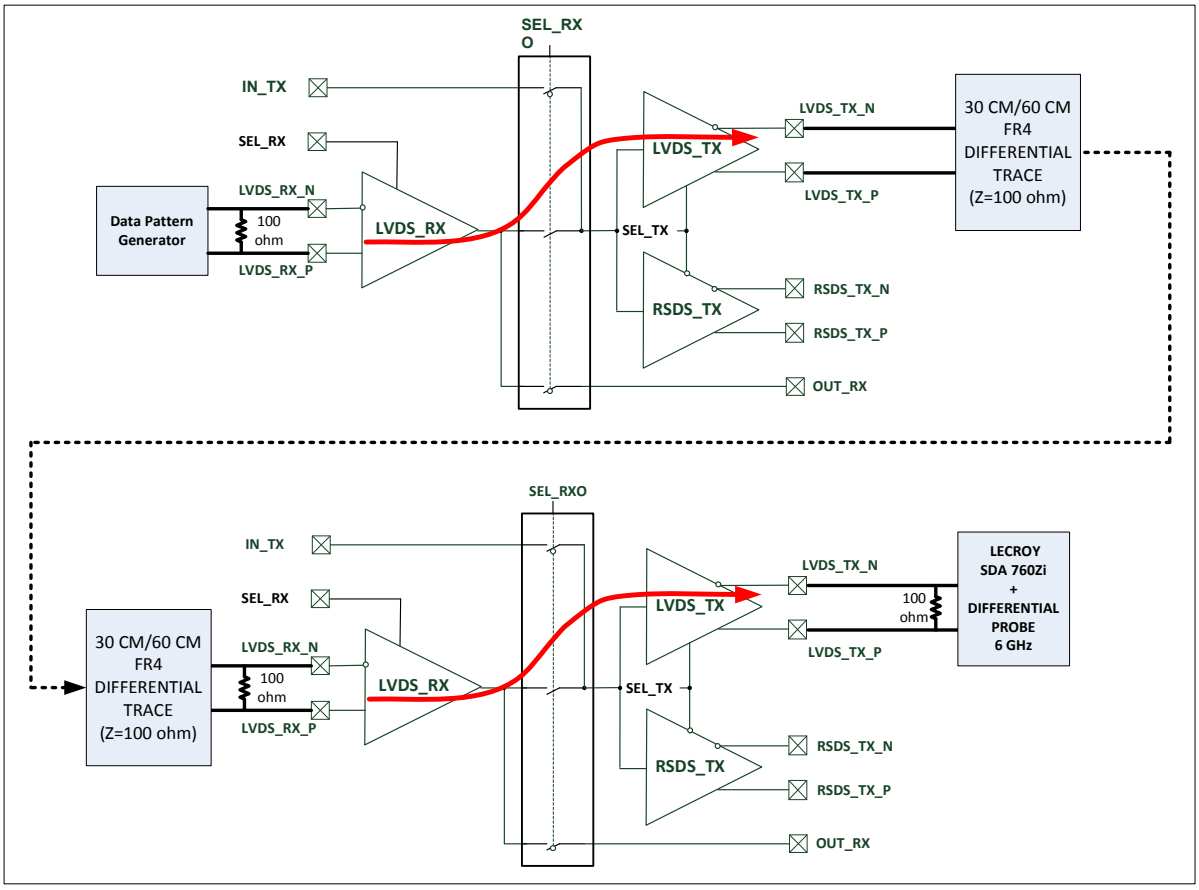


Figure 12. Differential Transmission Line with the LVDS Receiver Measurement Configuration for the LVDS Driver

7.4 Jitter Performance with clock data pattern

Following signal names are used in Legends of Figures in Chapter 7.

Name	Parameter
INPUT	Data Pattern is generated by Xilinx Kintex-7 with IBERT SCAN IP. The Cross-point Switch output LVDS signal (DS25CP152) is used as a input signal.
LVDS_TX	MI32TER_LVDS Board N° 1 board, See the Fig.10
LVDS_TX_30CM	MI32TER_LVDS Board N° 1 board, the LVDS Driver drives the Differential Transmission Line of 30 cm. See the Fig 11
LVDS_TX_60CM	MI32TER_LVDS Board N° 1 board, the LVDS Driver drives the Differential Transmission Line of 60 cm. See the Fig 12
LVDS_RX_TX_30CM_RX	MI32TER_LVDS Board N° 1 board works as a receiver for the Data Pattern Generator. The LVDS driver of the MI32TER_LVDS Board N° 1 board drives the Differential Transmission Line of 30 cm. This Transmission Line is connected to the LVDS receiver of the MI32TER_LVDS Board N° 2 board.
LVDS_RX_TX_60CM_RX	MI32TER_LVDS Board N° 1 board works as a receiver for the Data Pattern Generator. The LVDS driver of the MI32TER_LVDS Board N° 1 board drives the Differential Transmission Line of 60 cm. This Transmission Line is connected to the LVDS receiver of the MI32TER_LVDS Board N° 2 board.

In following Figure is shown the differential output voltage (V_{od}) versus data bit rate.

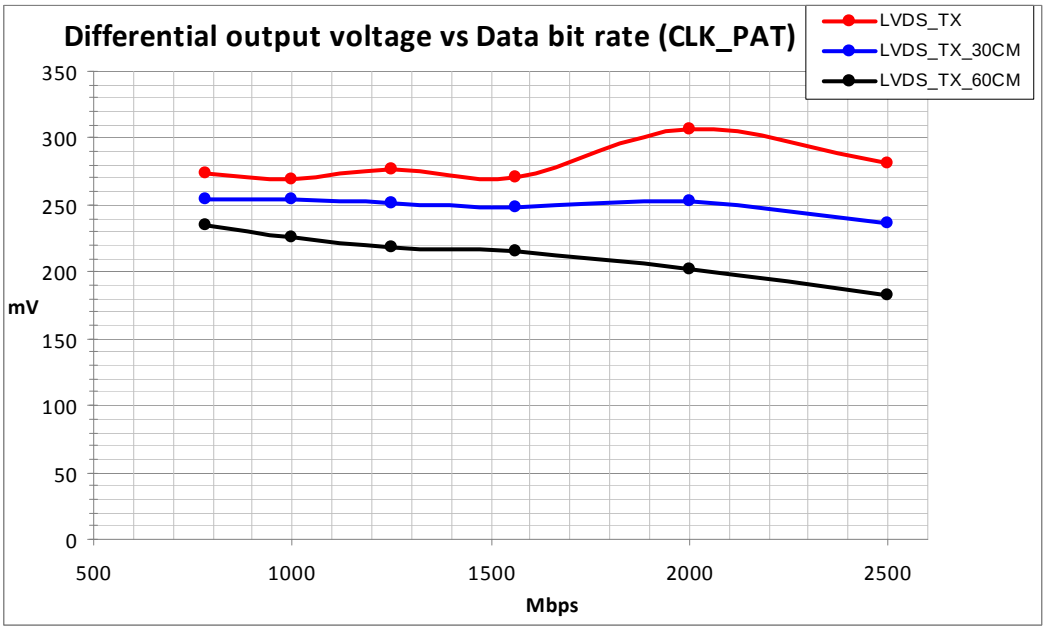


Figure 13. Differential Output Voltage vs. data bit rate (Clock Pattern data)

The Jitter Calculation method is based on extrapolation of Total Jitter (peak-peak) as a function of Bit Error Ratio (10^{-12}) in reasonable measurement time interval (10^6 ... 10^7 samples).

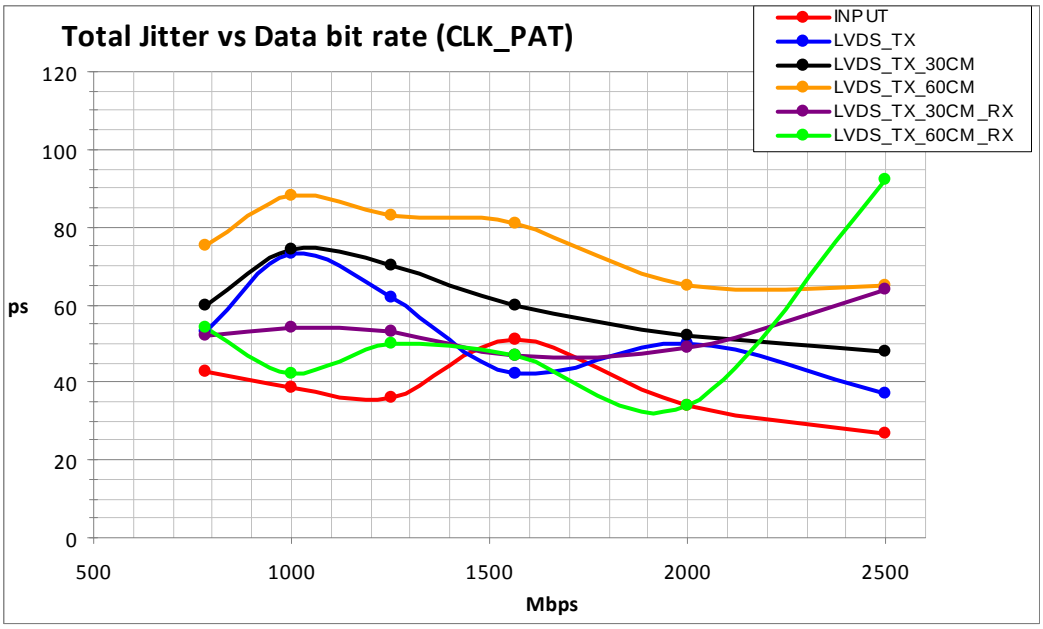


Figure 14. Total Jitter vs. data bit rate (Clock Pattern data)

In following Figure is shown estimated Total Jitter indexed to the corresponding Unit Interval.

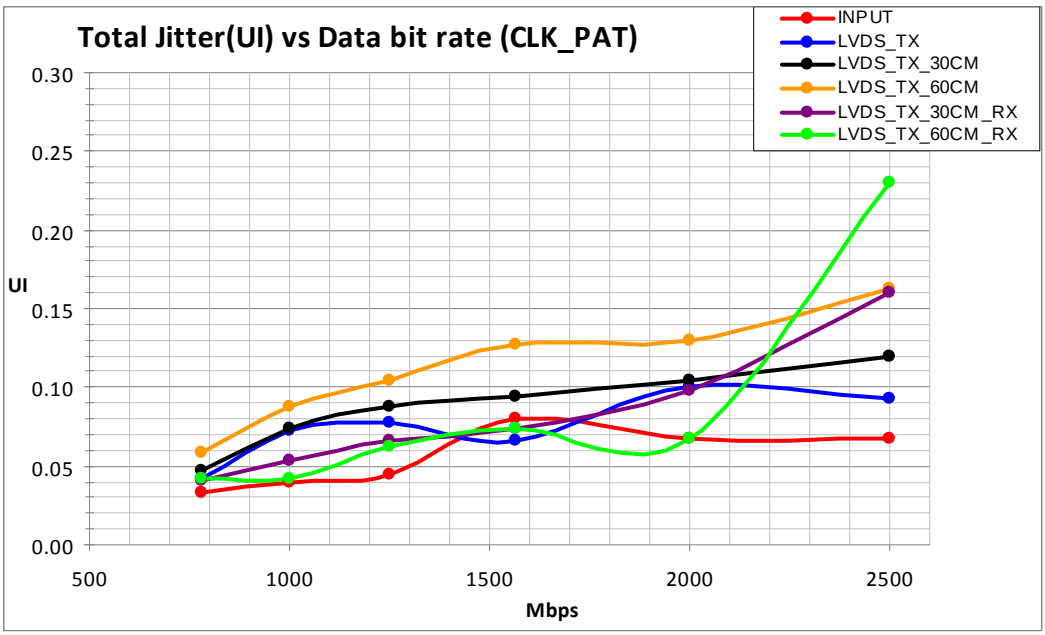


Figure 15. Total Jitter (UI) vs. data bit rate (Clock Pattern data)

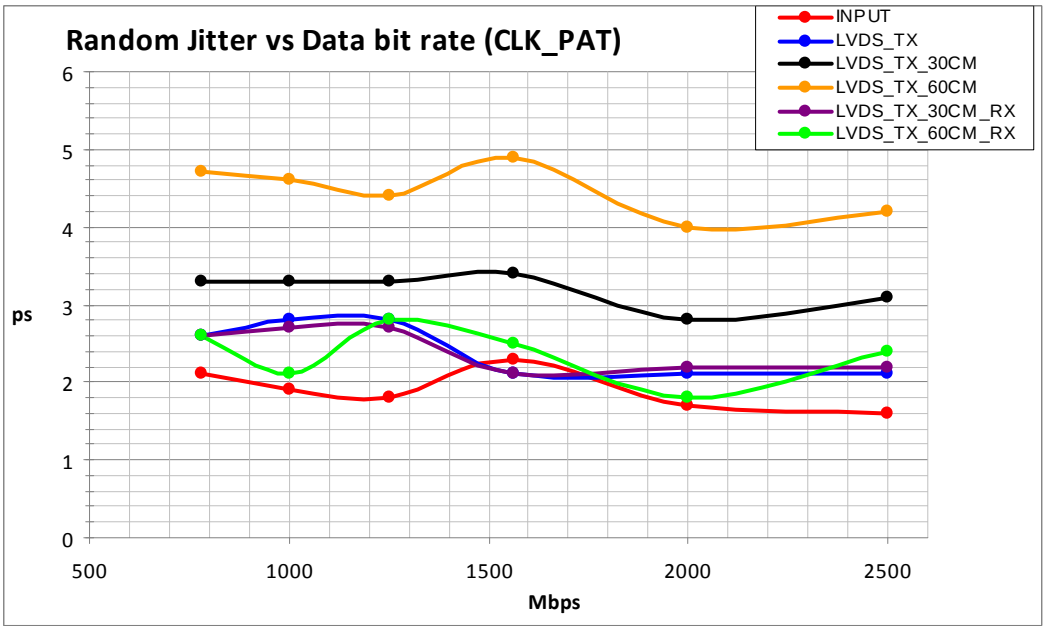


Figure 16. Random Jitter(UI) vs. data bit rate (Clock Pattern data)

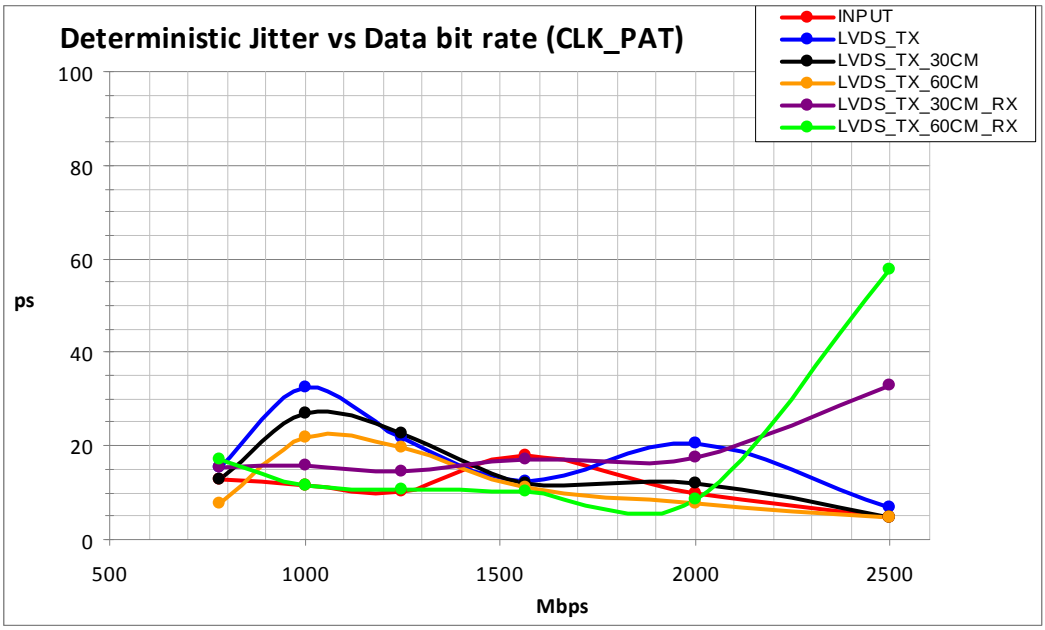


Figure 17. Deterministic Jitter vs. data bit rate (Clock Pattern data)

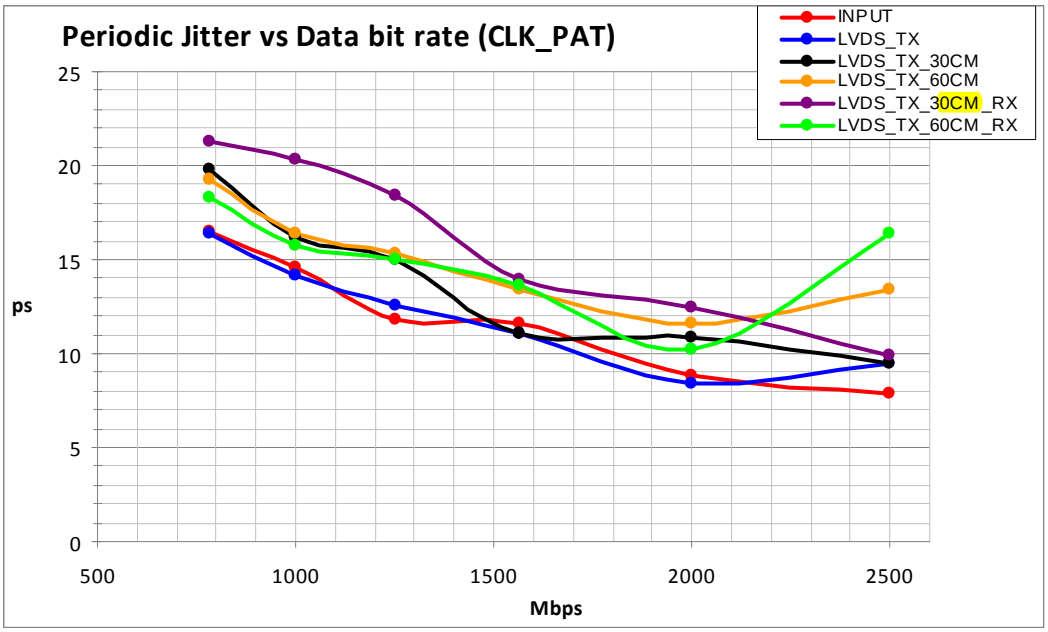


Figure 18. Periodic Jitter vs. data bit rate (Clock Pattern data)

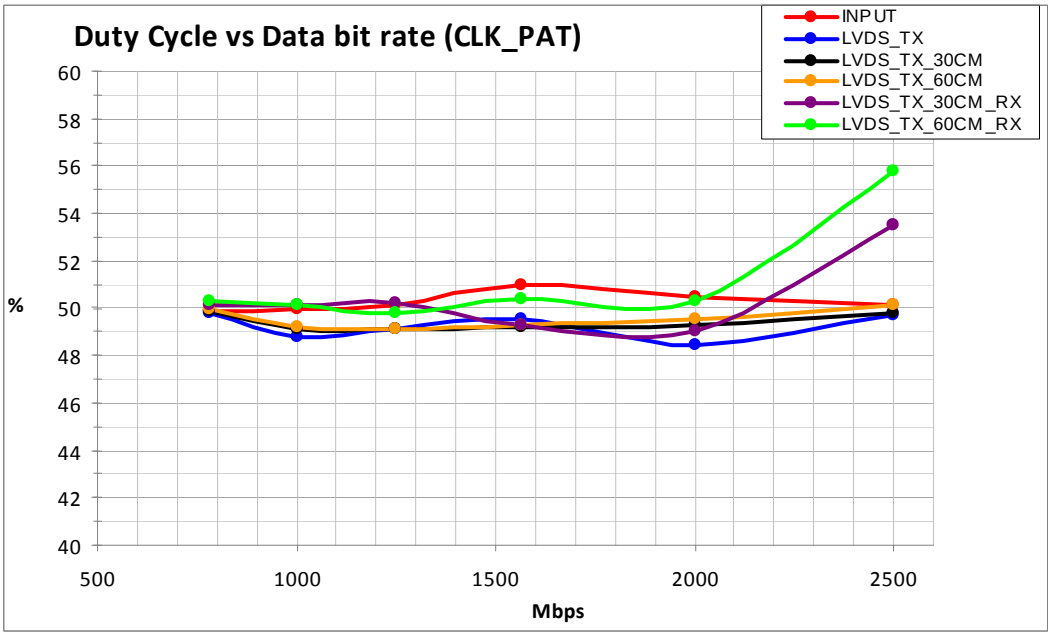


Figure 19. Driver Output Duty Cycle vs. data bit rate (Clock Pattern data)

7.5 Jitter Performance with PRBS7 data pattern

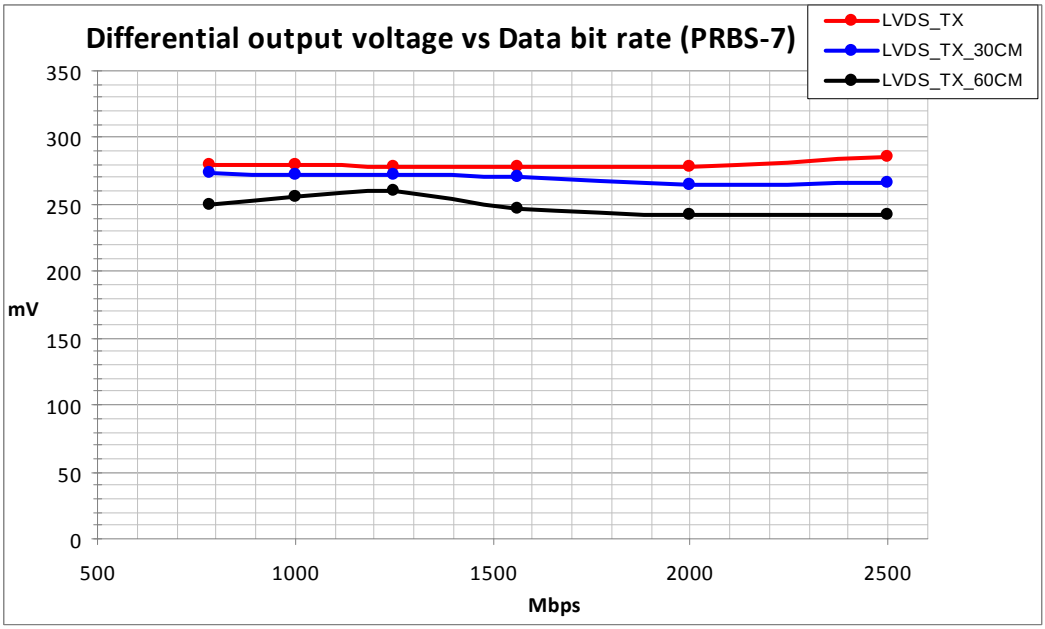


Figure 20. Differential Output Voltage vs. data bit rate (PRBS-7 Pattern data)

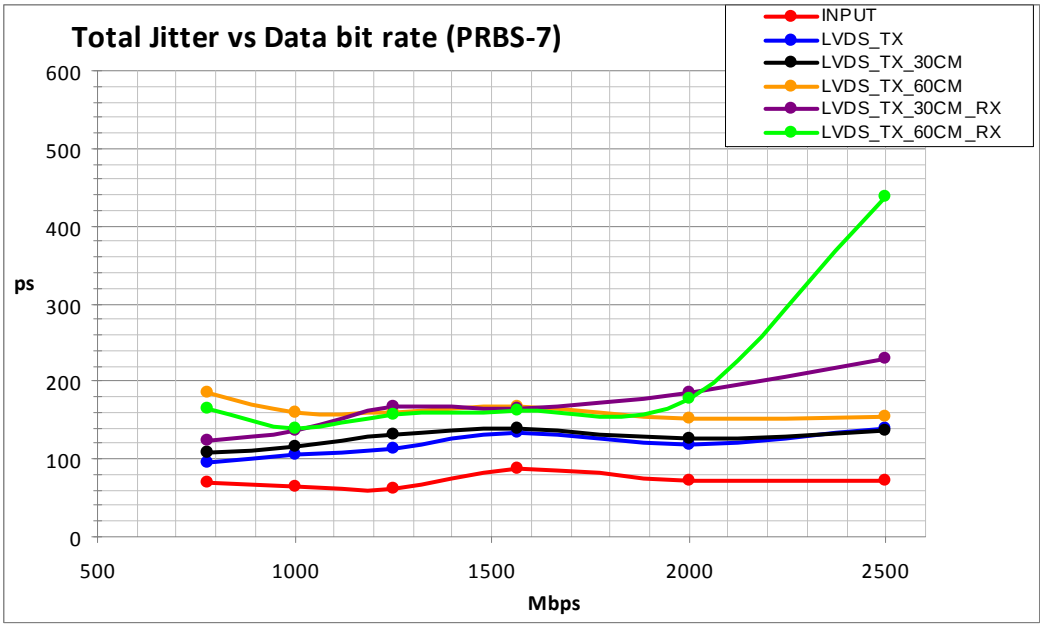


Figure 21. Total Jitter vs. data bit rate (PRBS-7 Pattern data)

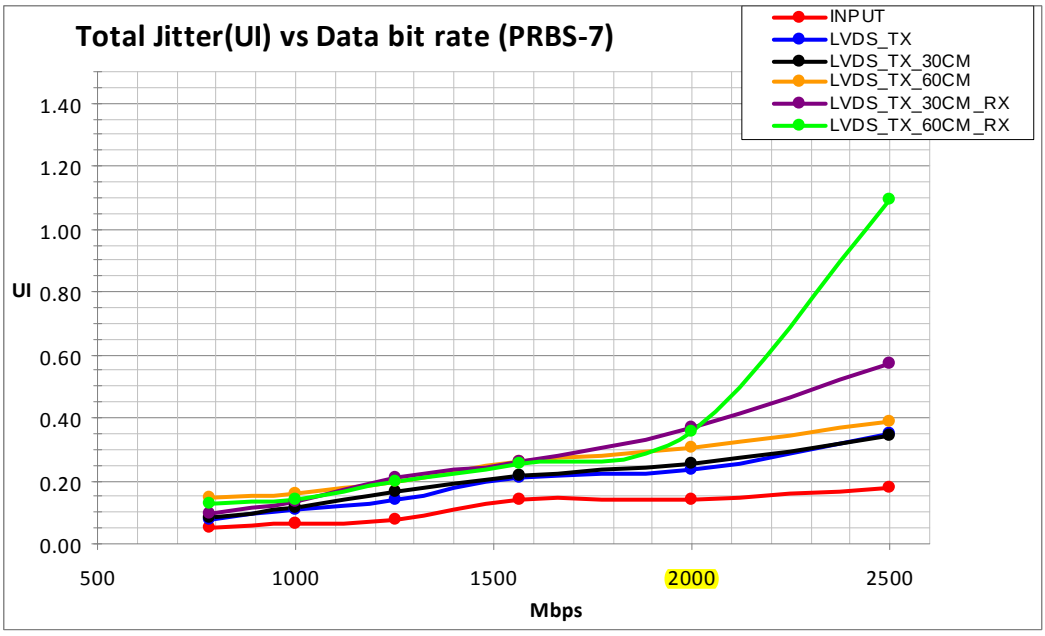


Figure 22. Total Jitter (UI) vs. data bit rate (PRBS-7 Pattern data)

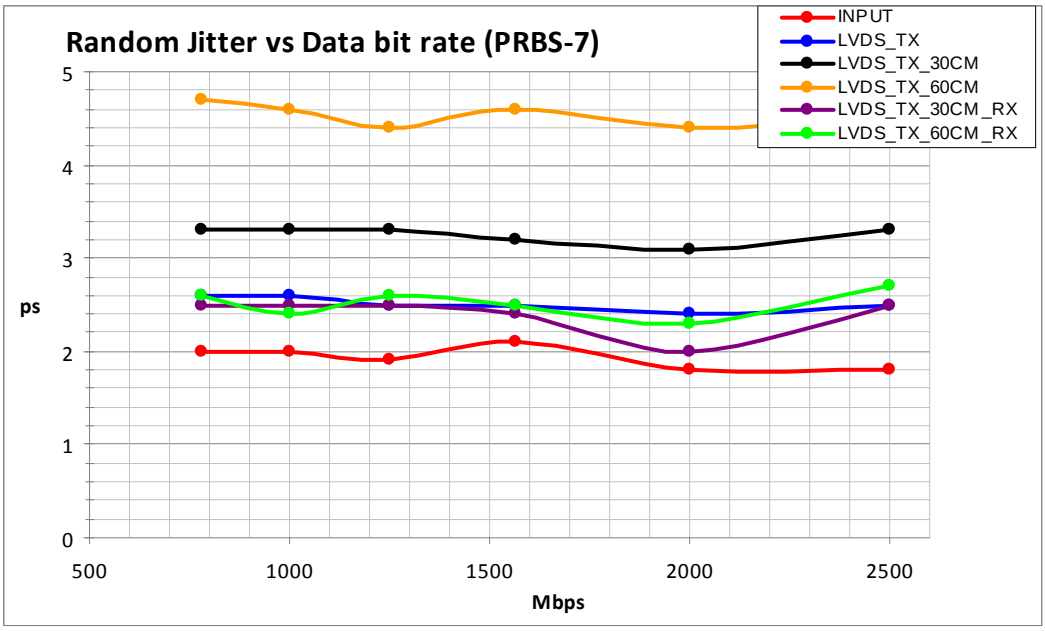


Figure 23. Random Jitter(UI) vs. data bit rate (PRBS-7 Pattern data)

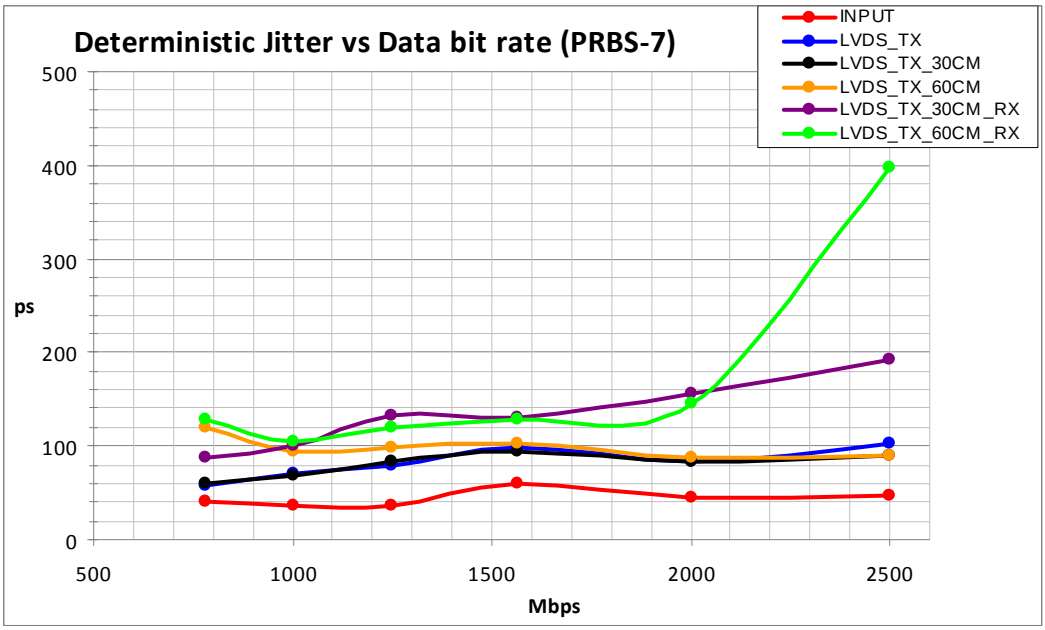


Figure 24. Deterministic Jitter vs. data bit rate (PRBS-7 Pattern data)

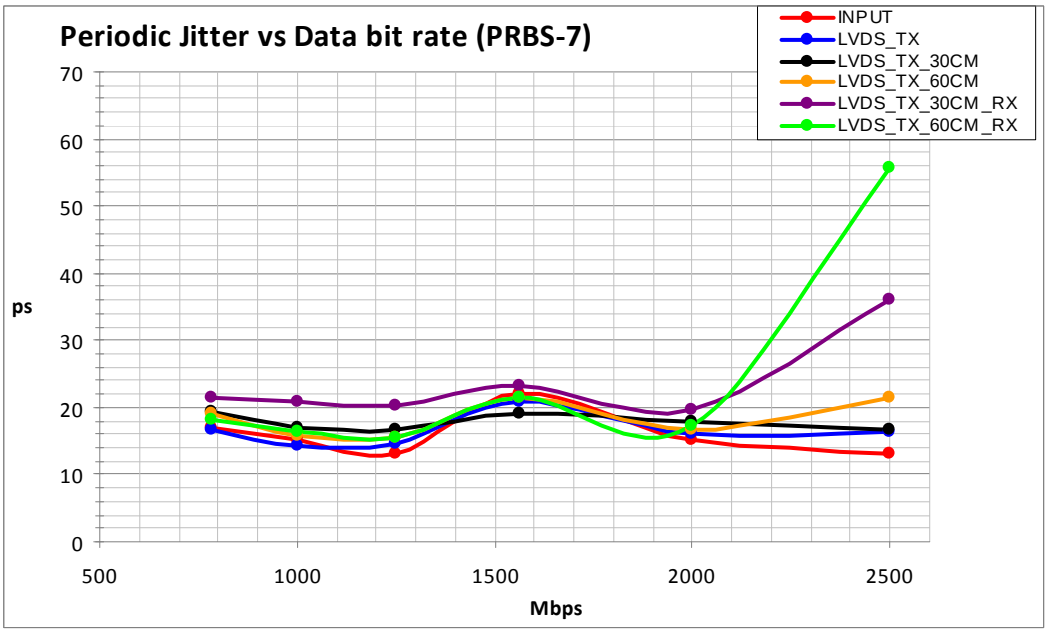


Figure 25. Periodic Jitter vs. data bit rate (PRBS-7 Pattern data)

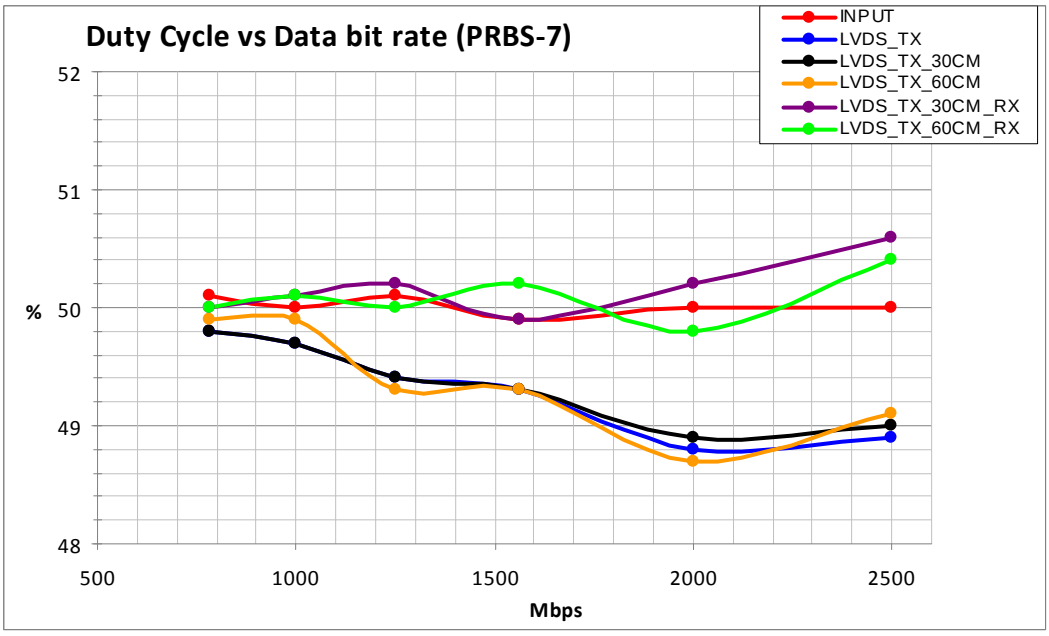


Figure 26. Driver Output Duty Cycle vs. data bit rate (PRBS-7 Pattern data)

8 LVDS Receiver and RSDS Driver Jitter Performance

8.1 Direct output Measurement

In following Figure is presented a block diagram of a direct output measurement configuration for the RSDS Driver. In this configuration the output signal of the RSDS Driver is measured with a short connection to the differential probe.

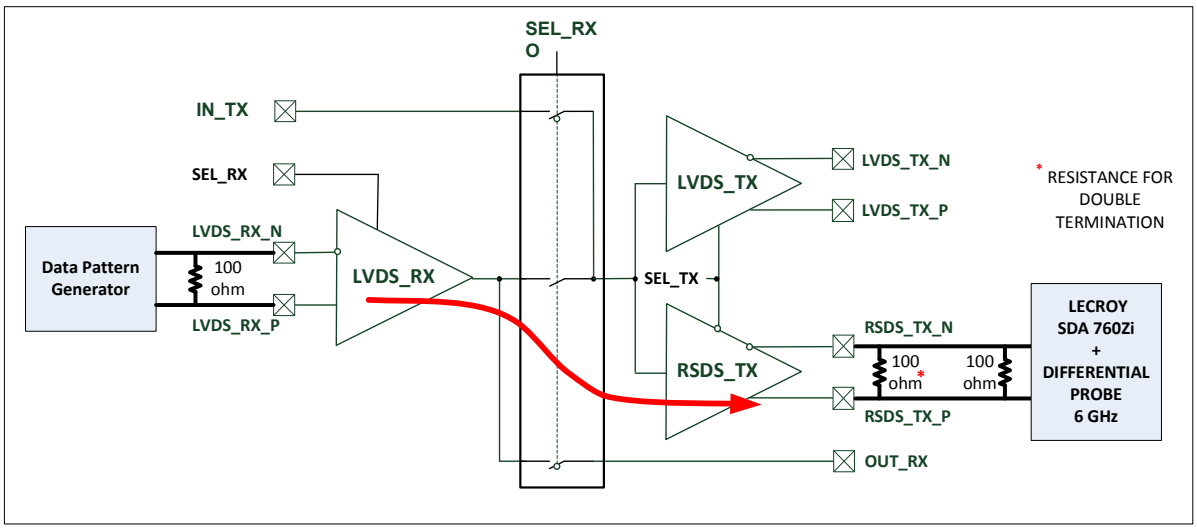


Figure 27. Direct Measurement Configuration for the RSDS Driver

8.2 Differential Transmission Line Measurement

In following Figure is presented a block diagram of a differential transmission line measurement configuration for the RSDS Driver. The length of the differential transmission line is 30 cm.

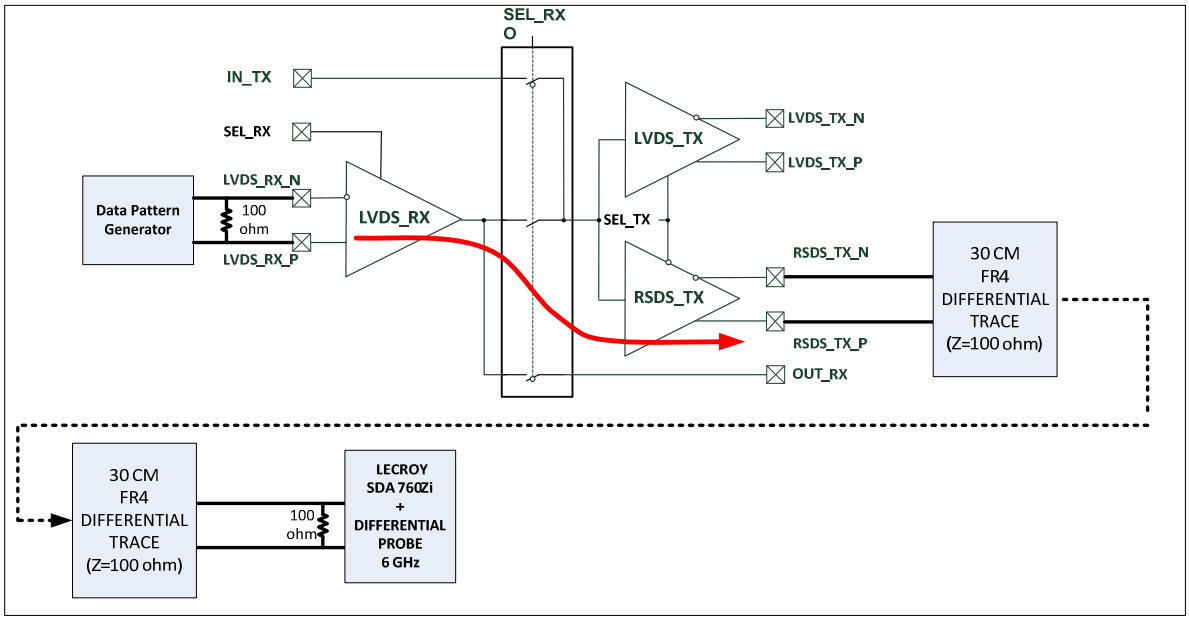


Figure 28. Differential Transmission Line Measurement Configuration for the RSDS Driver

8.3 Differential Transmission Line Measurement with the LVDS Receiver

In following Figure is presented a block diagram of a differential transmission line measurement configuration for the RSDS Driver with the LVDS Receiver.

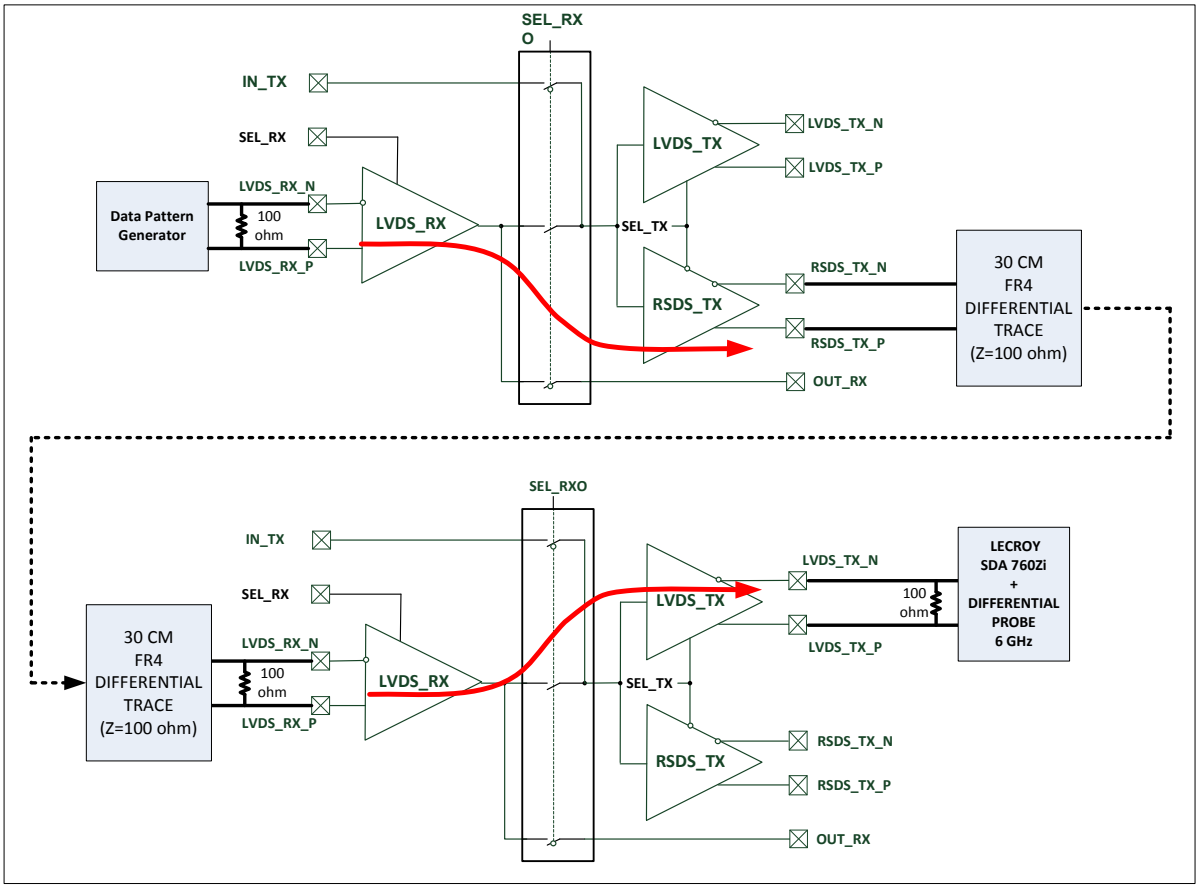


Figure 29. Differential Transmission Line Measurement Configuration for the RSDS Driver

8.4 Jitter Performance with clock data pattern

Following signal names are used in Legends of Figures in Chapter 8.

Name	Parameter
INPUT	Data Pattern is generated by Xilinx Kintex-7 with IBERT SCAN IP. The Cross-point Switch output LVDS signal (DS25CP152) is used as a input signal.
RSDS_TX	MI32TER_LVDS Board N° 1 board, See the Fig.27
RSDS_TX_30CM	MI32TER_LVDS Board N° 1 board, the RSDS Driver drives the Differential Transmission Line of 30 cm. See the Fig 28
RSDS_RX_TX_30CM	MI32TER_LVDS Board N° 1 board works as a receiver for the Data Pattern Generator. The RSDS driver of the MI32TER_LVDS Board N° 1 board drives the Differential Transmission Line of 30 cm. This Transmission Line is connected to the LVDS receiver of the MI32TER_LVDS Board N° 2 board.

In following Figure is shown the differential output voltage (V_{od}) versus data bit rate.

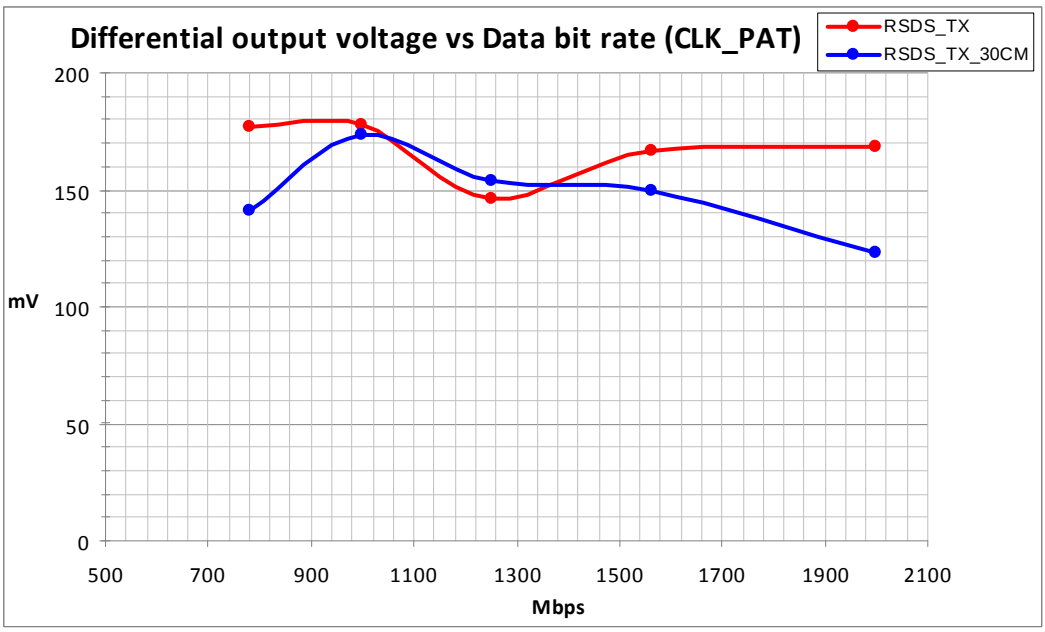


Figure 30. Differential Output Voltage vs. data bit rate (Clock Pattern data)

The Jitter Calculation method is based on extrapolation of Total Jitter (peak-peak) as a function of Bit Error Ratio (10^{-12}) in reasonable measurement time interval (10^6 ... 10^7 samples).

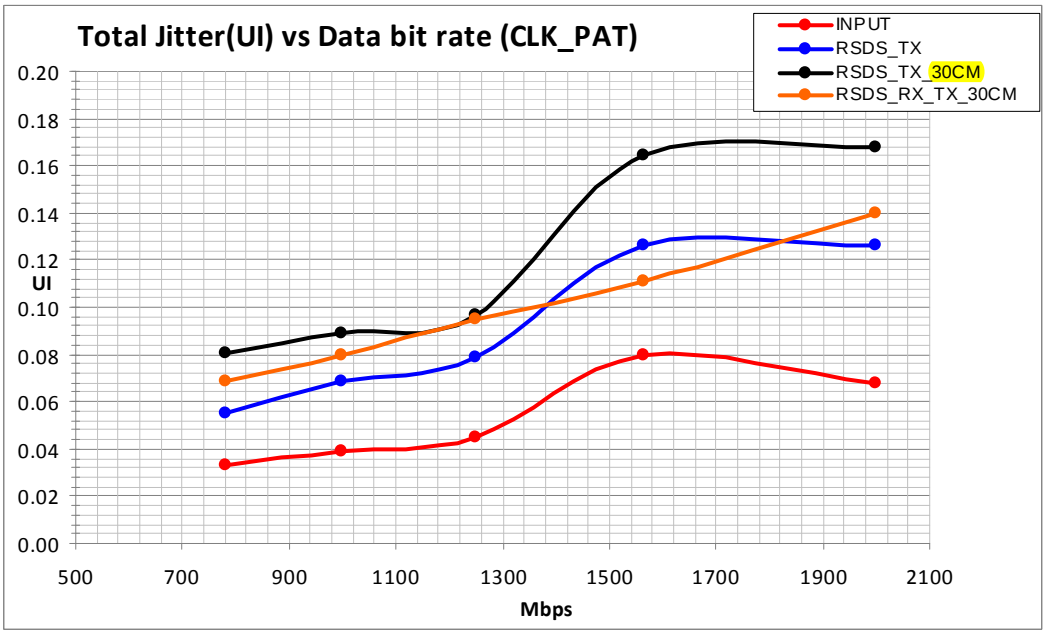


Figure 31. Total Jitter vs. data bit rate (Clock Pattern data)

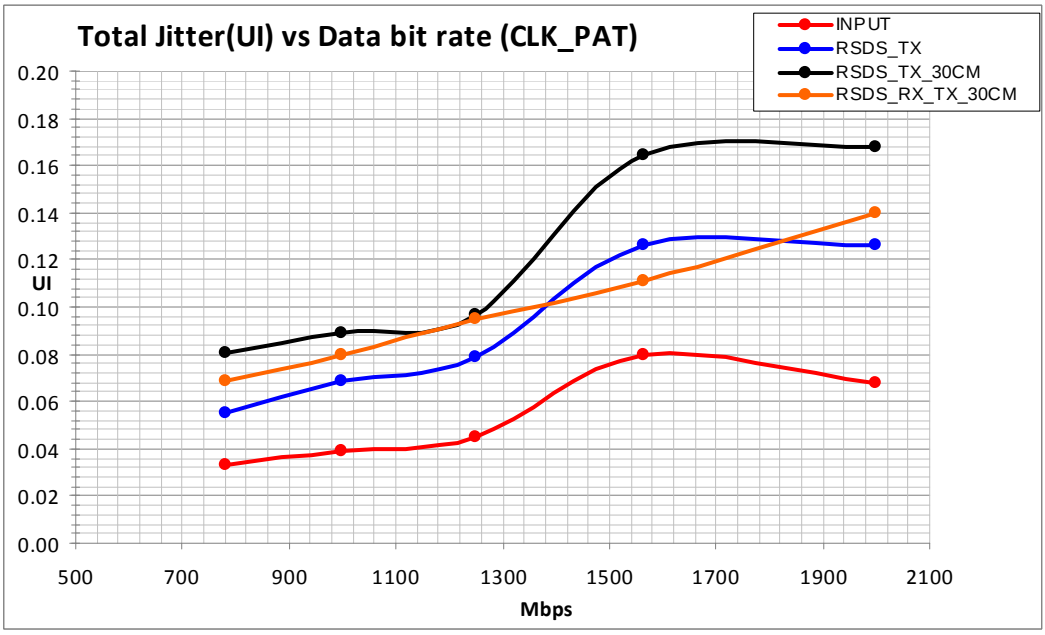


Figure 32. Total Jitter (UI) vs. data bit rate (Clock Pattern data)

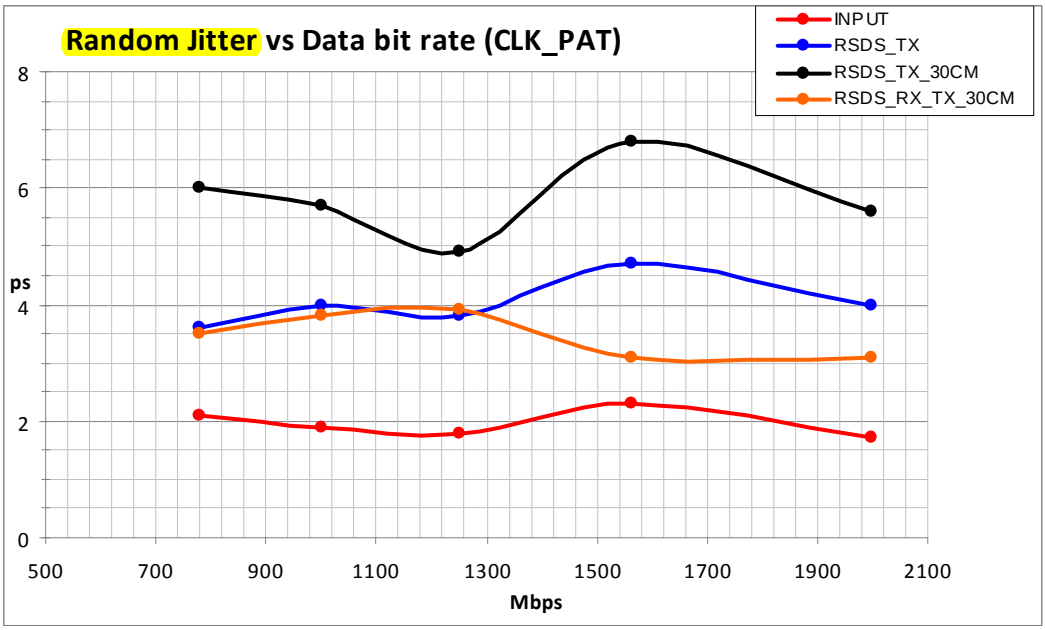


Figure 33. Random Jitter(UI) vs. data bit rate (Clock Pattern data)

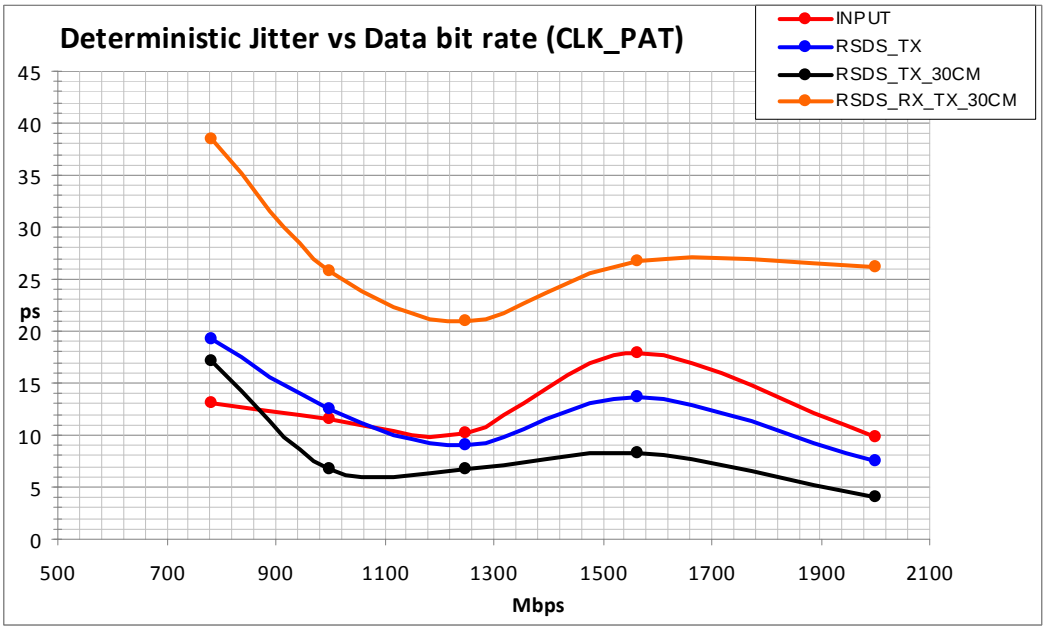


Figure 34. Deterministic Jitter vs. data bit rate (Clock Pattern data)

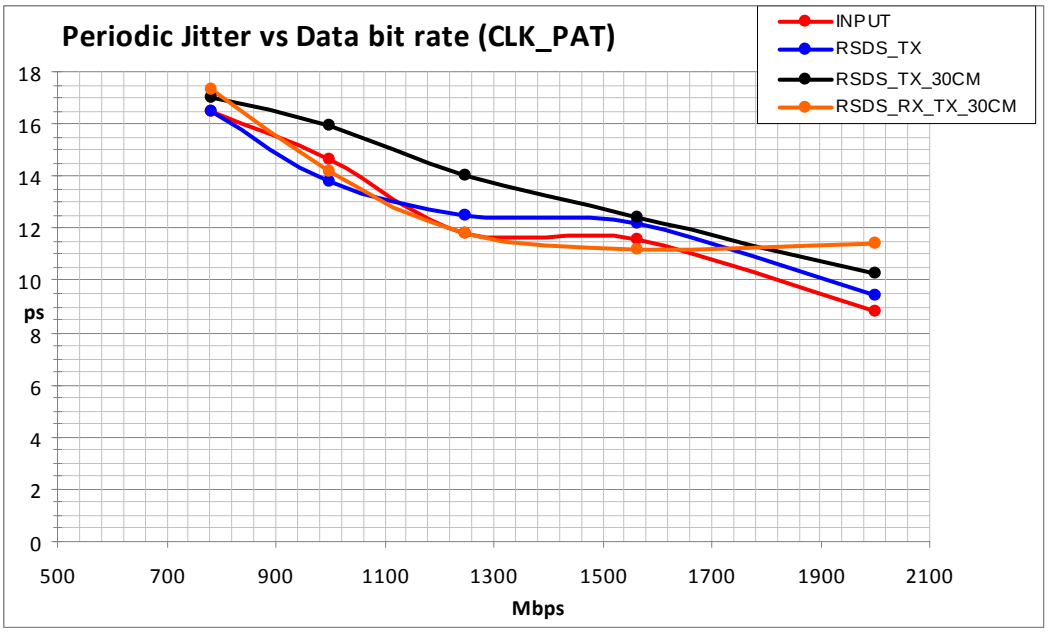


Figure 35. Periodic Jitter vs. data bit rate (Clock Pattern data)

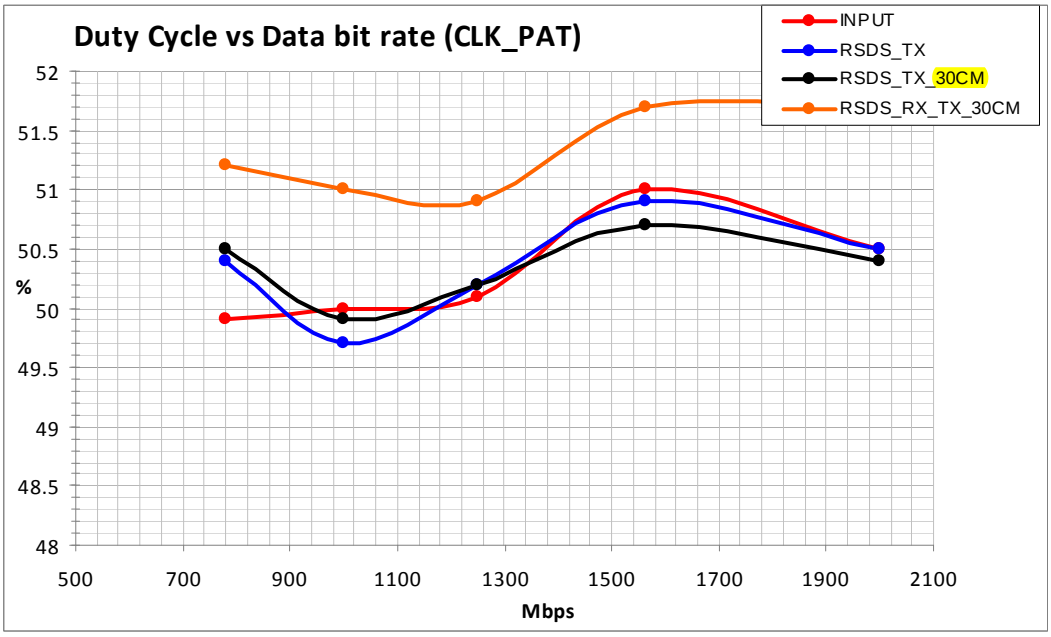


Figure 36. Driver Output Duty Cycle vs. data bit rate (Clock Pattern data)

8.5 Jitter Performance with PRBS7 data pattern

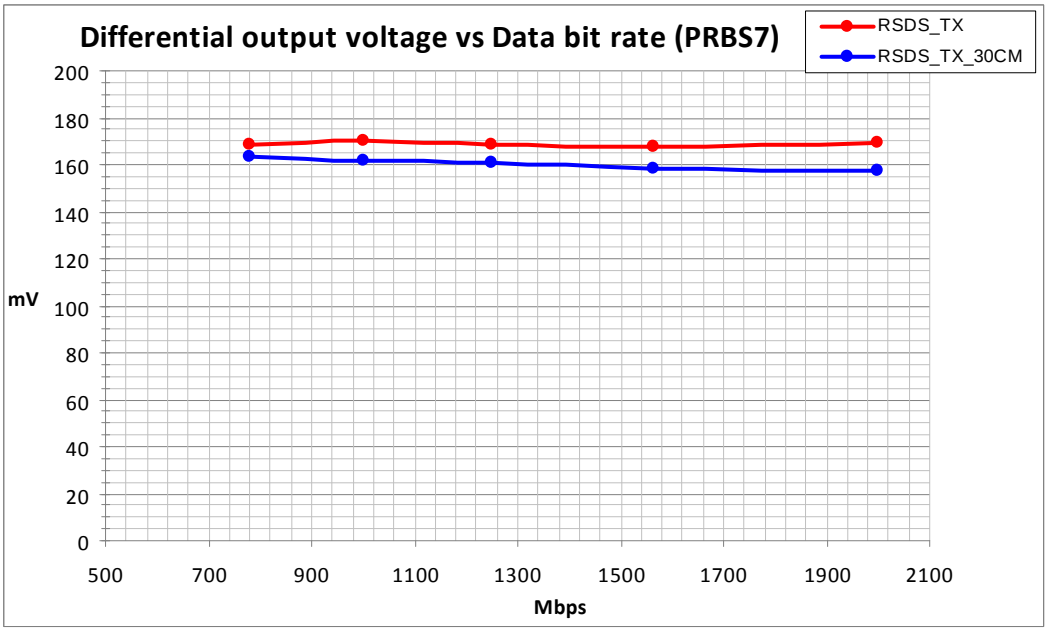


Figure 37. Differential Output Voltage vs. data bit rate (PRBS-7 Pattern data)

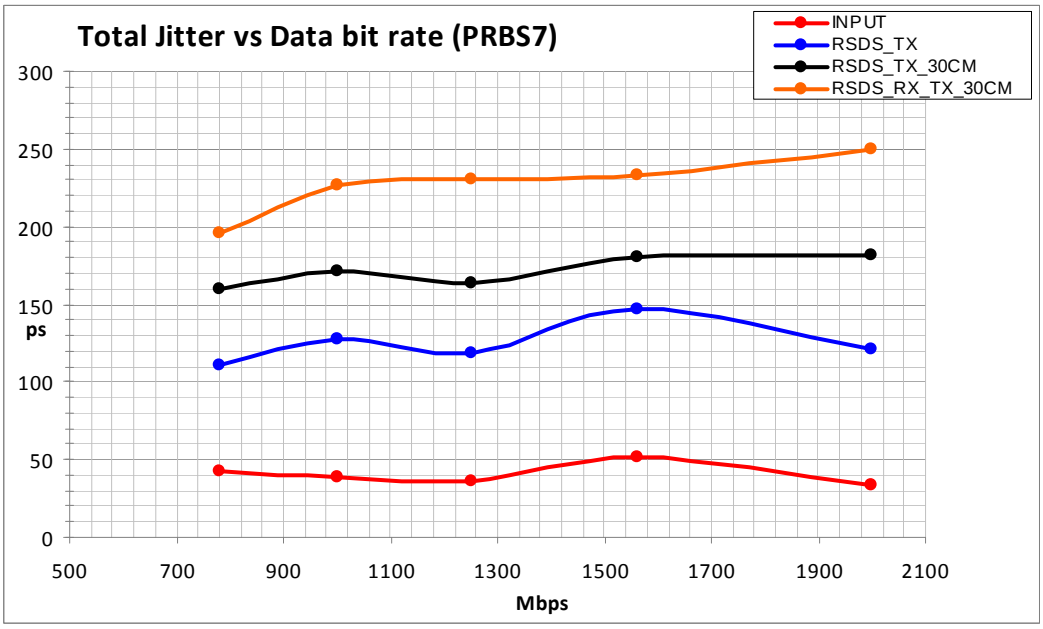


Figure 38. Total Jitter vs. data bit rate (PRBS-7 Pattern data)

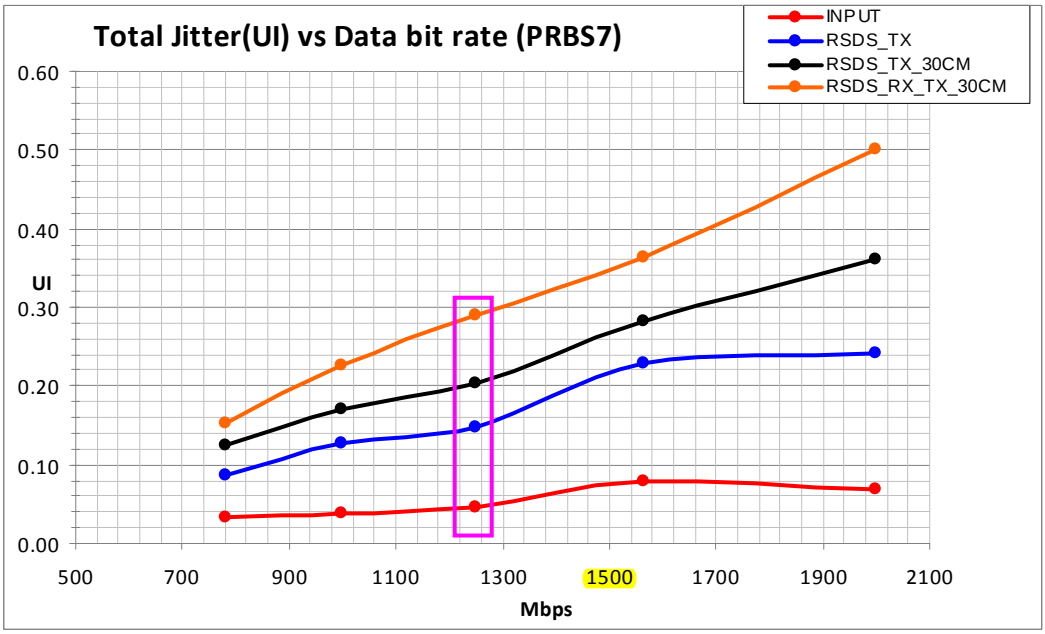


Figure 39. Total Jitter (UI) vs. data bit rate (PRBS-7 Pattern data)

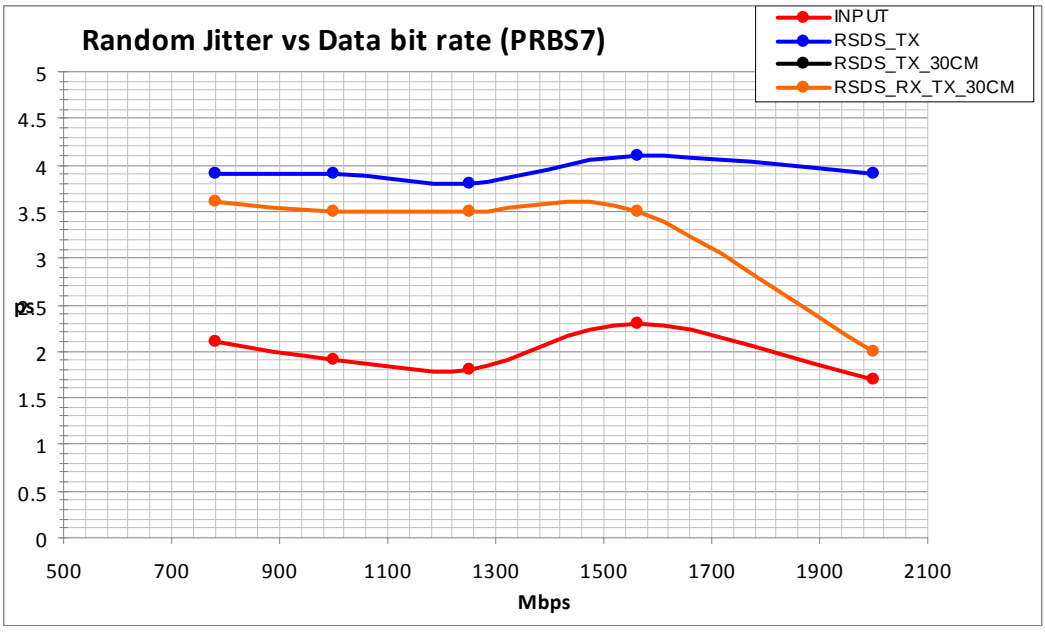


Figure 40. Random Jitter(UI) vs. data bit rate (PRBS-7 Pattern data)

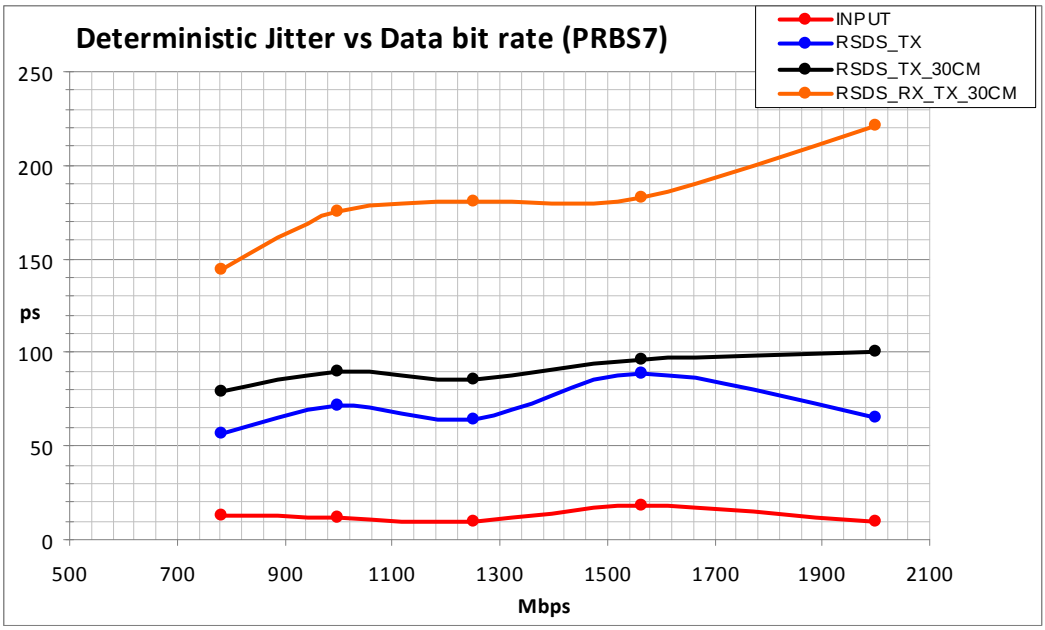


Figure 41. Deterministic Jitter vs. data bit rate (PRBS-7 Pattern data)

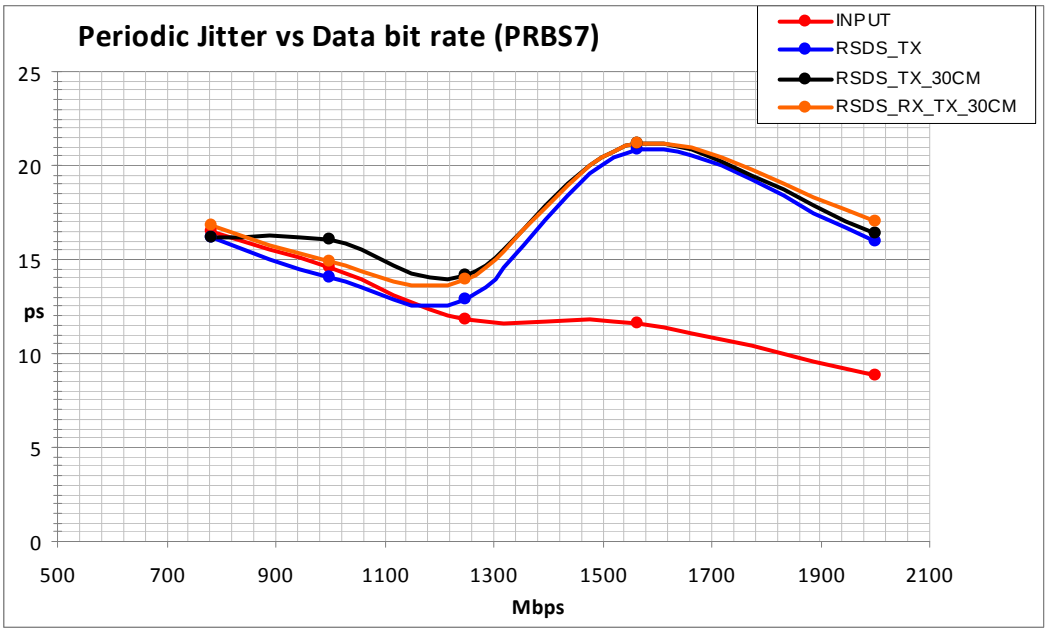


Figure 42. Periodic Jitter vs. data bit rate (PRBS-7 Pattern data)

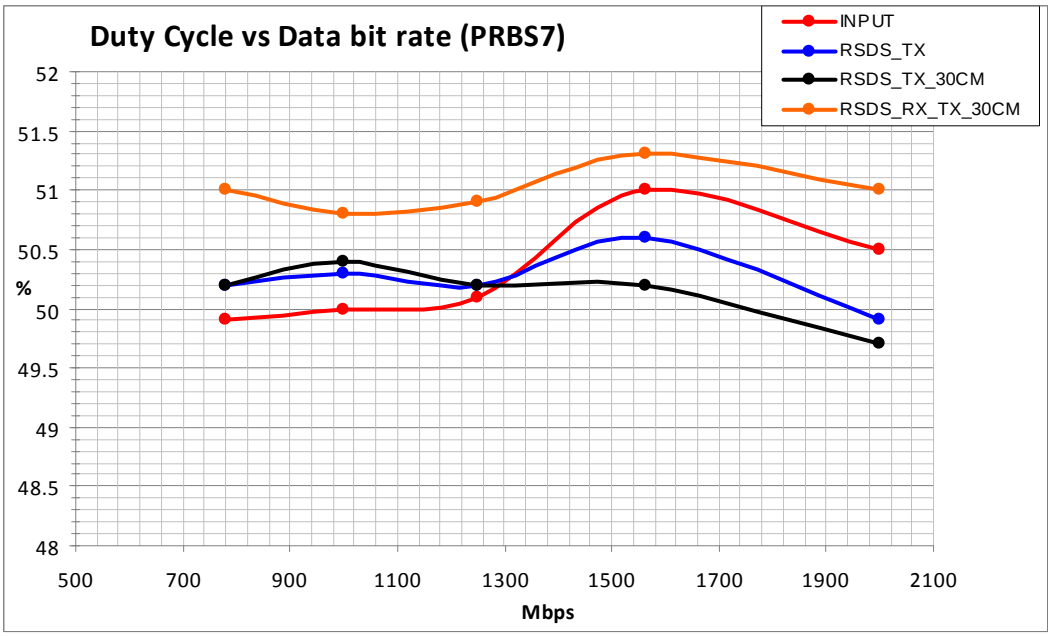


Figure 43. Driver Output Duty Cycle vs. data bit rate (Clock Pattern data)

9 Eye Diagram

The bit error ratio (BER) is a measure of the percentage of bits that a system under test does not transfer data bit correctly. The BER value of 0.0 means that all the data bits were transmitted correctly and at other hand, the BER value of 1.0 means that all the all data bits received are erroneous data.

The BERT Scan is performed with the Xilinx KINTEX-7 Evaluation board by using the BERT Scan IP. A block diagram of the measurement configuration is shown in Appendix C.

There is no appendix C

In following Figures 44 to 46 are shown an Eye Diagram at 2.0 Gbps with PRBS-23 Data Pattern in different length of the transmission line. The Direct Output and the Transmission Line measurement configurations are presented in Chapters 7.1 to 7.2.
In Figures 47 and 48 are shown Eye Diagram with the measurement configuration presented in Chapter 7.3.

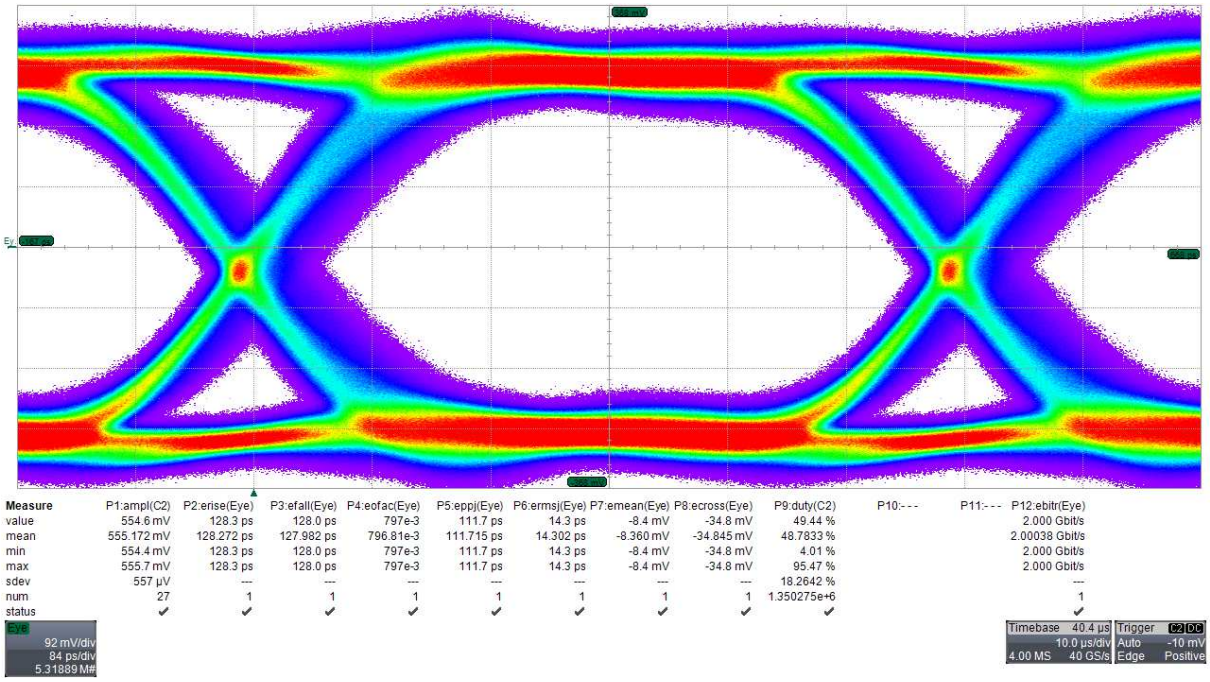


Figure 44. Eye Diagram of LVDS Driver with PRBS-23 Data Pattern at 2 Gbps (Direct output).

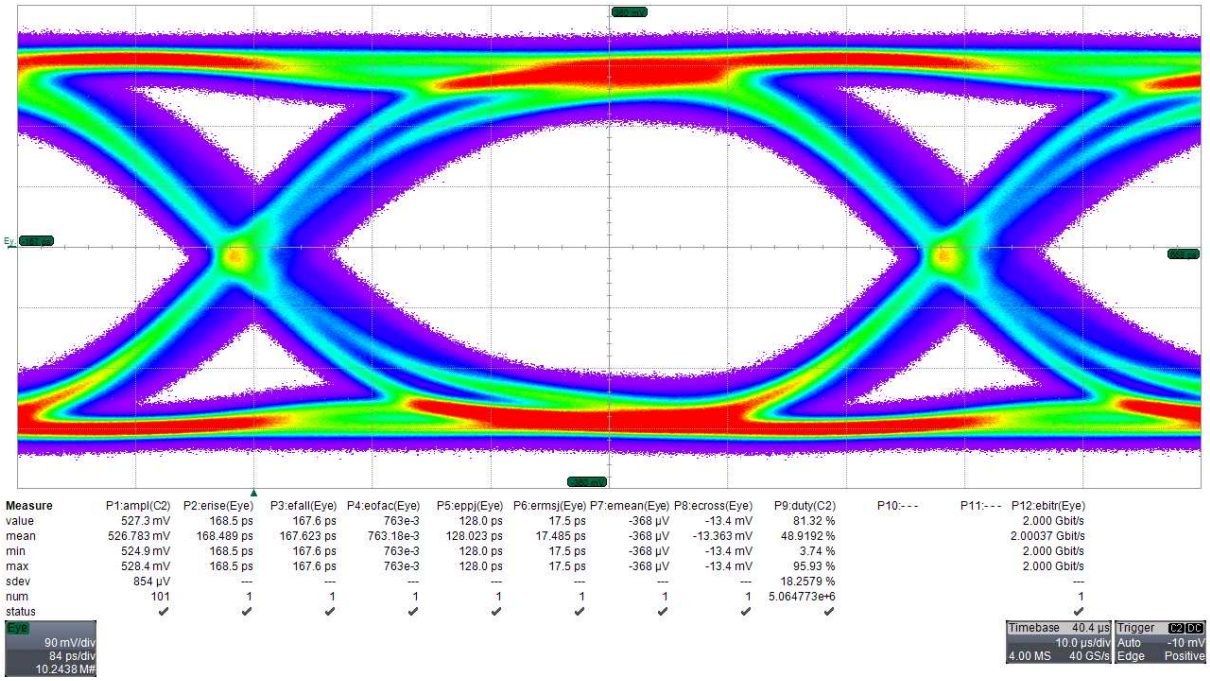


Figure 45. Eye Diagram of LVDS Driver with PRBS-23 Data Pattern at 2 Gbps (Transmission Line of 30 cm).

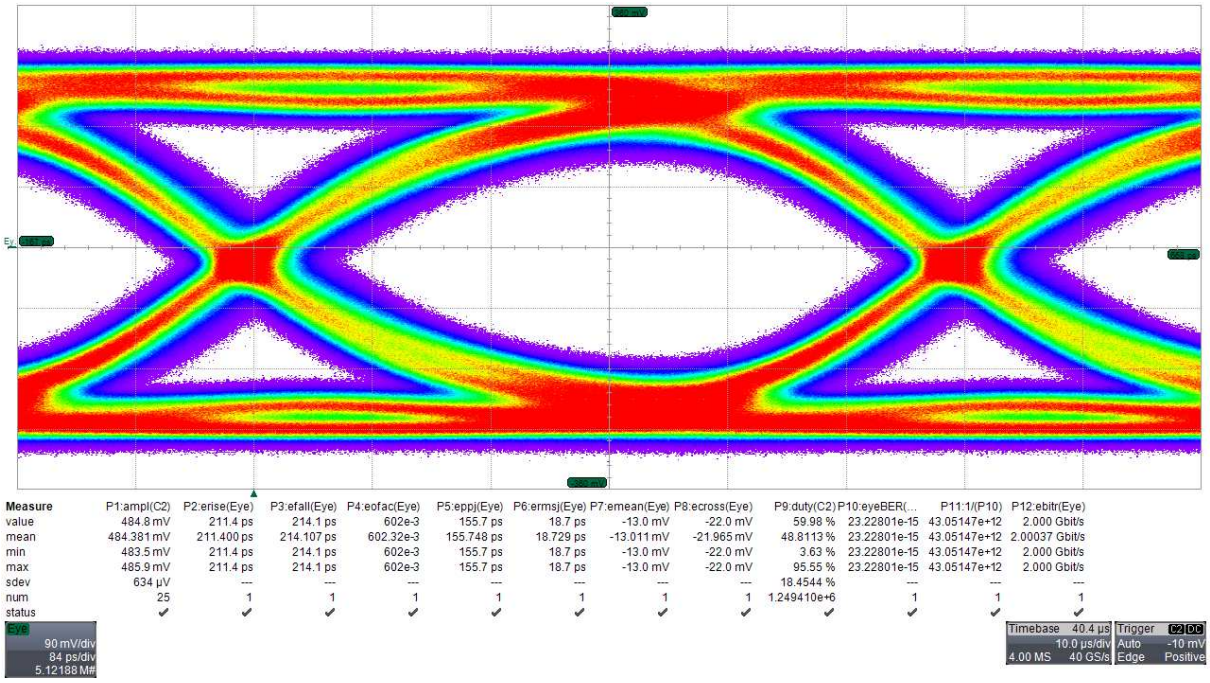


Figure 46. Eye Diagram of LVDS Driver with PRBS-23 Data Pattern at 2 Gbps (Transmission Line of 60 cm).

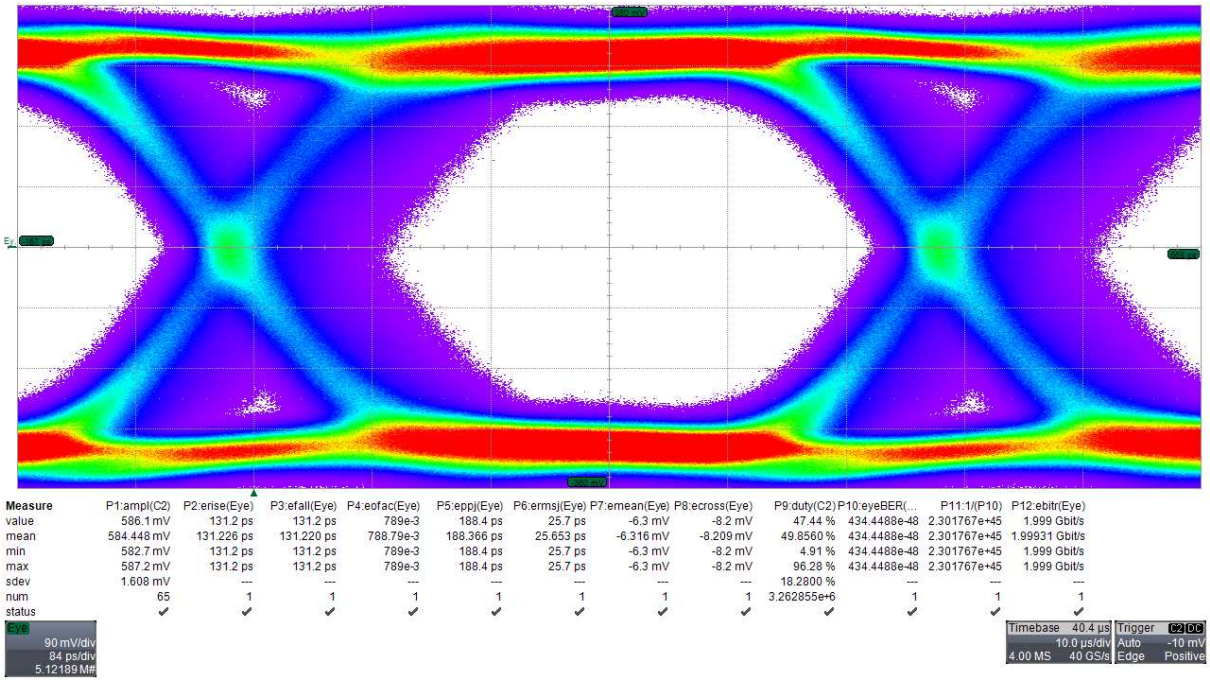


Figure 47. Eye Diagram of LVDS Driver and LVDS Receiver with PRBS-23 Data Pattern at 2 Gbps (Transmission Line of 30 cm).

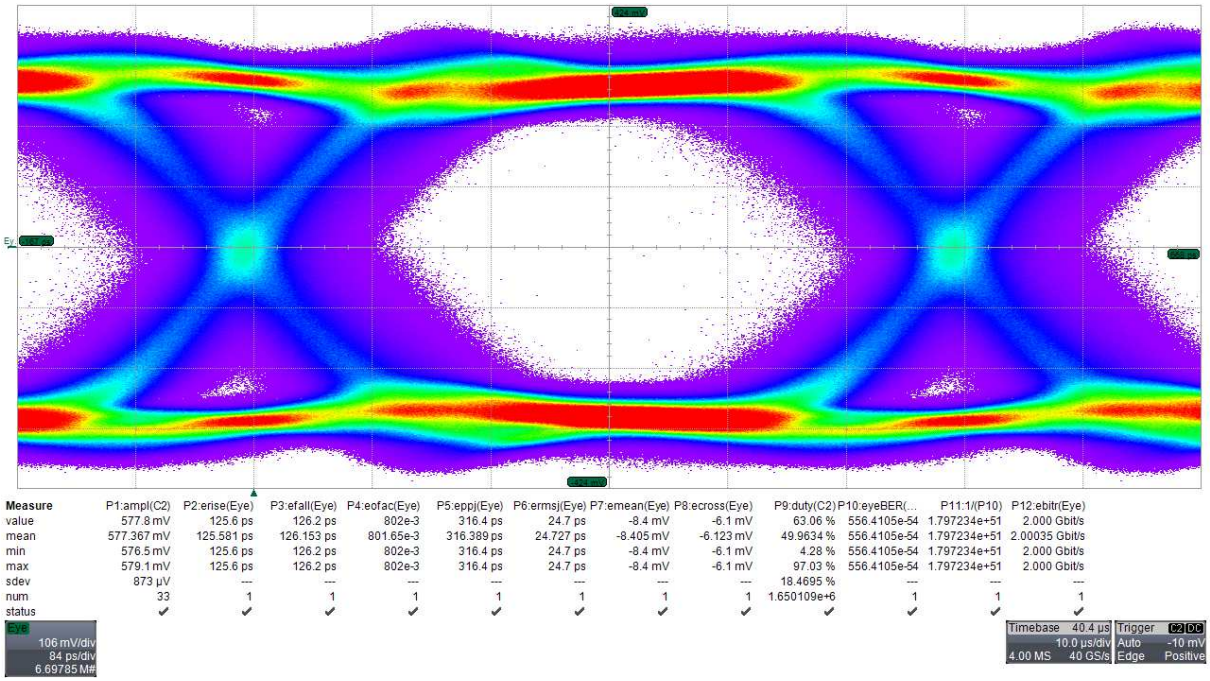


Figure 48. Eye Diagram of LVDS Driver and LVDS Receiver with PRBS-23 Data Pattern at 2 Gbps (Transmission Line of 60 cm).

10 Some remarks

Only two devices are used in characterization for this document.

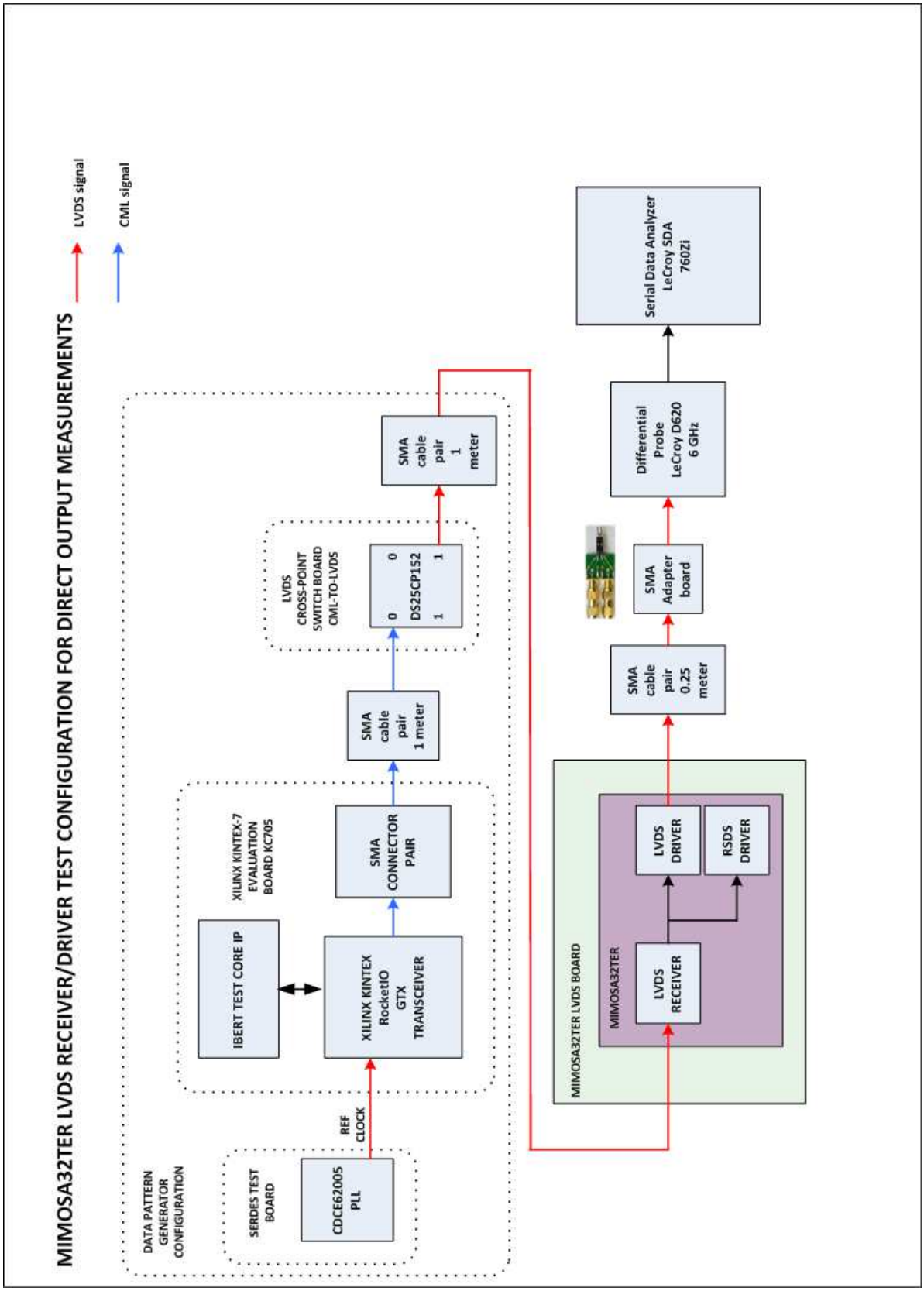
Transition Density is the ratio of transitions to the number of unit intervals (UI) in a data stream (*x* transitions / *y* unit intervals). For the jitter performance measurements, all the input data patterns used (clock pattern, PRBS-7 or PRBS-23) have approximately transition density of 0.5.

After the preliminary results, the LVDS Output Driver seems to have quite stable performance until 1.5 Gbps or 750 MHz in case of clock signal with the test configuration used in this characterization. For Example, the Total Jitter is increasing moderately when the data bit rate is less that 2 Gbps (Figure labeled as "Total Jitter (UI) vs. data bit rate (Clock Pattern data)" in Chapter 7.4 "Jitter Performance with clock data pattern".

The RSDS output Driver shows quite stable performance until 1.25 Gbps for the short distances (Fig. 39). Due to reduced output swing the power consumption is also reduced compared to LVDS Driver.

In case of use of power pulsing, it should be noted that the LVDS Driver Enable Time is more than 54 ns.

Appendix A Test Configuration with XILINX IBERT IP Pattern Generator to direct LVDS Driver measurements



Appendix B Test Configuration with XILINX IBERT IP Pattern Generator to the Differential Transmission Line measurements