Simulation and layout

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2018-10-18

Simulation

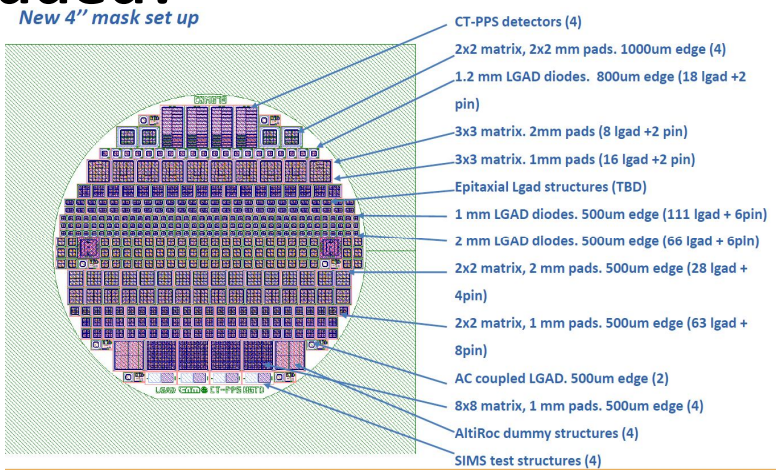
- Wafers available： 4 inch, >10kΩ㎝ FZ, 5kΩcm FZ
- Foundry available

- Build model based on process
- Simulation:
  I_V, Gain
  p layer doping concentration:3e16, 5e16
- Not get all the results, report next week

Layout

- Plan of the layout

Which structure should be included?



- Each line same structure
- 1.3mm or 1mm
- Single

  2×2 matrix

  5×5 matrix
- JTE width(5μm\10μm)
- Space between pstop and JTE

- PIN
- Test structure