Status of Digital Pixel

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15-10-2018

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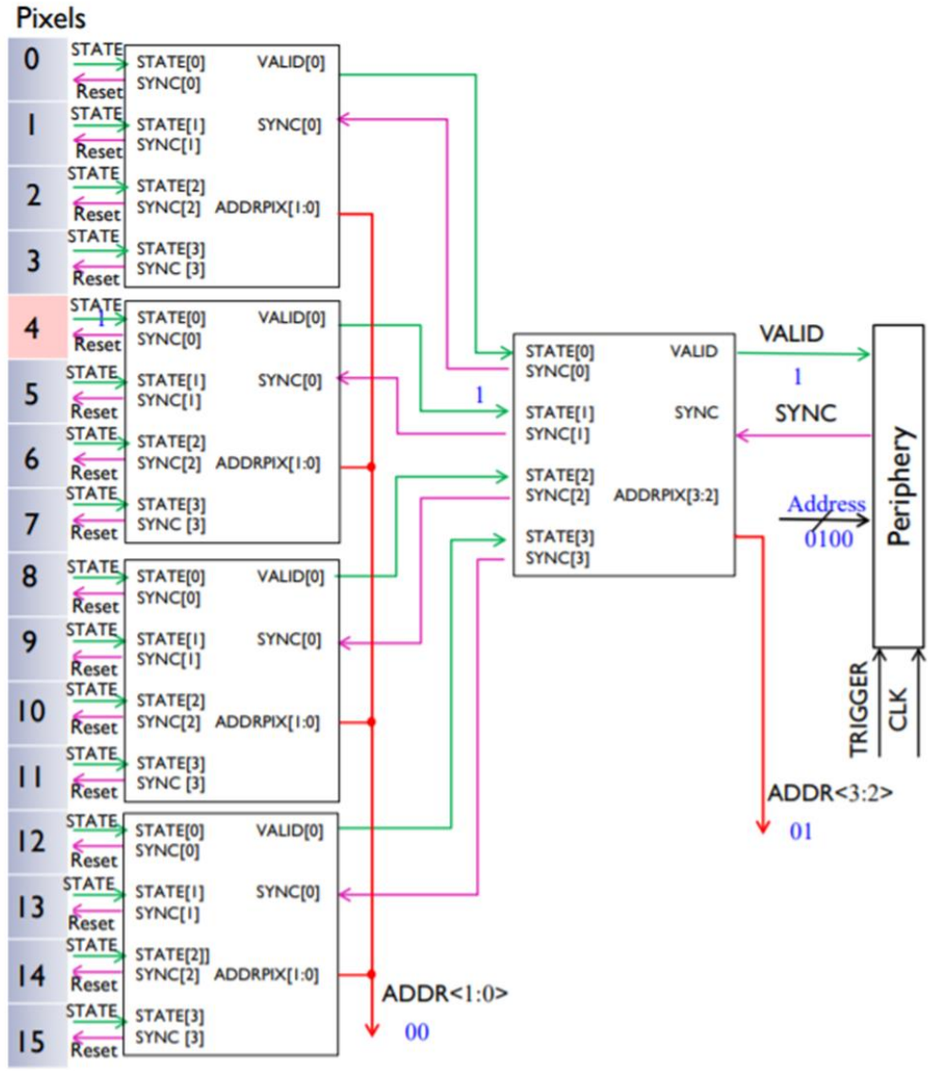
Delay evaluation of the decoder

We are going to use the AERD decoder circuits which is the same with ALPIDE. It proposed a double column architecture and encoder the 1024 pixels with fifth-order coding units.

- From the experience, we calculate the minimum width(0.23um) with the capacitance of 0.26fF/um. If the bus length of address is 12.8mm， then the parasitic capacitance is around 3.3pF.



Analysis of delay

From the analysis of Ping's paper, the delay of address and read is around 11ns.

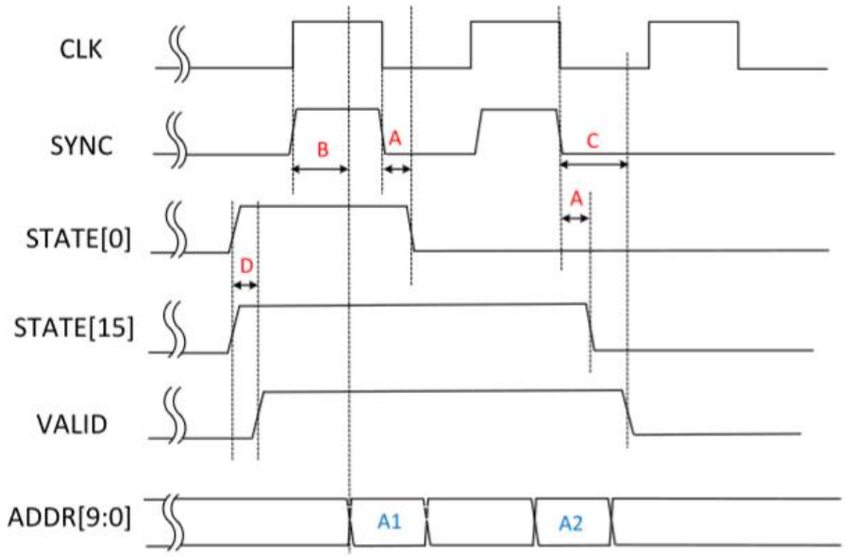


Fig. 6. Readout timing diagram of the AERD.

required from the falling edge of the CLK signal as seen from the EoC until the pixel is reset.

3. The ADDRESS value is sampled at the falling edge of the CLK. The sampling window duration is $T/2-B+A$.

4. Delay C is the time required for readout of the last hit pixel in the double-columns, from the falling edge of the CLK to the falling edge of the VALID signal. Delay C must be smaller than T, to avoid an additional readout cycle.

Assuming a duty clock cycle of 50%, these parameters set the top limit of the CLK frequency as demonstrated by the following equation:

$$f_{max}=\frac{1}{T_{min}}=\max\left[\frac{1}{2B},\frac{1}{C}\right]. \quad (4)$$

2.2.2. Delay analysis

The estimated loads in this technology are $R=4.3\ \mathrm{k\Omega}$, $C=3.7\ \mathrm{pF}$ for a 15 mm long wire. Without any buffers, the propagation delay is simply estimated as $t_d=0.7\times RC=11.11\ \mathrm{ns}$. To optimise the delay where N_{buf} is the number of buffers, $t_{d_{inv}}$ is the average propagation delay of one inverter, the minimum delay t_{dopt} can be calculated as

$$t_{dopt}=0.7\times\frac{RC}{N_{buf}}+t_{d_{inv}}\times N_{buf}\times 2. \quad (5)$$

Assuming $t_{d_{inv}}=200\ \mathrm{ps}$, then $N_{buf}=8$ is the number of buffers needed. The minimum propagation delay equals:

$$t_{dopt}=3.4\ \mathrm{ns} \quad (6)$$

The timing of the AERD basic block has been fully characterised in the digital flow, the average internal delay t_{davg} of the signals to propagate through each of the hierarchical levels has been characterised as approximately 800 ps. The worst case delay of the read out occurs when the first row of pixels is hit, as this results in the largest loads on the ADDRESS and SYNC drivers. Therefore, the time required

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P. Yang et al. / Nuclear Instruments and Methods in Physics Research A 785 (2015) 61–69

Simulation of delay

17	Delay_addr9	820.037p	☑	☐	
18	Delay_addr8	894.802p	☑	☐	
19	Delay_addr7	1.02786n	☑	☐	
20	Delay_addr6	1.0348n	☑	☐	
21	Delay_addr5	1.24115n	☑	☐	
22	Delay_addr4	1.24886n	☑	☐	
23	Delay_addr3	1.56131n	☑	☐	
24	Delay_addr2	1.57302n	☑	☐	
25	Delay_addr1	2.30389n	☑	☐	
26	Delay_addr0	2.33134n	☑	☐	

Plot after simulation: Auto Plotting mode: Replace

When I try to add equivalent capacitance resistance(r : 4K & c : 3.3pF) to EoC, the decoder circuit was not working. The simulation result comes from ideal case which delay of the bus is in a low level.

Simulation of delay

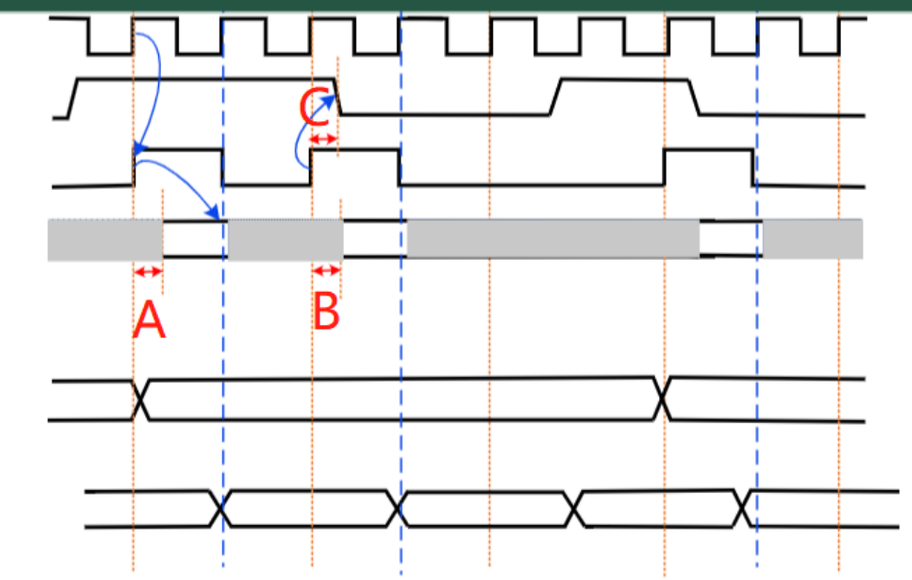


Fig.1 Timing sequence of double column readout.

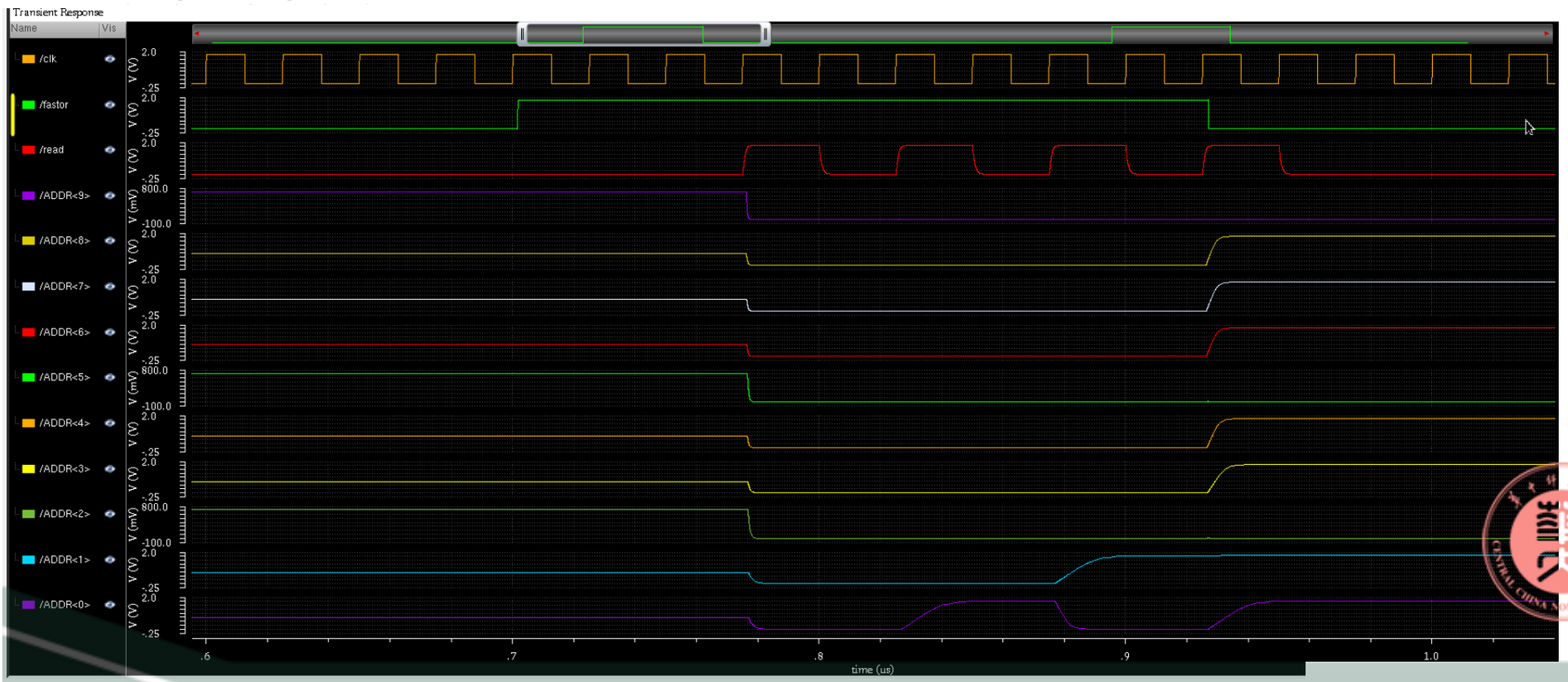
tA=2.4ns

tB=8.4ns

tC=1.5ns

T_read=25ns

T_CLK=12.5ns



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Thanks for your attention.

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