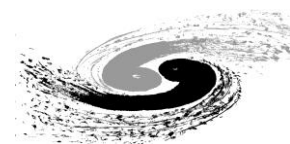


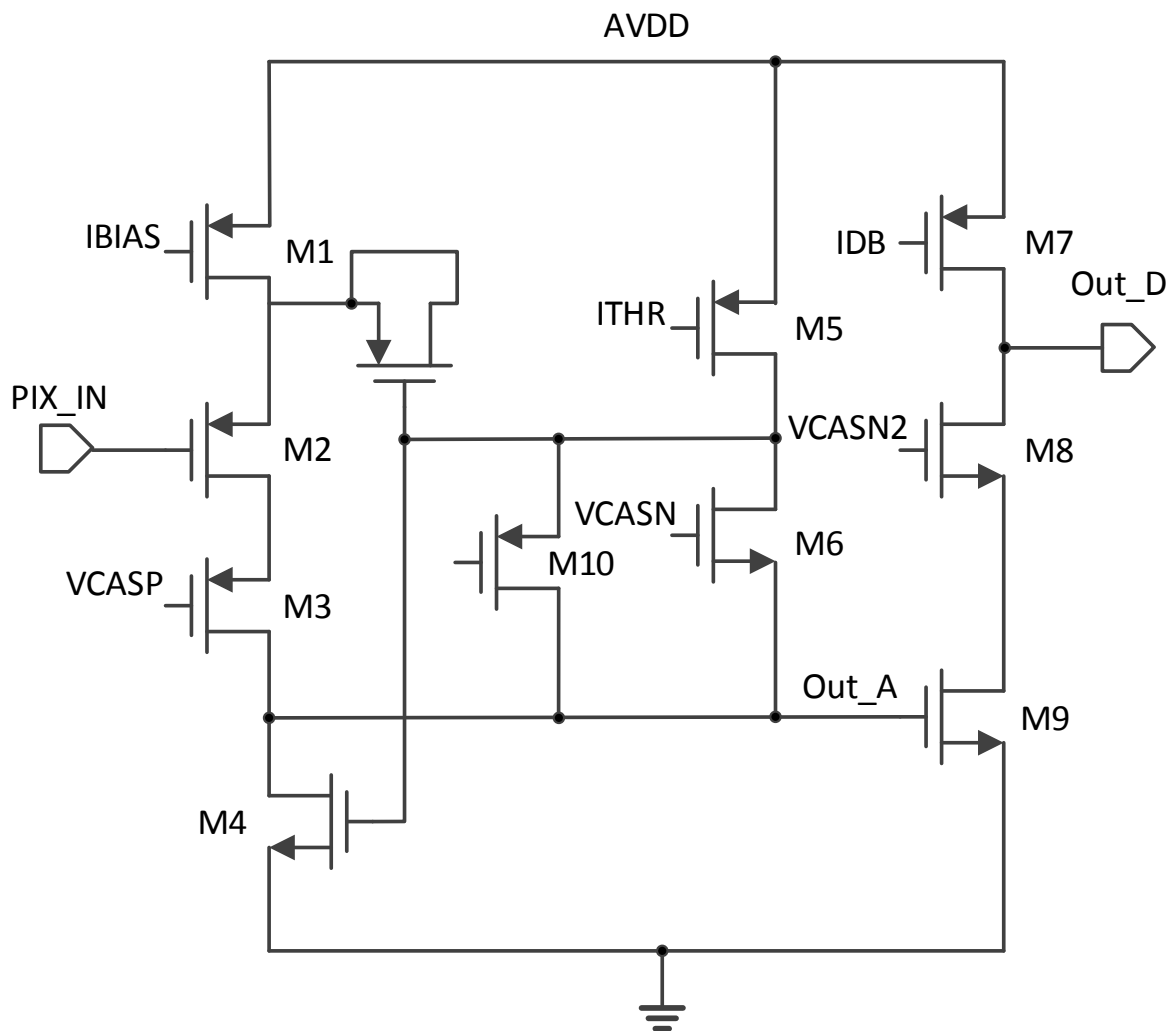
# Analog front-end design

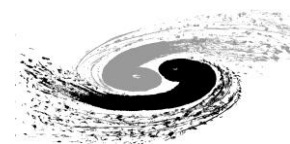
Ying ZHANG

2018-10-29



# Front-end design

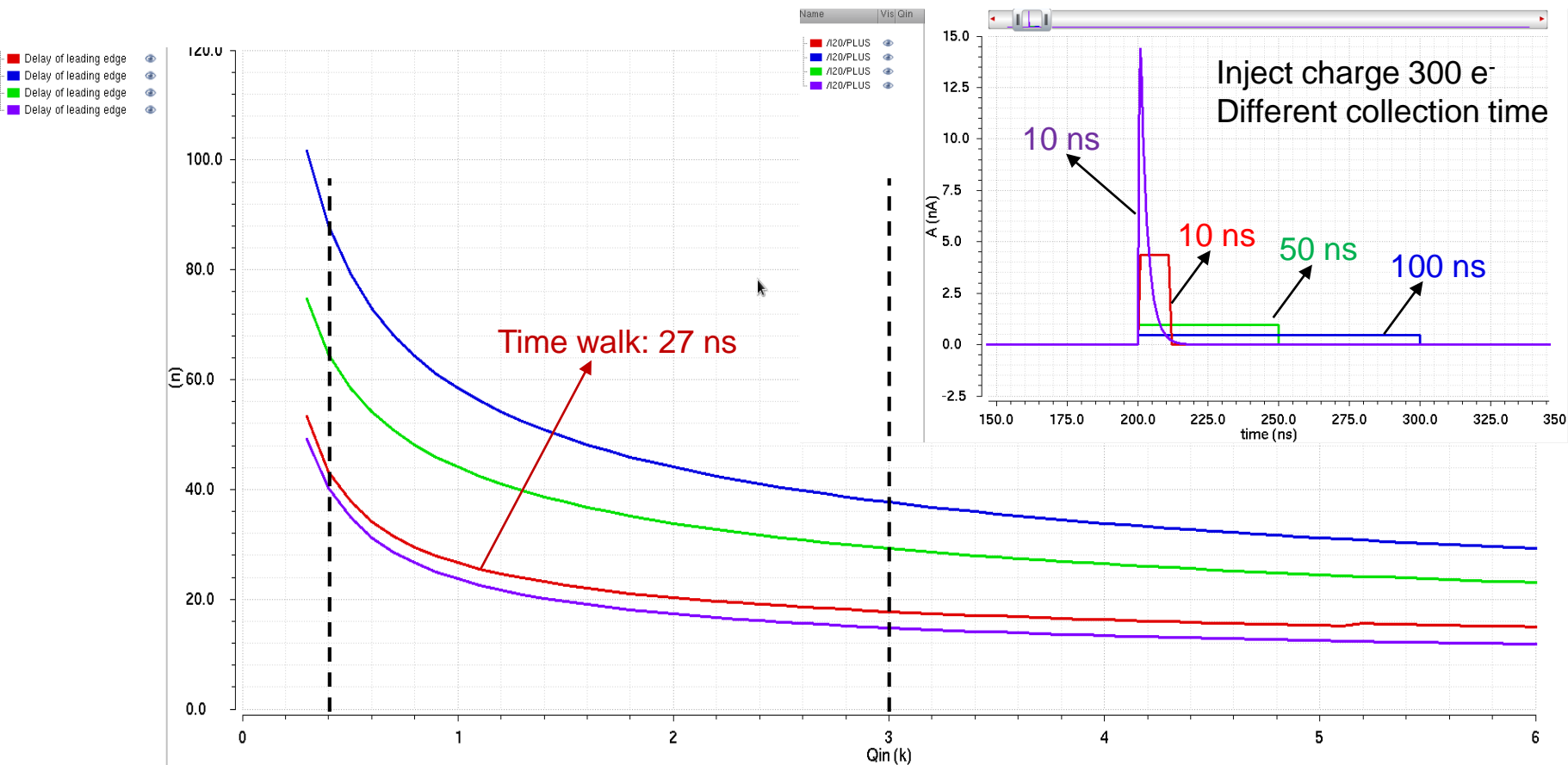




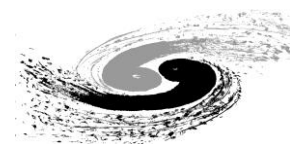
# Front-end simulation

Simulation condition:  $C_d = 2.5$  fF,  $I_{BIAS} = 440$  nA

Delay of leading edge vs. input charge vs. charge collection time



**Time walk increases with collection time**



# Front-end simulation

Simulation condition:  $C_d = 2.5 \text{ fF}, 5 \text{ fF}, 7 \text{ fF}$ ,  $I_{BIAS} = 440 \text{ nA}$

Delay of leading edge vs. input charge vs. detector capacitance

