Design specification of Peripheral readout for MOST2

Modification record

No.	Modification	Date	Note
1	Creation	2018-7-21	Xiaomin WEI
2	Fig.5 TDA<12.5ns→TDA<25ns	2018-10-1	Xiaomin WEI
3	Modify Trigger rate 20kHz→50kHz; ModifyTable.1, Fig.1~Fig.5	2018-10-8	Xiaomin WEI
4	Delete the low power mode	2018-10-20	Xiaomin WEI
5	Add Fig.6	2018-10-22	Xiaomin WEI
6	Modify DOUT→LVDS_DATA; Delete DOUT_AVA; Add LVDS_REF_CLK; Delete PCN1, PCN2; Modify the frequency range defined by DOFREQ[1:0].	2018-10-29	Xiaomin WEI

1. Introduction

This design aims for the readout of pixel array in MOST2.

The CPS is designed for CEPC. The hit density and the chip data rate are calculated in Table.1. In this estimation, the chip area is 3.2768cm^2 (1024*512 pixel array, 25um pixel pitch), and the cluster size is 3 pixels. Each hit pixel is recoded with 32 bits (See Fig.3, Timestamp: 8 bits, Address: 19 bits). The trigger latency is supposed 3~6 us, and the average trigger rate is **50 kHz**.

Table. 1 The hit density of CEPC

Parameter	Unit	Higgs	W	Z
Bunch spacing	**ns**	**680**	**210**	**25**
Hit density	**hits/bunch/cm^2**	**2.5**	**2.5**	**0.2**
	hits/bunch	8.2	8.2	0.66
	pixels/bunch	25	25	2
Hit pixel rate	MHz/cm^2	11	36	24
	MHz/chip	36	120	80
Chip data rate (triggerless)	Gbps	1.15	3.84	2.56
	MHz/32bit	36	120	80
Chip data rate (trigger, no error)	Mbps（Average）	40	40	3.2
	MHz/32bit	1.25	1.25	0.1

Chip data rate (trigger, 7LSB error)	Mbps （Average）	40	40	25.6
	MHz/32bit	1.25	1.25	0.8
Designed data rate (trigger)	MHz/32bit	**5**	**5**	**5**
Designed data rate (triggerless)	MHz/32bit	**160**	**160**	**160**

2. Features

- Pixel array 512*1024
- Pixel pitch 25 μm
- Support trigger and triggerless mode
- Data compression
  Suggested in triggerless mode
- Parity check for output data

3. Interface Discription

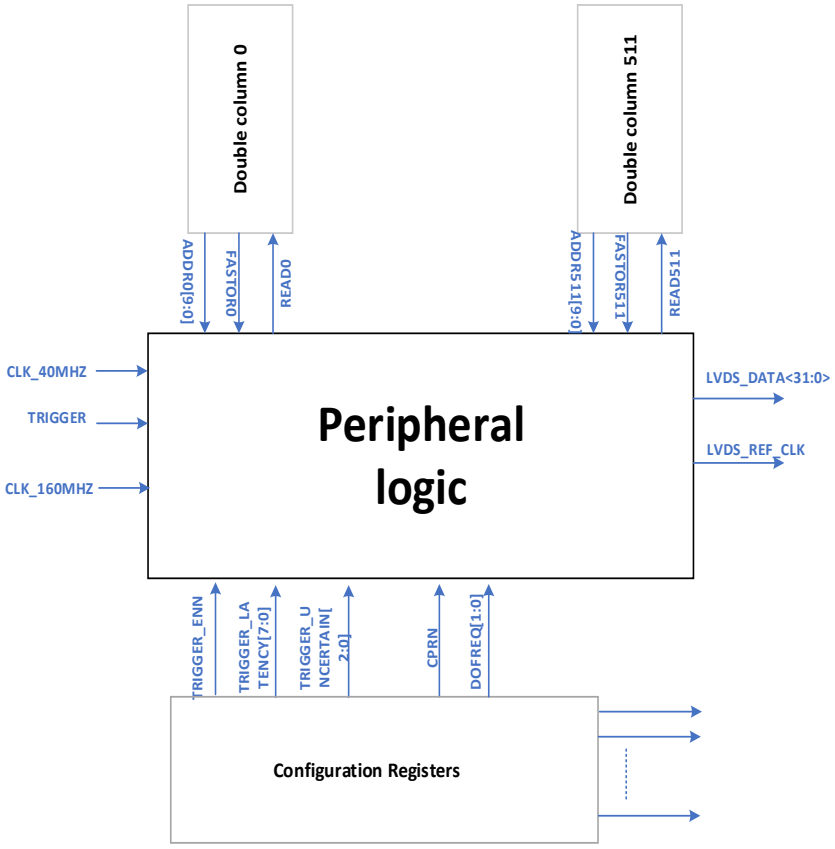

Fig.1 the interface between peripheral logic and related blocks

Table.2 Interface Signal Description

Signal Name	Type	Descriptions
Chip input		
CLK_160MHZ	I	160MHz
CLK_40MHZ	I	Input system clock, 40MHz
TRIGGER	I	Fig.2. The average frequency is 50KHz. The actual frequency depends on the happen of true event. In the trigger mode, the data fit the TRIGGER arriving time are read out, and the other data will be disposed. It is disable in the triggerless mode. See Fig.4 for the data transmission.
Data output		
LVDS_DATA [31:0]	O	Data output to LVDS transmitter. LVDS_DATA [31:24] are 8 bits time stamp. LVDS_DATA [23:15] are the double column address. LVDS_DATA [14:5] are the hit pixel address in a double column. LVDS_DATA [4:2] is the data compression pattern. LVDS_DATA[1] is the data available flag. 1: data valid. 0 : data invalid. LVDS_DATA[0]: Parity check bit. (It's not available in design V0.1) See Fig.3 for the data format.
LVDS_REF_CLK	O	LVDS PLL reference clock. In trigger mode , the output frequency is defined by DOFREQ[1:0] , the minimum output frequency is 2MHz. In triggerless mode, the output frequency is the constant 160MHz. LVDS_DATA [31:0] should be received on the rising edge of LVDS_REF_CLK. Note: The LVDS PLL should support a 2MHz~160MHz reference input.
Pixel array		
READi (i=0,1,…,511)	O	Hit address read signal. Reset the hit pixel when high.
FASTORi (i=0,1,…,511)	I	OR results of all the pixel digital output in a double column.
ADDRi[9:0] (i=0,1,…,511)	I	The address of the hit pixel in a double column.
Signals from Configuration registers		

TRIGGER_MODE	W	0 tigger mode 1 triggerless mode
TRIGGER_LATENCY [7:0]	W	Trigger latency: 0-6us 00000000: 0ns 00000001: 25ns … 11110000: 6us 11110001~11111111: invalid
TRIGGER_UNCERTAIN [2:0]	W	Negative trigger error: 000: 0ns 001:25ns 010:50ns (default) 011:75ns 100:100ns 101:125ns 110:150ns 111:175ns If the trigger uncertain is negative, please adjust the trigger latency and provide negative trigger error. See Fig.6.
CPRN	W	0: default, data compression for the addresses of four adjacent pixels in a double column. The first pixel address is DOUT[23:5]. DOUT[4],DOUT[3] and DOUT[2] note whether the address of DOUT[23:5]+3, DOUT[23:5]+2, DOUT[23:5]+1 is '1', respectively. For example, DOUT[23:5]=19'd0, DOUT[4:2]=3'b001, then the pixel digital outputs of addresses 19'd0,19'd1,19'd2,19'd3 are 1,1,0, and 0. 1: by pass the data compression block
DOFREQ[1:0]	W	Set the data output (DOUT[31:0]) frequency in trigger mode. 00: 2MHz 01: 5MHz, 10:10MHz, 11: 20MHz

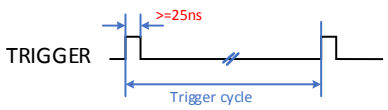

Fig.2 Timing of input signal TIGGER. The TRIGGER arriving time are recoded at the positive edge of Trigger_syn (See Fig. 4(b)). The average trigger cycle is 20us.

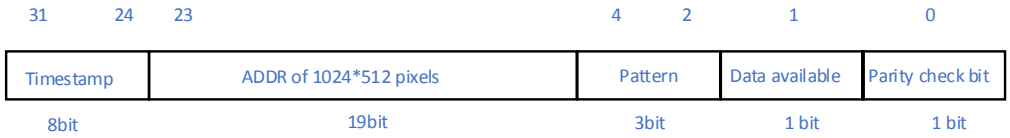

Fig.3 The output data format. LVDS_DATA [31:24] are 8 bits time stamp. LVDS_DATA [23:15] are the double column address. LVDS_DATA [14:5] are the hit pixel address in a double column. LVDS_DATA [4:2] is the data compression pattern. LVDS_DATA[1] is the data available flag. 1:data valid. 0 : data invalid. LVDS_DATA[0]: Parity check bit. (It's not available in design V0.1)

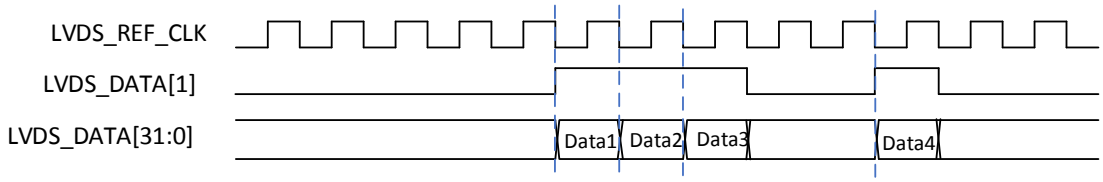

Fig.4 Data output Timing. The output data LVDS_DATA are sending at the falling edge of LVDS_REF_CLK. In the triggerless mode, the output frequency is 160MHz. In the trigger mode, the external trigger start signal (trigger) is synchronized (Trigger_syn) by CLK_40MHz. The output data frequency is set by DOFREQ[1:0].

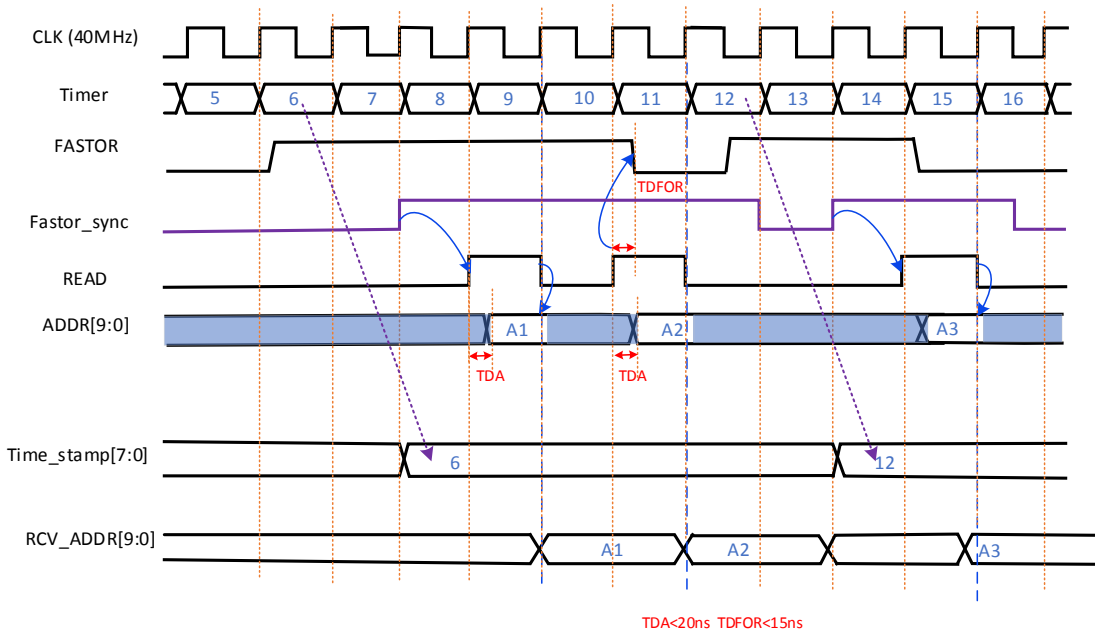

Fig.5 Timing of double column readout. FASTOR is generated when any pixel in the double column is hit. Since the hit pixel will be reset after readout, FASTOR changes into zero when the last hit address is readout. FASTOR is synchronized as Fastor_syn. READ is active when FASTOR_sync is "1". The cycle of READ is 50ns which corresponds the maximal delay of the addressing encoding (TDA) is 20 ns. For the peripheral logic, the hit timestamp (Time_stamp[7:0]) is recoded at the positive edge of Fastor_sync. The address of hit pixel (ADDR[9:0]) is taken at the clock positive edge when ADDR[9:0] are available.

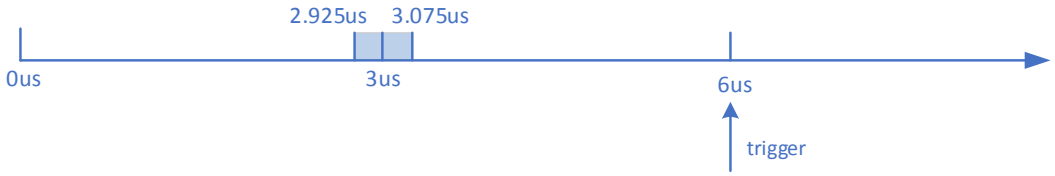

Fig.6 Example of setting trigger latency and trigger uncertain. Suppose the trigger signal comes at 6us, and users wants to acquire the hits from 2.925us to 3.075us, then we should set TRIGGER_LATENCY as 8'd 123 (123*25ns=3.075us), and TRIGGER_UNCERTAIN as 3'b110. (0.15us).