Status of Digital Pixel

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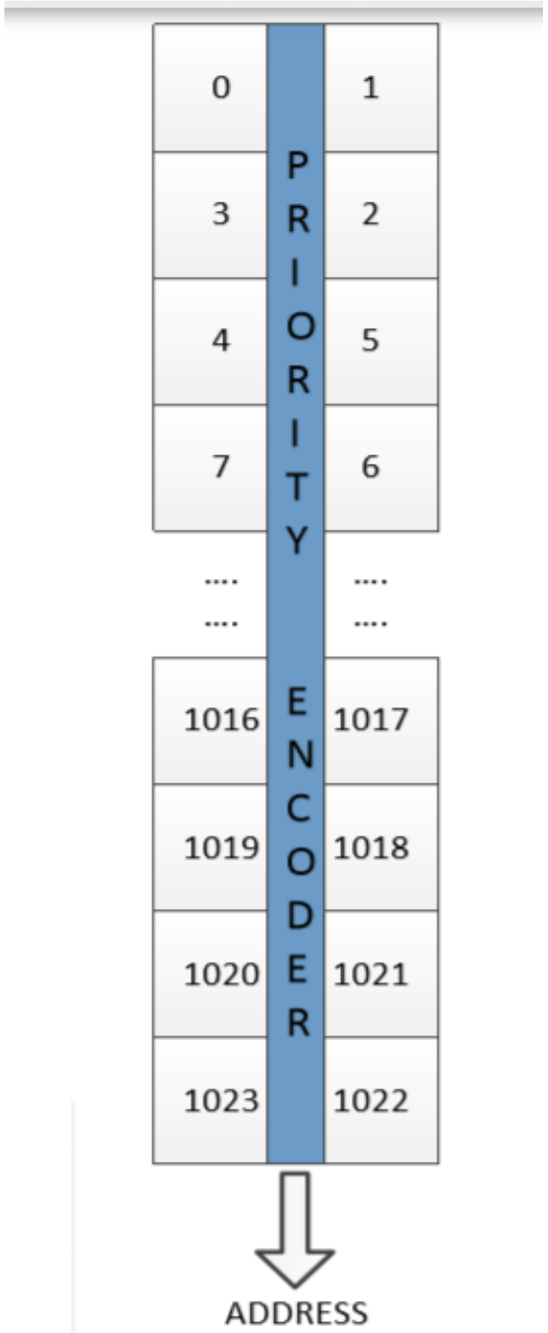
Double column structure



- The matrix of pixels is read out by an array of 1024 Priority Encoder blocks.
- The pixels are arranged in double columns and the regions at the middle of each double column are occupied by the Priority Encoders.
- The indexing of the pixels in the readout data words is defined by the Priority Encoders.
- Top pixels have highest priority.

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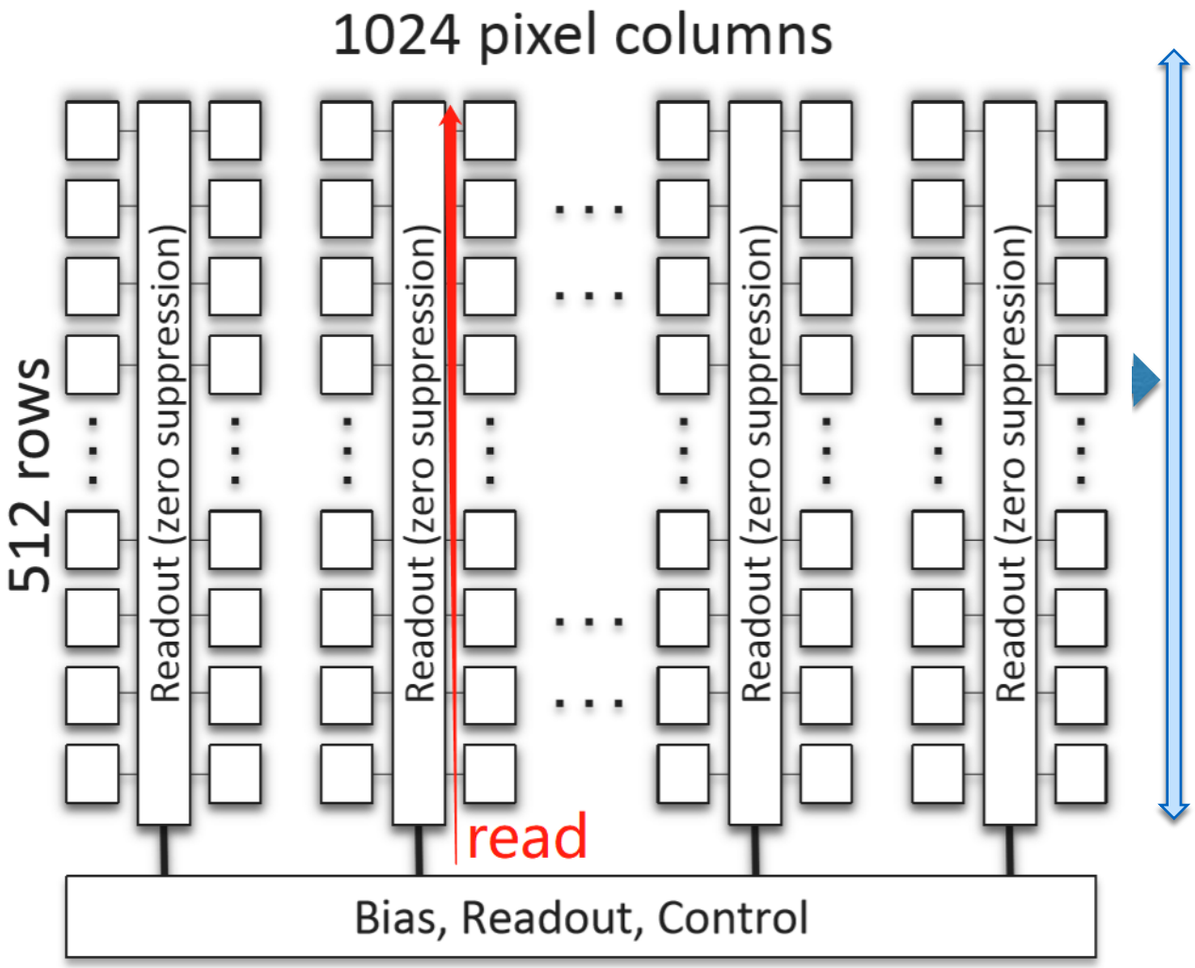
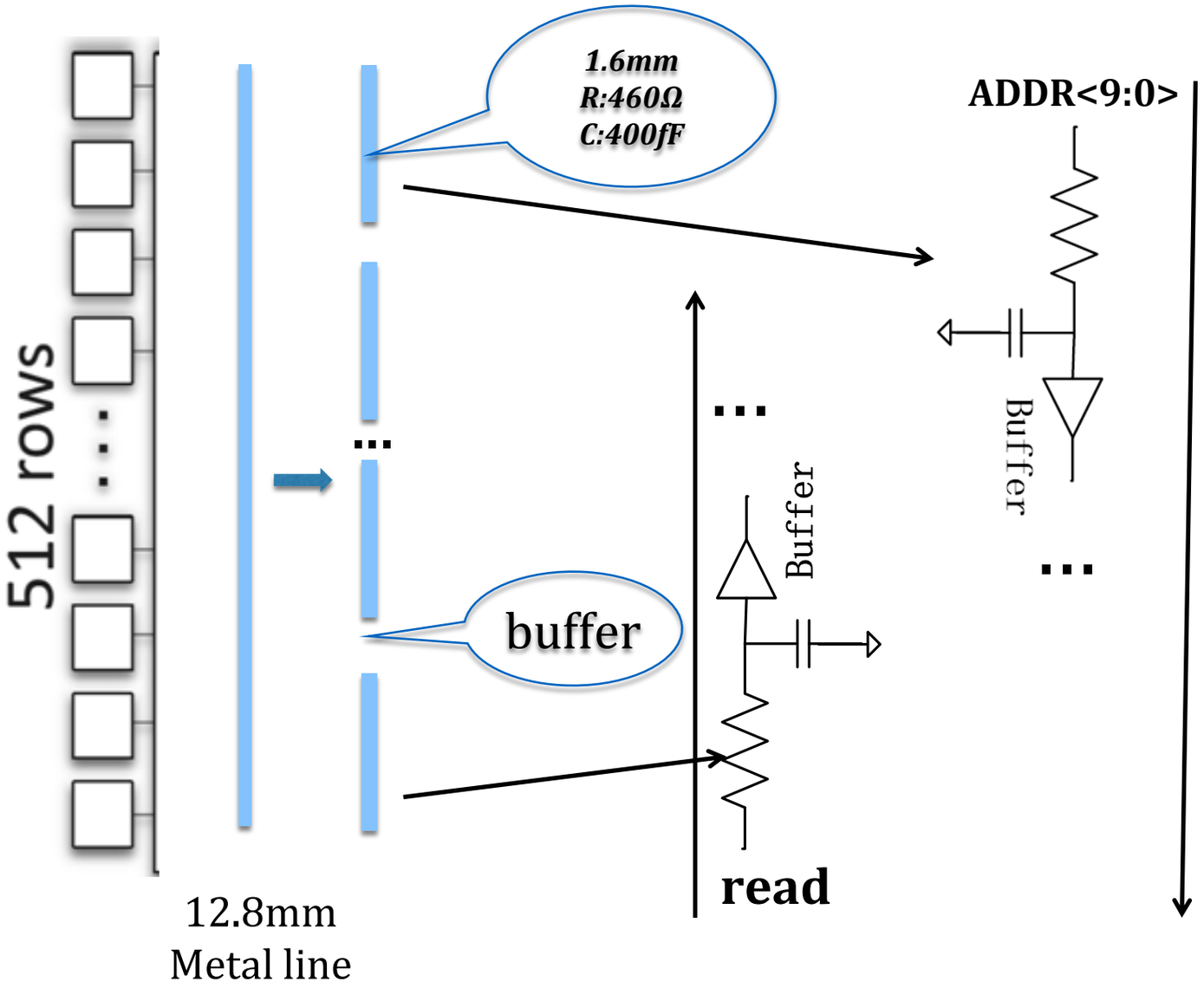
Parasitic resistor and capacitor simulation



- The read signal start from end of column , the worst case delay of the read out occurs when the first row of pixels is hit.
- The schematic can't work with such a big load.

Optimize the delay with buffers

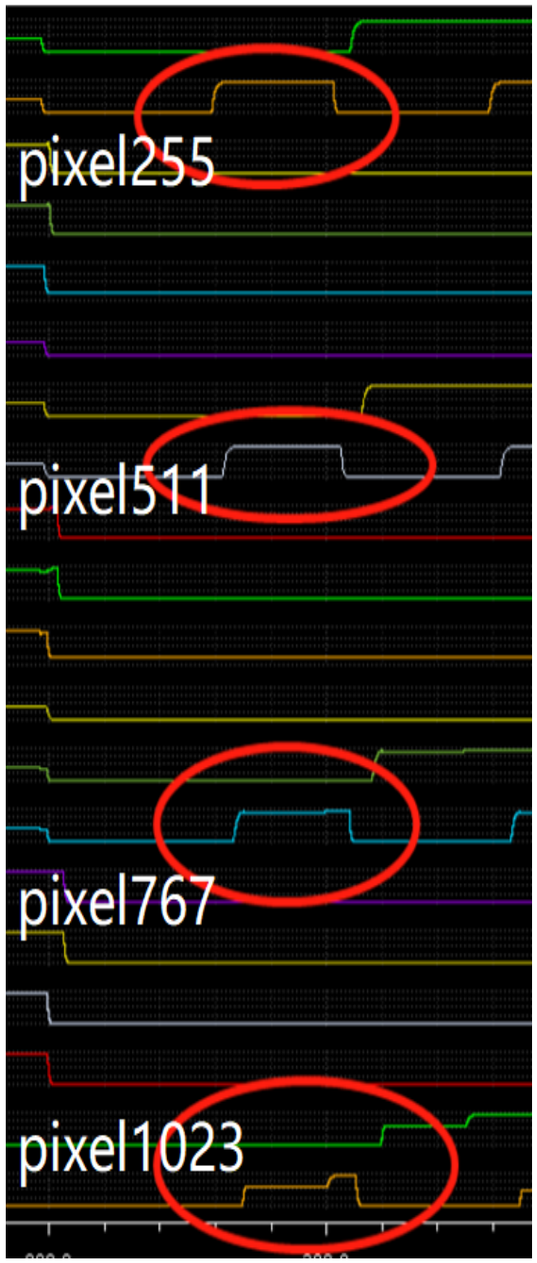


- Divide into 8 segments
- Insert 8 buffers
- The delay of each segment is :
  td_seg=0.13ns
- The delay of buffer:
  td_buf=0.11ns
- Total delay:
  td_total=1.92ns <Td(8.11ns)

Parasitic simulation

The change of output signal ADDR<0> pass from pixel_0 to pixel_1023

Use the minimum size transistors of buffer and encoder to drive the long metal line. There exists an obvious distortion.



Enhance the driving strength of the output stage(Buffers and encoders). All pmos dimension is 3 times lager than the nmos at output stage.

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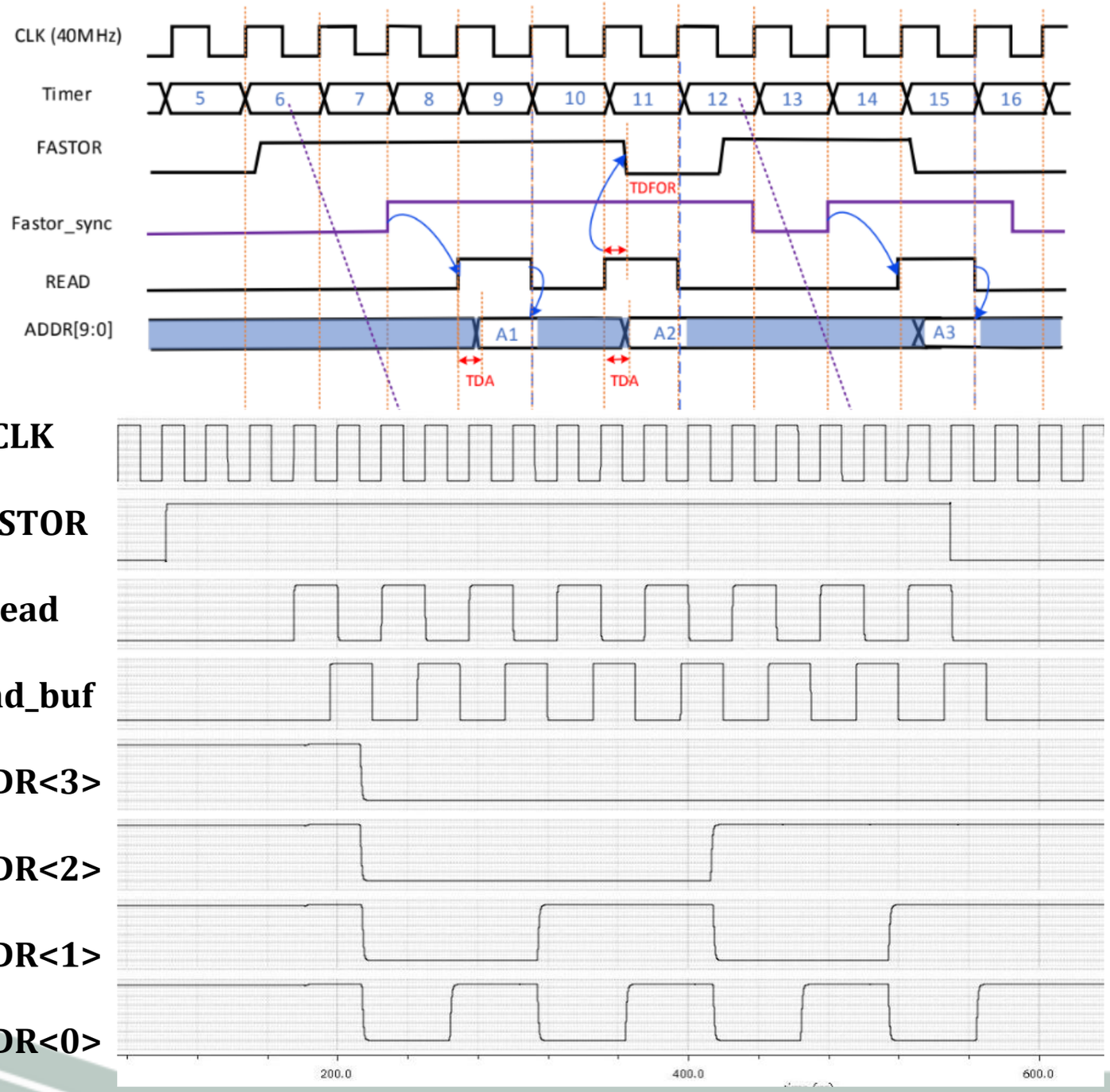
The evaluation of total delay



TT ; 1.8V ; 27℃	
Signal	Delay
FASTOR	1.7ns
read	14.35ns
TDA	26.75ns
TDFOR	16.36ns

SS ; 1.6V ; 50℃	
Signal	Delay
FASTOR	2.527ns
read	20.67ns
TDA	39.33ns
TDFOR	24.11ns

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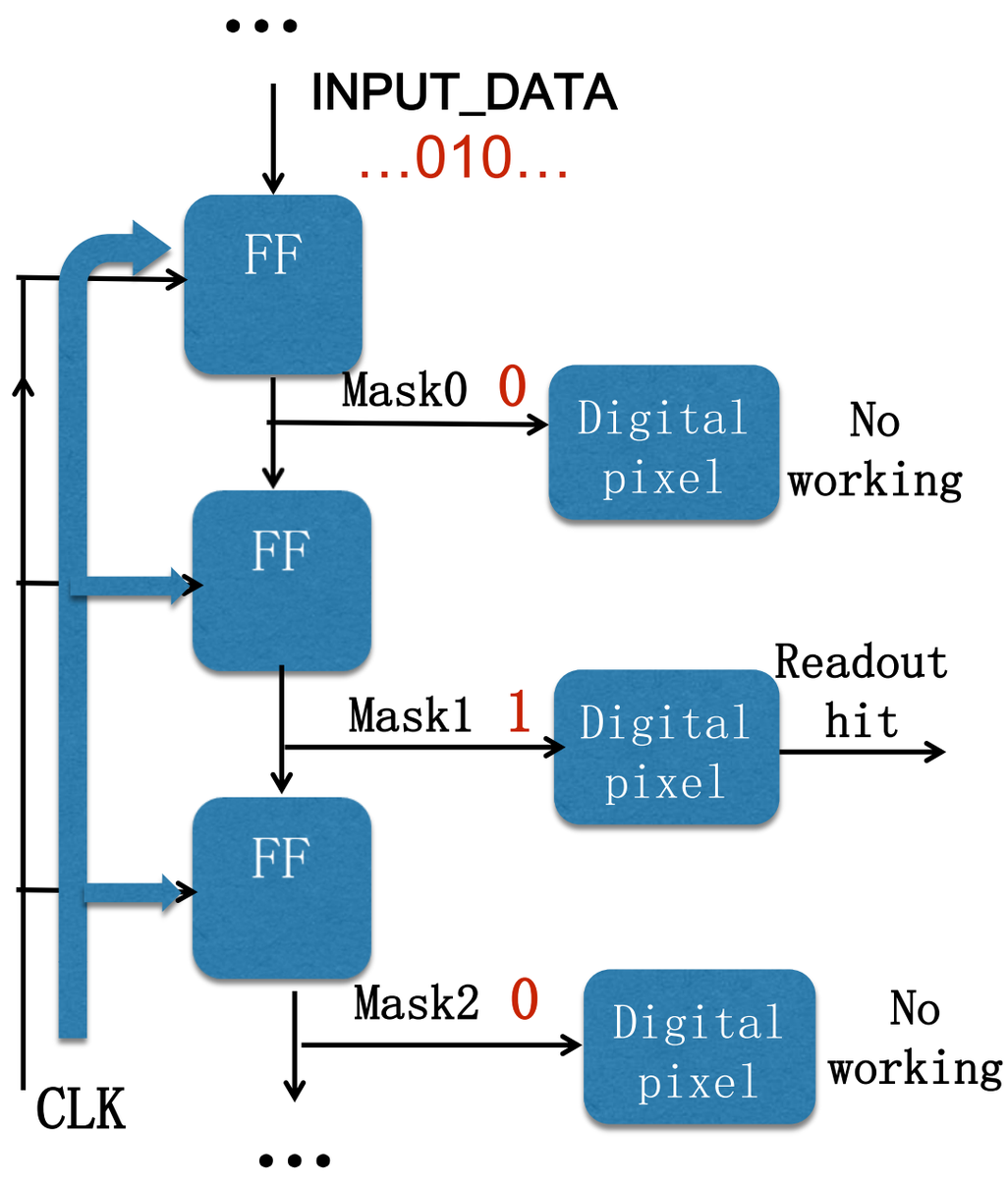
The evaluation of masking circuits



- CLK of 1bit shifting register works from bottom to top.
- Masking data start from top.
- Total CLK delay of masking circuits is around 12.5ns.

OUTLOOK

- I simulated the parasitic r&c with the estimated value, the layout should be done to ensure the circuits performance.

- I need determine the area of digital pixels .

- The layout of priority encoder is challenging, I need some expert help on the digital layout.

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Thanks for your attention.

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