Status of Digital Pixel

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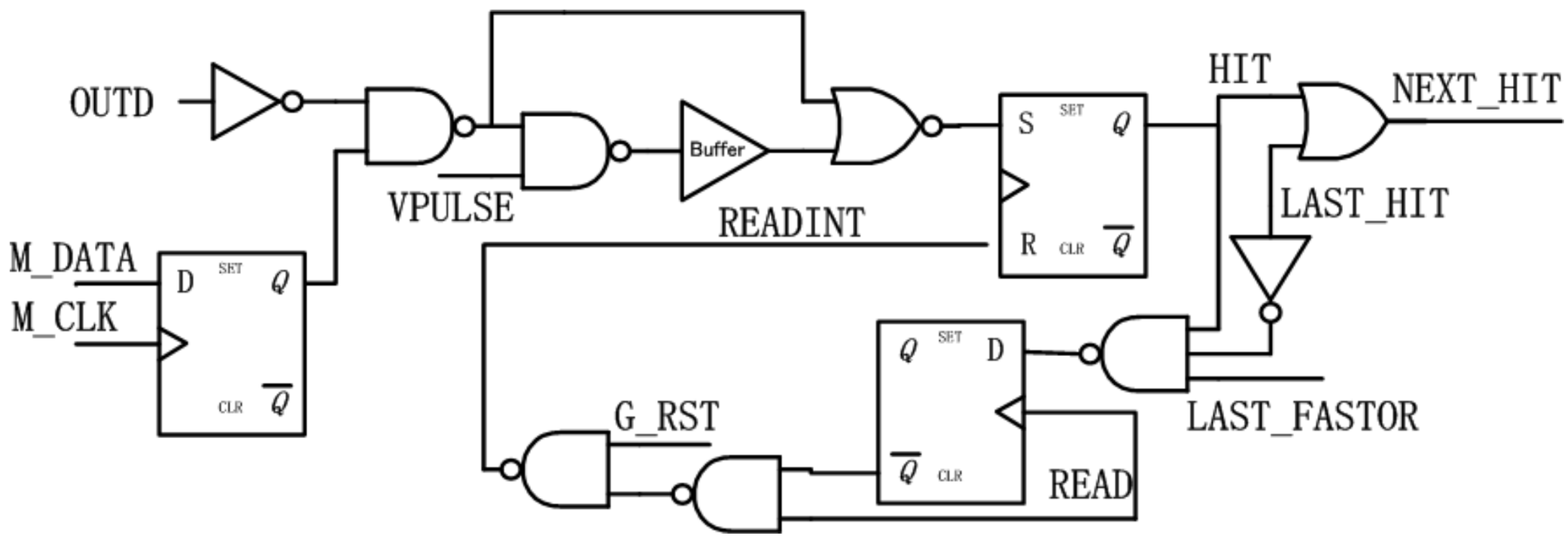
Optimization of digital pixel

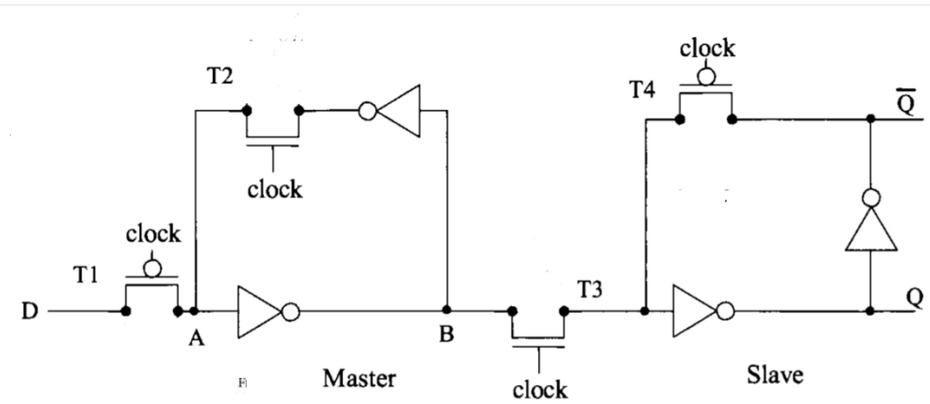
Simplify the digital logic gates

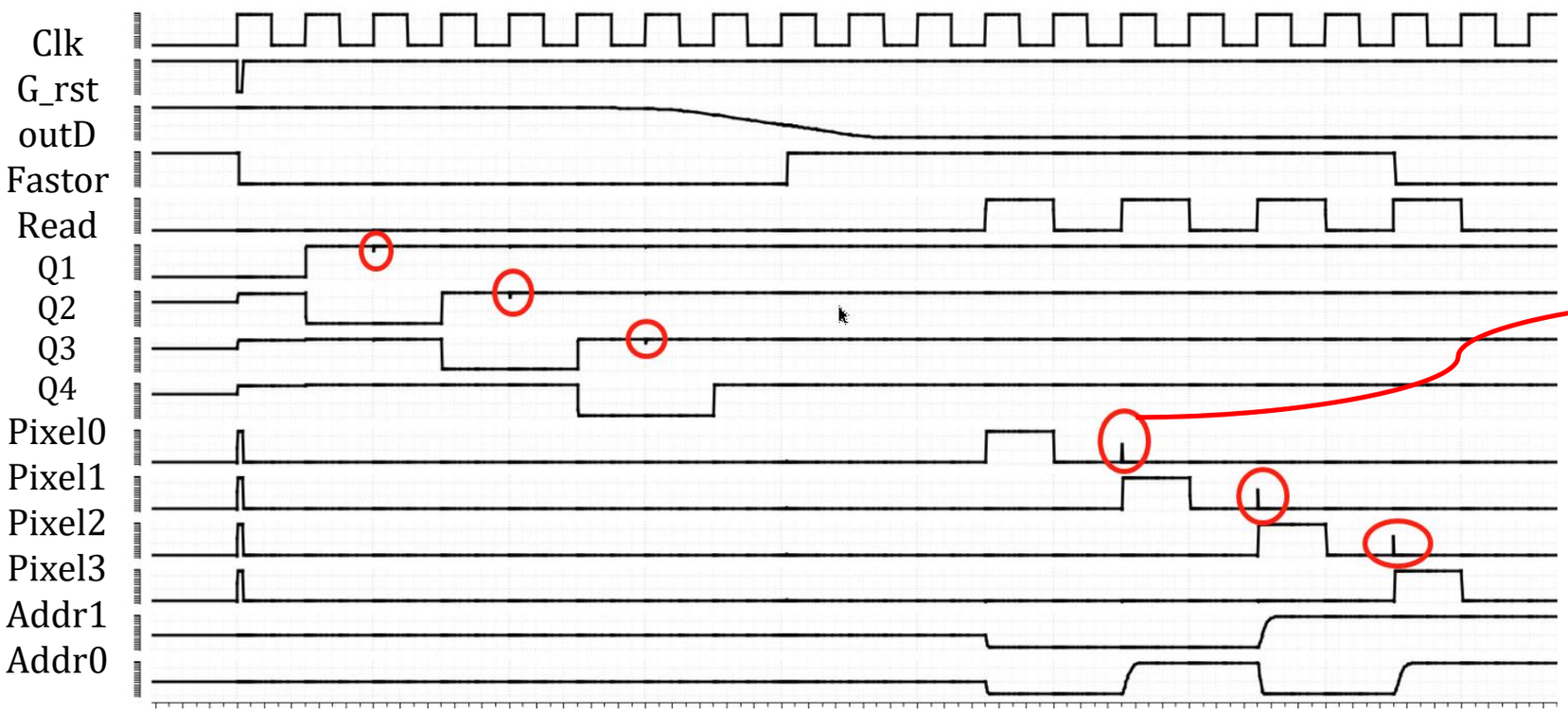
- *Replace OR&AND gates with NOR or NAND gates*
- *Use dynamic DFF instead of the standard one*



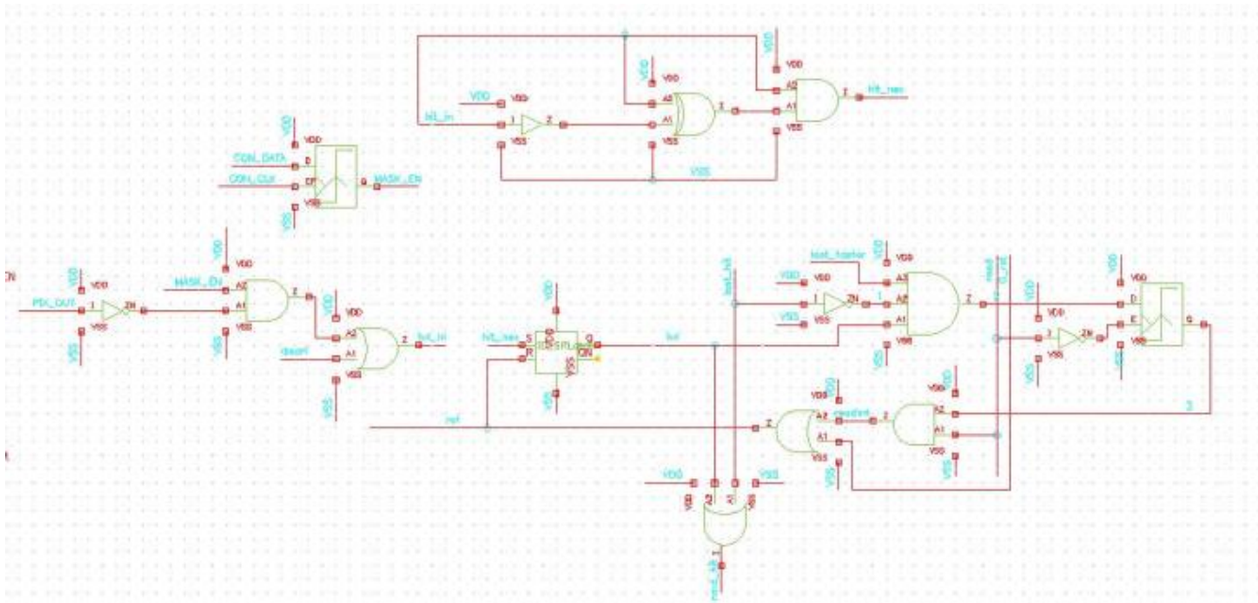
Dynamic DFF structure

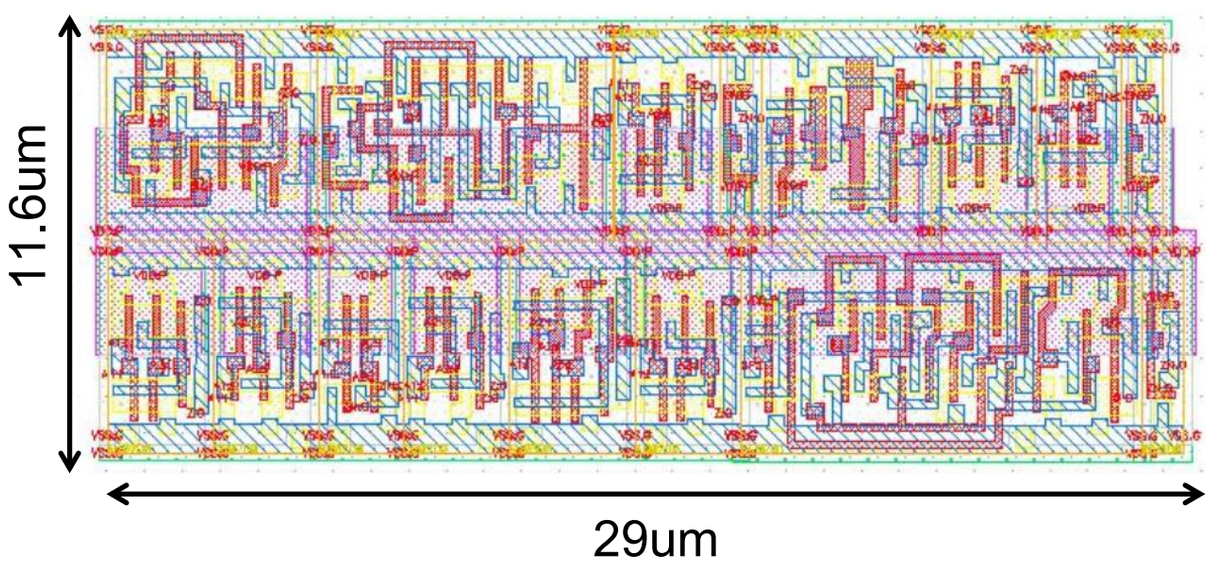
- The dynamic DFF only cost 12 transistors
- It works fine with the pixel masking.
- The encoder can readout correctly





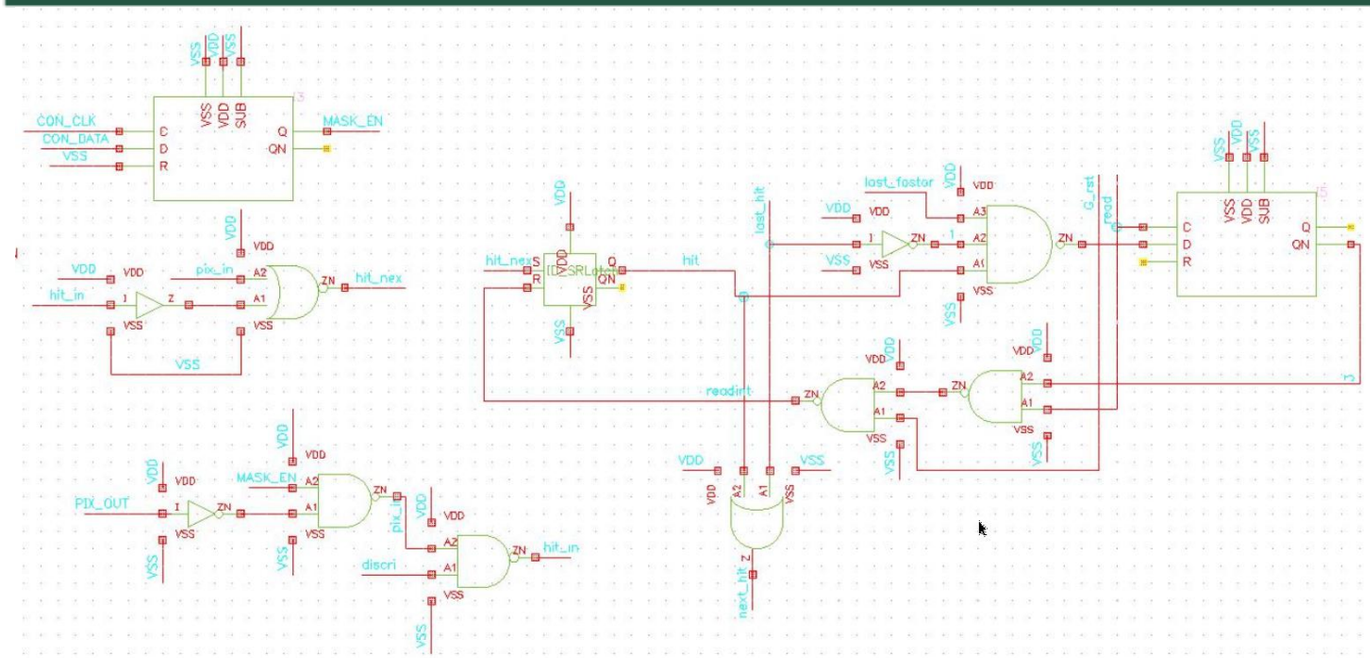
Evaluate the area of the digital pixel

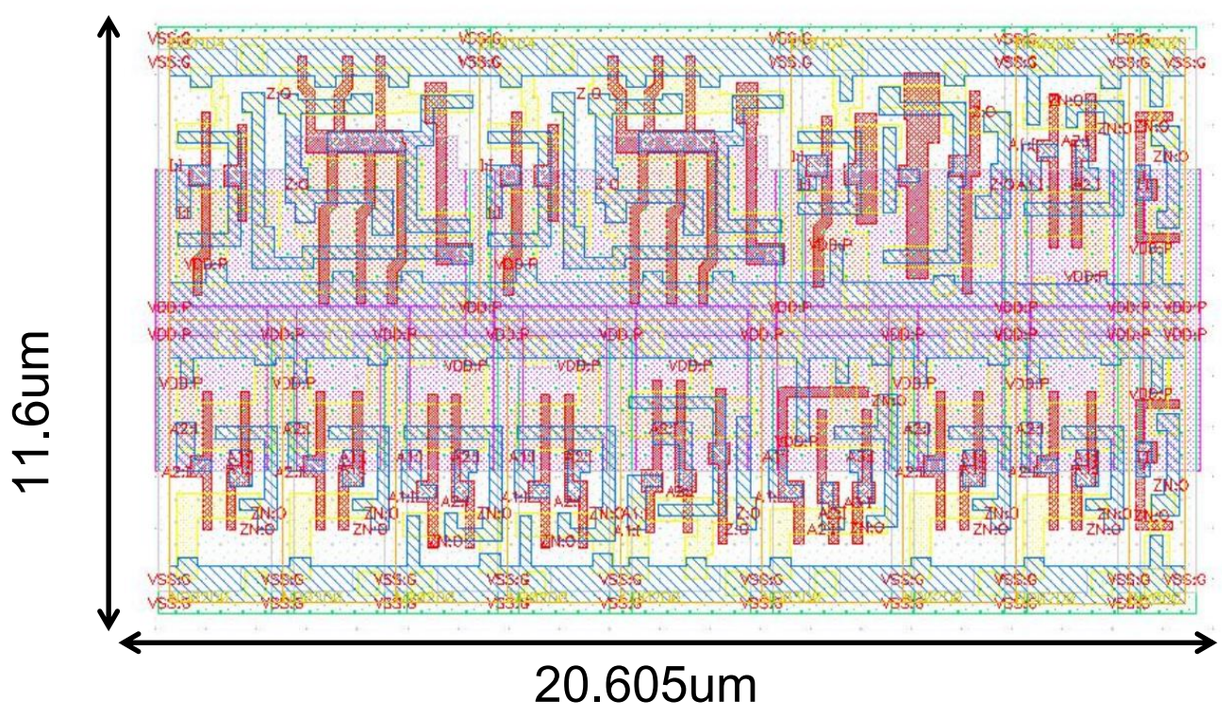




Standard cell area table			
Type	**amount**	**transistors**	**Cell area(um)**
Inverter	3	2 x 3	1.7 x 6.11
D flip-flop	1	24 x 1	***11.22 x 6.11***
Delay buffer	1	8 x 1	5.06 x 6.11
3-in AND gate	1	8 x 1	3.94 x 6.11
2-in AND gate	3	6 x 3	3.38 x6.11
SR Latch	1	8 x 1	5.06x6.11
D Latch	1	16 x 1	***8.42 x 6.11***
OR gate	3	6 x 3	3.38x6.11
XOR gate	1	14 x 1	6.18x6.11
Total	***15***	***120***	***65.32 x 6.11***

Evaluate the area of the new structure





It saves 44 transistors , around 30% area.

Standard cell area table			
Type	**amount**	**transistors**	**Cell area(um)**
Inverter	2	2 x 2	1.7 x 6.11
Dynamic DFF	2	12 x 2	***6.74 x 6.11***
Delay buffer	1	8 x 1	5.06 x 6.11
3-in NAND gate	1	6 x 1	3.38 x 6.11
NAND gate	4	4 x 4	2.82 x6.11
SR Latch	1	8 x 1	5.06x6.11
OR gate	1	6 x 1	3.38x6.11
NOR gate	1	4 x 1	2.82x6.11
Total	***13***	***76***	***47.86 x 6.11***

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Thanks for your attention.

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