Discussion on Pixel digital part

1. The pixel address encoder output high-z state addresses when READ is low. We try to avoid or to reduce the leakage current probably cased by the high-z state.
2. At the end of column, we can implement some circuits to stop the high-z state transmitting to the periphery circuits. **But there are still some other problems.**

Method1: Let the addresses (EOC) connect to GND or VDD when Valid is low as Fig.1 (a). Timing sequence is shown in Fig.1(b). The pull up/down transistor size depends on the parasitic RC.

The high-z state will be transmitted to peripheral logic in a short period (less than 100 ns). **Leakage current may be induced in peripheral logic during the short period (high-z state).**

****

Fig.1 (a)



Fig.1（b）

Method2: Latch the addresses when the addresses are available as Fig.2 (a). Timing sequence is shown in Fig.2(b)

**The high-z state will be not transmitted to peripheral logic. The latch enable should be probably generated according the estimated TDA.** If TDA<37.5ns, then the latch enable can keep high from 37.5ns to 50ns.



Fig.2 (a)



Fig.2 (b)

1. **The leakage current in the address encoder should be also considered. It would be better to consider the circuits in Fig.1 (a) /Fig.2 (a) and the buffer on the address lines together.**
2. The peripheral logic will not register the tri-state data. If TDA is evaluated as 40ns, we prefer to give a READ signal with cycle of 3 clks. (2 clks high and 1 clk low). Some important parameter should be given as shown in Fig.1(b).

TDFOR: From positive edge of READ (EOC) to the invalid of FASTOR(EOC). (hit in pixel 0)

TDA: From positive edge of READ (EOC) to the stable address. (hit in pixel 0)

TDAHZ1: From negative edge of READ (EOC) to the high-z address. (hit in pixel 0)

TDAHZ2: From negative edge of READ (EOC) to the high-z address. (hit in pixel 1023)

TDVALID1: From negative edge of READ (EOC) to VALID(EOC) low. (hit in pixel 0)

TDVALID2: From negative edge of READ (EOC) to VALID(EOC) low. (hit in pixel 1023)

1. The present circuits contain two duplicated functions: (1) FASTOR and VALID; (2) FASTOR controlled priority and Encoder asserted priority. Three choices:
2. Keep present design and estimate the circuit area.
3. ALPIDE-like: Keep the encoder and suppress the FASTOR logic as Fig.3. The periphery logic should be modified according the new design (The input signal change from FASTOR to VALID). **Probably, TDA will be smaller than the present design.**



Fig.3

1. FEI3-like: Keep the FASTOR logic and design an encoder like FEI3. They use a sense amplifier. Probably it will cause the smallest area, but it still needs large efforts.
2. **Shall we consider the improved ALPIDE sequence in Yang’s paper?** It will be much reliable if we can read a pixel address in 50 ns. **Then the timing should be redefined.**
3. Some comments for the circuits from Tianya.
4. No buffer found on READ
5. No load on FASTOR, SYNC, VALID
6. Suggest all the buffers on addresses lines with enable. It would be better to consider the enable of each buffer separately.
7. Suggest finding someone to review the circuits before layout. Especially the logic gates connecting with a long transmission lines should be carefully concerned. The drive ability of some logic is too small.

**(5)The timing sequence should be evaluated with proper loads and buffers again.**