SiW-ECAL
Progresses and Challenges

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for the SiW-ECAL groups

Topical Workshop on the CEPC Calorimetry,
12/03/2019, IHEP

TNA support + WP14

Requirements from detectors

Basis: sep of H ⟶ WW/ZZ ⟶ 4j

- $\sigma_Z/M_Z \sim= \sigma_W/M_W \sim= 2.7\% \oplus 2.75\sigma_{sep}$

⇒ σ_E/E (jets) < 3.8%

- Sign ~ S/√B ~ $(\text{resol})^{-1/2}$
  60%/√E ⟶ 30%/√E ⇔ +~40% L

Large Tracker

- Precision and low X_0 budget
- Pattern recognition

High precision on Si trackers

- Tagging of beauty and charm

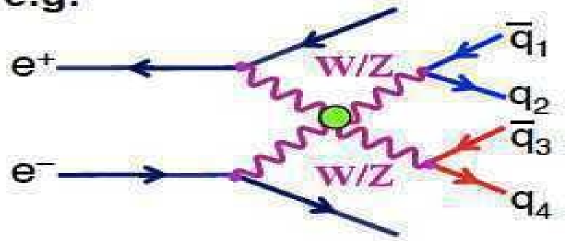
Large acceptance

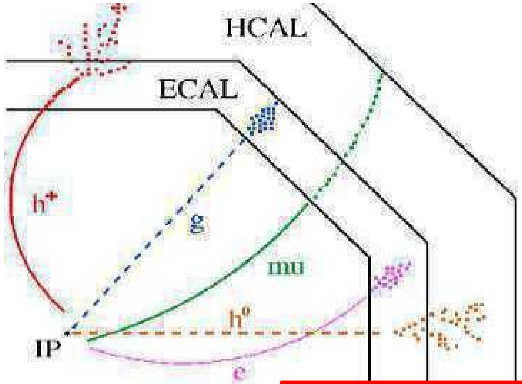
Fwd Calorimetry:

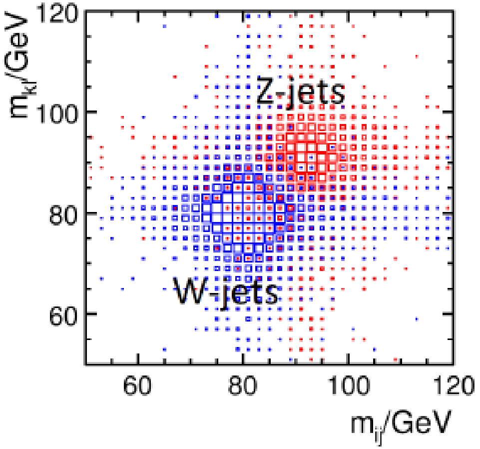
- lumi, veto, beam monitoring

Imaging Calorimetry

e.g.







Photons in jets

Tau physics (γ vs π_0)

2/3 of Hadr IA in ECAL

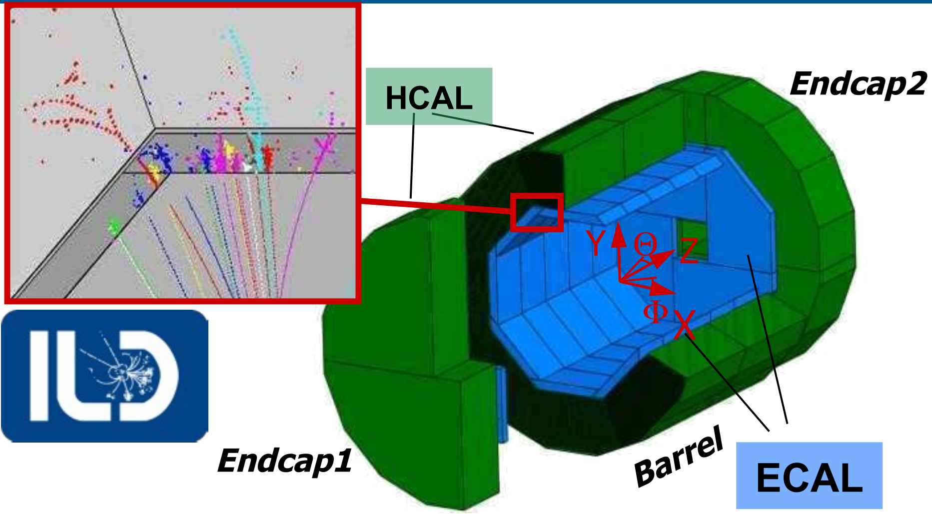
Particle Flow Algorithms :

- Jets = 65% charged Tracks + 25% γ ECAL + 10% h^0 CALO's
- TPC $\delta p/p \sim 5 \cdot 10^{-5}$; VTX $\sigma_{x,y,z} \sim 10$ µm

+ timing ?

H. Videau and J. C. Brient, "Calorimetry optimised for jets," in Proc. 10th International Conference on Calorimetry in High Energy Physics (CALOR 2002), Pasadena, California. March, 2002.

An Ultra-Granular SiW-ECAL for experiments



Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability (*E*, *(θ,φ)*, *t*)
- PFlow requirements:
  - Extremely high granularity
  - Compacity (density)

SiW+CFRC baseline choice for future Lepton Colliders:

- Tungsten as absorber material
  - $X_0 = 3.5$ mm, $R_M = 9$ mm, $\lambda_I = 96$ mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - **Support compact design: Sensor+RO≤2mm**
  - Allows for ~any pixelisation
  - Robust technology
  - **Excellent signal/noise ratio: ≥10**
  - **Intrinsic stability (vs environment, aging)**
  - **Albeit expensive…**
- Tungsten–Carbon alveolar structure
  - **Minimal structural dead-spaces**
  - **Scalability**

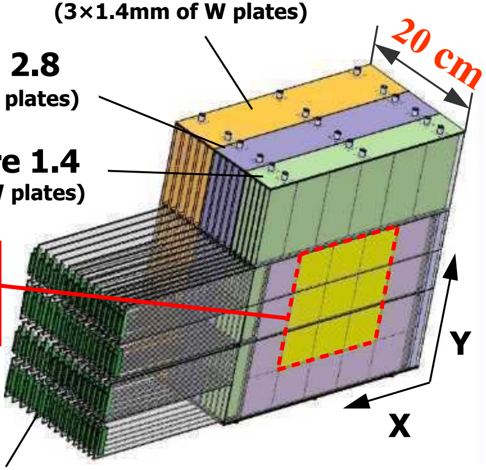
To be assessed by prototypes

CALICE SiW ECAL:
Physics & Technological prototypes

Physics prototype: 2005–2011

PFA proof of concept with comparison to MC
Electronics outside

- 1 × 1 cm² pixels



Structure 4.2
(3×1.4mm of W plates)

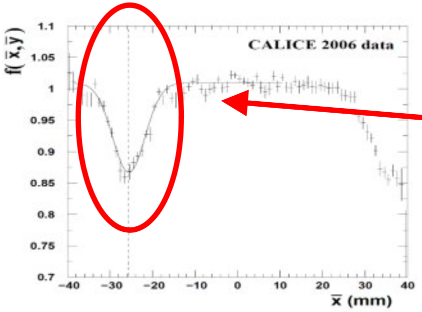
Structure 2.8
(2×1.4mm of W plates)

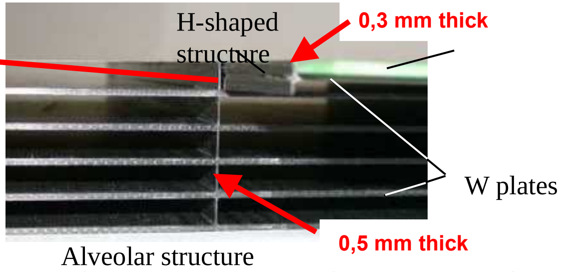
Structure 1.4
(1.4mm of W plates)

Active zone
~10000 pixels in 0.01 m³

16.5%(stochastic) 1–2% (constant) with 1–45 GeV e⁻/e⁺ at 2006/2008 BT

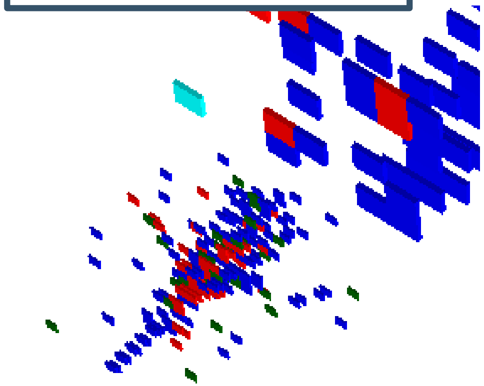
Detector slab (x30)



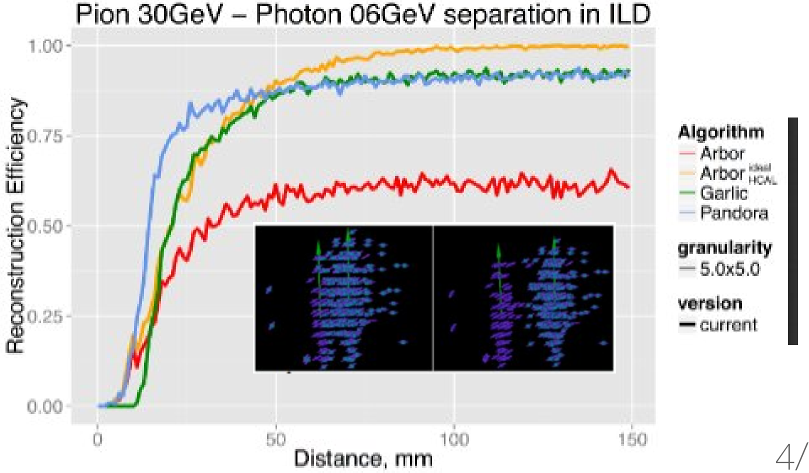


Alveolar structure

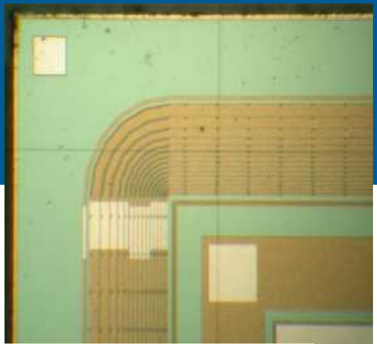
GEANT4

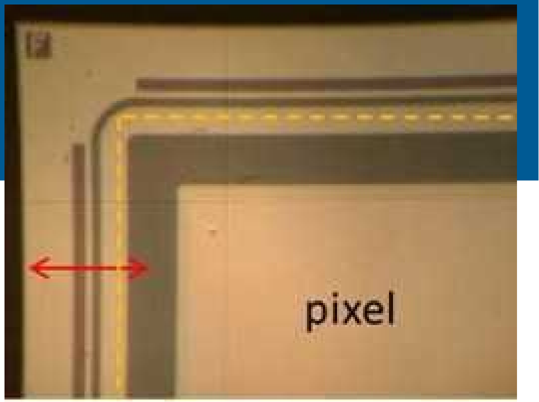


PFA reconstruction



Silicon Sensors





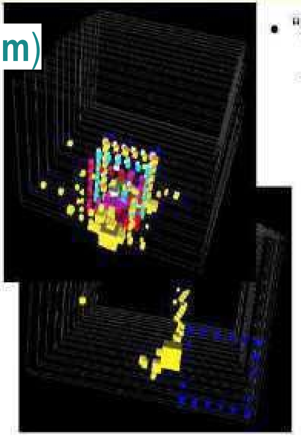
Cost driver

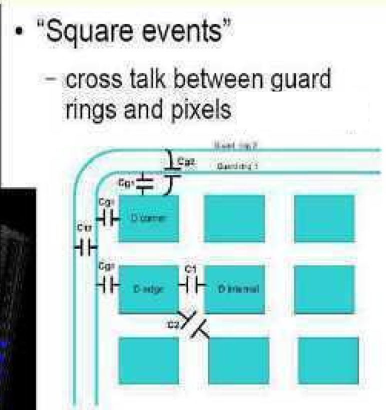
- ~30% of the total cost of the SiW-ECAL
    - ⇒ Units Cost reduction(**CALIIMAX ANR program**)
- Decoupling of Guard Ring (Square Events).
- new design of ILD detector

Wafers glued onto PCB's

Command Sensors (@ Hamamatsu)

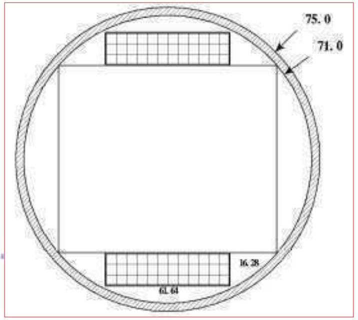
- ⚠ Minimal cost of Command ≥ 20k€
- direct contact with HPK engineers
- Possibility of design for 8'' in 186mm alveola 320 ⟶ 550, 650 ⟶ 725 μm ?

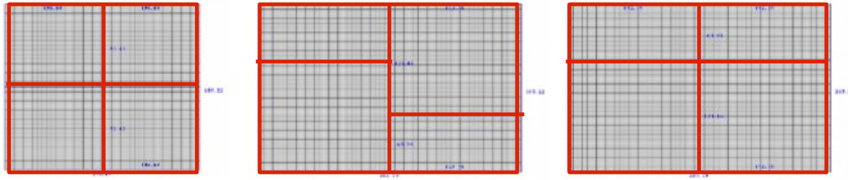




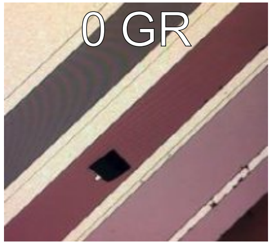
- "Square events"
    - cross talk between guard rings and pixels

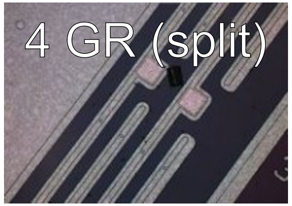
'quantum unit' of ILD dimensions (here 6'' wafer)

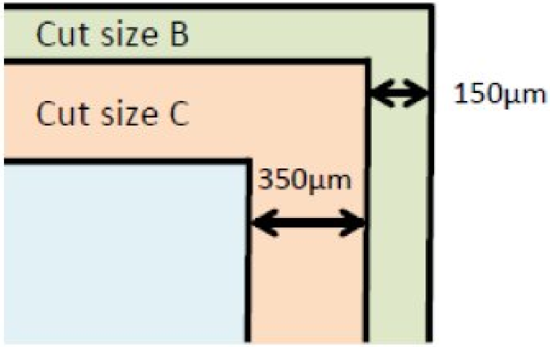




Guard Ring Studies (HPK)







Baby wafers: contig. & segmented Guard ring - 0, 1, 2, 4

- Floating 1 GR ⇒ ‘square events’
- Addit’l GR ⇒ higher BD voltage

Cuts size ~ insensitive edge

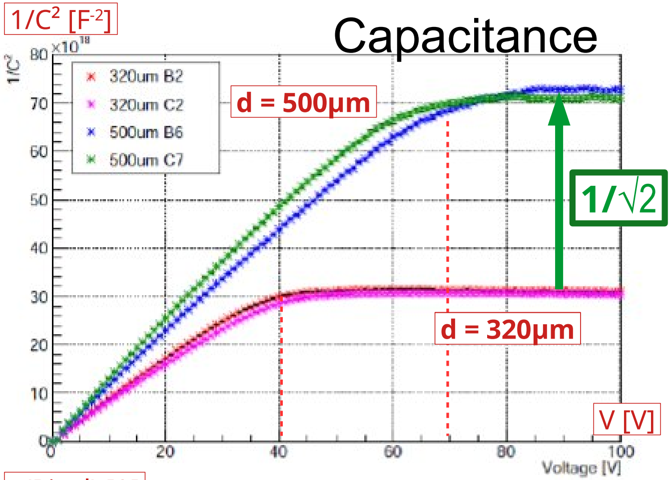
- Cut size B = 500 µm
- Cut size C = 350 µm

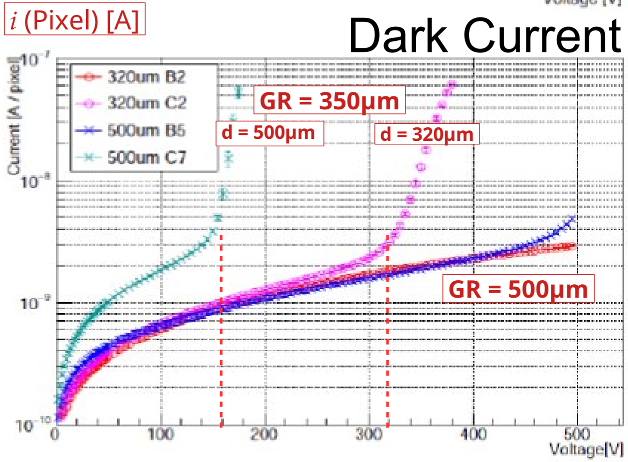
Prelim Conclusions:

- 320µm cut size C ✔
- 500 µm cut size B preferable

new 2018: 550 & 650µm wafers

- no yet used

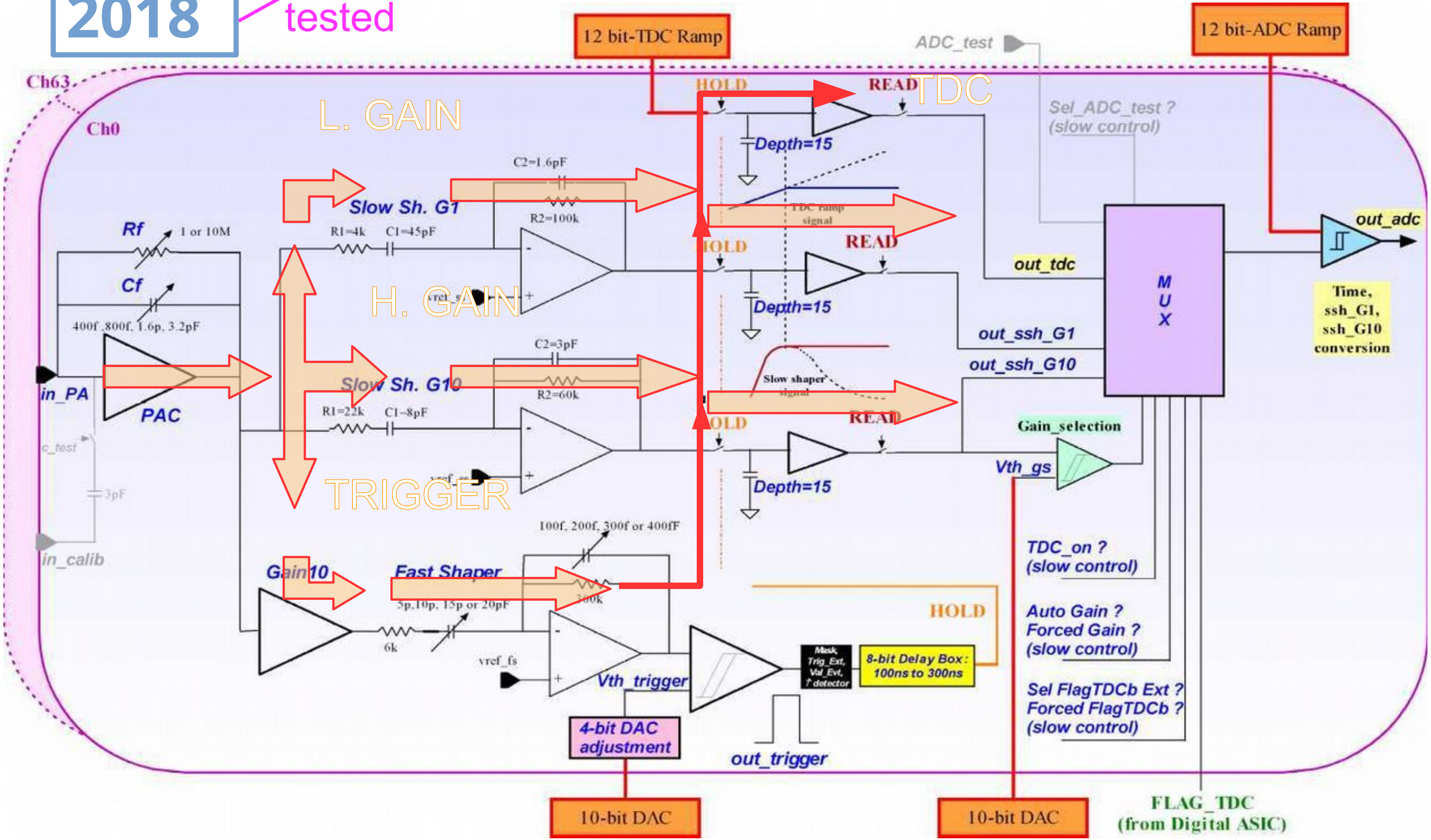




SKIROC2 / 2A Analogue core

2018

tested



Similar to SiD Kpix

- 64 channels
- Preamp
  + 2 (auto)Gains
  + TDC (~1.4ns)
- Auto-triggered
  - per cell adj.
- 15 (×2) analogue memories
- Low consumption
  - 25 µW/ch
    with 0.5% ILC-like duty cycle
- Power-pulsed

Not final chip
(full 0-suppr.)

SiW-ECAL Building blocks: SLAB’s & ASU’s

R&D for “mass production” and QA

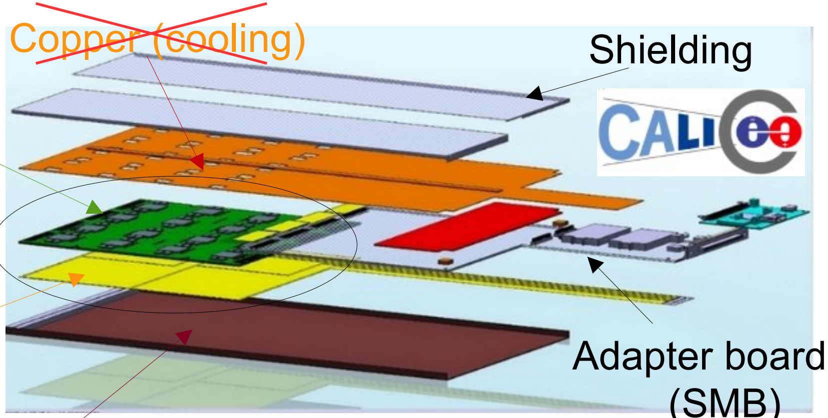
- Quality tests & preparation of large production
- Modularity → ASU & SLABs
- Choice of square wafers
  - (≠ from hex: SiD, CMS HGCAL)

Numbers (RECAL = 1,8 m, |ZEndcaps|=2,35m) (likely to be reduced by 30–40%)

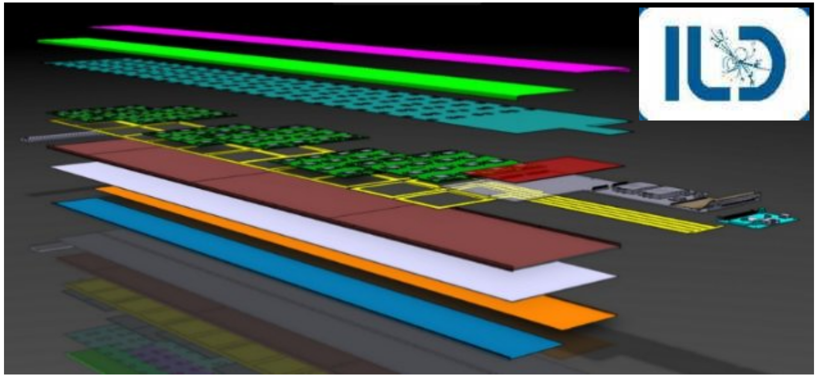
- Barrel modules: 40 (as of today all identical)
- Endcap Modules: 24 (3 types)
- ASUs = ~75,000
  - Wafers ~ 300,000 (2500 m²)
  - VFE chips ~ 1,200,000
  - Channels: 77Mch
- Slabs = 6000 (B) + 3600 (EC) = 9600
  - ≠ lengths and endings

Tests of producibility

Tests of feasability



U layout of a **short slab**



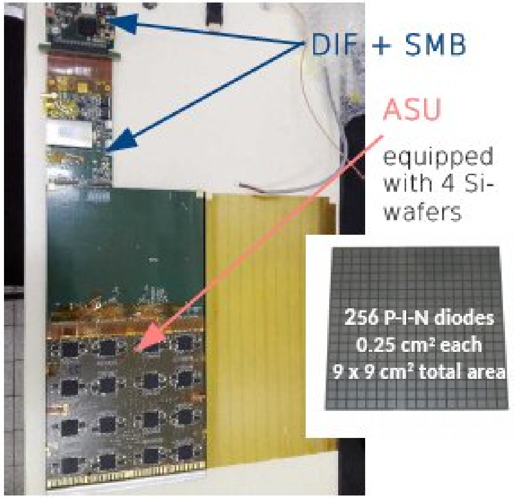
U layout of a **long slab**

ASU: 11 years of R&D

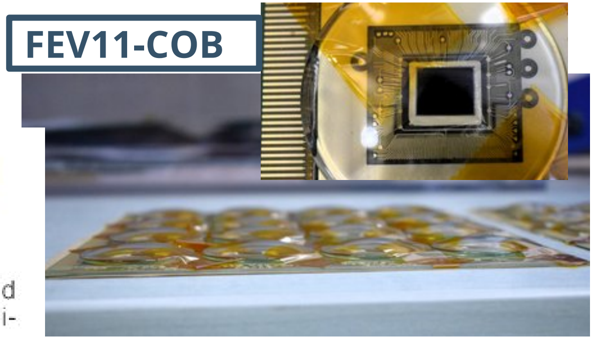
Most complex element: electro-mechanical integration

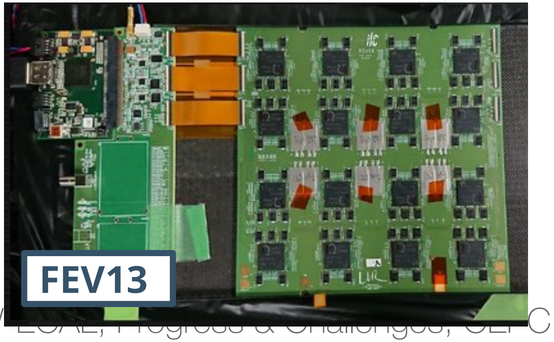
- Distrib / Collect signals from VFE (ASICs),
  Analog & Digital with dyn. range ≥ 7500
- Mechanical placer & holder for Wafers → precision
- Thickness constraints

FEV11



FEV11-COB





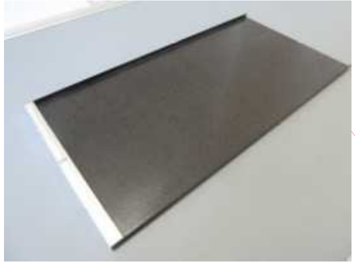
FEV13

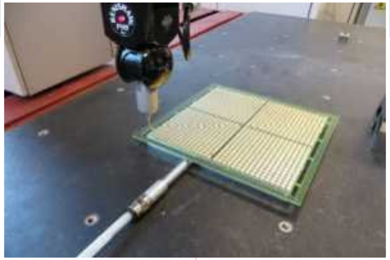
Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	FEV11	7 units	
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 (12)$_{\text{Trig}}$, 6–8 % masked
1st technological ECAL	2018	SLABvFEV11 & FEV13 SK2a+ Compact stack Long Slab	SK2 & SK2a (ↄtiming) 8 ASUs	Improved S/N Timing...

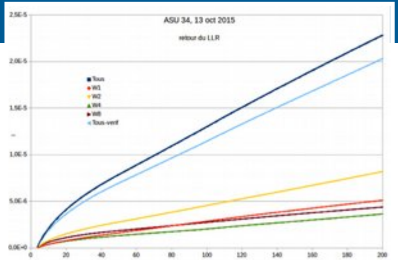
Assembly chain Paris

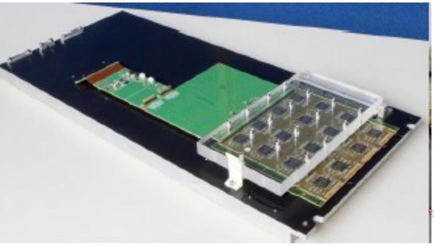
‘Simplified view’

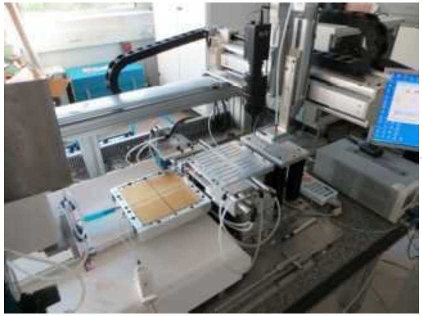
AIDA 2020

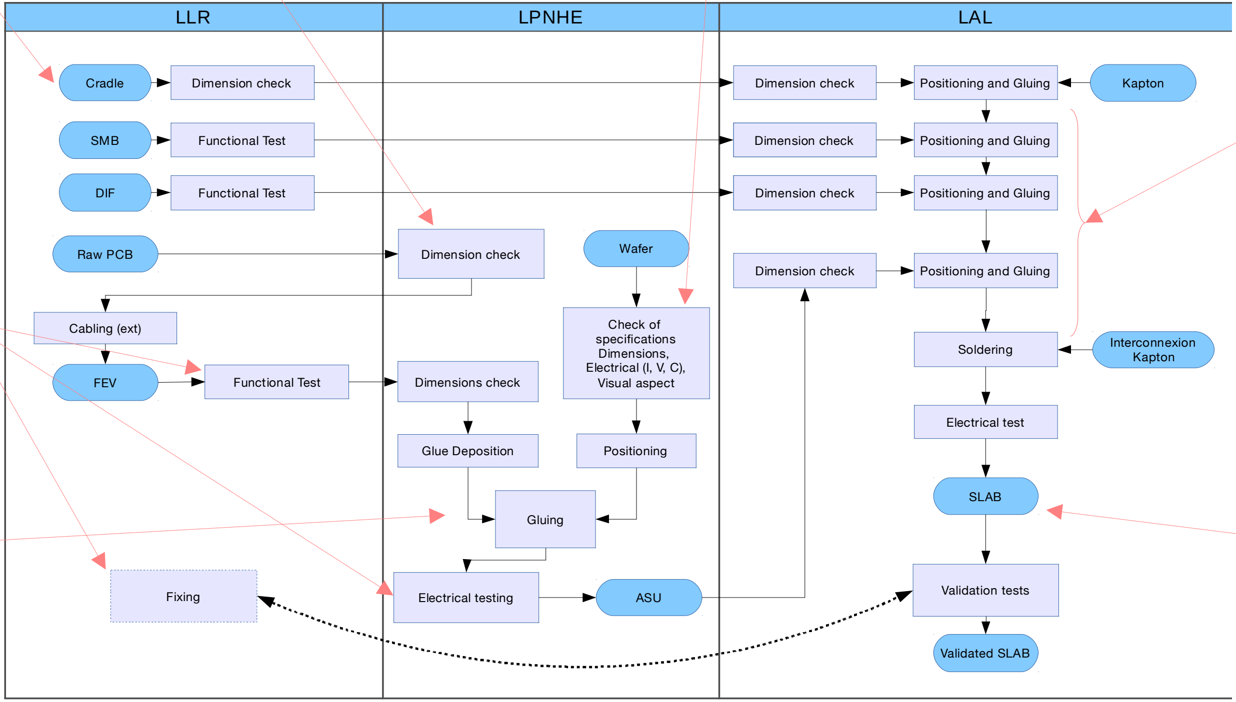












LLR

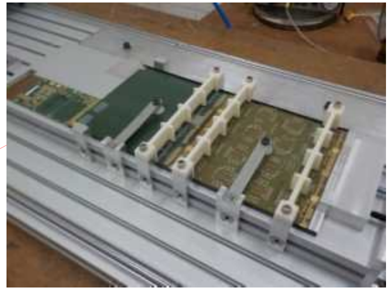
- Cradle → Dimension check
- SMB → Functional Test
- DIF → Functional Test
- Raw PCB
- Cabling (ext)
- FEV → Functional Test
- Fixing

LPNHE

- Dimension check
- Wafer → Check of specifications Dimensions, Electrical (I, V, C), Visual aspect → Positioning
- Dimensions check → Glue Deposition
- Gluing
- Electrical testing → ASU

LAL

- Dimension check → Positioning and Gluing ← Kapton
- Dimension check → Positioning and Gluing
- Dimension check → Positioning and Gluing
- Dimension check → Positioning and Gluing
- Soldering ← Interconnexion Kapton
- Electrical test
- SLAB
- Validation tests
- Validated SLAB

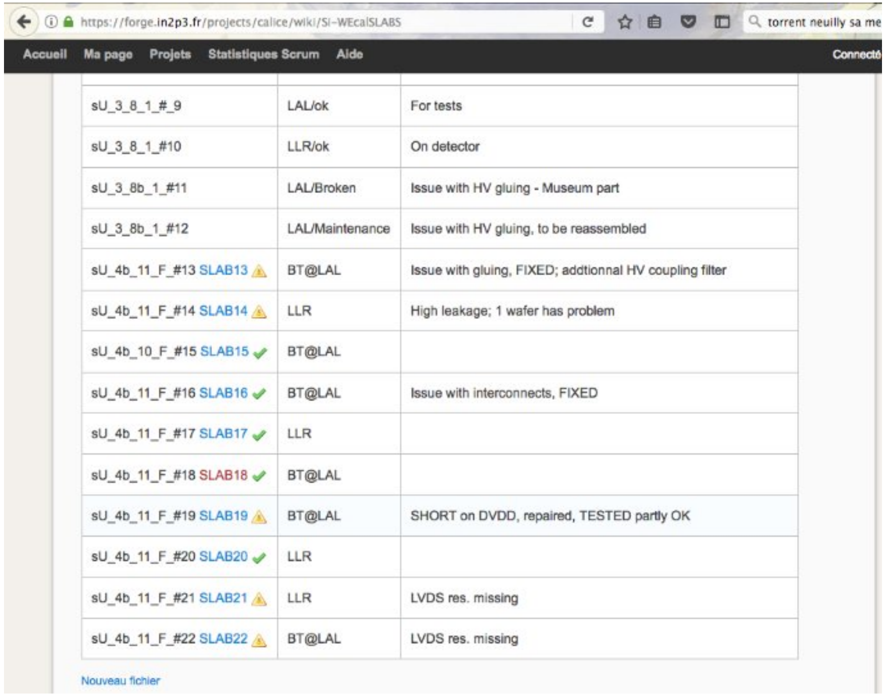


Data-Quality: 10 SLABs produced in 2016

Forge Page (redmine in2p3, LLR) Boards

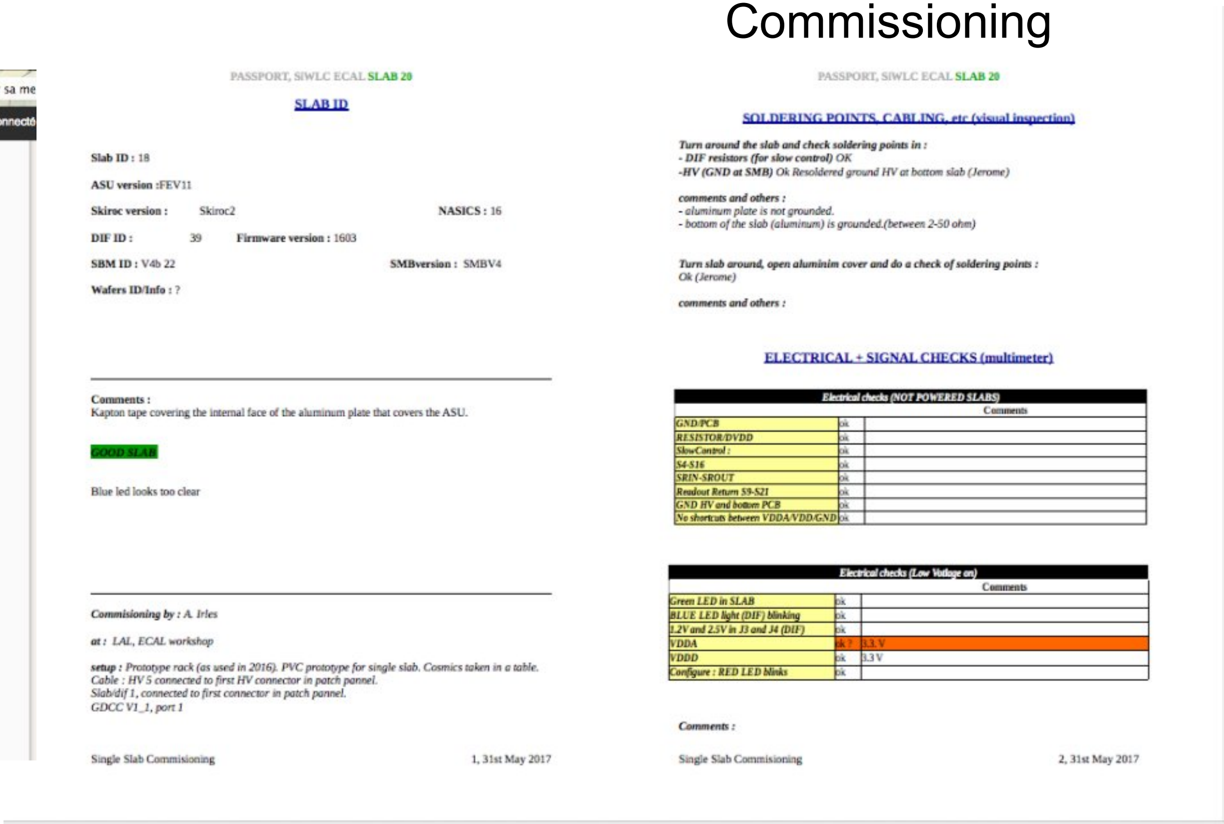
Files: Wafer test (LPNHE),

Passport (LAL) Commissioning



sU_3_8_1_#_9	LAL/ok	For tests
sU_3_8_1_#10	LLR/ok	On detector
sU_3_8b_1_#11	LAL/Broken	Issue with HV gluing - Museum part
sU_3_8b_1_#12	LAL/Maintenance	Issue with HV gluing, to be reassembled
sU_4b_11_F_#13 SLAB13 ⚠	BT@LAL	Issue with gluing, FIXED; addtionnal HV coupling filter
sU_4b_11_F_#14 SLAB14 ⚠	LLR	High leakage; 1 wafer has problem
sU_4b_10_F_#15 SLAB15 ✓	BT@LAL	
sU_4b_11_F_#16 SLAB16 ✓	BT@LAL	Issue with interconnects, FIXED
sU_4b_11_F_#17 SLAB17 ✓	LLR	
sU_4b_11_F_#18 SLAB18 ✓	BT@LAL	
sU_4b_11_F_#19 SLAB19 ⚠	BT@LAL	SHORT on DVDD, repaired, TESTED partly OK
sU_4b_11_F_#20 SLAB20 ✓	LLR	
sU_4b_11_F_#21 SLAB21 ⚠	LLR	LVDS res. missing
sU_4b_11_F_#22 SLAB22 ⚠	BT@LAL	LVDS res. missing

Nouveau fichier



PASSPORT, SIWLC ECAL **SLAB 20**

SLAB ID

Slab ID : 18

ASU version :FEV11

Skiroc version : Skiroc2 **NASICS :** 16

DIF ID : 39 **Firmware version :** 1603

SBM ID : V4b 22 **SMBversion :** SMBV4

Wafers ID/Info : ?

Comments :
Kapton tape covering the internal face of the aluminum plate that covers the ASU.

GOOD SLAB

Blue led looks too clear

Commisioning by : *A. Irles*

at : *LAL, ECAL workshop*

setup : *Prototype rack (as used in 2016). PVC prototype for single slab. Cosmics taken in a table.*
Cable : HV 5 connected to first HV connector in patch pannel.
Slab/dif 1, connected to first connector in patch pannel.
GDCC V1_1, port 1

Single Slab Commisioning 1, 31st May 2017

PASSPORT, SIWLC ECAL **SLAB 20**

SOLDERING POINTS, CABLING, etc (visual inspection)

Turn around the slab and check soldering points in :
- DIF resistors (for slow control) *OK*
-HV (GND at SMB) *Ok Resoldered ground HV at bottom slab (Jerome)*

comments and others :
- aluminum plate is not grounded.
- bottom of the slab (aluminum) is grounded.(between 2-50 ohm)

Turn slab around, open aluminim cover and do a check of soldering points :
Ok (Jerome)

comments and others :

ELECTRICAL + SIGNAL CHECKS (multimeter)

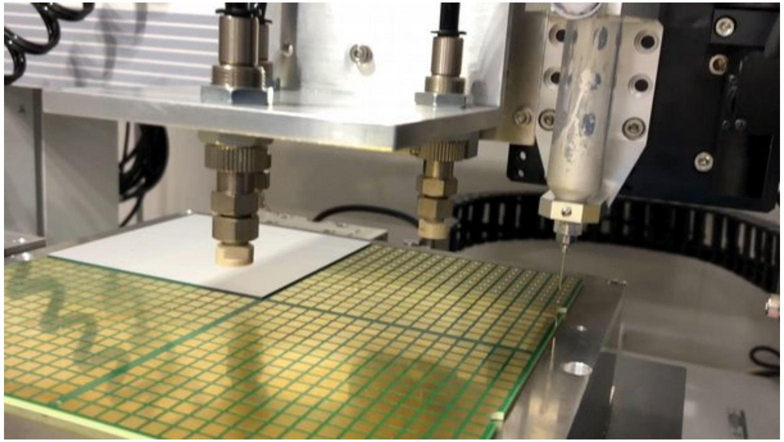
Electrical checks (NOT POWERED SLABS)		
		Comments
GND/PCB	ok	
RESISTOR/DVDD	ok	
SlowControl :	ok	
S4-S16	ok	
SRIN-SROUT	ok	
Readout Return S9-S21	ok	
GND HV and bottom PCB	ok	
No shortcuts between VDDA/VDD/GND	ok	

Electrical checks (Low Voltage on)		
		Comments
Green LED in SLAB	ok	
BLUE LED light (DIF) blinking	ok	
1.2V and 2.5V in J3 and J4 (DIF)	ok	
VDDA	ok ?	3.3. V
VDDD	ok	3.3 V
Configure : RED LED blinks	ok	

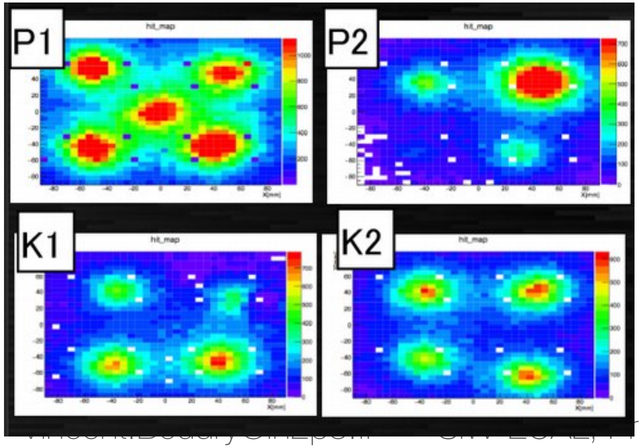
Comments :

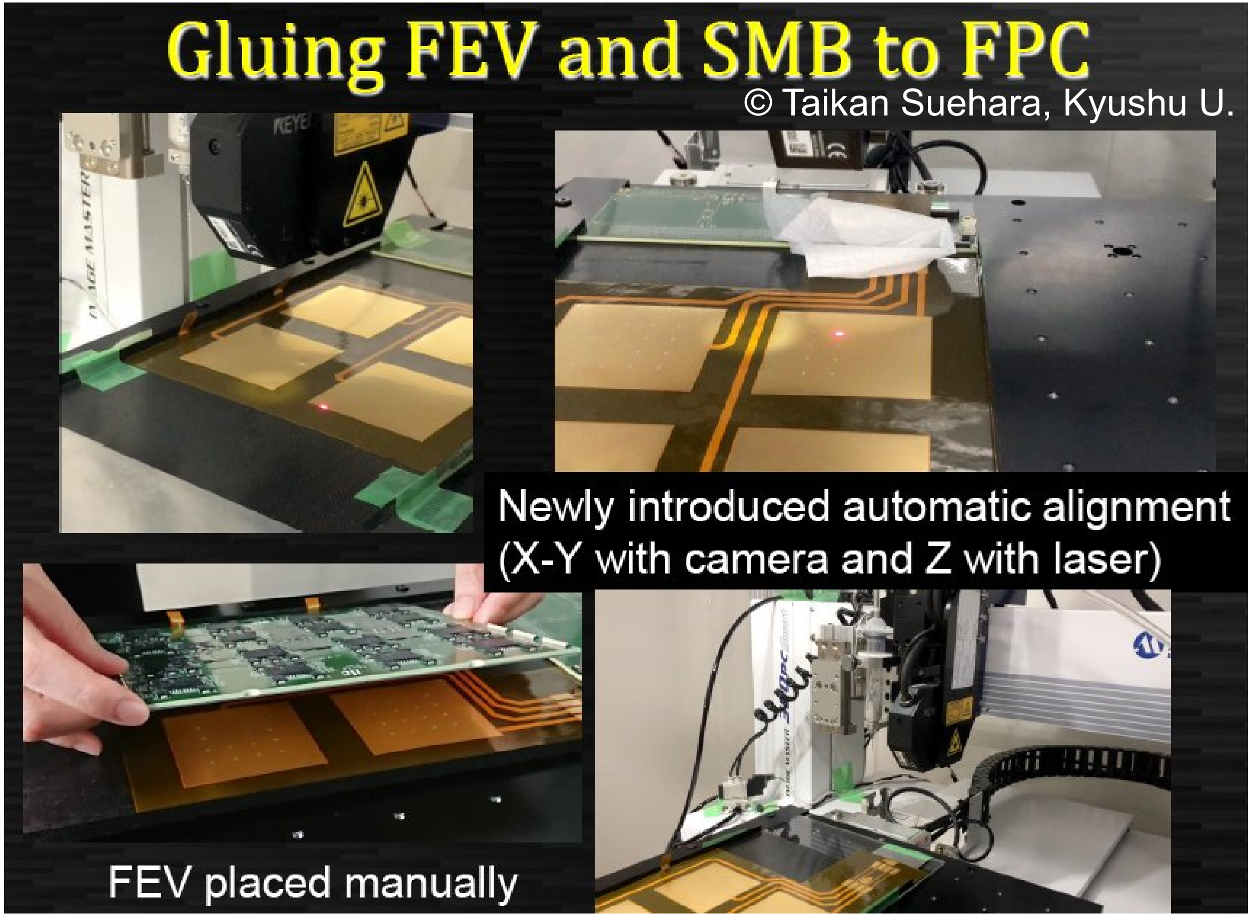
Single Slab Commisioning 2, 31st May 2017

Second assembly bench @ Kyushu



^{57}Co response   S/N$_{ADC}$ ~ 30





Gluing FEV and SMB to FPC

© Taikan Suehara, Kyushu U.

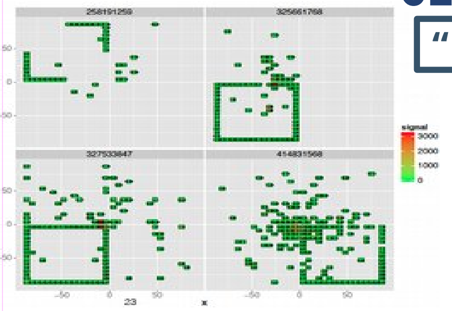
Newly introduced automatic alignment (X-Y with camera and Z with laser)

FEV placed manually

Beam-test 2015–2018

CERN 2015

"Naked FEV11"

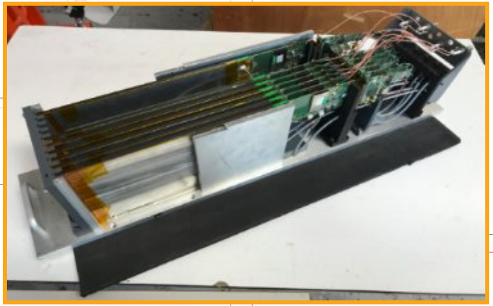


S/N_{ADC} = 16–17

(MIP – ped) / σ_{ped}

Defaults cataract :

- Negative signals
- re-triggers
- ~ high thr.
- sq events / 10



DESY 2018

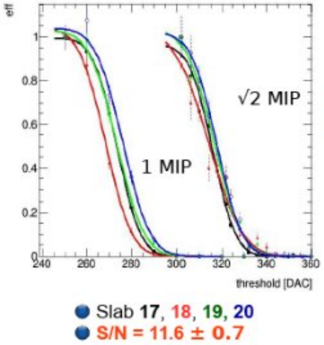
7 FEV11 + 1 FEV13(650µm)

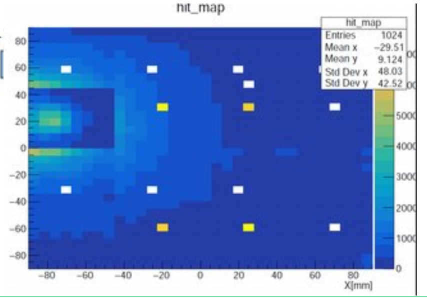
S/N_{Trig} ~ 11.6±0.7

Trigger → ~1/3 mip (est.)

First comm. of FEV13

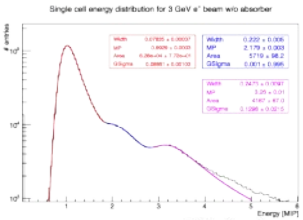
S/N_{ADC} ~ 30-40

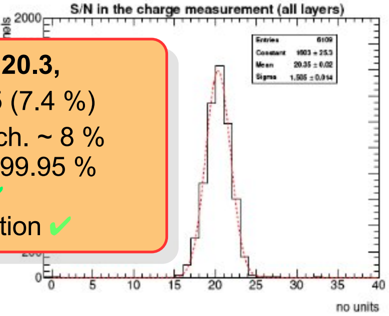




DESY 2017

7 FEV11





S/N_{ADC} = 20.3,

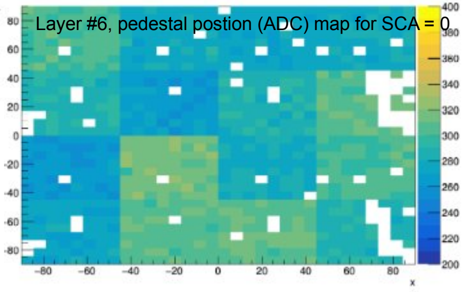
$\sigma_{S/N}$ = 1.5 (7.4 %)

masked ch. ~ 8 %

Hit eff. ~ 99.95 %

0°, 45° ✓

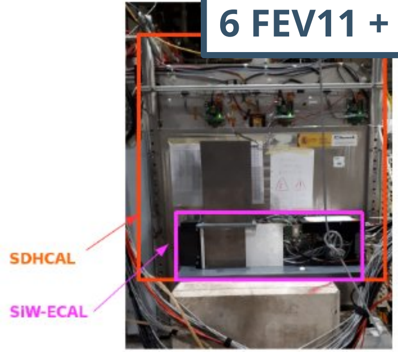
1T operation ✓

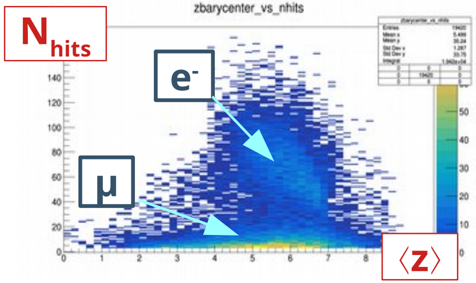


CERN 2018

Masked ch (FEV11) ~ 4 %

6 FEV11 + 4 FEV13(320 & 650µm) + 24X_0 W





Mechanical Assembly for SLABs

Assembly bench for:

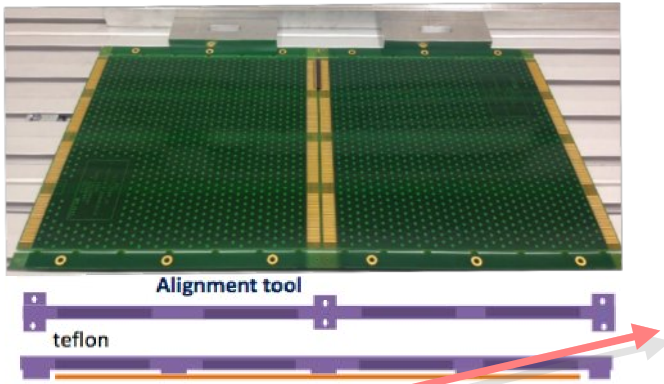
- Fragile Wafer
- Precision of PCB's ~ 50µm

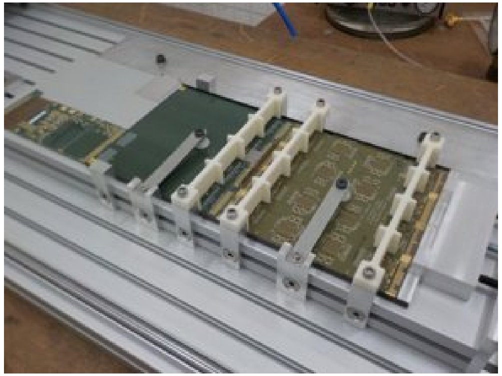
  ⇒ precision of 100µm on SLAB
- Interconnection

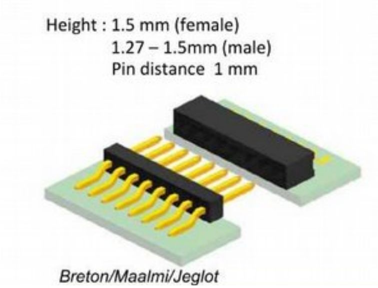
Connections to be handled by industry

- Dedicated Kaptons ✘
- Connectors

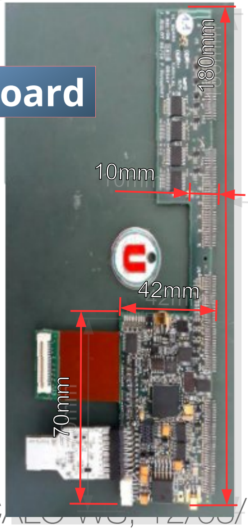
End of Slab and DAQ R&D

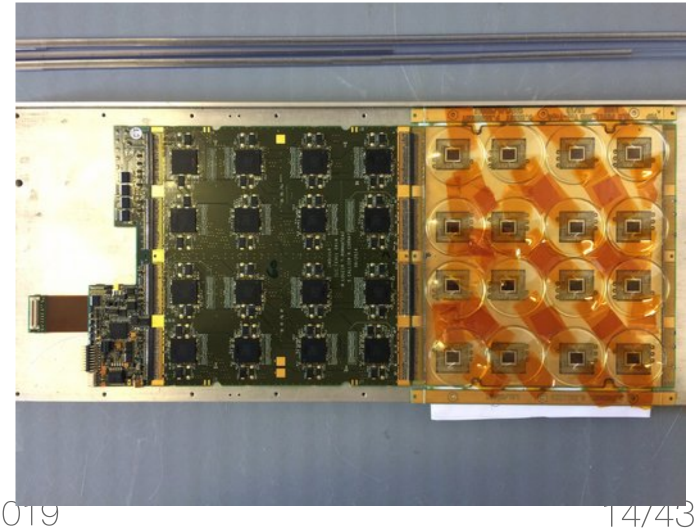






SL-board



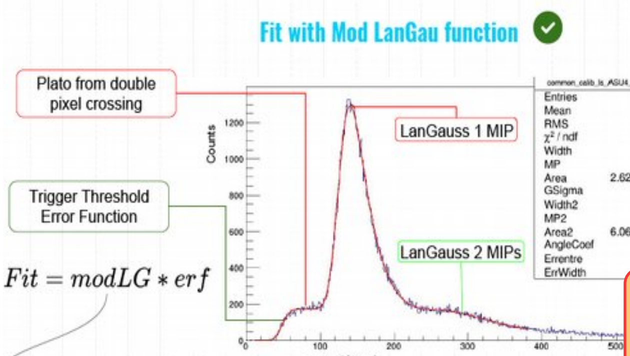


1st ‘electric long slab’ (2018)

Support of interface boards + 12 ASUs (DBD)

- 2+6+4 ASUs = ~3.2 m
- Rotatably along long axis (for beam test)

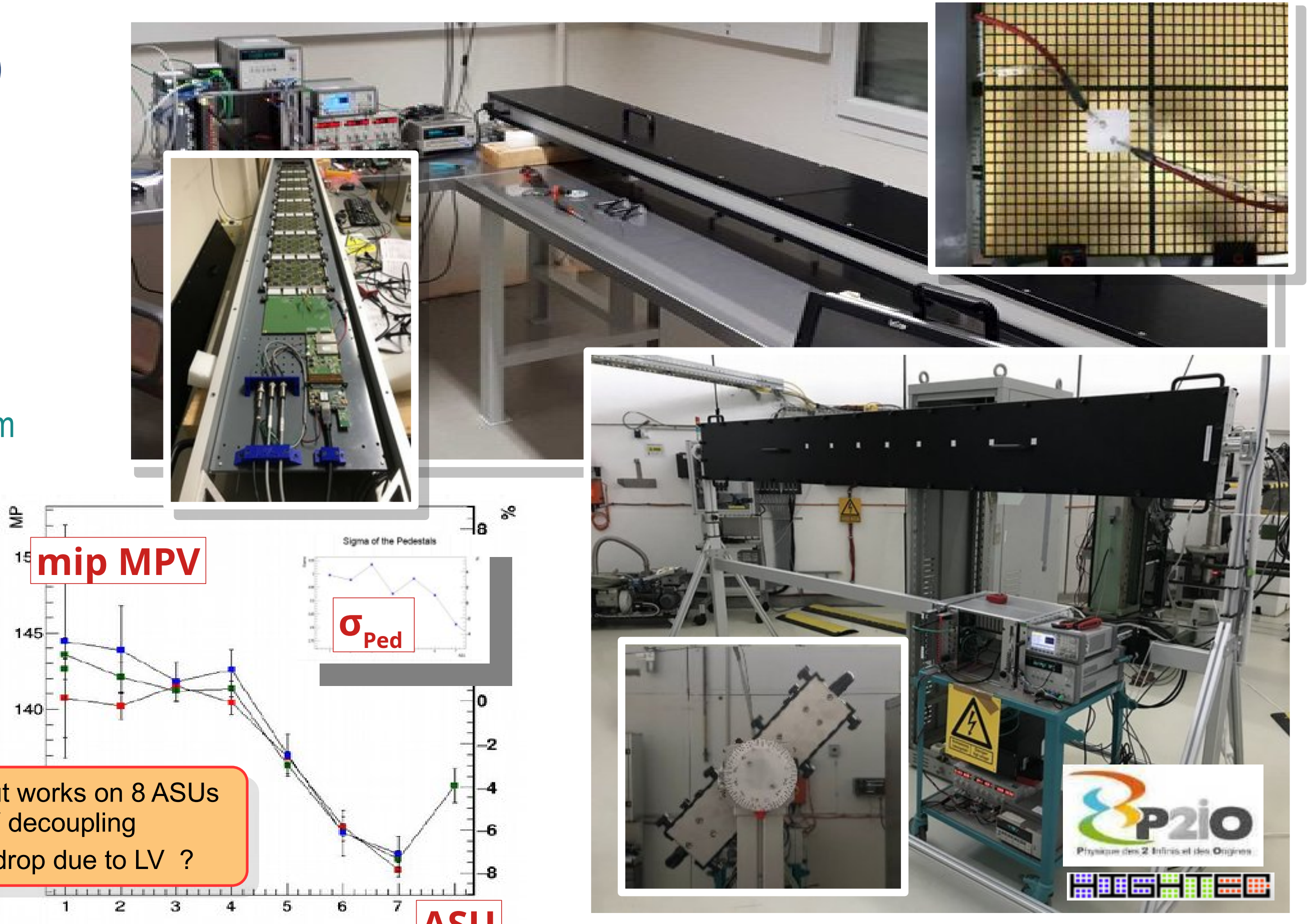
  Rigidity : ≤ ~1 mm per ASU
- Total access to upper and lower parts
  - 320µm Baby wafers (4×4 pixels) on the bottom



$$Fit = modLG * erf$$

$$modL(x,\mu,\sigma) = (1-c) * L(x,\mu,\sigma) + c * \int_{x}^{+\infty} \frac{L(t,\mu,\sigma)}{t} dt$$

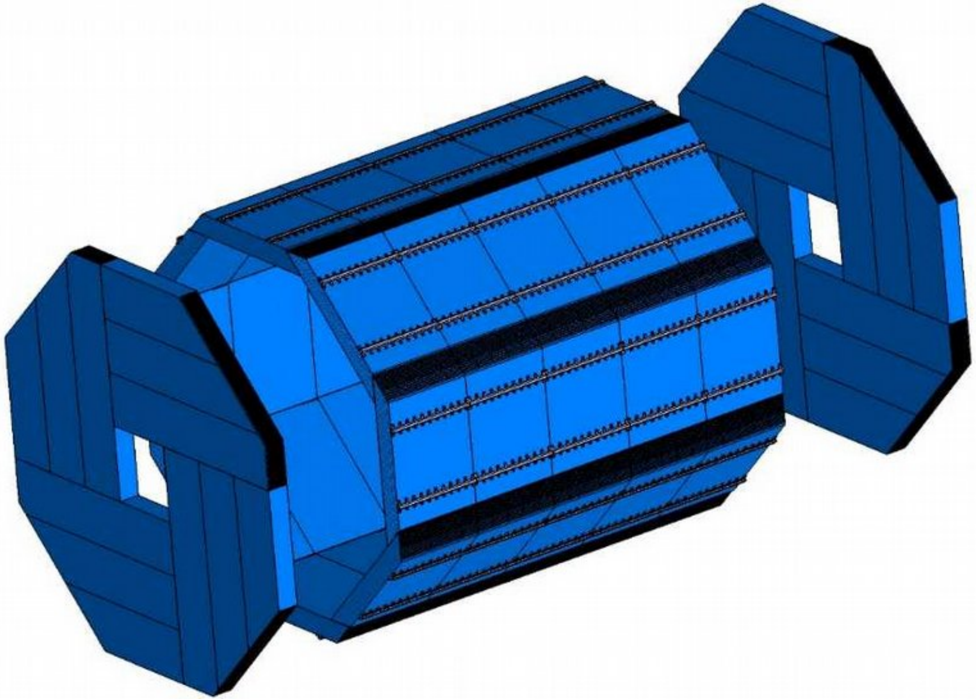
$$modLG = \int_{-\infty}^{+\infty} modL(t,\mu,\sigma) * G(x-t,\mu_G,\sigma_G) dt$$

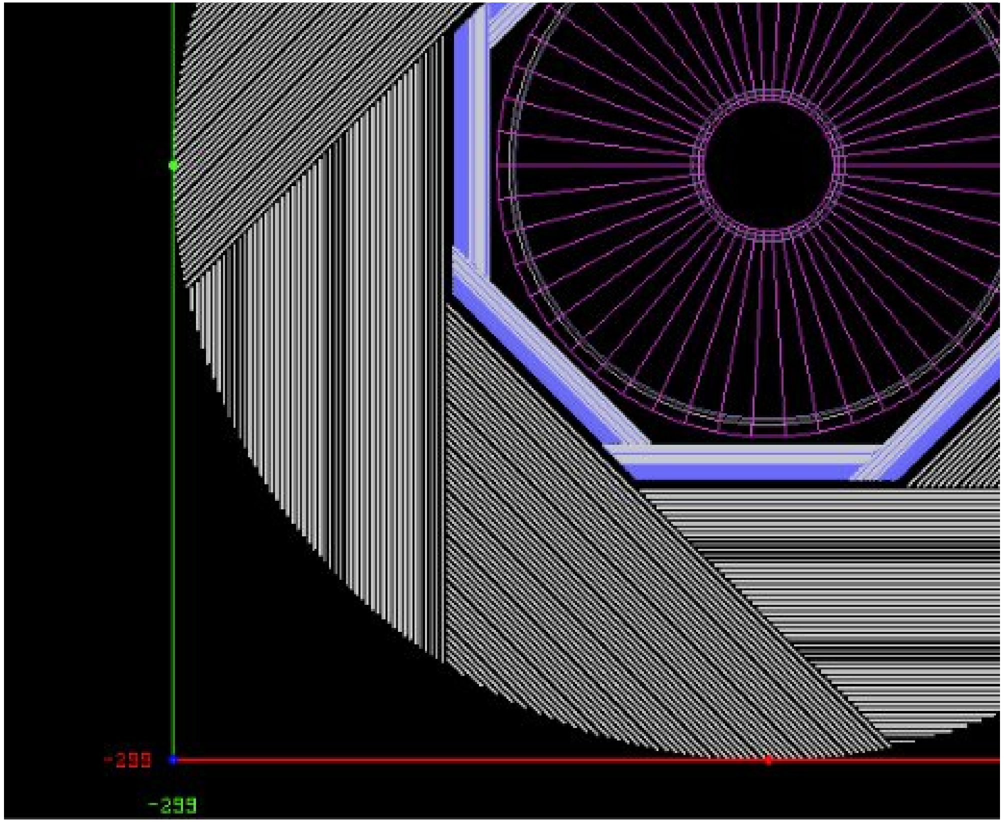


- Readout works on 8 ASUs with HV decoupling
- ~10 % drop due to LV ?

ILD conception

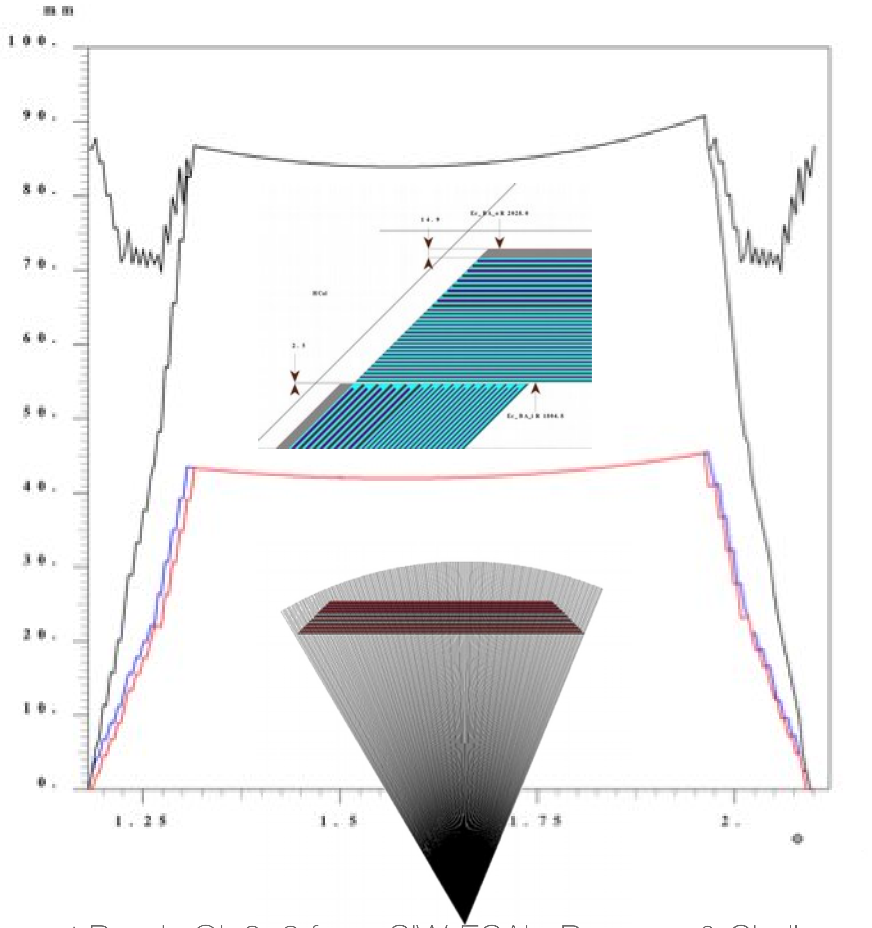
A crack-less ECAL geometry

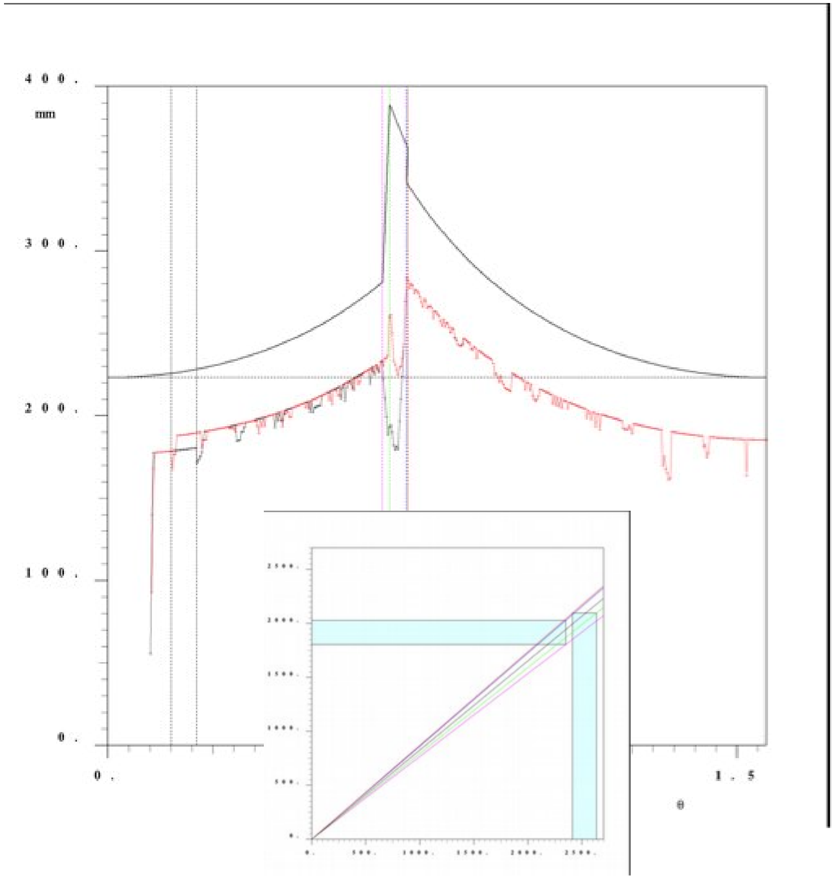




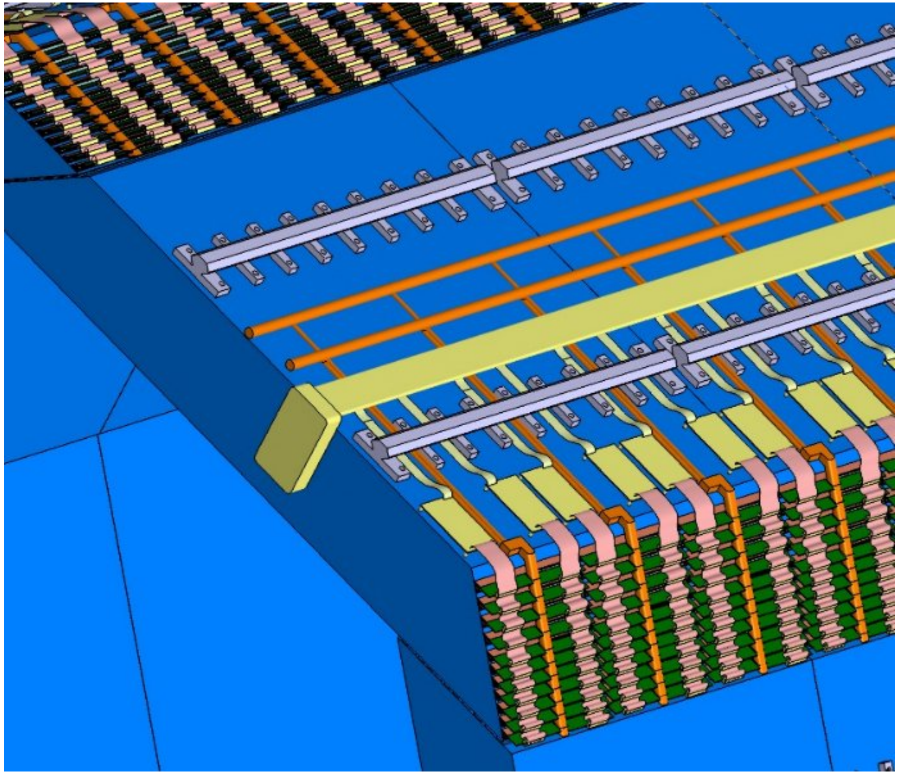
Vincent.Boudry@in2p3.fr

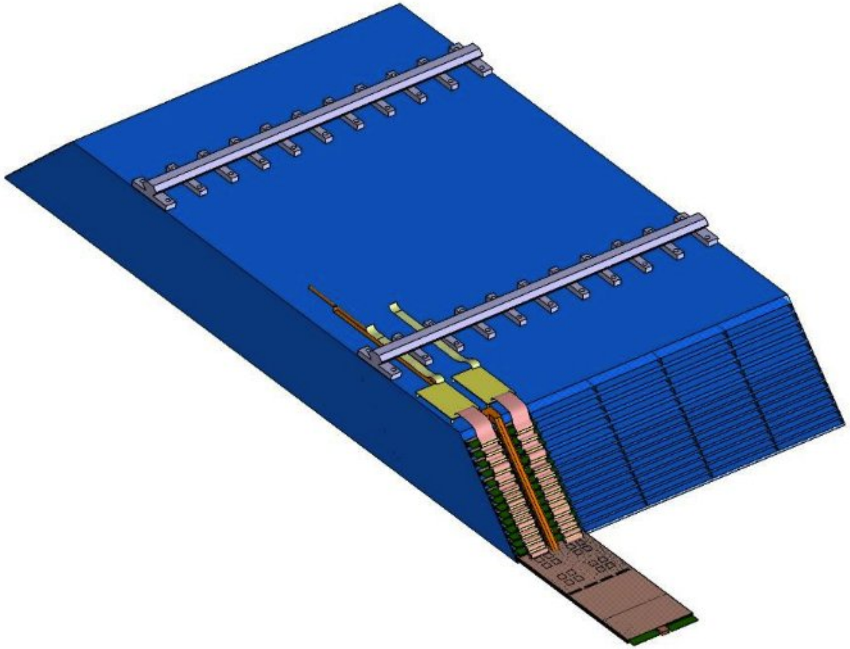
ILD ECAL Uniformity



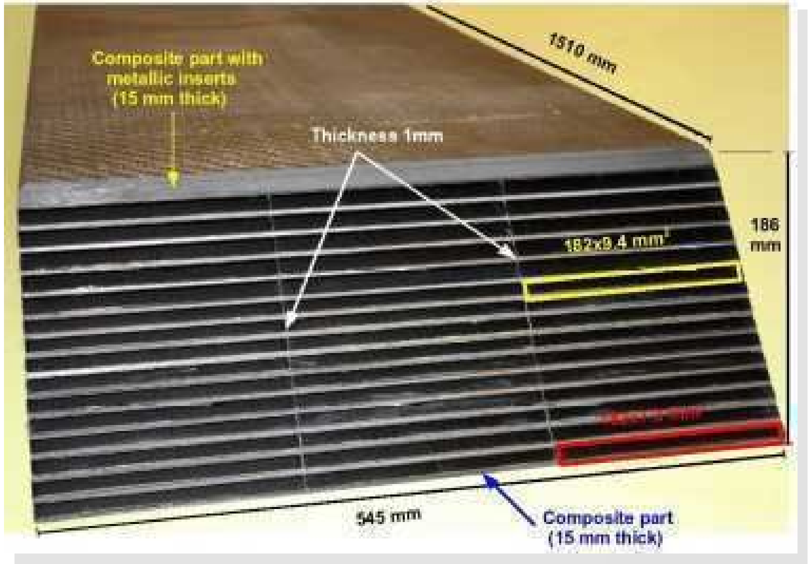


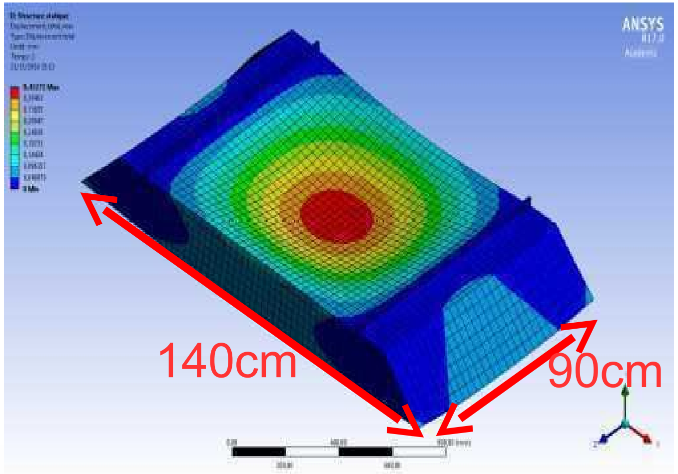
Modules





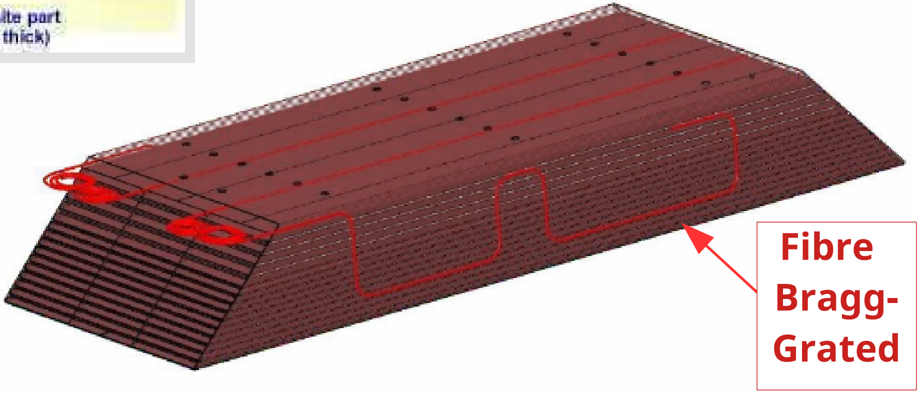
CFRC+W Structures ILD Design





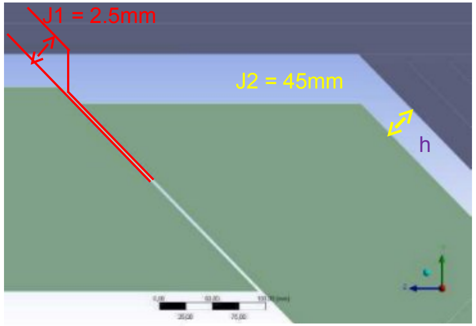
Study by M. Anduze

Measurements
with FBG
still to be done...

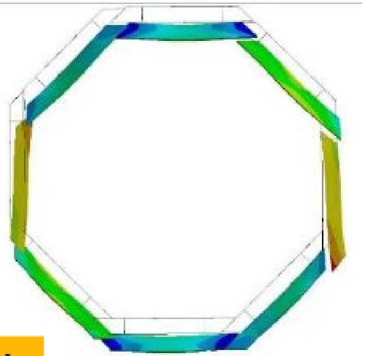


Fibre Bragg-Grated

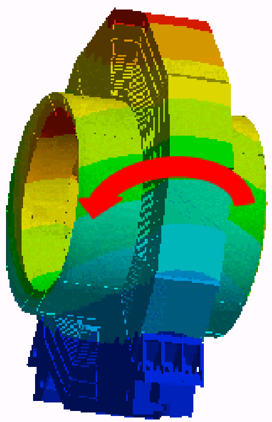
Static and Dynamic Simulations



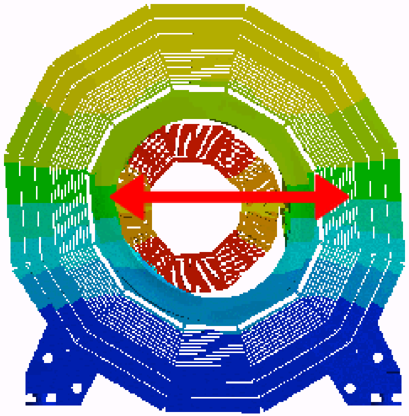
Study by T. Pierre-Émile Thomas



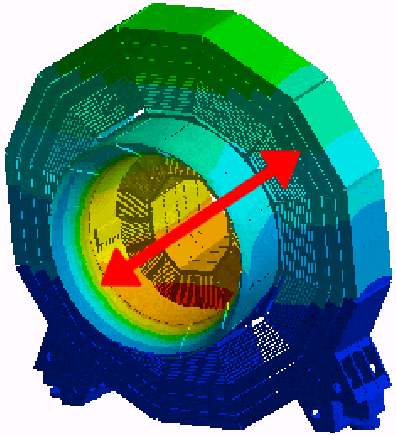
Mode 1 @ 2,3Hz



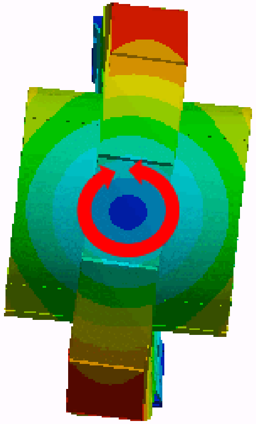
Mode 2 @ 3,05Hz



Mode 3 @ 3,8Hz



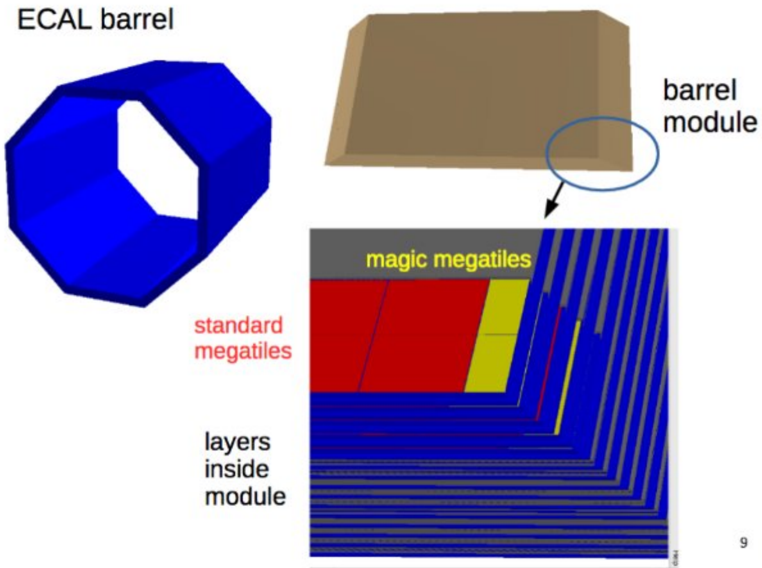
Mode 6 @ 7Hz



Simulation

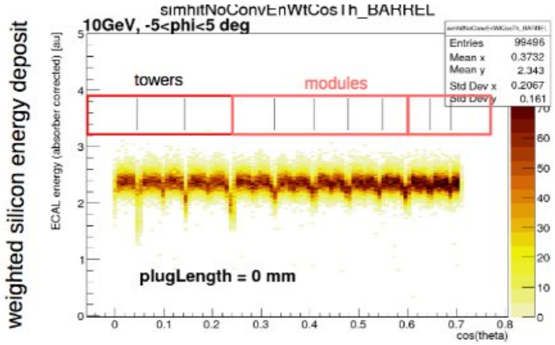
ECAL driver used in ILD models has been largely re-written (Mokka → DD4HEP)

- more modular code:
- less duplication Barrel & Endcap
- more configurable…

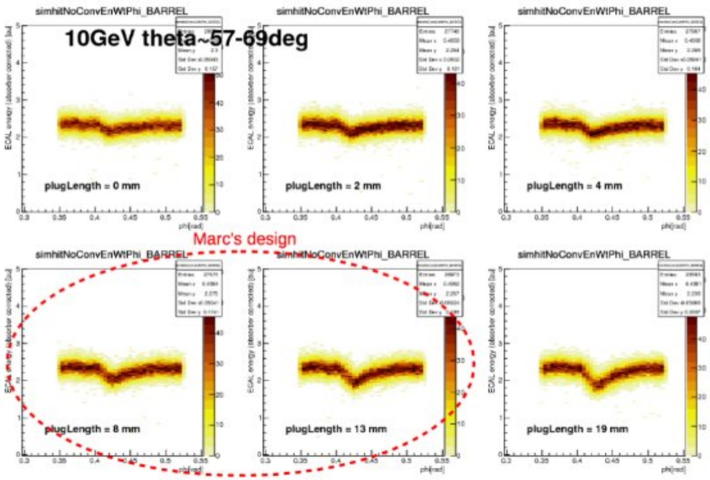


Effect of cracks [RAW= no correction at all!!]

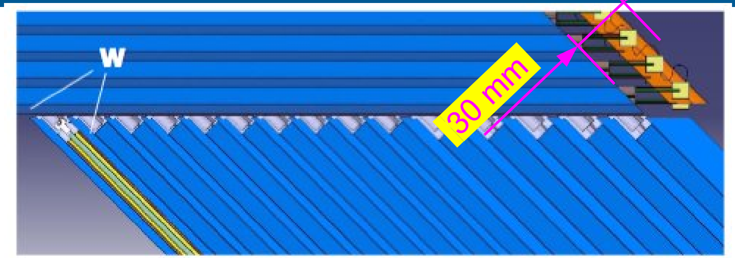
- Drop ~ 15%

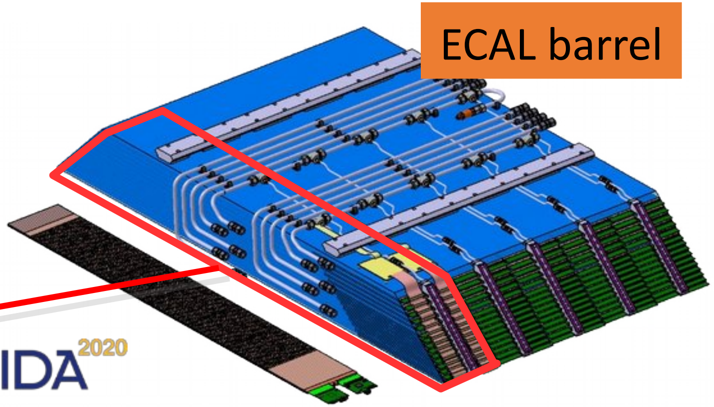


Effect of plug (missing in previous simulations)

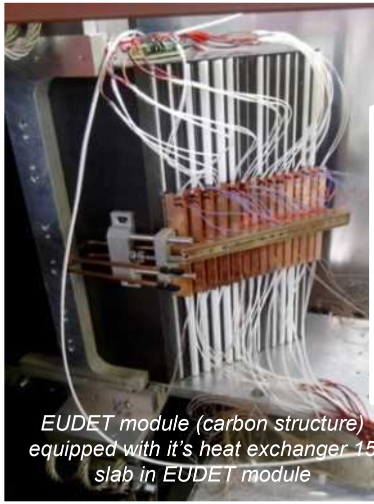


Rails, Cables & Pipes (Services)

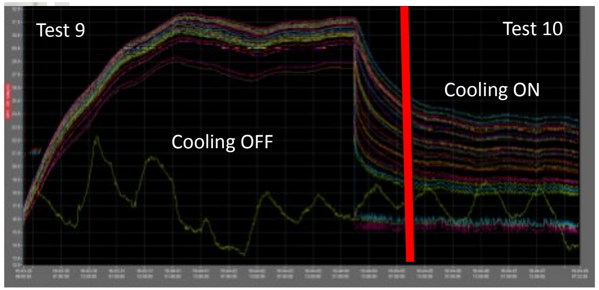




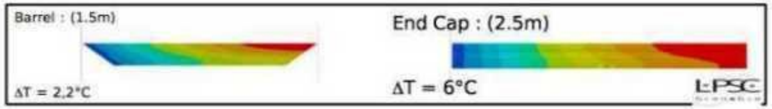
ECAL barrel



EUDET module (carbon structure) equipped with it's heat exchanger 15 slab in EUDET module



First tests results in line with simulations

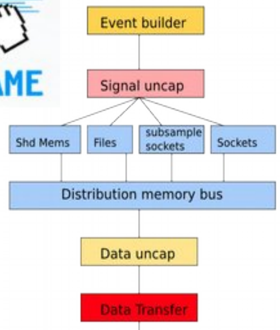


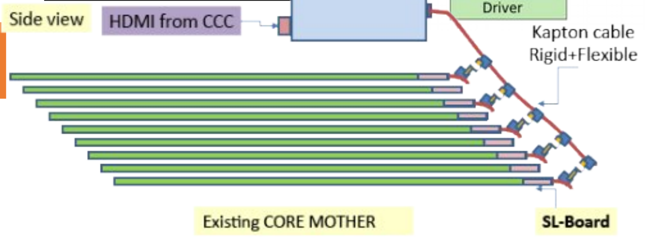
AIDA 2020

ECAL end cap

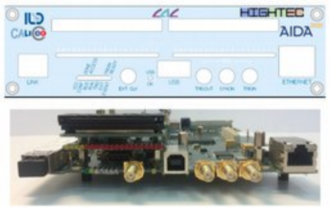
DAQ

PYRAME





Existing CORE MOTHER



P2IO Physique des 2 Infinis et des Origines

HIGHTEC

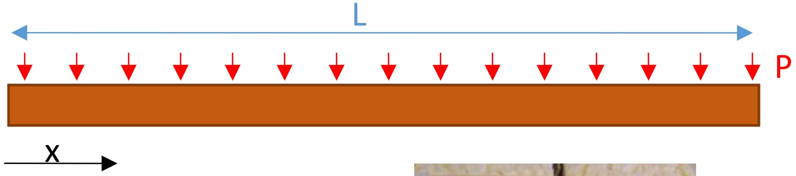
on going...

Active cooling

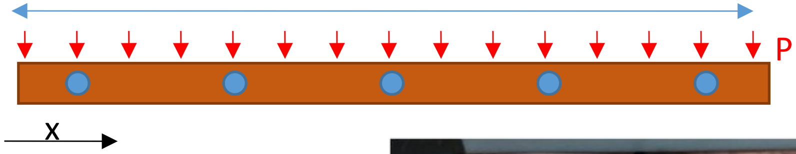
R&D using CMS studies (Thanks to Th. Pierre-Emile from CMS-LLR group)

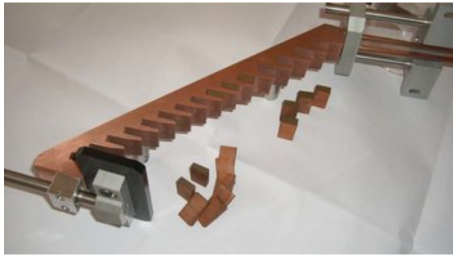
J.C. Brient @ CEPC 2018

Passive cooling

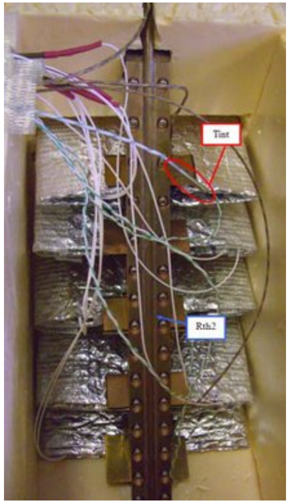


Active cooling





Passive cooling ramp example



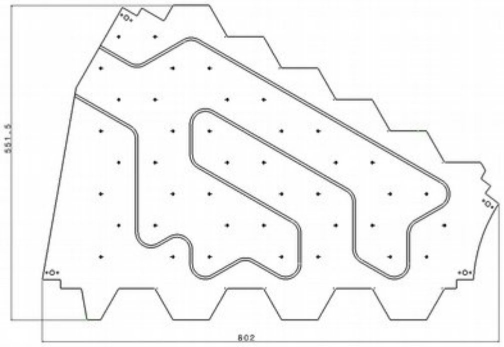
Passive cooling ramp set up test

Active cooling test layout (400mm x 300mm x 3mm thick copper plate with 1,8OD pipes embedded)

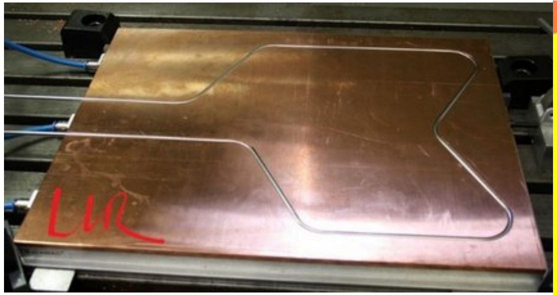
Active cooling set up test with water at room temperature

Active cooling

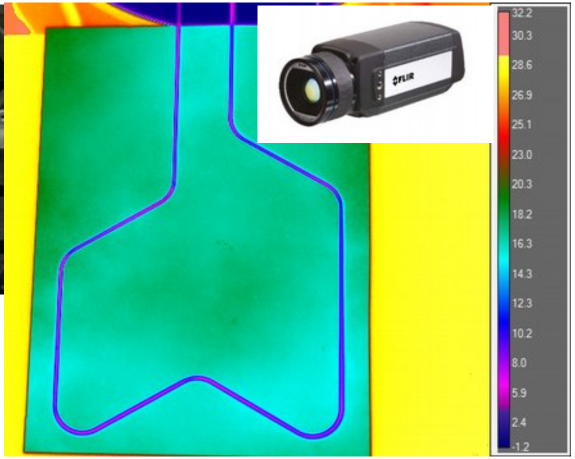
R&D using CMS studies (Thanks to Th. Pierre-Emile from CMS-LLR group)

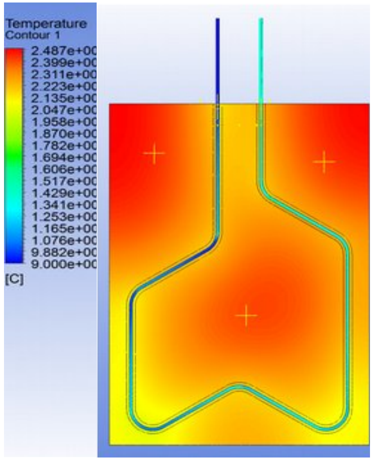


Copper plate prototype dimensions information



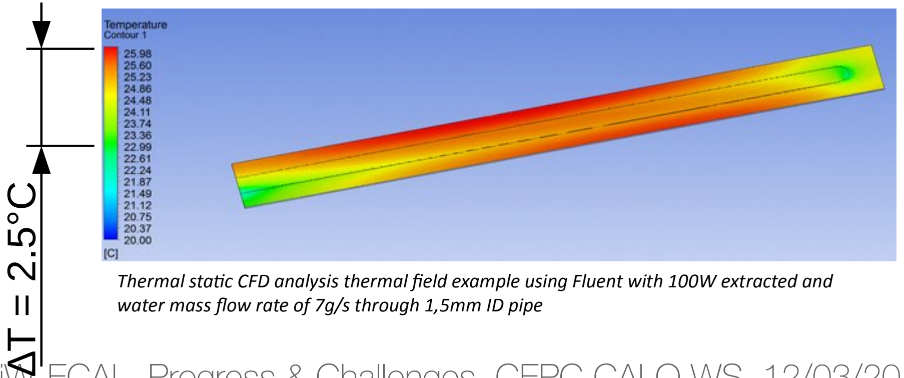
Pipe insertion on a cooling prototype for FEA correlation



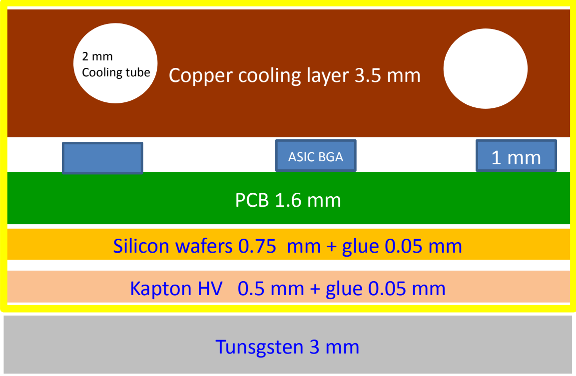


Pipe insertion on a cooling prototype

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling



Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe



2 mm Cooling tube

Copper cooling layer 3.5 mm

ASIC BGA

1 mm

PCB 1.6 mm

Silicon wafers 0.75 mm + glue 0.05 mm

Kapton HV 0.5 mm + glue 0.05 mm

Tunsgsten 3 mm

⇒ 9 mm / layer

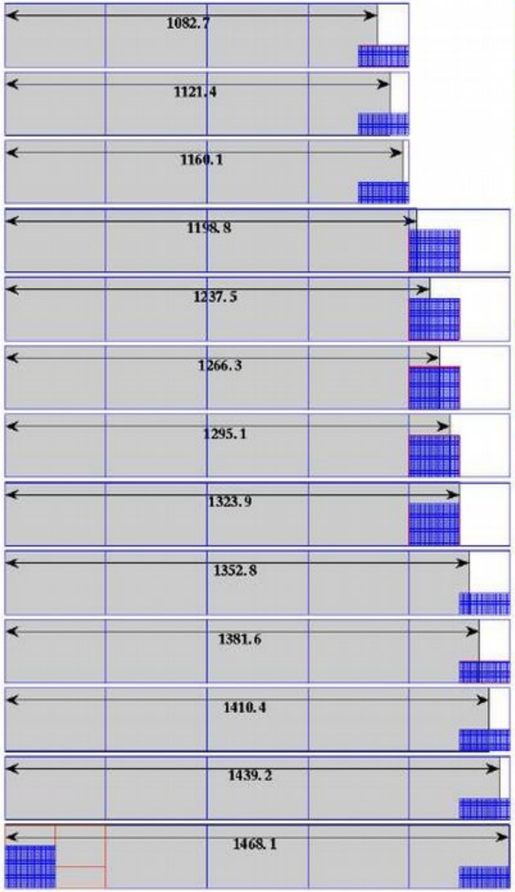
Redefinition of dimensions

- **Full costing (hardware and man-power) and integration planning done by Henri Videau**
- **3 designs looked at**

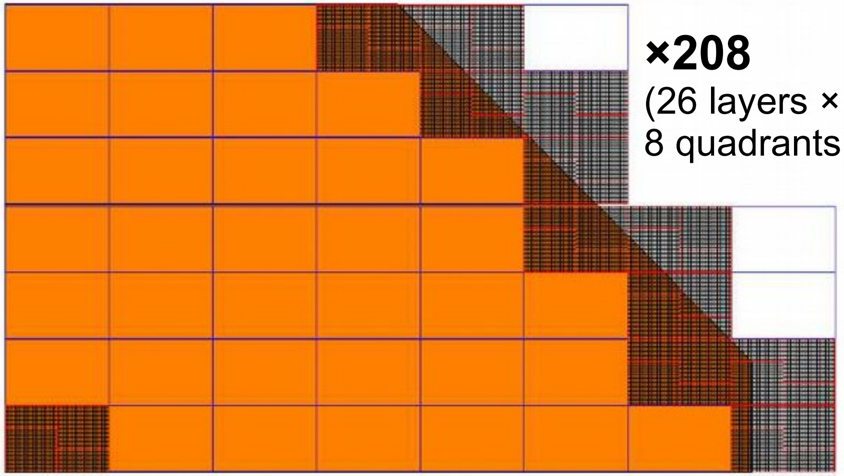
    under work version of **ECal Technical Design Document** (TDD, ~100 pages)
    by Henri Videau (LLR), Marc Anduze (LLR) and Denis Grondin (LPSC)

  - a “baseline” (or “large”) with inner ECal radius at RECal =1804mm, (model close to the DBD) with 30 layers
  - a “small ILD” model RECal ~1500 mm (all related quantities adapted ↔ $R_{outer}^{Endcaps}$)
  - a model with slightly reduced number of layers = 26 layers
- **725µm thickness with 200mm (8”) wafers ; 5.08 → 6mm cell size**
  - ~ identical photon resolution expected
  - 13% gain cost on Silicon surface, PCB, and 40% on electronics (and power consumption) wrt DBD
  - Improved S/N ratio & timing, less channeling @ 90°

Tiling



×400
(2 sides × 5 columns ×40 modules)



×208
(26 layers ×
8 quadrants)

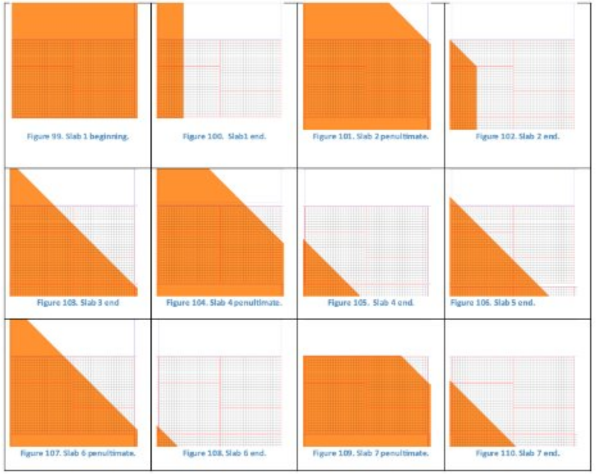
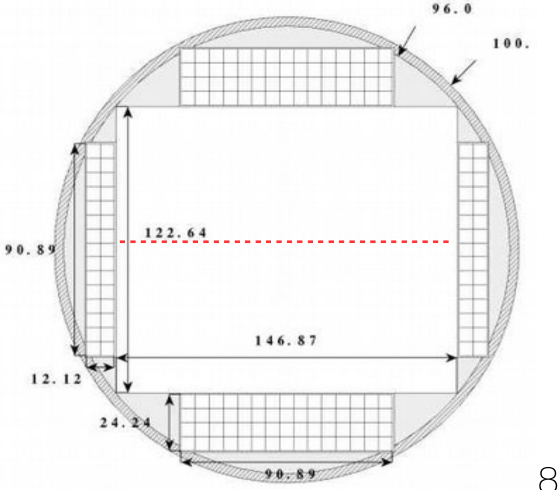


Figure 99. Slab 1 beginning.
Figure 100. Slab1 end.
Figure 101. Slab 2 penultimate.
Figure 102. Slab 2 end.
Figure 103. Slab 3 end
Figure 104. Slab 4 penultimate.
Figure 105. Slab 4 end.
Figure 106. Slab 5 end.
Figure 107. Slab 6 penultimate.
Figure 108. Slab 6 end.
Figure 109. Slab 7 penultimate.
Figure 110. Slab 7 end.

Matching of large and small rectangles, triangles and diamonds to be detailed for optimal use



add'l small rectangles:
87 % use of surface
(83 % for an hexagonal shape)

Conclusions & perspectives

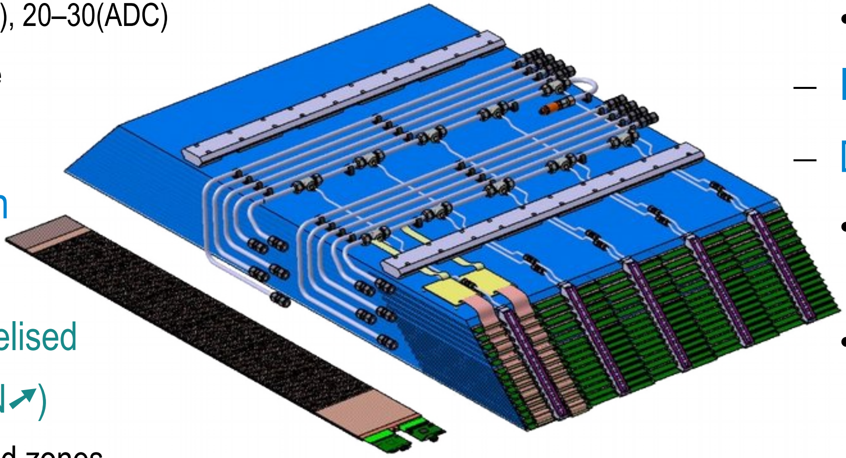
Technical Milestones:

At hand on CALICE prototype:

- Workable, scalable design
- ASU with 1024 channel
  - Signal/Noise > 10 (trigger), 20–30(ADC)
  - on-going: HE e- response
- Reduced GR event rates

On-going on ILD-like design

- Connection over 8 ASU's
- Mechanics & Cooling modelised
- Thicker & larger wafer (S/N↗)
  - red. number of layers, dead zones
- Compact DAQ



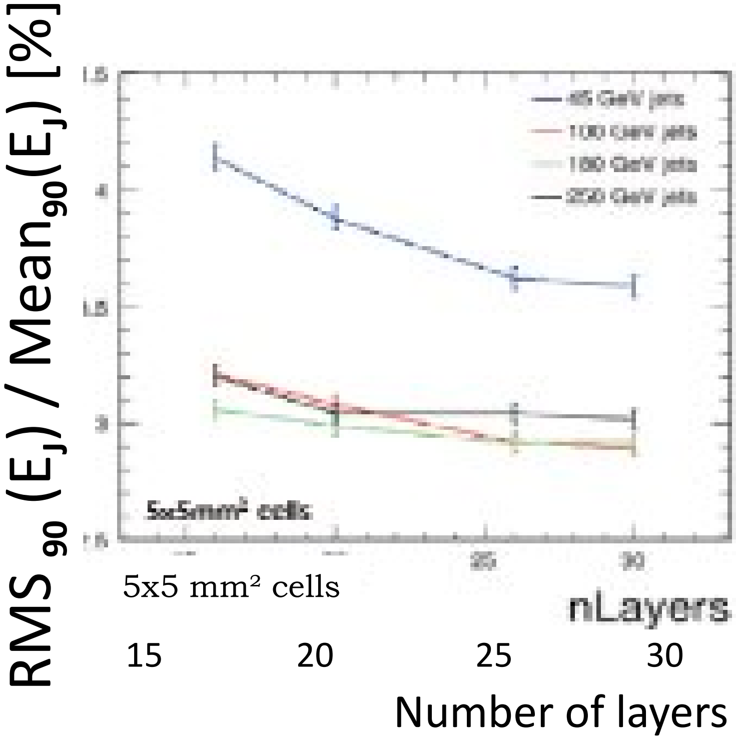
Next steps

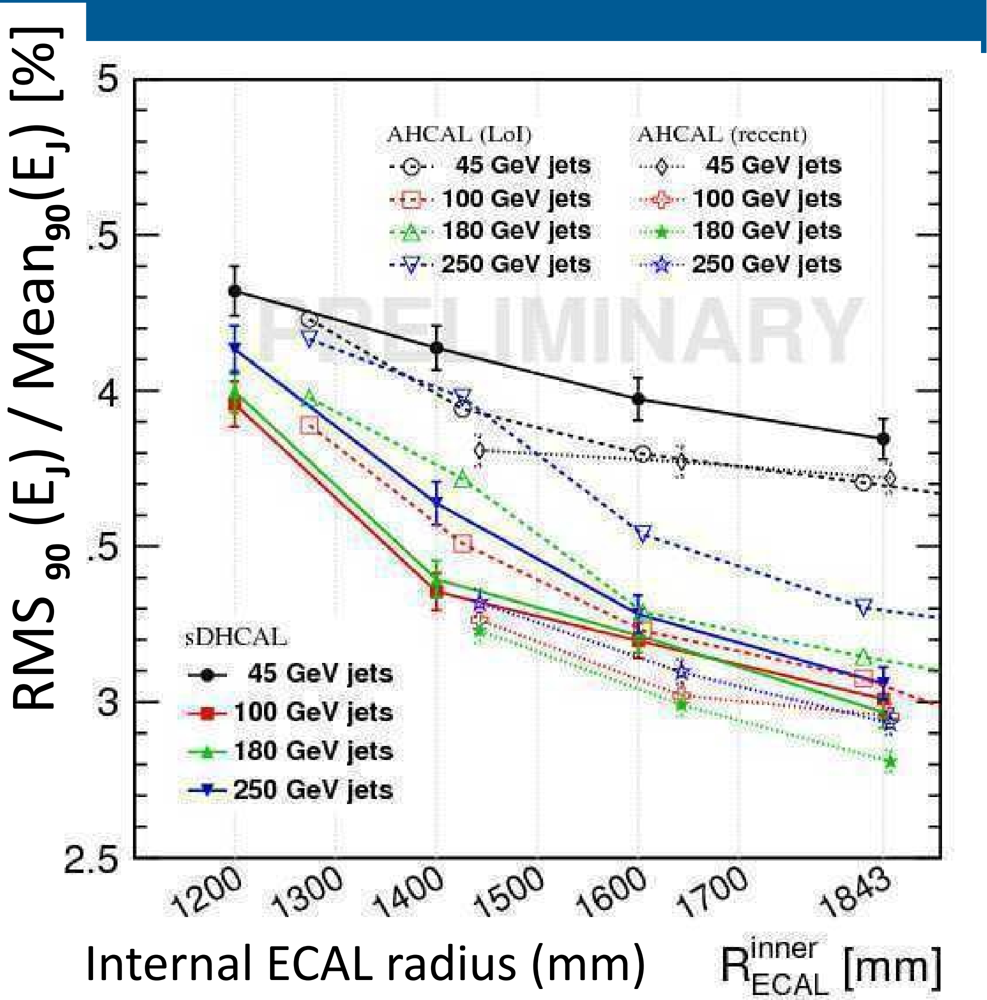
- Final chips (SK3-like): full 0-suppr …
  - machine dependant (duty cycle, timing)
  - continuous running for circular colliders
  - Embedded cooling
- Industrial aspects (components, aging, …)
- Double Layered Long Slab Prototype
  - Design with Larger & Thicker wafers
    - Cost ~ stable
  - Demonstrator for industry
    - Estimated cost ~160k€ / piece

BACK-UP

Parameter optimisations

A new feeling , **AFTER** the staging proposal





Reduced number of Layers

Going from 30 to 22 layers

- Reduction of cost; (small) reduction of R_M ; increase of Energy resolution
  - “better separation at the expanse of the intrinsic resolution”

Increasing the Si thickness to 725µm, if really feasible (next slide)

Energy resolution σ(E)/E:

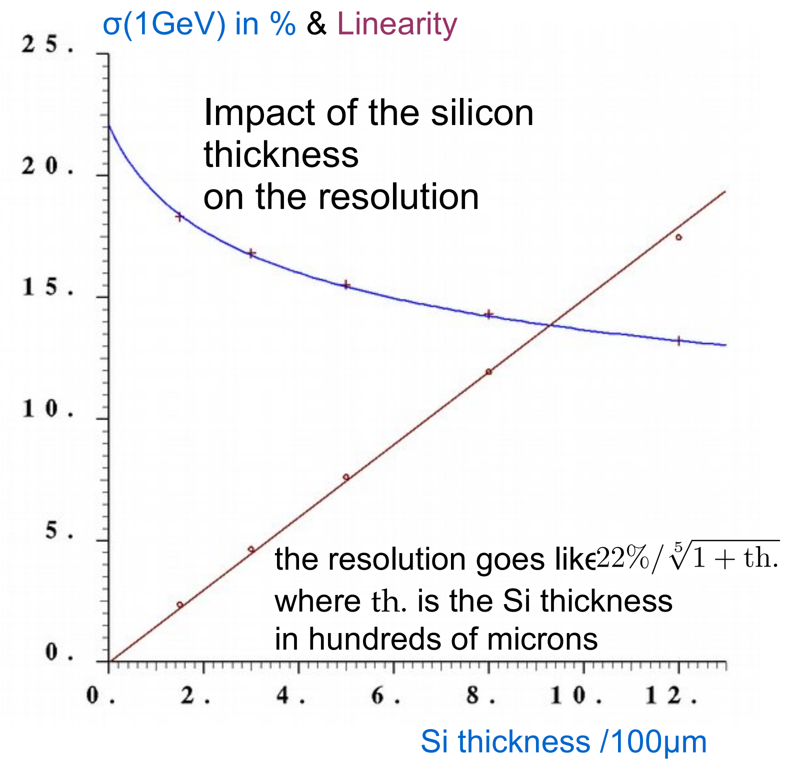
- for 22 layers w.r.t. 30: +16.8%
- with 725µm w.r.t 500µm : –6.1%

ECal thickness = 190.1 mm (close to 185 mm of DBD).

- 22 layers = 14 layers with 2.8mm thickness
  + 8 layers with 5.6mm shared between structure and slabs.

Study needed on separation, resolution and efficiency performances at low energy.

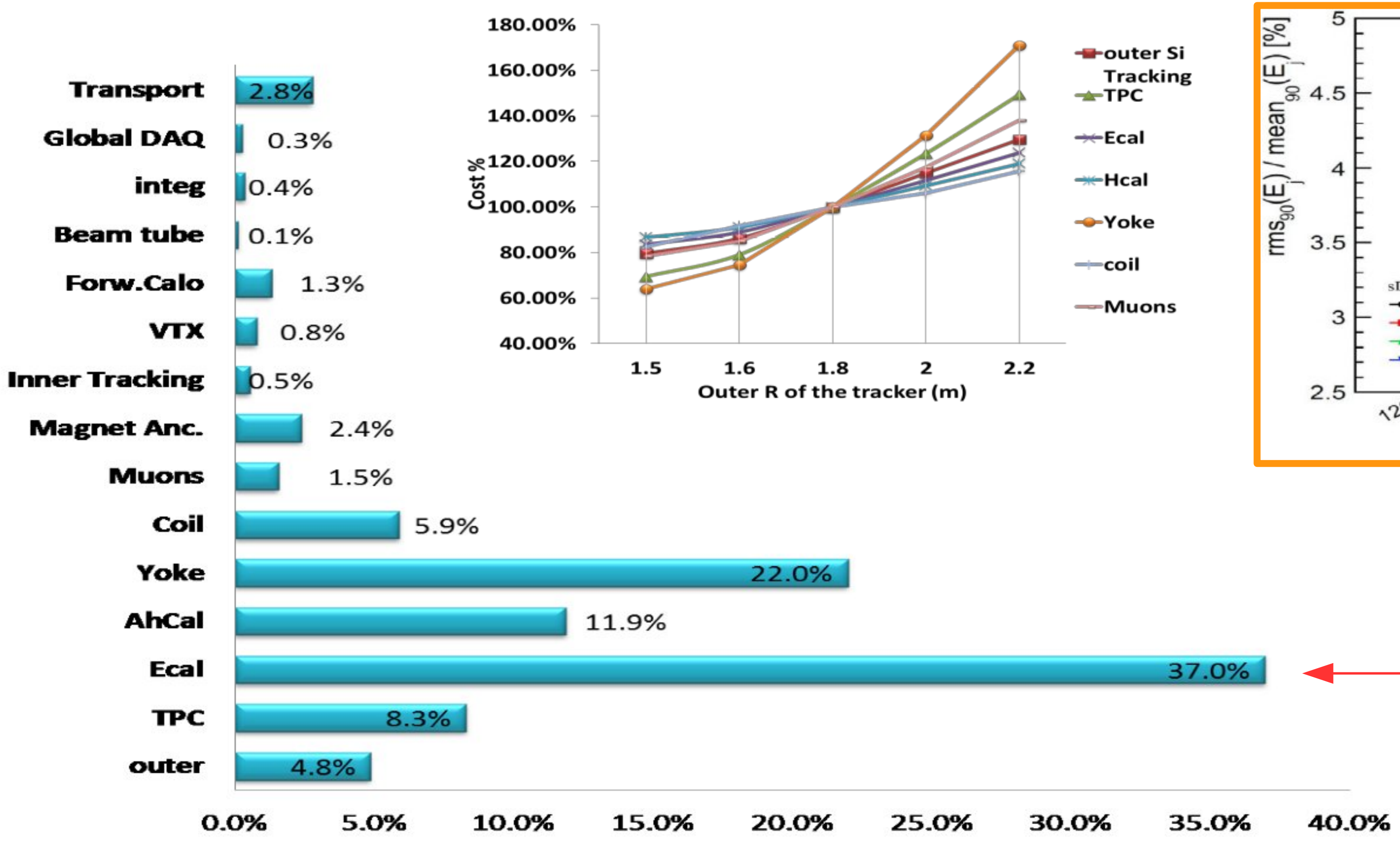
- JER : $\sigma(E_J)/E_J$ +10% for 20 layers (500 µm).

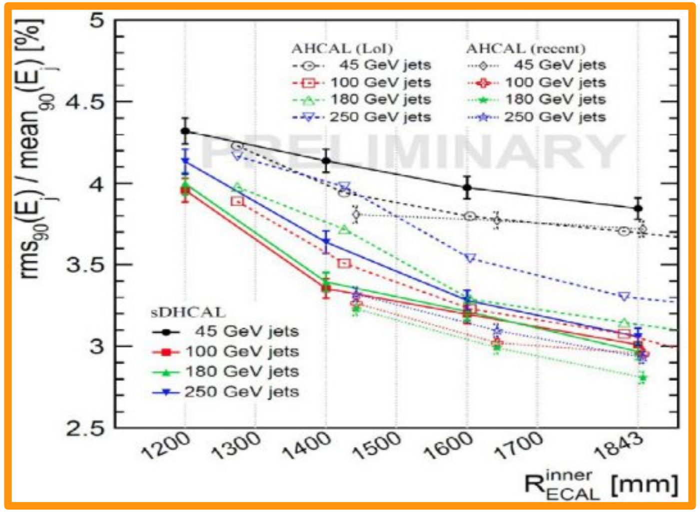


Impact of the silicon thickness on the resolution

the resolution goes like $22\%/\sqrt[5]{1+\mathrm{th.}}$ where $\mathrm{th.}$ is the Si thickness in hundreds of microns

Cost Structure of ILD

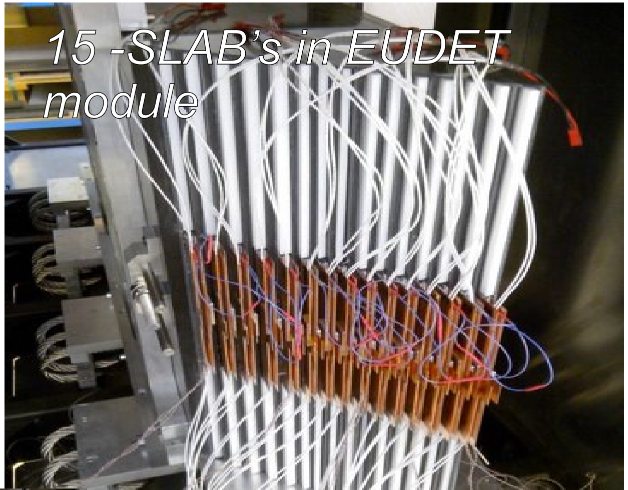




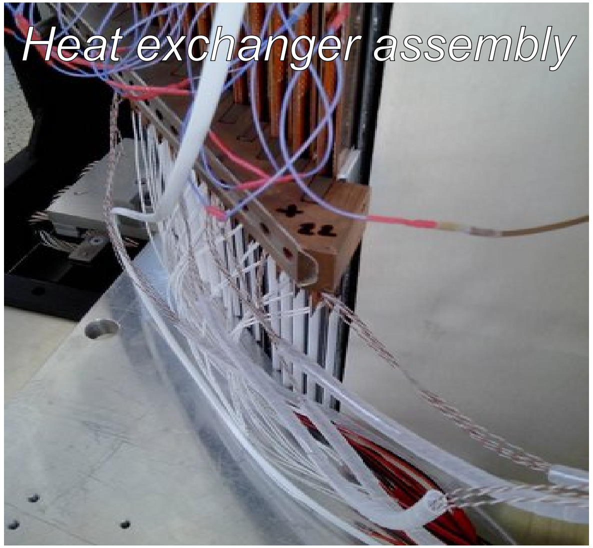
Full Silicon option

Integration in ILD: thermal studies

by Denis GRONDIN / Julien GIRAUD (LPSC)

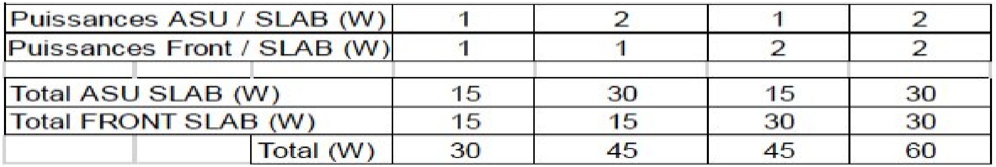


15 -SLAB's in EUDET module



Heat exchanger assembly

Insulation



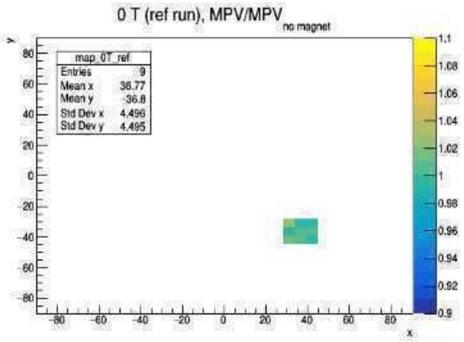
Puissances ASU / SLAB (W)	1	2	1	2
Puissances Front / SLAB (W)	1	1	2	2
Total ASU SLAB (W)	15	30	15	30
Total FRONT SLAB (W)	15	15	30	30
Total (W)	30	45	45	60

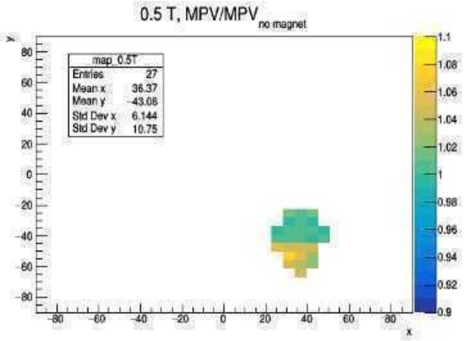
Important thermal inertia => 4 days minimum of stabilization

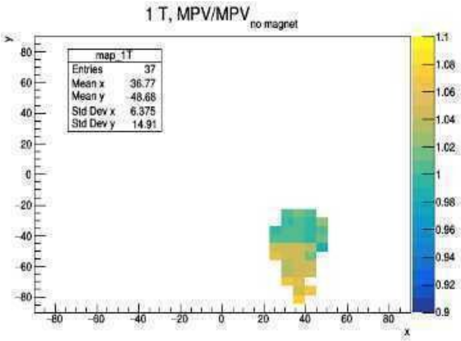
Test in B field

Magnetic field tests

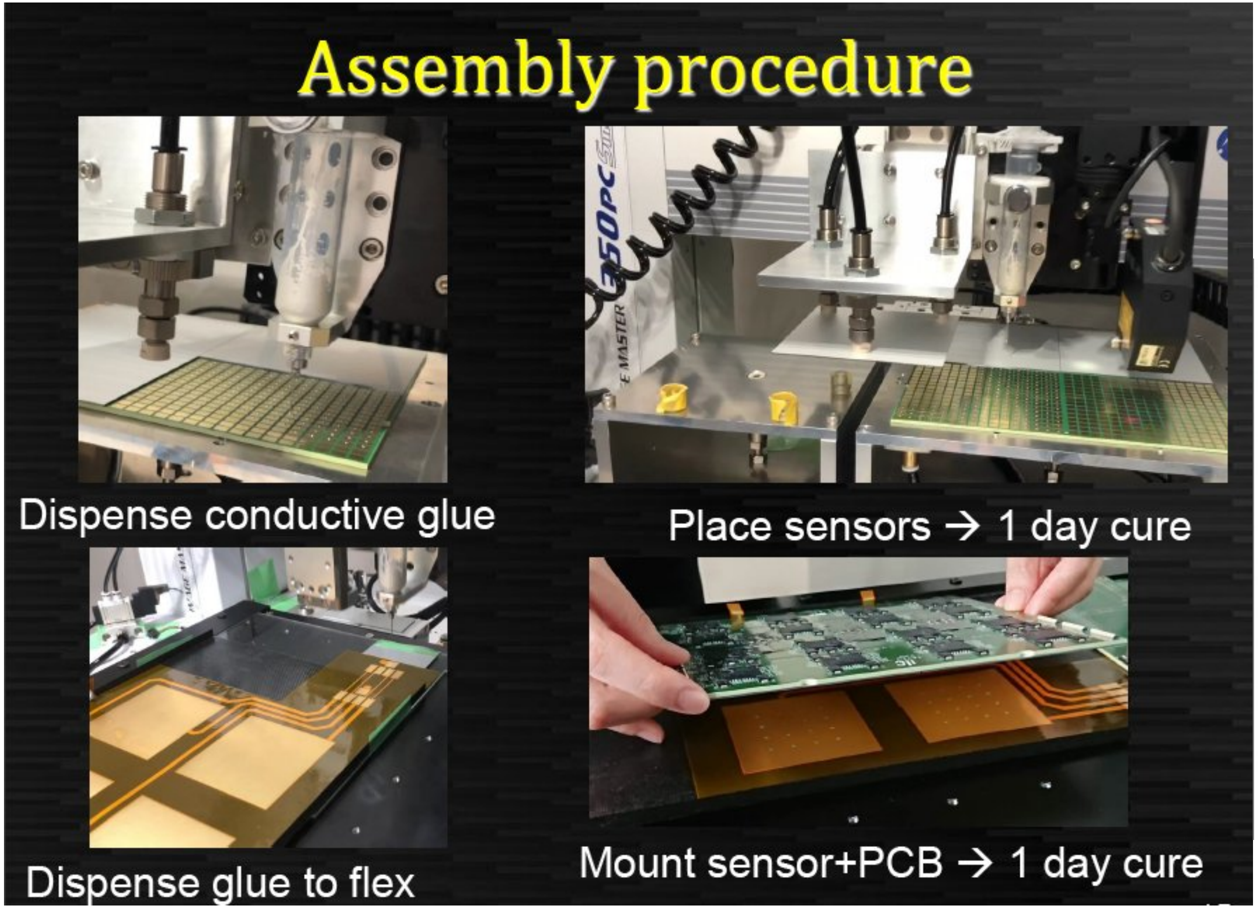
- Single Slab (21, first layer in the full stack)
- (Magnetic field from 0, 0.5, 1 T) ⊗ (With and without beam)
  - Same configuration than in the other beam area.
- Not evident failure/loss of performance during visual inspection on the web cam & online monitor.
- ~20 hours of data in total







FEV13 assembly in Japan



Assembly procedure

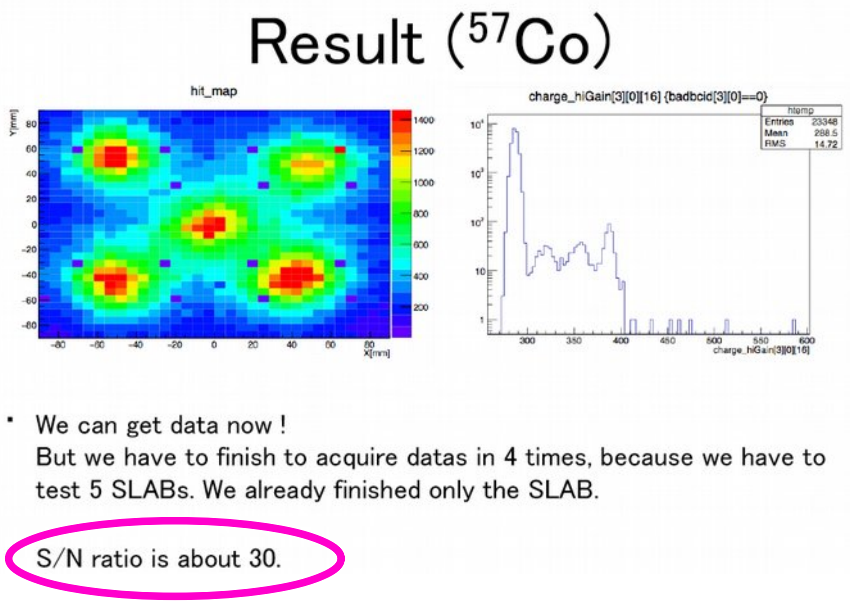
Dispense conductive glue

Place sensors → 1 day cure

Dispense glue to flex

Mount sensor+PCB → 1 day cure

Similar to production in Paris region



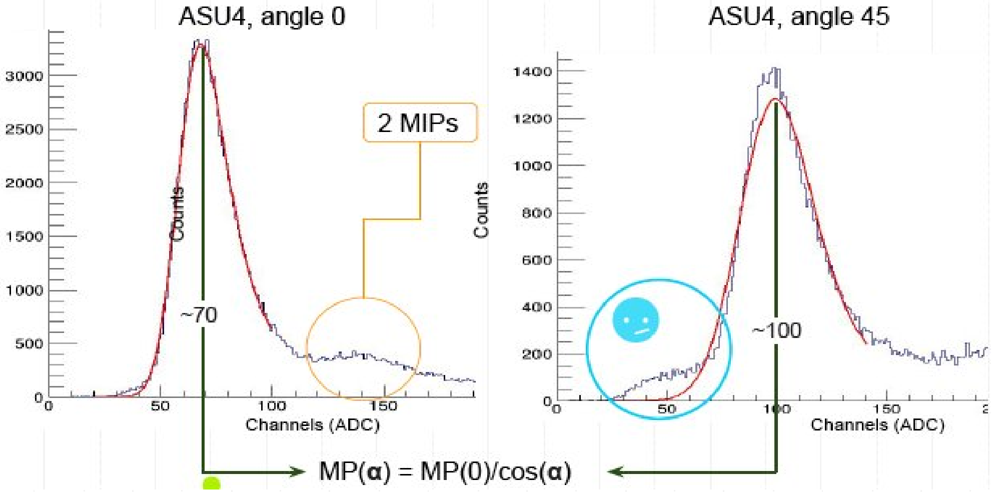
Result (^{57}Co)

- We can get data now !
  But we have to finish to acquire datas in 4 times, because we have to test 5 SLABs. We already finished only the SLAB.

S/N ratio is about 30.

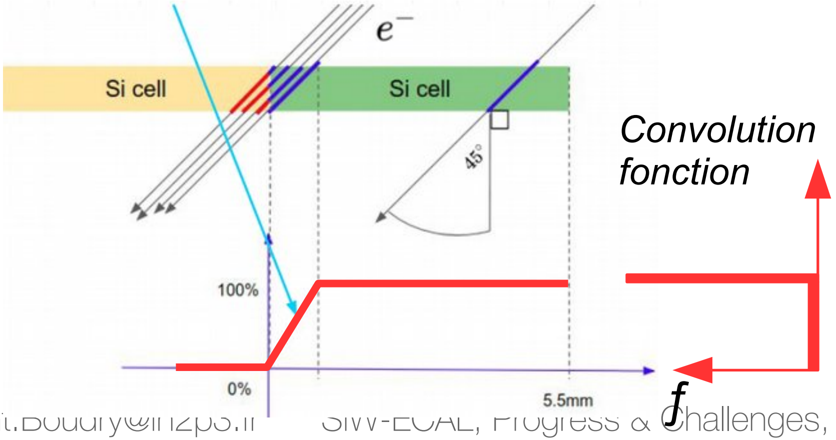
Mip analysis

O. Korostyshevskiy

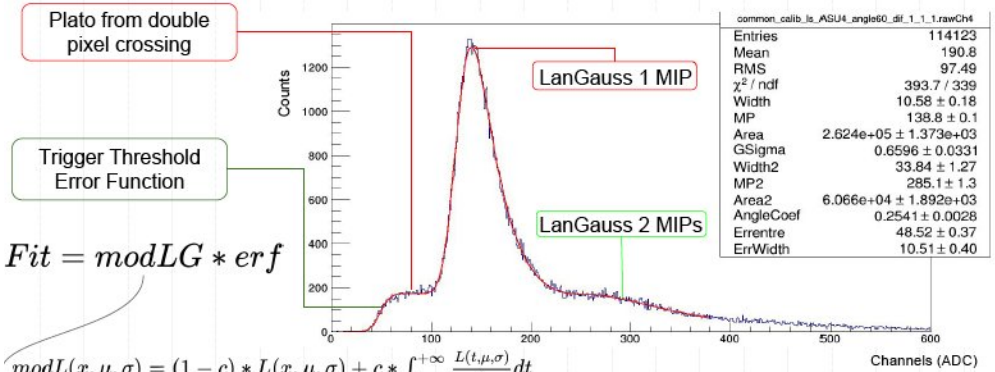


MP(**α**) = MP(0)/cos(**α**)

Pixel energy fraction depends linearly on crossing position



Fit with Mod LanGau function ✓

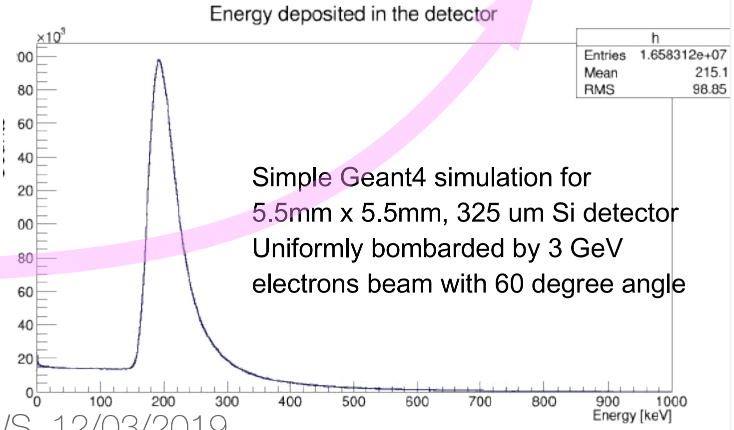


common_calib_ls_ASU4_angle60_dif_1_1_1.rawCh4	
Entries	114123
Mean	190.8
RMS	97.49
χ^2 / ndf	393.7 / 339
Width	10.58 ± 0.18
MP	138.8 ± 0.1
Area	2.624e+05 ± 1.373e+03
GSigma	0.6596 ± 0.0331
Width2	33.84 ± 1.27
MP2	285.1 ± 1.3
Area2	6.066e+04 ± 1.892e+03
AngleCoef	0.2541 ± 0.0028
Errentre	48.52 ± 0.37
ErrWidth	10.51 ± 0.40

$$Fit = modLG * erf$$

$$modL(x,\mu,\sigma) = (1-c) * L(x,\mu,\sigma) + c * \int_x^{+\infty} \frac{L(t,\mu,\sigma)}{t} dt$$

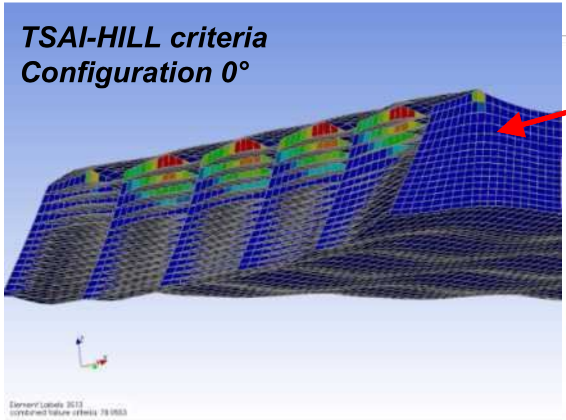
$$modLG = \int_{-\infty}^{+\infty} modL(t,\mu.\sigma) * G(x-t,\mu_G,\sigma_G) dt$$



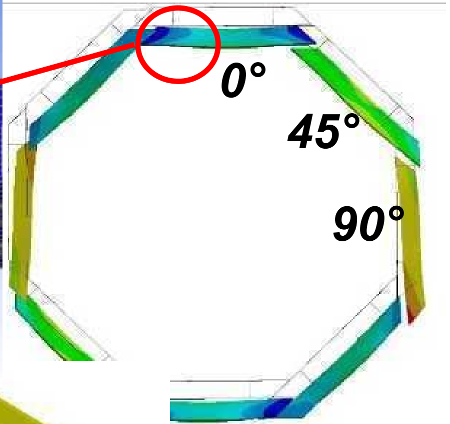
Simple Geant4 simulation for
5.5mm x 5.5mm, 325 um Si detector
Uniformly bombarded by 3 GeV
electrons beam with 60 degree angle

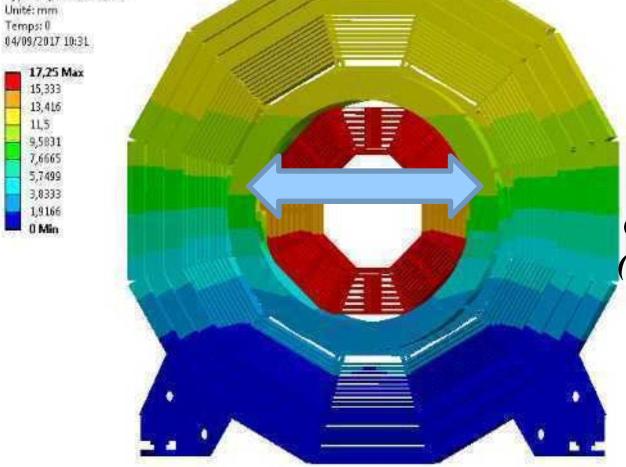
Mechanical simulations

- All dimensions of the ILD prototype are defined according to FEA results in static and dynamic (earthquake) conditions and for all positions of final modules in the barrel (8 cases)
- Study of deformations and limit stresses analysis using composite criteria (TSAI-HILL)
  Max stresses are located on the top ribs, a strong effort is needed to define correctly its thickness
- <u>Proposal:</u> Study internal stresses by using new sensors : optical fiber Bragg grating sensors embedded directly within ribs (strain gauge behaviour)

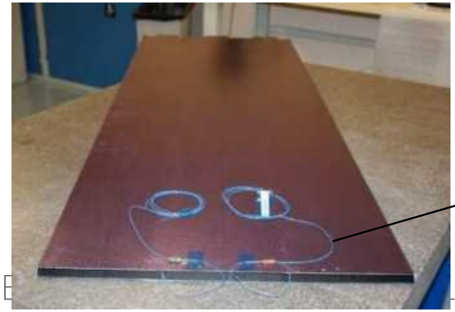


Global deformation of ECAL module (static case)





Global déformation (Response spectrum in lateral only)



Optical fiber equipped with BG sensors

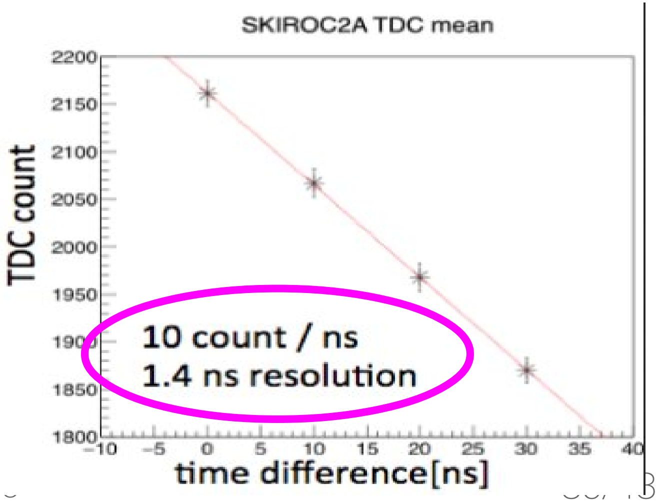
Test of SK2A → Timing ?

Adding 5th dimension:

- Can:
  - Improve Particle Flow SW ***with ~ns mip precision***
    - Tracking of particles
    - Removal of late neutrons
    - Identification of back scattered
  - Allow Particle identification by ToF ***with sub-ns precision***
- *Clean Clock distribution*
  - *Shower timing ~ 1/√E*
- *@ LHC See presentation on HGCAL*

Checked SK2A on Test Board

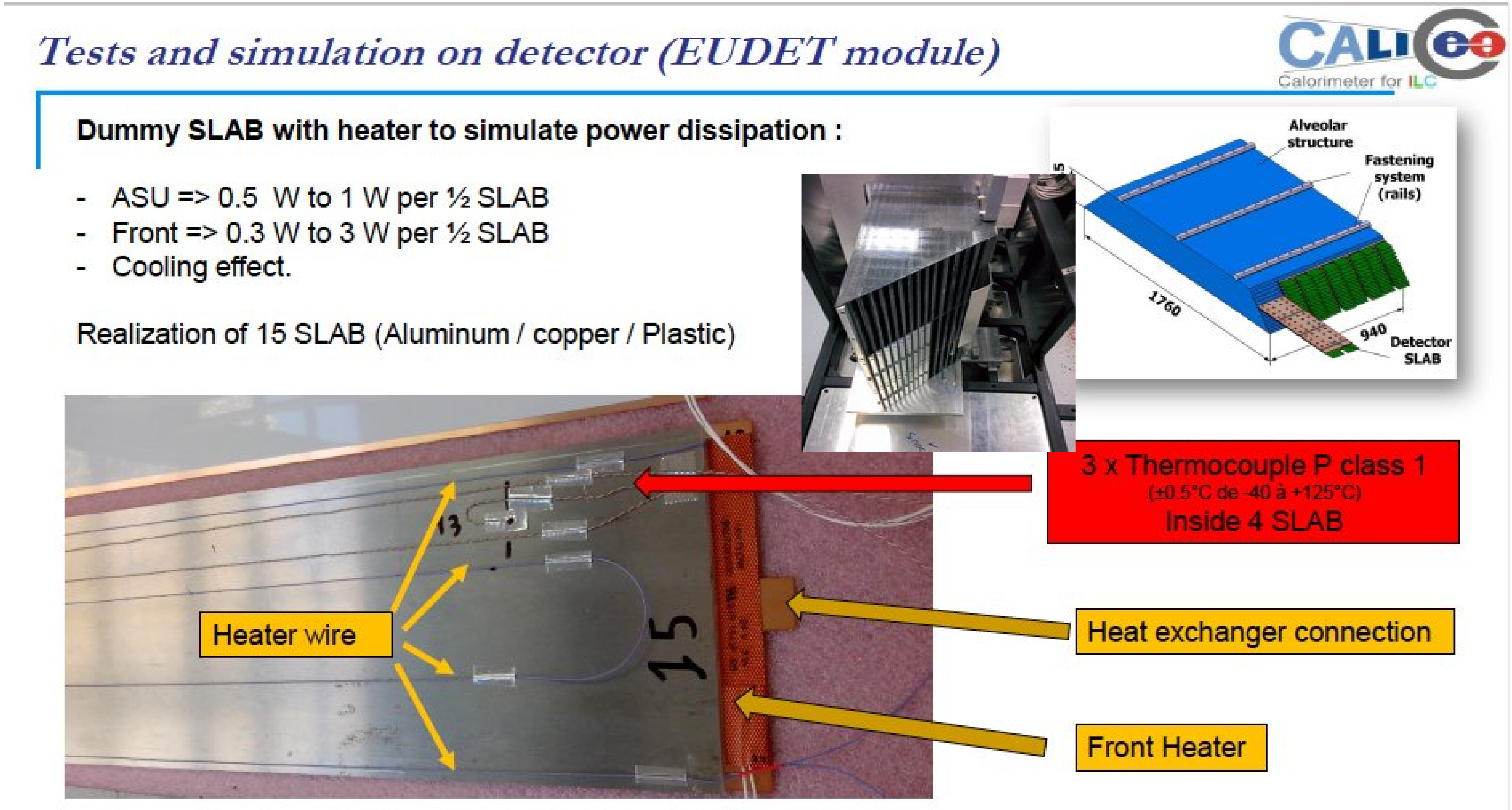
- Thorough checks on 1–2 mip injected signal
  - All seems OK
  - No difference in Analog part
- Trigger:
  - large channel-by-channel adjustment ✔
  - TDC: OK


SKIROC2A TDC mean

10 count / ns
1.4 ns resolution

Integration in ILD: thermal studies

by Denis GRONDIN / Julien GIRAUD (LPSC)



Tests and simulation on detector (EUDET module)

Dummy SLAB with heater to simulate power dissipation :

- ASU => 0.5 W to 1 W per ½ SLAB
- Front => 0.3 W to 3 W per ½ SLAB
- Cooling effect.

Realization of 15 SLAB (Aluminum / copper / Plastic)

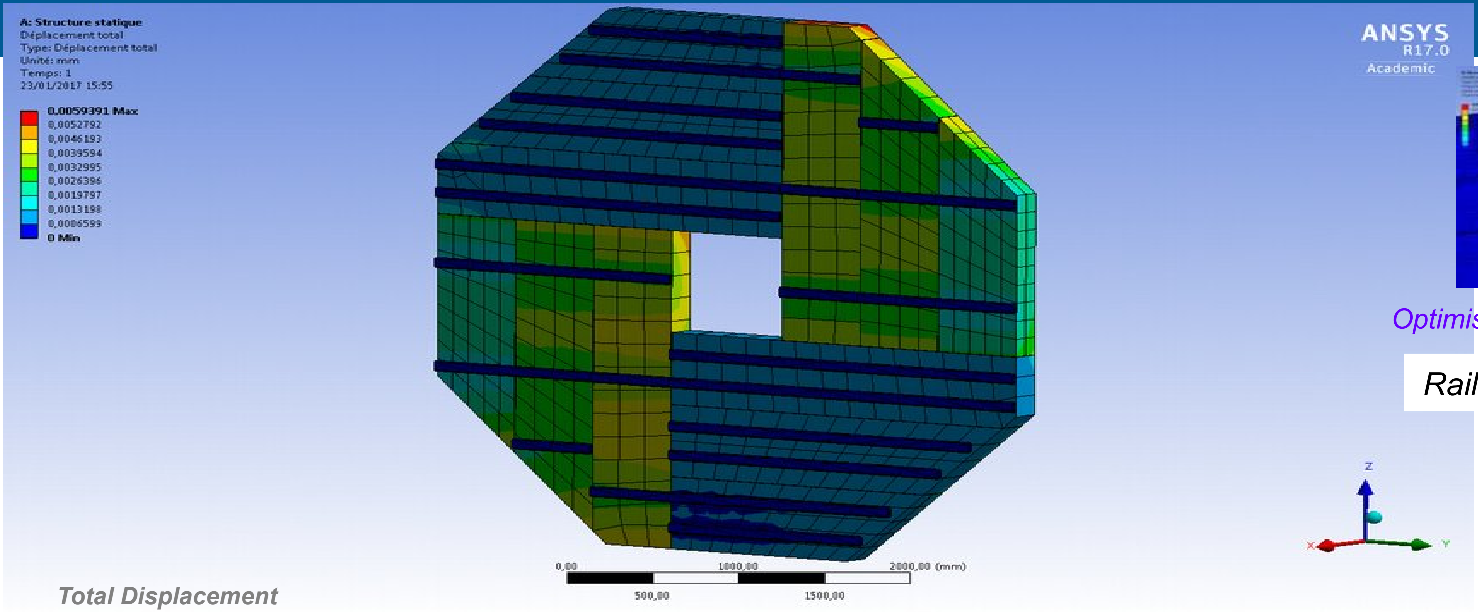
3 x Thermocouple P class 1
(±0.5°C de -40 à +125°C)
Inside 4 SLAB

Heater wire

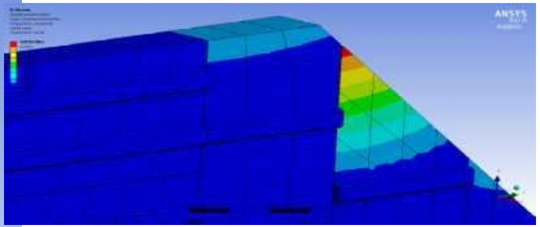
Heat exchanger connection

Front Heater

Structure composite & séisme



Total Displacement

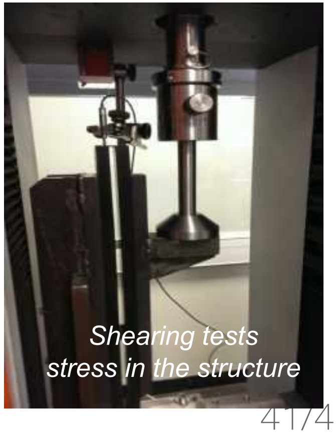


Optimisation on going / rails localisation/ on going

Rails fixed

Mode	Fréquence [Hz]
1,	203,56
2,	204,24
3,	206,17
4,	208,13
5,	211,64
6,	212,02

Impact on ECAL dead z



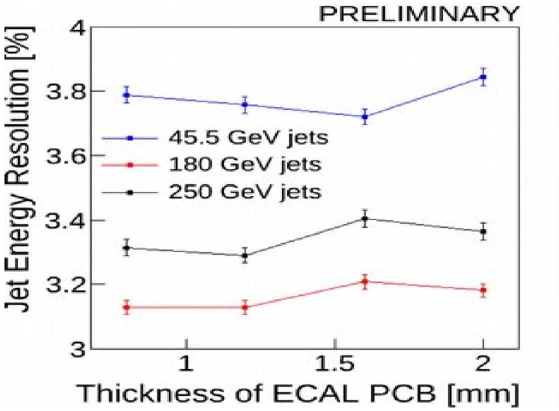
Shearing tests
stress in the structure

Problem of bending stress of alveoli skins: influence / evolution of thickness of outer plies

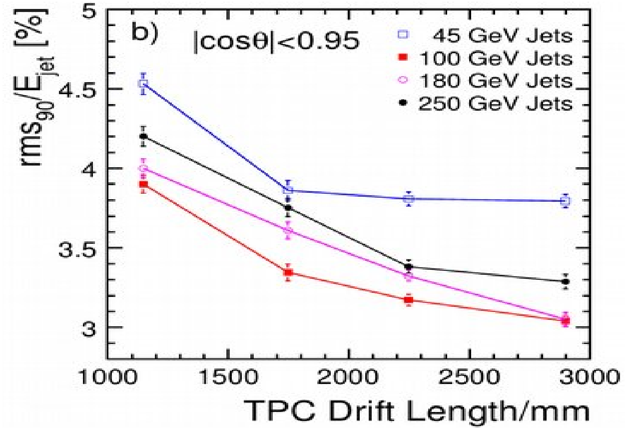
Safety coefficient

- Static: Sufficient / to the stress induced by weight of modules
- just sufficient / seism (s =3.2 for Japan?)
  / risks during integration and transport

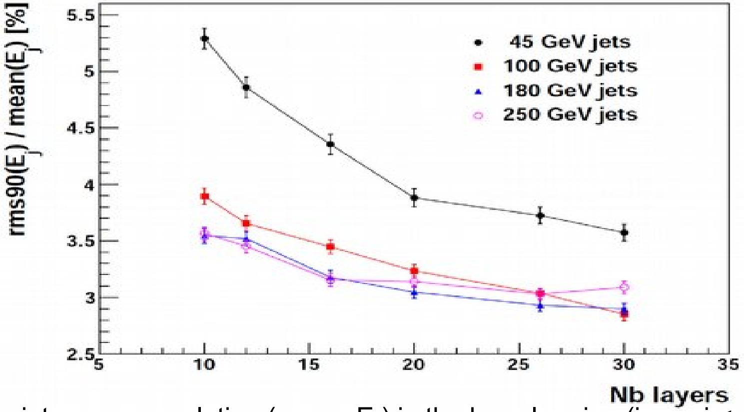
-> increase nb of ext. plies... Impact on ECAL dead zone=0,5mm= 1 extra external ply on modules



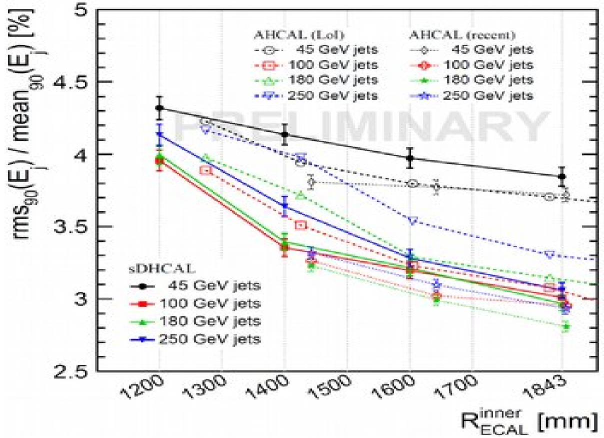
Single jet energy resolution as a function of the thickness of PCB with embedded electronics.



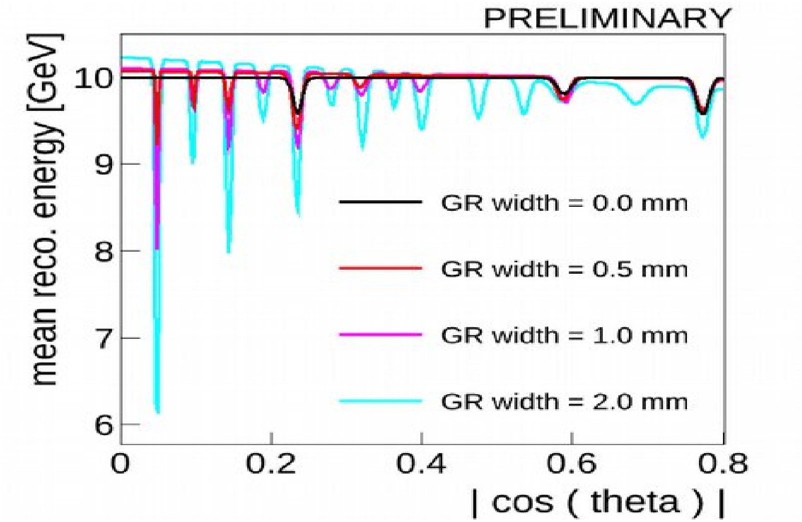
Single photon energy resolution as a function of the number of silicon layers for four photon energies.

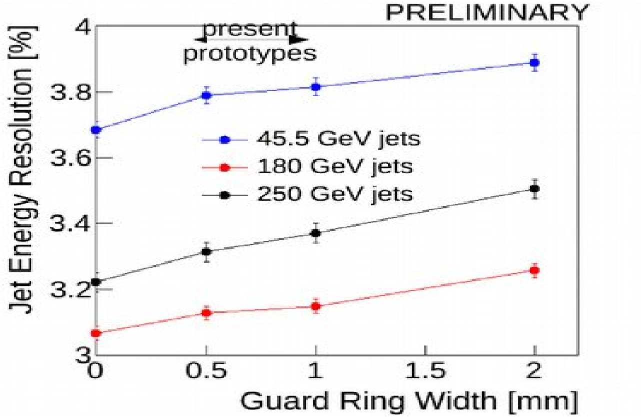


Single jet energy resolution (rms$_{90}$=E) in the barrel region (j cos j < 0: 7) as a function of the number of ECAL silicon layers in events e^+e^- →ZX → usd



ILD jet energy resolution in the barrel region j cos j < 0: 7 as a function of its radius.

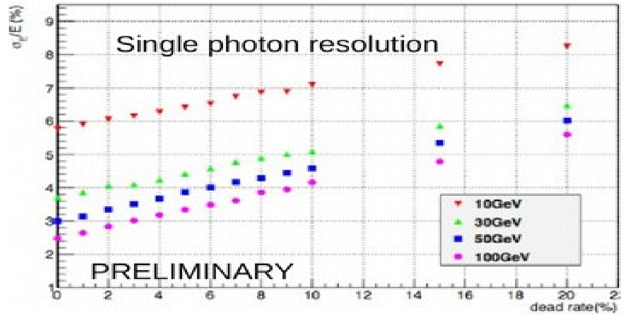


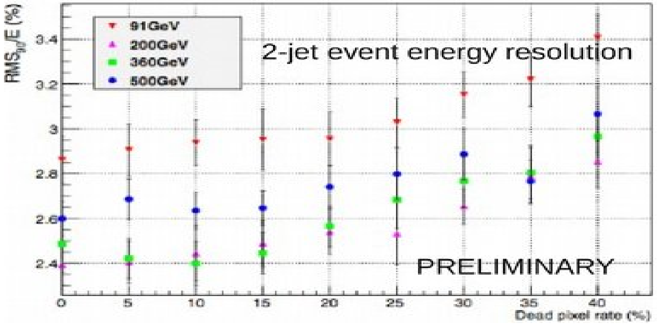


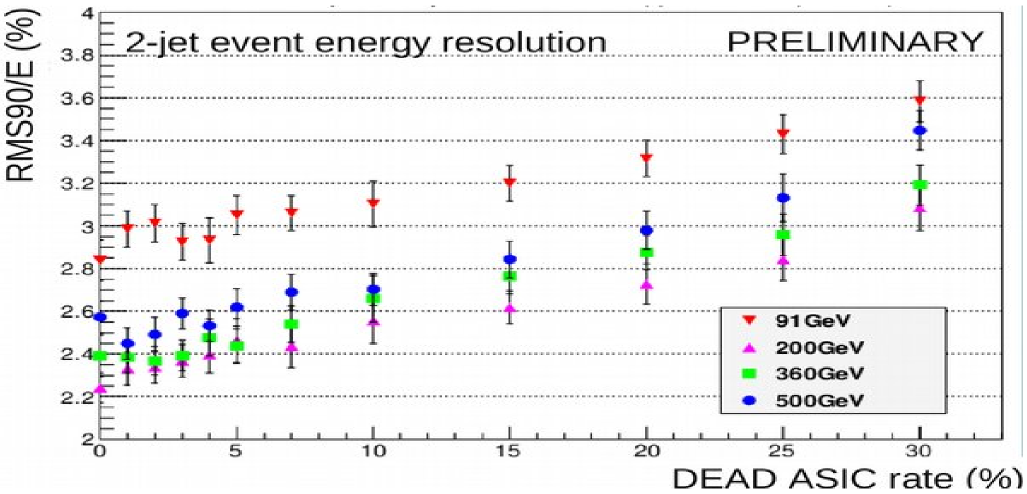
the single jet energy resolution after a simple dependent correction as a function of the guard ring thickness.

An ECAL average signal versus azimuthal angle. The loss in inter-sensor dead areas is visible (between barrel modules, barrel and endcap
and between the sensors, the latter depends on the guard ring).

Resilience


Single photon resolution
σE/E (%)
dead rate(%)
PRELIMINARY
10GeV
30GeV
50GeV
100GeV
1
2
3
4
5
6
7
8
9
0
2
4
6
8
10
12
14
16
18
20


2-jet event energy resolution
RMS90/E (%)
Dead pixel rate (%)
PRELIMINARY
91GeV
200GeV
360GeV
500GeV
2.4
2.6
2.8
3
3.2
3.4
0
5
10
15
20
25
30
35
40


2-jet event energy resolution
PRELIMINARY
RMS90/E (%)
DEAD ASIC rate (%)
91GeV
200GeV
360GeV
500GeV
2
2.2
2.4
2.6
2.8
3
3.2
3.4
3.6
3.8
4
0
5
10
15
20
25
30