Status of Semi-Digital HCAL

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(on behalf of the CALICE SDHCAL Group)

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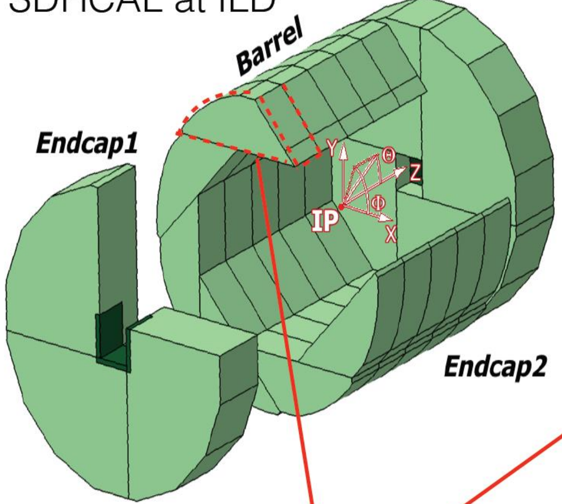
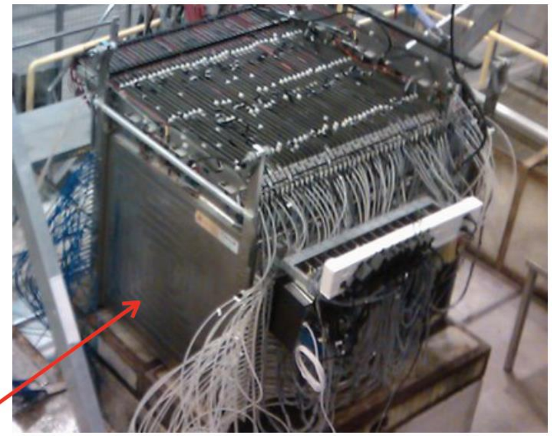
Outline

- SDHCAL Technological Prototype
  - Description, Test Beam, Hadronic Shower Studies
- R&D for Large SDHCAL Modules
  - Electronics, Mechanical, Gas Distribution
- New PCB Readout Scheme
  - less readout channels, less power consumption
- MRPC with good time resolution
  - about 30ps time resolution, help to identify neutrons
- Summary and Conclusion

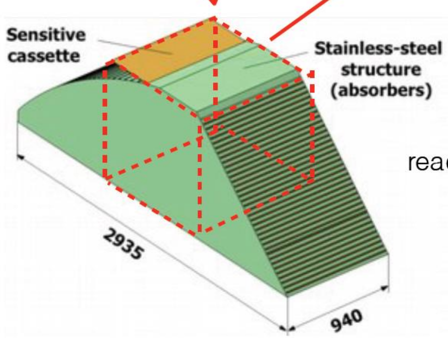
SDHCAL Prototype

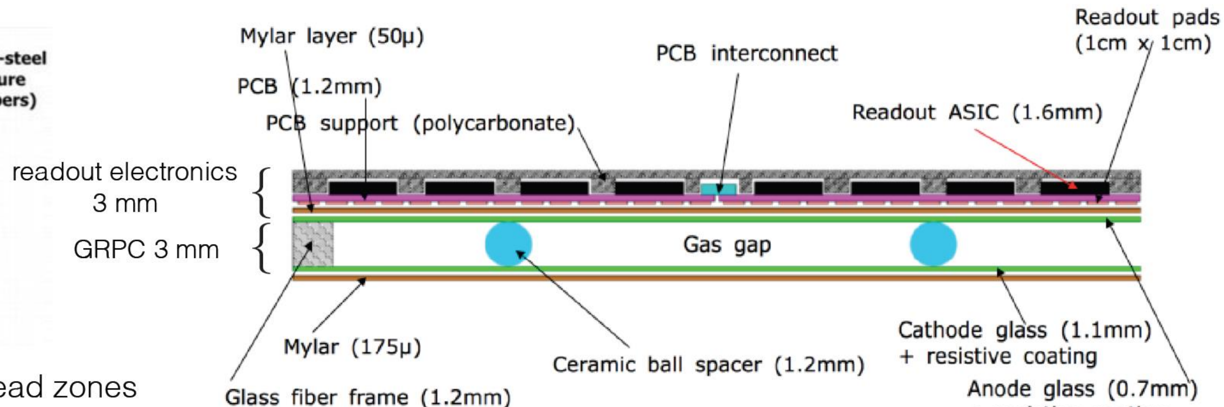
SDHCAL at ILD





- 48 layers, 6 λ_I
- GRPC (1×1 m²)
- Cell pads:1×1 cm²
- On each layer, ASIC: 12 x 12; 64 ch. on each ASIC; 9612 ch. in total
- Three thresholds readout (2 bits): (0.11, 5, 15) pC
- Power-pulsing electronics
- Self-supporting mechanical structure as absorber as well



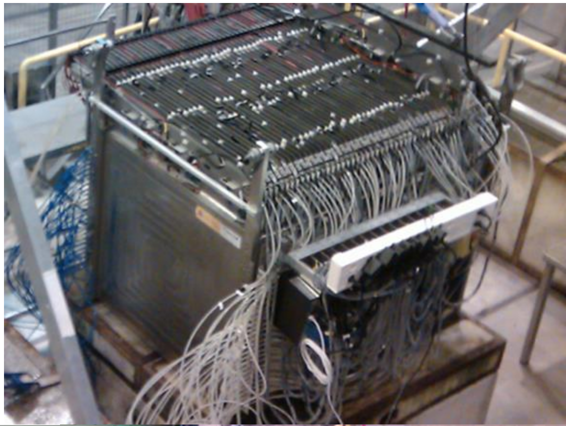


- Very compact with negligible dead zones
- Eliminates projective cracks
- Minimizes separation of barrel and endcap

arXiv:1602.02276

SDHCAL Prototype Construction

- ✓ 10500 64-ch ASICs were tested and calibrated using a dedicated ASICs layout.
- ✓ 310 PCBs were produced, cabled and tested, assembled by sets of six to make $1m^2$ ASUs
- ✓ 170 DIF, 20 DCC were built and tested.
- ✓ 50 detectors were built and assembled with electronics into cassettes.
- ✓ DAQ system using both USB and HTML protocol was developed and used.
- ✓ Self-supporting mechanical structure.
- ✓ **Full assembly and 5 test beam at CERN since 2012**.



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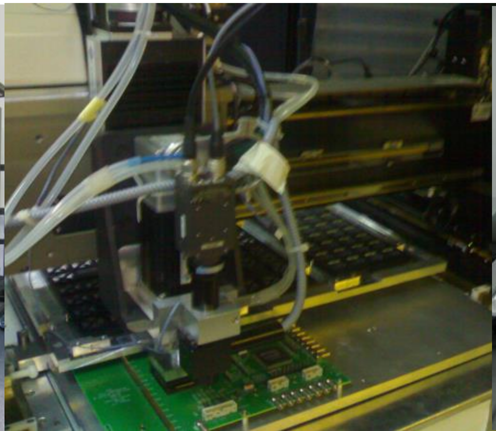
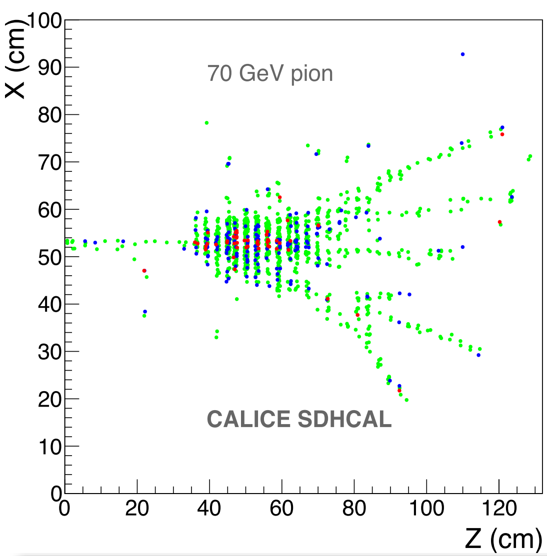
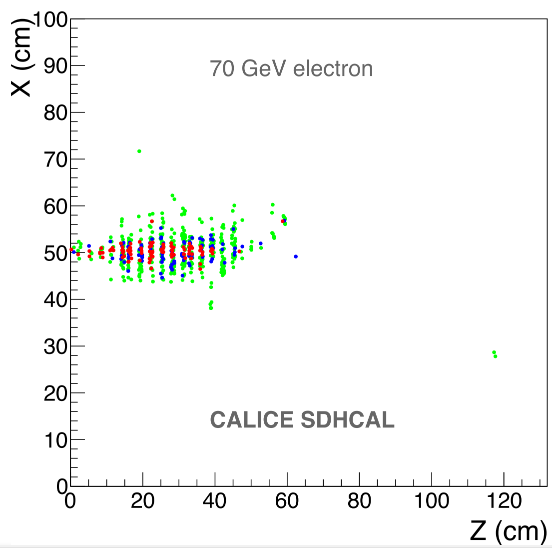
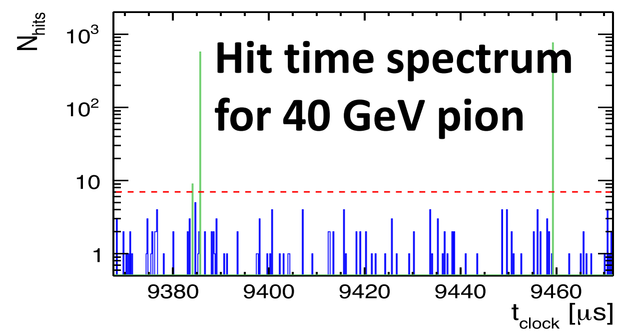


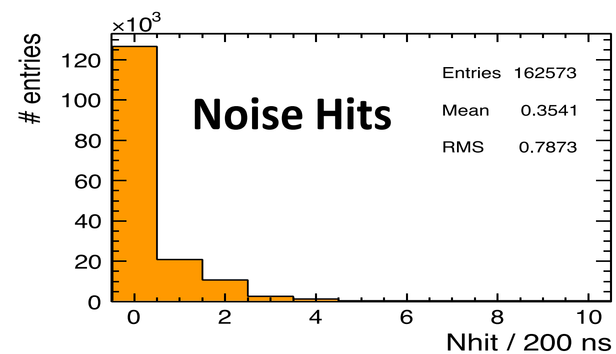
SDHCAL Performance

- The SDHCAL prototype was exposed to hadron, muon and electron beams in 2012, 2015 and 2016, 2017 on PS, H2, H6 and H8-SPS lines.
- Power-pulsing using the SPS spill structure was used to reduce the power consumption.
- Self-triggering mode is used but external trigger mode is possible
- The threshold information helps to improve on the energy reconstruction by better accounting for the number of tracks crossing one pad
- 2018 TB with SiW ECAL prototype









Energy Reconstruction (χ^2)

◆ **Energy reconstruction formula:**

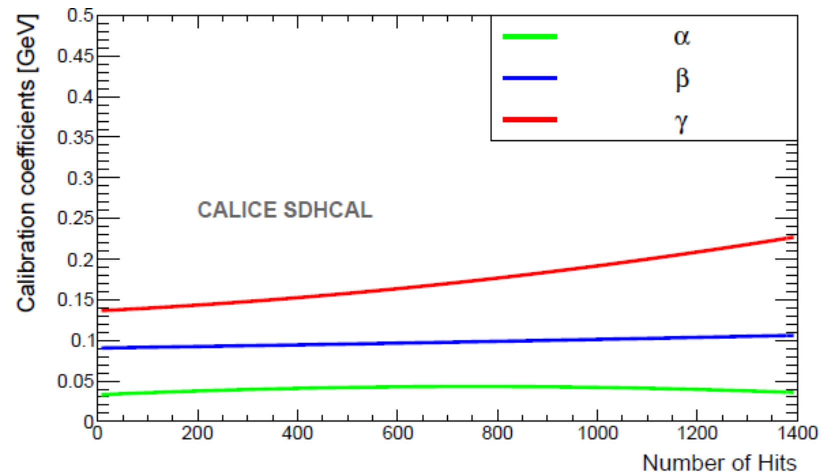
$$E_{reco} = \alpha N_1 + \beta N_2 + \gamma N_3$$

α, β, γ are parameterized as functions of total number of hits(N1+N2+N3)

$$\alpha = \alpha_1 + \alpha_2 N_{total} + \alpha_3 N_{total}^2$$

$$\beta = \beta_1 + \beta_2 N_{total} + \beta_3 N_{total}^2$$

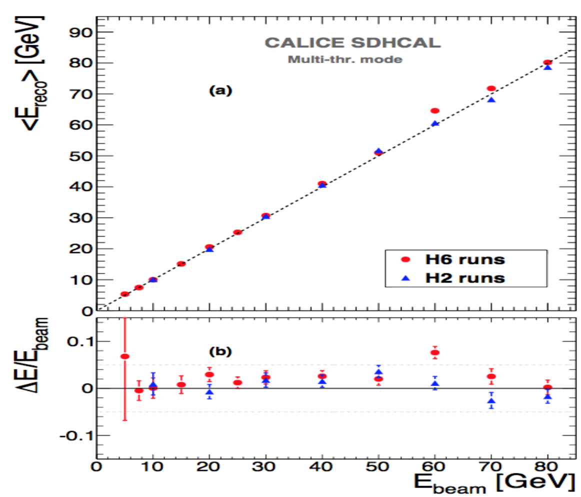
$$\gamma = \gamma_1 + \gamma_2 N_{total} + \gamma_3 N_{total}^2$$

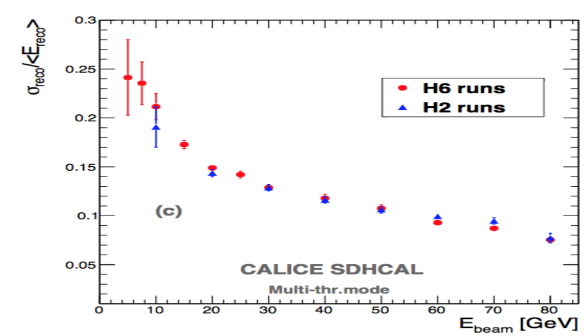


◆ **optimizer**

$$\chi^2 = \sum_{i=1}^{N} \frac{(E_{beam}^i - E_{reco}^i)^2}{\sigma_i^2}$$

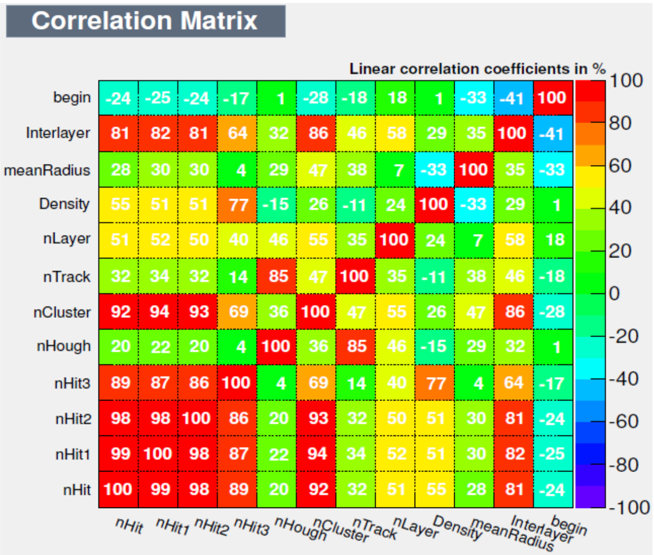
$$\sigma_i = \sqrt{E_{beam}^i}.$$



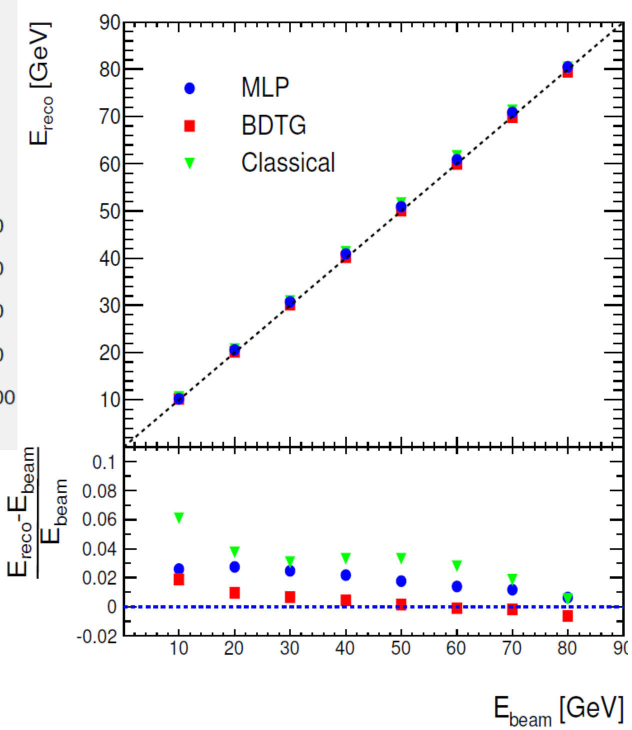


Energy Reconstruction (MVA)

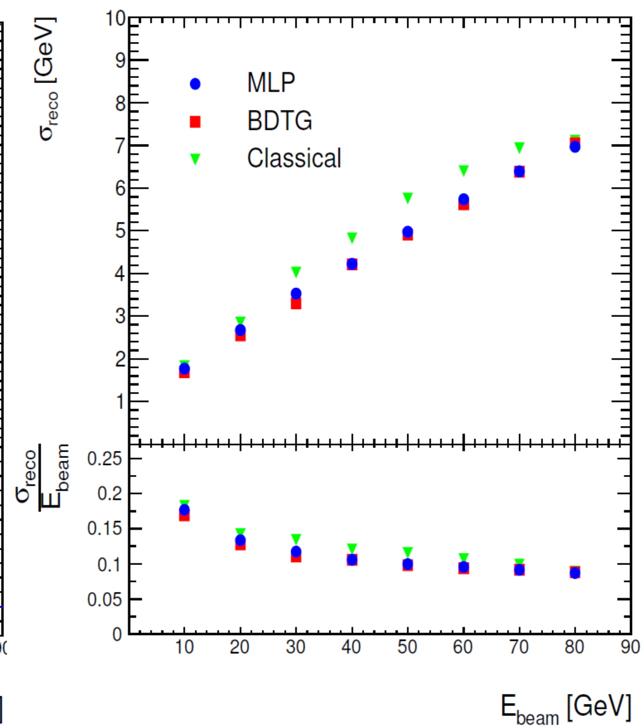
In Progress



Energy shift reduces from 3% to 1% level using BDTG



Energy resolution improves about 10-15% using MVA



Besides 4 Nhits variables, We add 8 new variables to describe hadronic showers

Energy Resolution (Binary vs 3-threshold)

Comparison of semi-digital versus binary readout

E_{rec} (binary) = $C\, N_{tot} + D\, N^2_{tot} + F\, N^3_{tot}$

E_{rec} (semi-digital) = $\alpha(N_{tot})\, N_1 + \beta(N_{tot})\, N_2 + \gamma(N_{tot})\, N_3$

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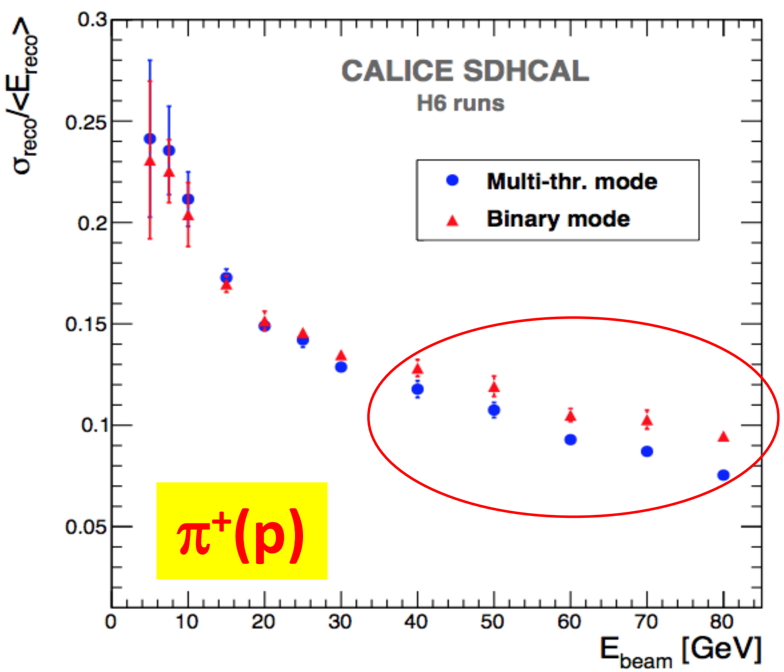

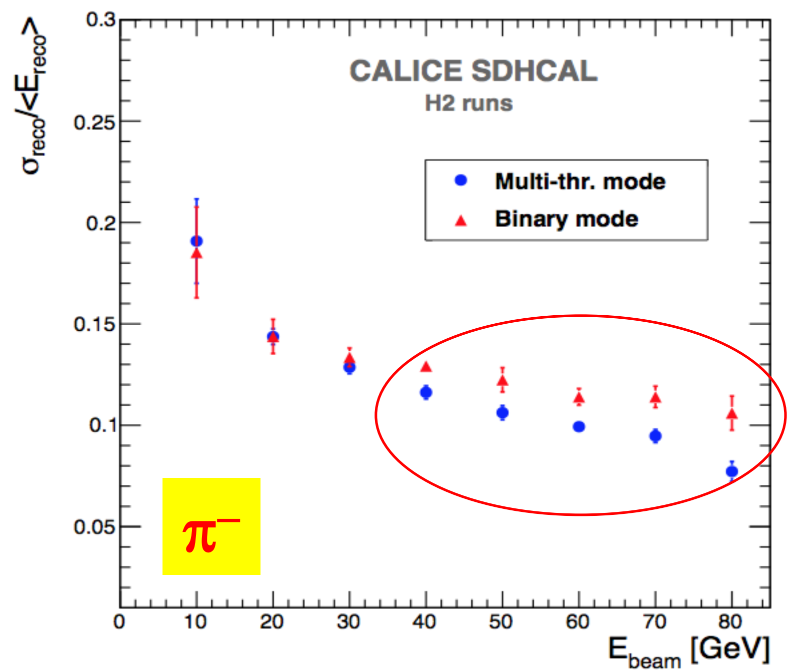

➔ **Multi-threshold mode performs better than binary mode for energy > ~ 40 GeV**

Data vs MC： Efficiency and Multiplicity

SDHCAL Efficiency (Data/MC): 96% / 97%
SDHCAL Multiplicity (Data/MC): 1.8 / 1.74

➔ **Good Data/MC agreement for efficiency and multiplicity obtained with cosmic muons and test beam muons.**

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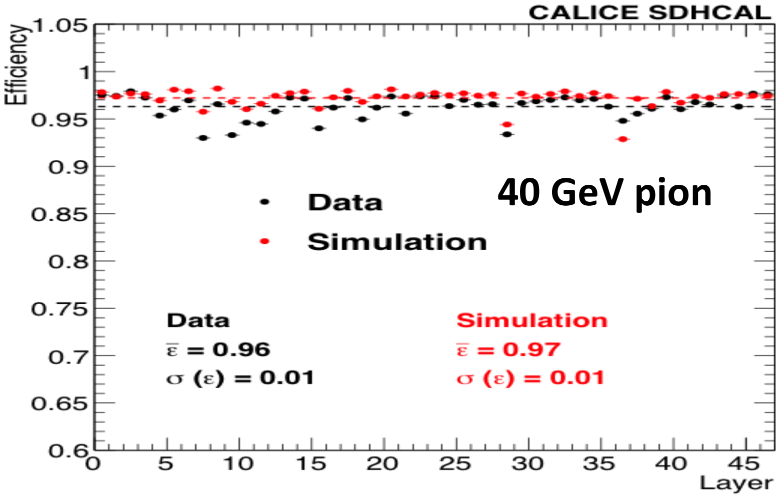

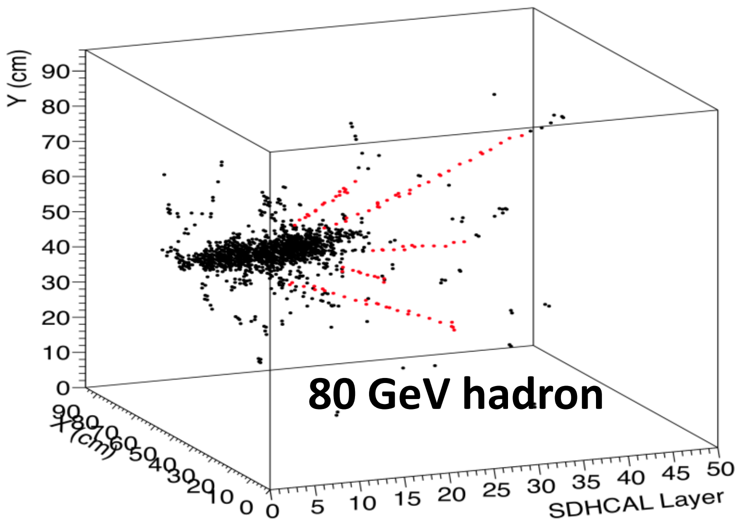

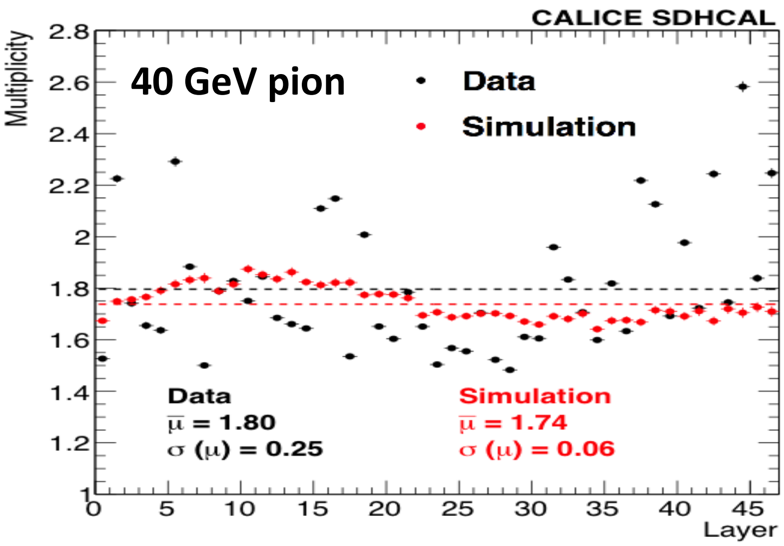

Data vs MC

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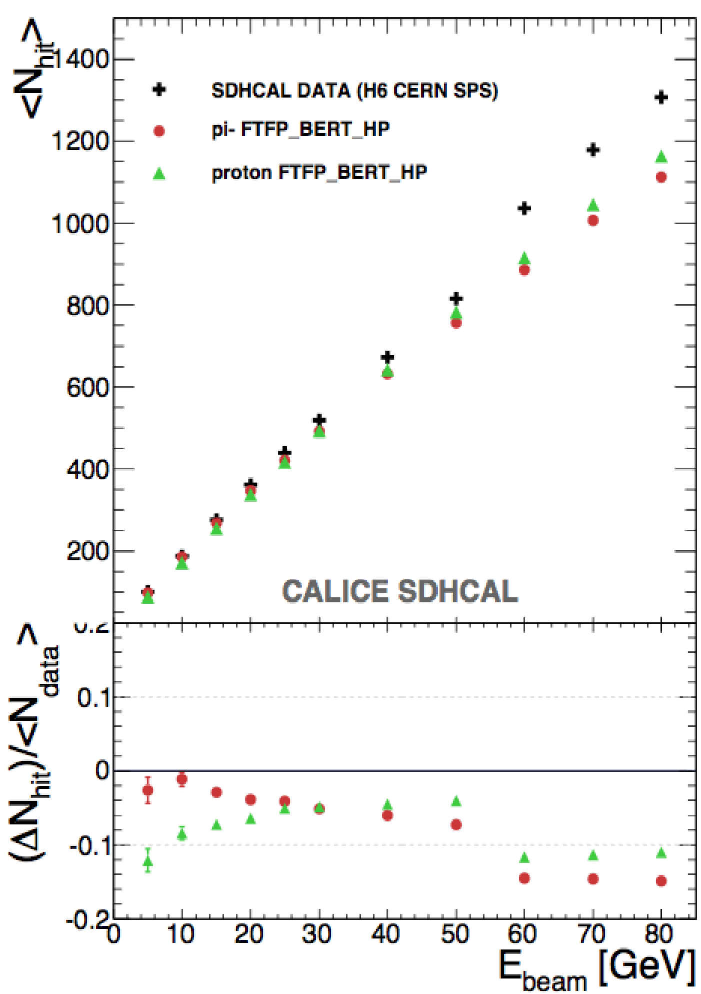
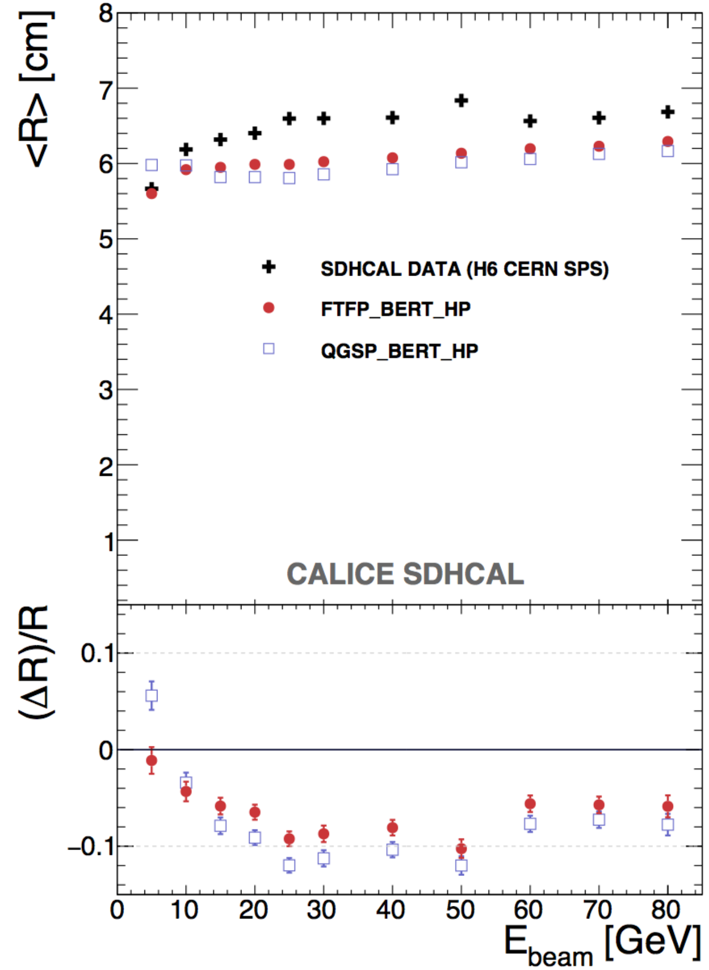
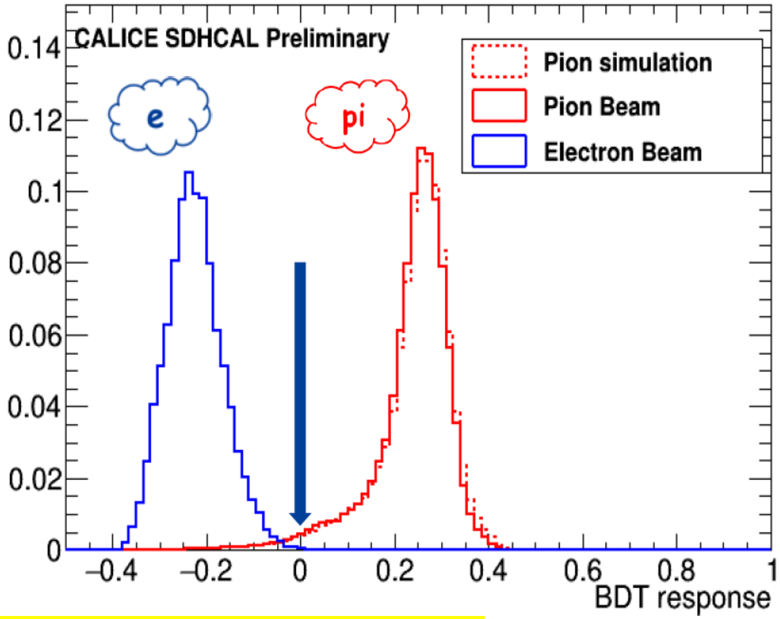
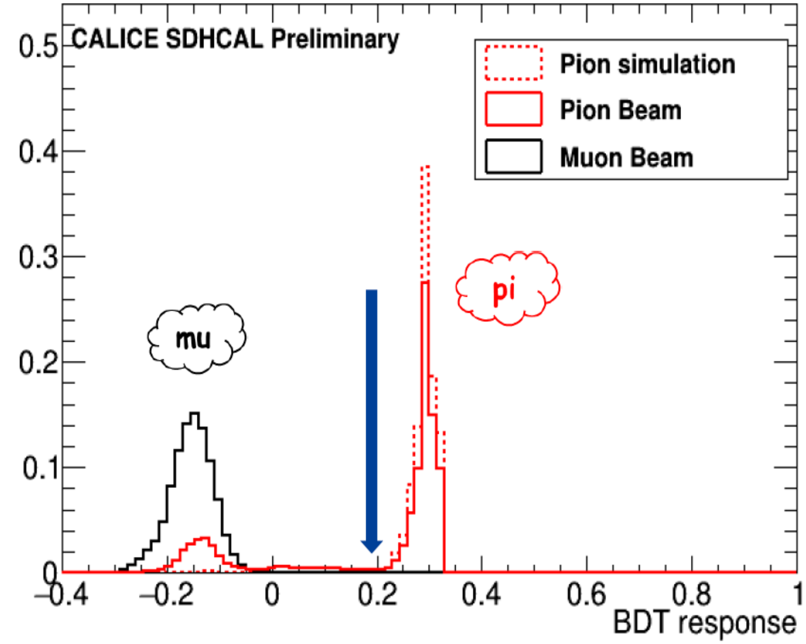




Hadronic shower is more compact in MC than in data

Pion/e, mu ID using BDT





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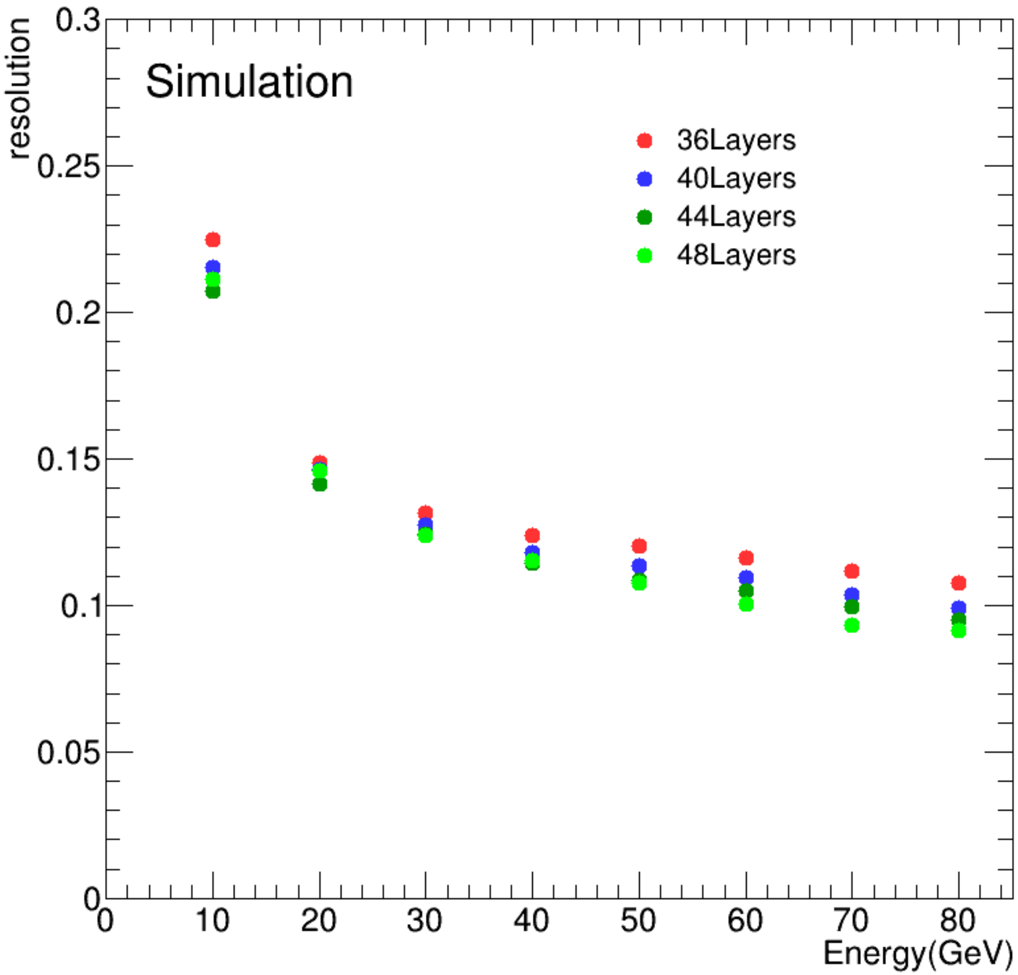
➔ **SDHCAL is a powerful tool to identify pion/e/mu**

➔ **BDT helps to improve the hadron/e/mu PID**

Energy	simple cut			BDT		
	eff_{pion}	$eff_{electron}$	eff_{muon}	eff_{pion}	$eff_{electron}$	eff_{muon}
10GeV	55.7%	0.0%	0.1%	55.7%	0.0%	0.0%
20GeV	70.5%	0.0%	0.3%	70.5%	0.0%	0.0%
30GeV	80.9%	0.0%	0.6%	80.9%	0.0%	0.1%
40GeV	87.2%	0.1%	0.6%	87.2%	0.0%	0.1%
50GeV	90.6%	0.1%	0.9%	90.6%	0.1%	0.1%
60GeV	93.0%	0.2%	1.0%	93.0%	0.2%	0.2%
70GeV	94.7%	0.3%	1.2%	94.7%	0.2%	0.2%
80GeV	95.7%	0.3%	1.1%	95.7%	0.2%	0.2%

Energy Resolution vs No. of Layers



$(0.12\lambda_I, 1.14X_0)$

Stainless steel Absorber(15mm)

Stainless steel wall(2.5mm)

GRPC(6mm$\approx 0\ \lambda_I, X_0$)

Stainless steel wall(2.5mm)

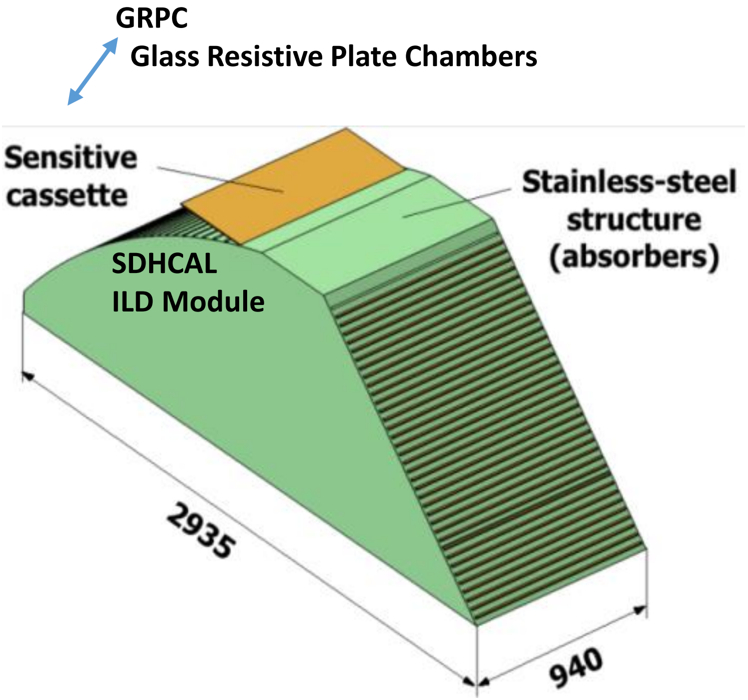
➔ **SDHCAL has 48 layers which aims for ILC Detector 6mm gRPC + 20mm absorber**

➔ **Optimization no. of layers for CEPC at 240GeV**

➔ **40-layer SDHCAL yields decent energy resolution.**

SDHCAL for Future Experiments

- ❑ Detectors as large as 3m × 1m need to be built
- ❑ Electronic readout should be the most robust with minimal intervention during operation.
- ❑ DAQ system should be robust and efficient
- ❑ Mechanical structure to be similar to the final one
- ❑ Envisage new features such as timing, etc..



Goal: to build new prototype with few but large GRPC and new components

New Electronics

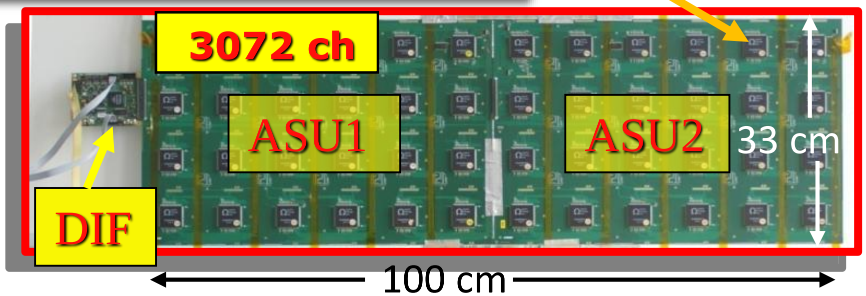
Electronics readout for the 1m³ prototype

HADROC chip (ASIC)

1m² board ➔ 6 ASUs hosting 24 ASICs

USB

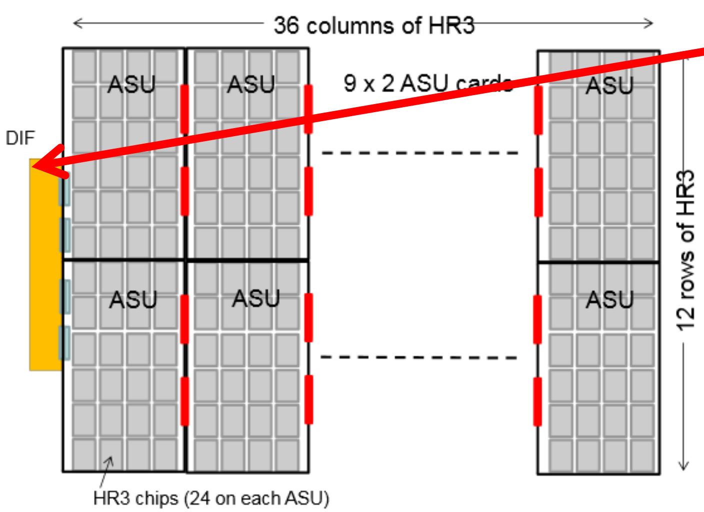
HDMI



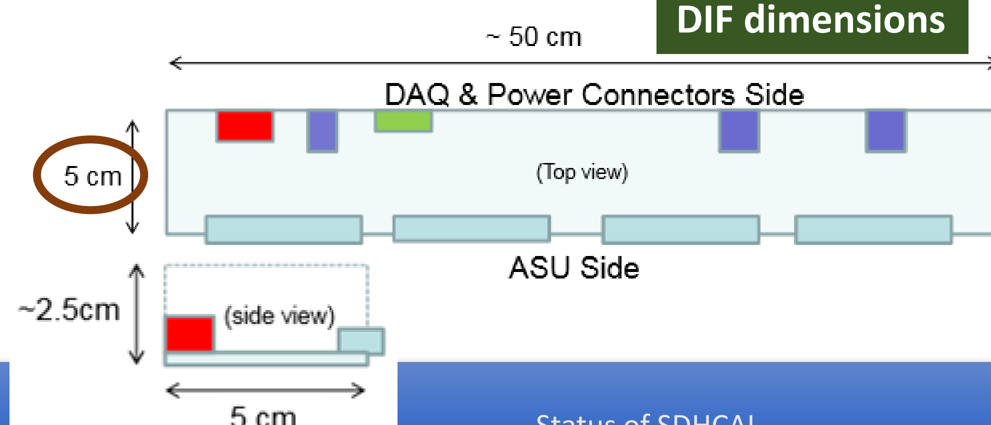
1 DIF (Detector InterFace) for **2 ASU** (Active Sensor Unit.- PCB+ASICs) ➔ **3 DIFs for ONE 1m² GRPC detector**

Electronics readout for the final detector

Only **1 DIF per GRPC (any size)** with small dimensions to fit in the **small** space available at the **ILD detector**



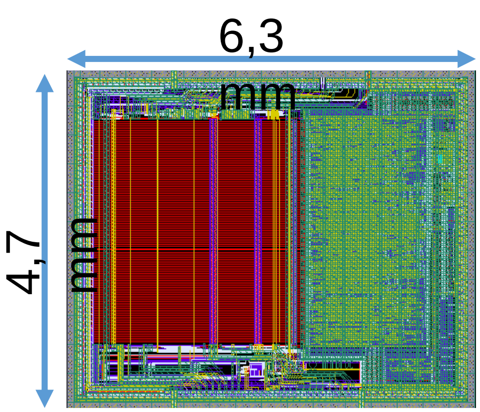
DIF dimensions

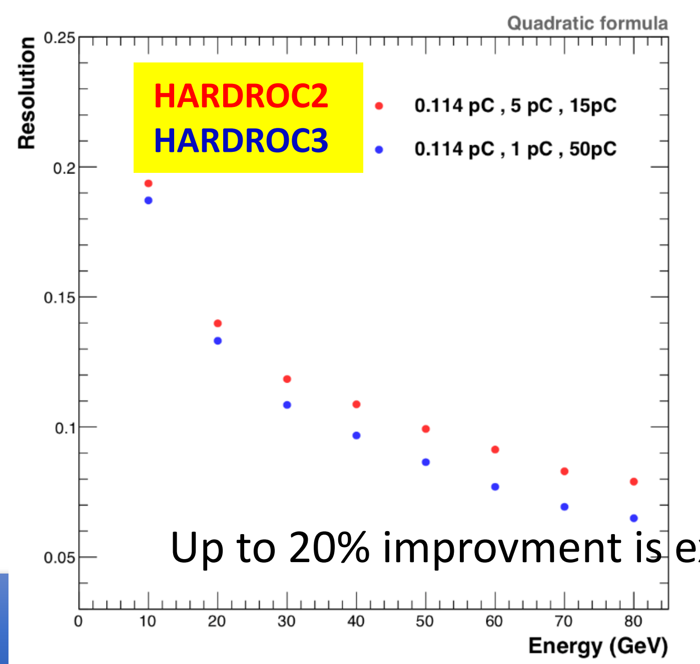


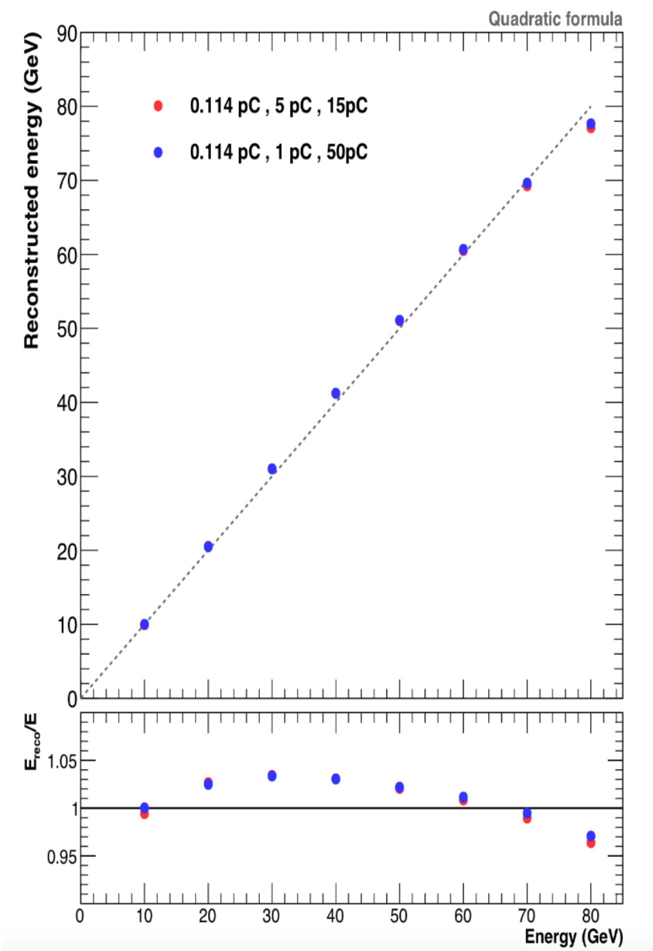
New Electronics: ASICs

HARDROCR3 main features:

- **Independent channels**
- **Zero suppress**
- Extended dynamic range (**up to 50 pC**)
- **I2C link with triple voting for slow control par.**
- packaging in QFP208, die size ~30 mm^2
- Consumption increase (internal PLL, I2C)



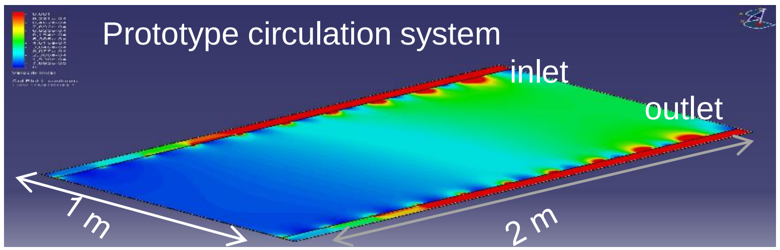


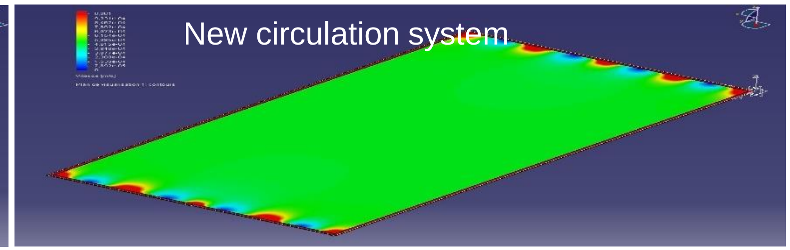


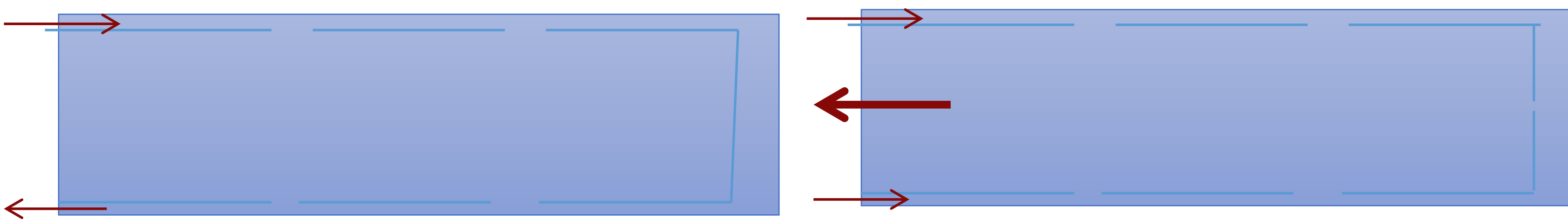
Up to 20% improvment is expected

New Gas Distribution

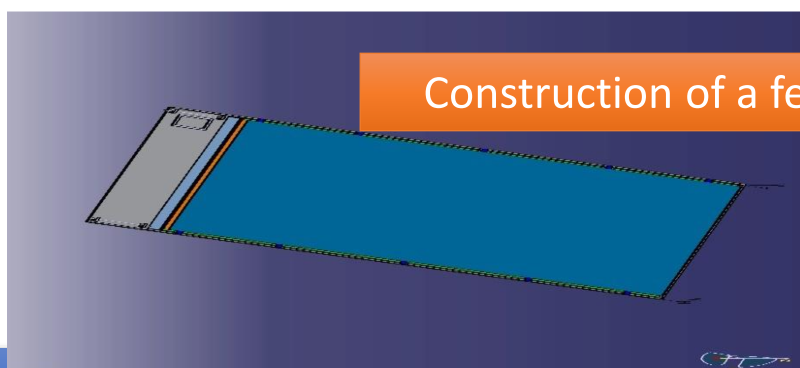
Construction and operation of large GRPC need some improvements with respect to the present scenario. **Gas distribution** : new scheme is proposed



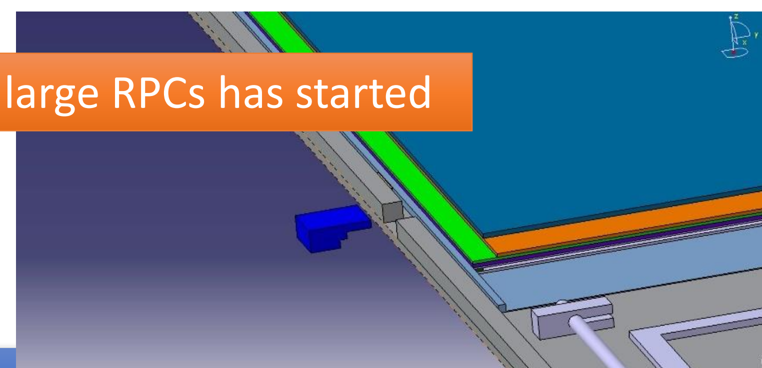




Cassette conception to ensure good contact between the detector and electronics is to be improved

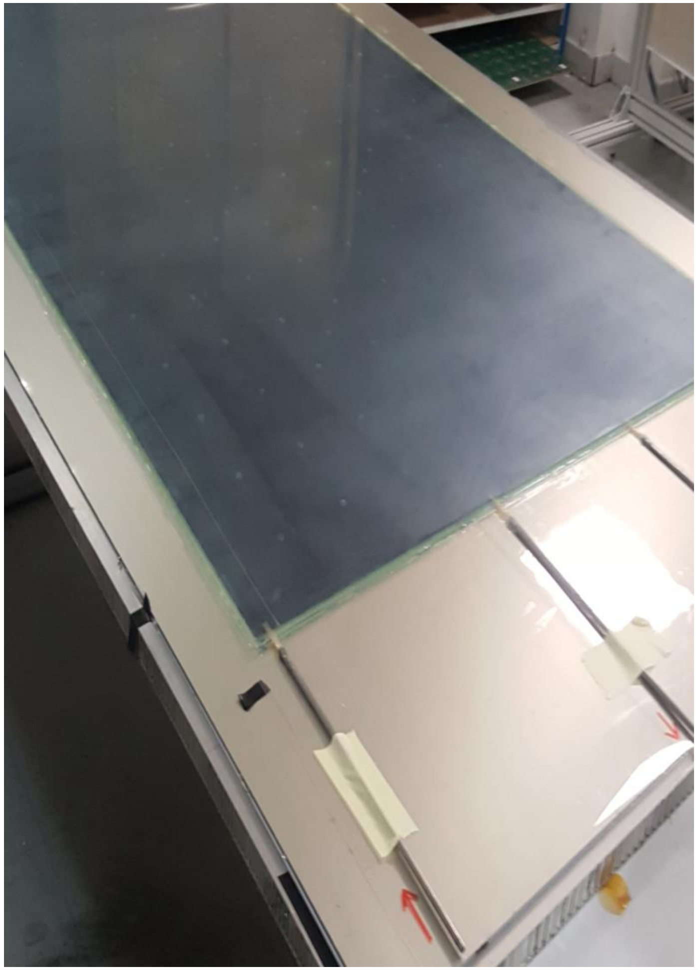


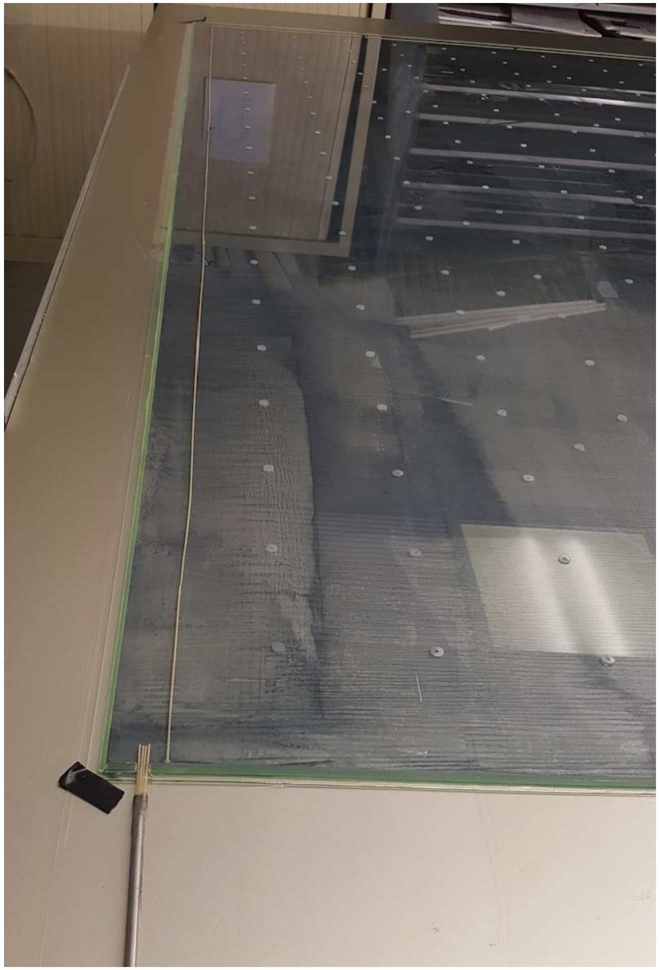
Construction of a few large RPCs has started



Construction of Large RPC

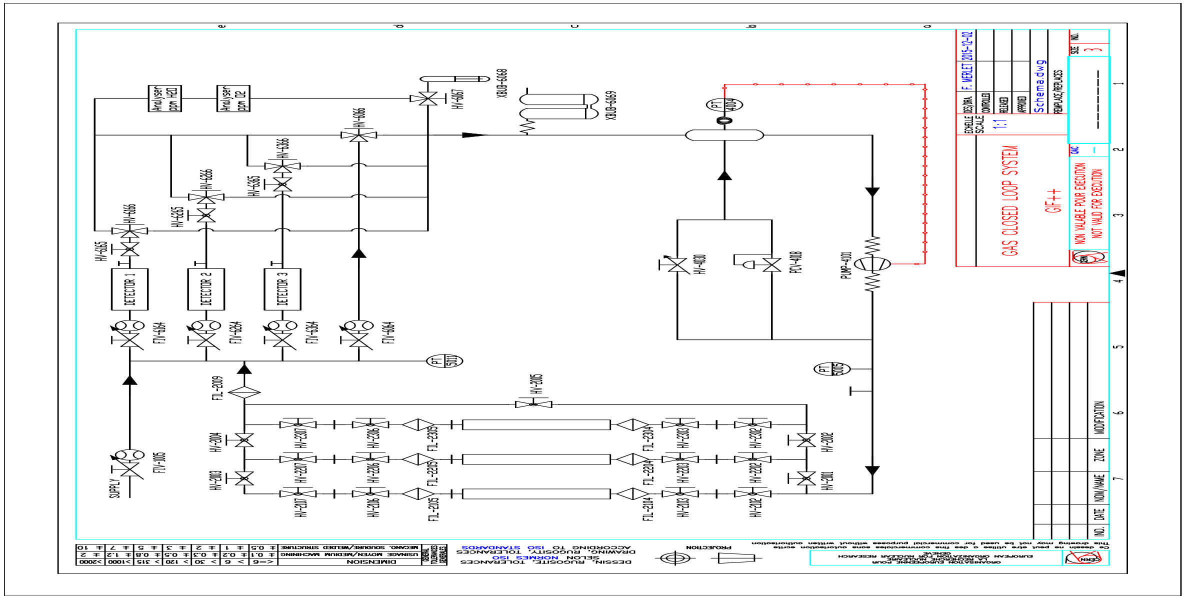
First 2x1 m^2 RPC chamber was successfully built with a new gas circulation system





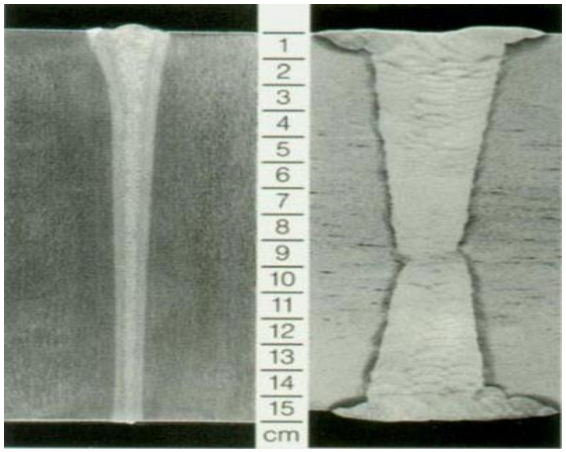
Recycling Gas System

- Successfully tested recycling gas system.
- A reduction of gas consumption by a factor up to 7 was achieved on a subset of the prototype.



Mechanical Structure

Improvement on the present system is being made by using **Electron Beam Welding** rather than bolts to reduce the deformation and the spacers thickness.



Industrial production of **flat** large absorber plates (3 m X 1 m) by **roller leveling** process

Major Challenges

- CEPC bunch spacing is 690ns/210ns/25ns for H/W/Z) → operating at continuous mode
- High granularity for SDHCAL → ~66M channels
- Estimated power consumption → ~110kW

→ Possible solutions:

- Active cooling
- To reduce electronic channels

Estimated HCAL Channels

- HCAL Barrel, R_{in} = 2.3m, R_{out} = 3.34m, length = 2.67*2=5.34m, N_{layer}=40
  - Area of HCAL barrel = $2*PI*[(R_{in}+R_{out})/2]*L*N_{layer}$ = 3782 m^2
- HCAL Endcap (2), R_{in} = 0.35m, R_{out} = 3.34m, N_{layer}=40
  - Area of HCAL endcap = $2*PI*(R_{out}*R_{out} – R_{in}*R_{in})*N_{layer}$ = 2772 m^2

Cell Size \ channels	HCAL Barrel	HCAL Endcap	Channels (N_{ch})	Power AHCAL	Power SDHCAL
1cm x 1cm	37.82M	27.72M	65.5M		110 kW
2cm x 2cm	9.455M	6.93M	16.4M		52 kW
3cm x 3cm	4.2M	3.08M	7.3M	110 kW	43 kW
4cm x 4cm	2.36M	1.73M	4.1M	88 kW	
5cm x 5cm	1.51M	1.11M	2.6M	77 kW	

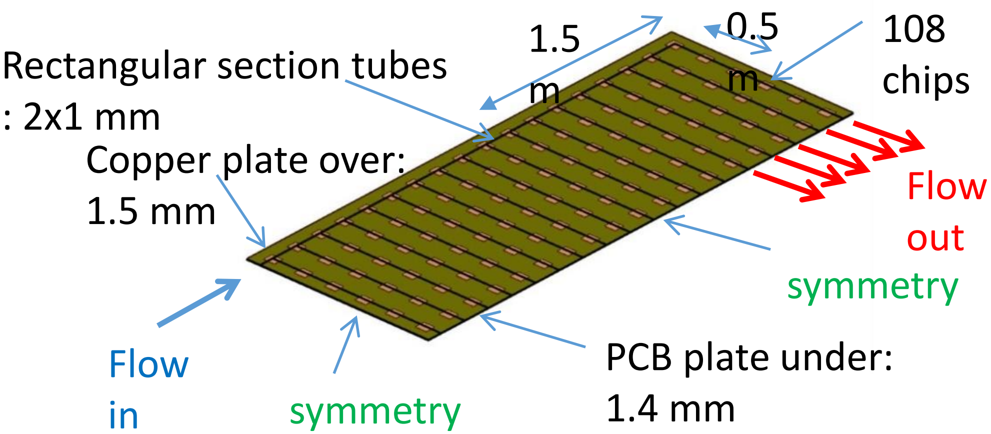
Power Consumption (rough estimation):

AHCAL: 7mW/ch * N_{ch3} + 9W/DIF/m^2 * 6554 (59kW)

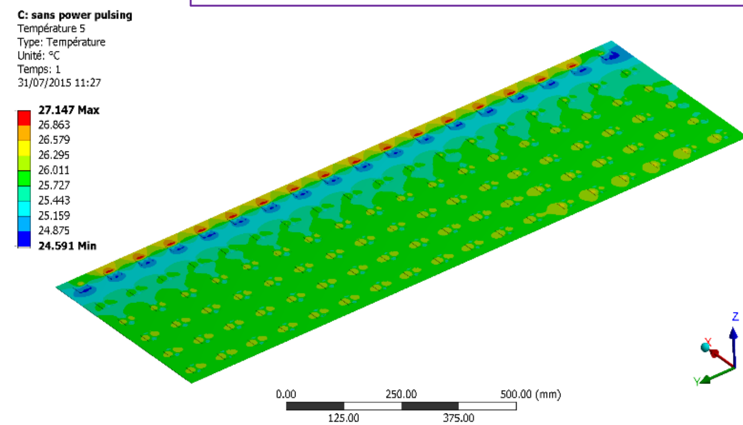
SDHCAL: 1mW/ch * N_{ch1} + 5.4W/DIF/m^2 * 6554 (35.4kW)

Active Cooling

Cooling may become necessary if it is operating at continuous mode (CEPC)



27.147 (max) – 24.591 (min) =2.556 °C



- A water-based cooling system inside copper tubes in contact with the ASICs to absorb excess heat.
- Temperature distribution in an active layer of the SDHCAL.

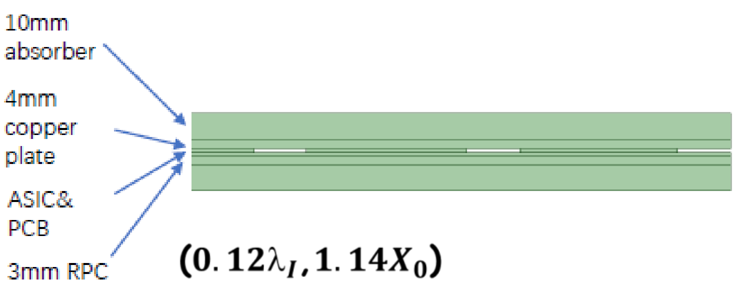
- **To simulate temperature distribution in an active layer**
- **To simulate temperature distribution for multi-layer SDHCAL**
- **optimize tube size and geometry**
- **optimize water flow rate and cooling capacity**

Water cooling : h = 10000 W/m²/k
Thermal load : 90 mW/chip

Simulation of Active Cooling

In Progress

ANSYS Simulation of RPC+PCB With copper plate & water tubes



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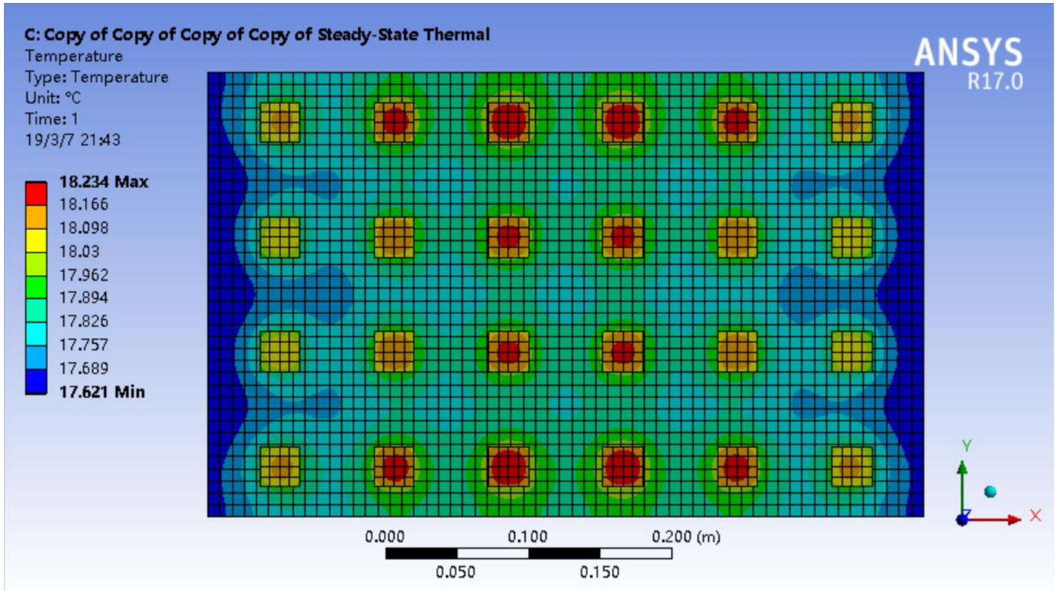
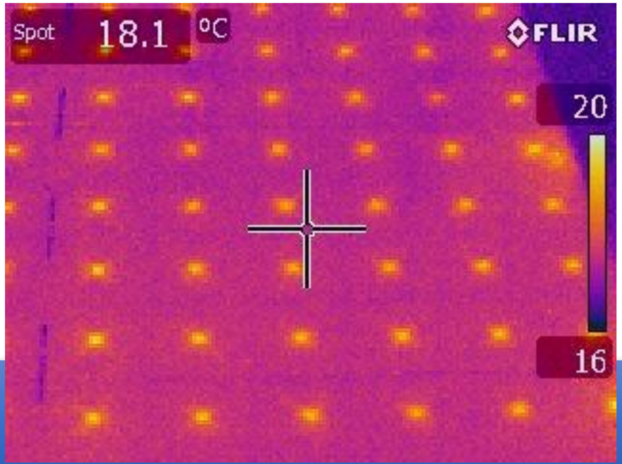


Temperature test of RPC+PCB

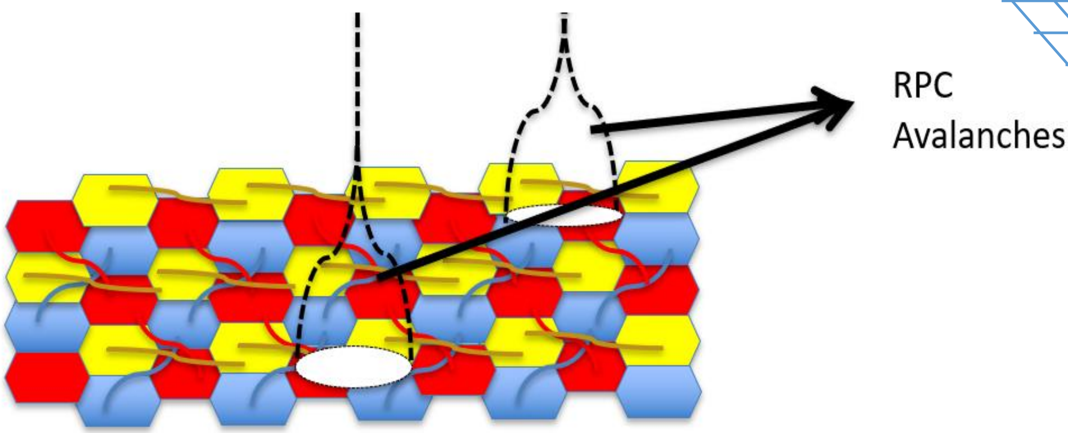


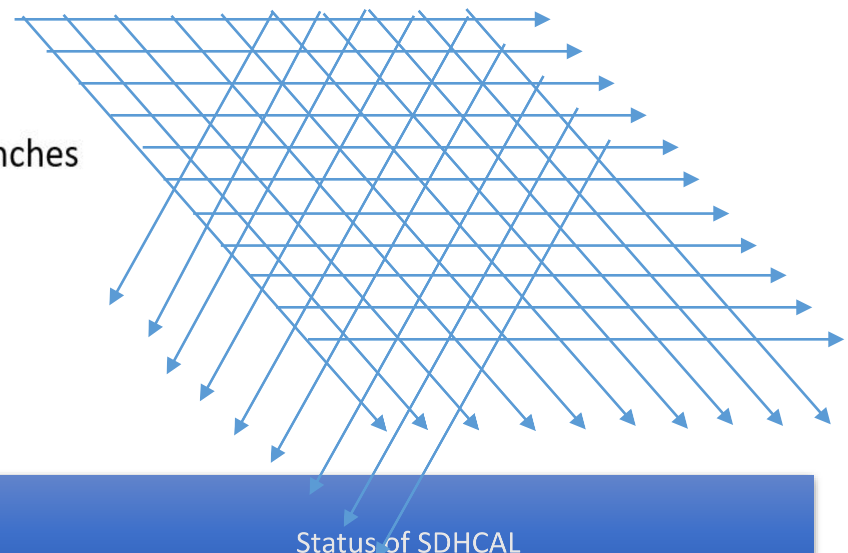
New PCB Design: reduce channels

- SDHCAL for CEPC is ~65M channels, only 2-5K will be fired for each collision, most of channels are idle almost all of the time.
- Reducing no. of cells will lead to less granularity ➔ **bad PFA**

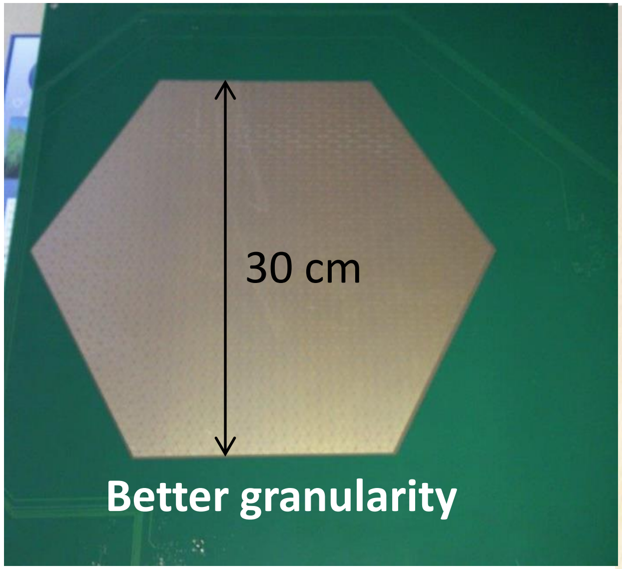
➔ Solution (Imad Laktineh @IPNL):

- **The principle: charge is shared among several cells. The cells are inter-connected in a smart way** so that one can identify the position of the impinging particle by identifyingfired strips and find hit as crossing points.
- At least 3-directions strips ➔ no ambiguity





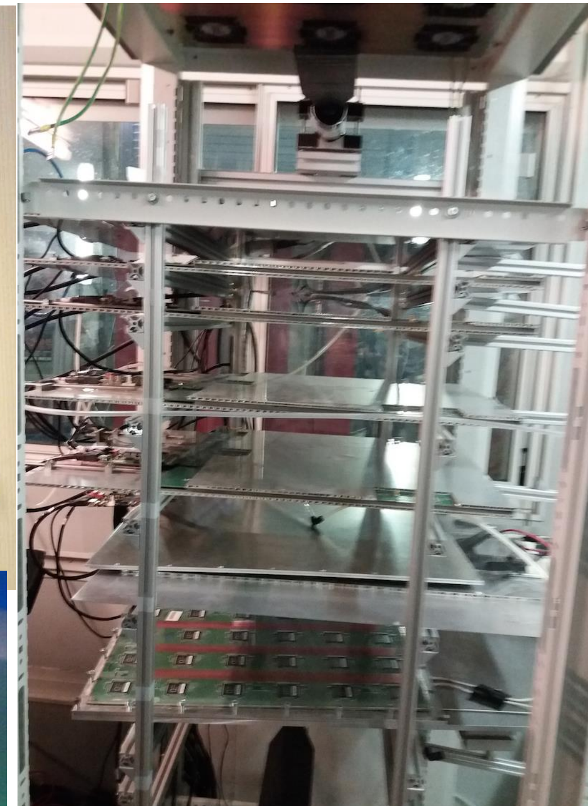
New PCB Design



30 cm

Better granularity

3 HR2 ASICs rather than 20 for the same surface

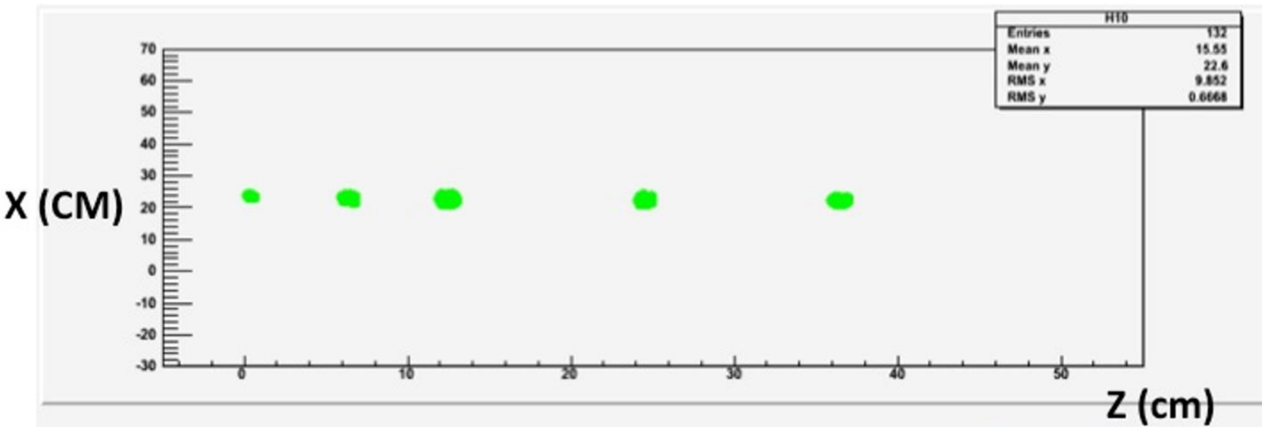


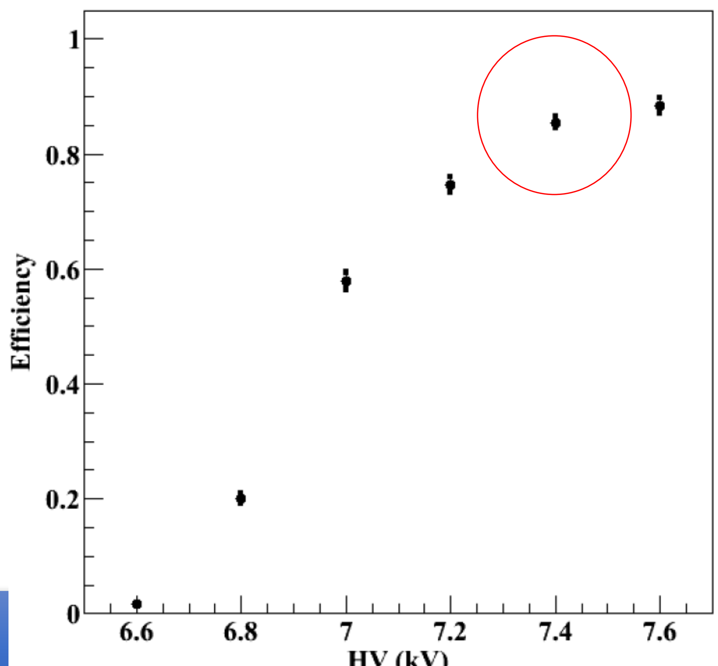
Setup with 5 detectors equipped with new PCB

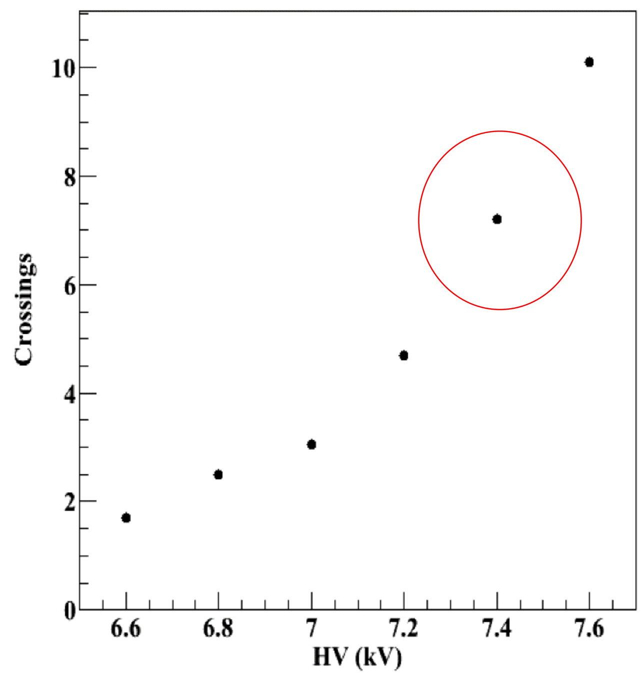
The scheme was used to design a new PCB with lozenges structure and 3 directions.

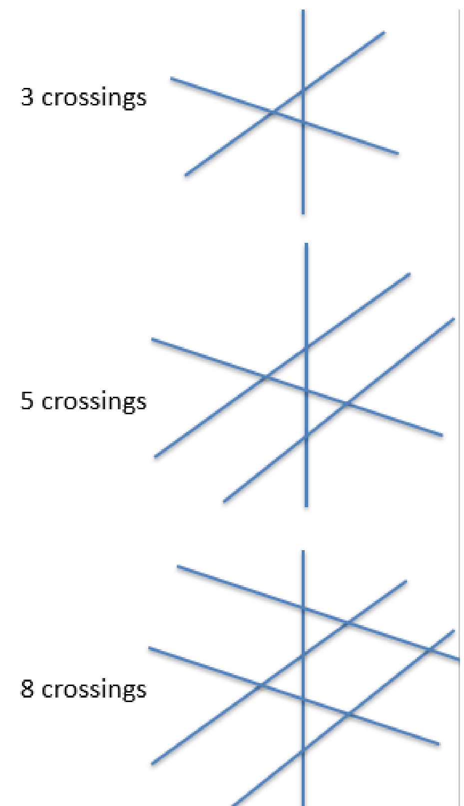
Lozenge's large diagonal : 1 cm

New PCB Design





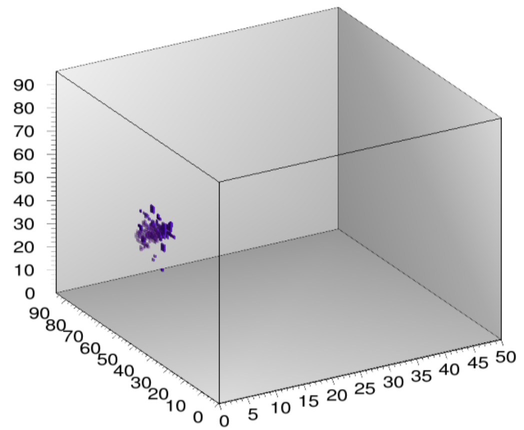


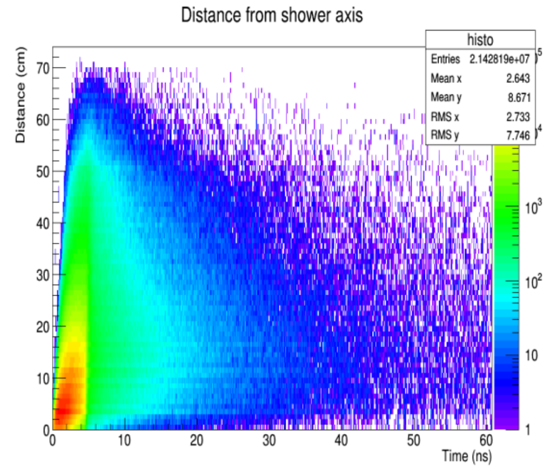


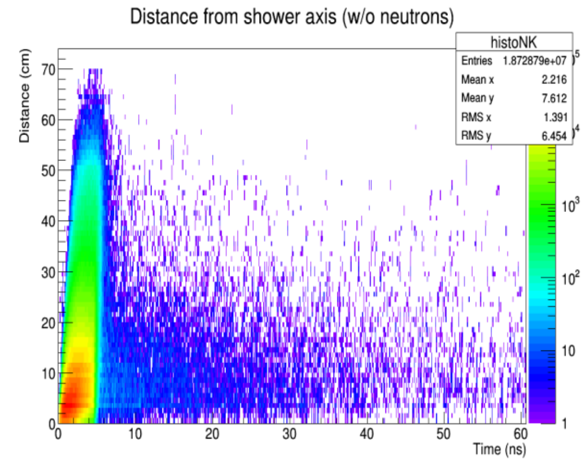
Better Timing: MRPC

In Progress

Timing could be an important factor to **separate showers** and **better reconstruct their energy**



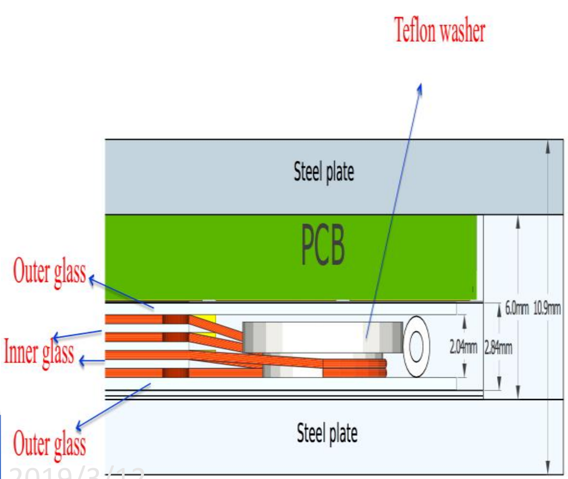


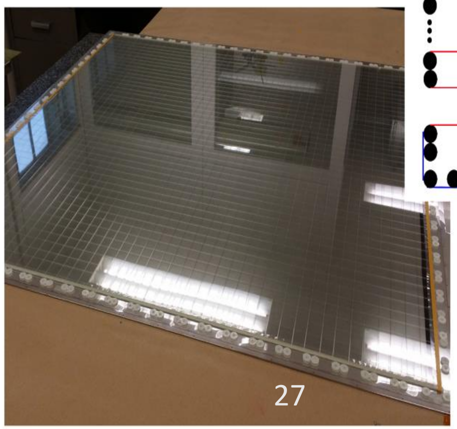


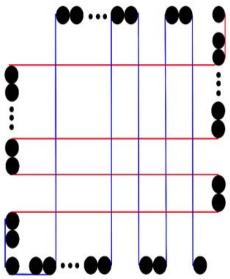
Multi-gap RPC are excellent fast timing detectors

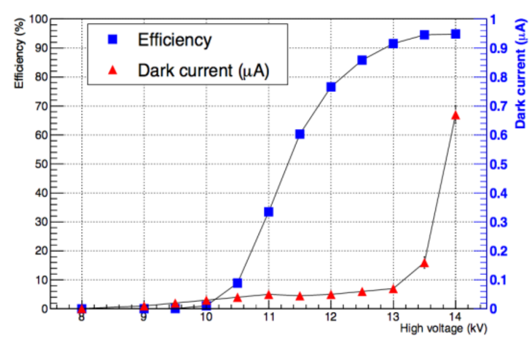
Several MRPC were designed and built . Excellent efficiency when tested with HARDROC ASICs.

Next step use PETIROC (< 20 ps time jitters) to single out neutron contributions.



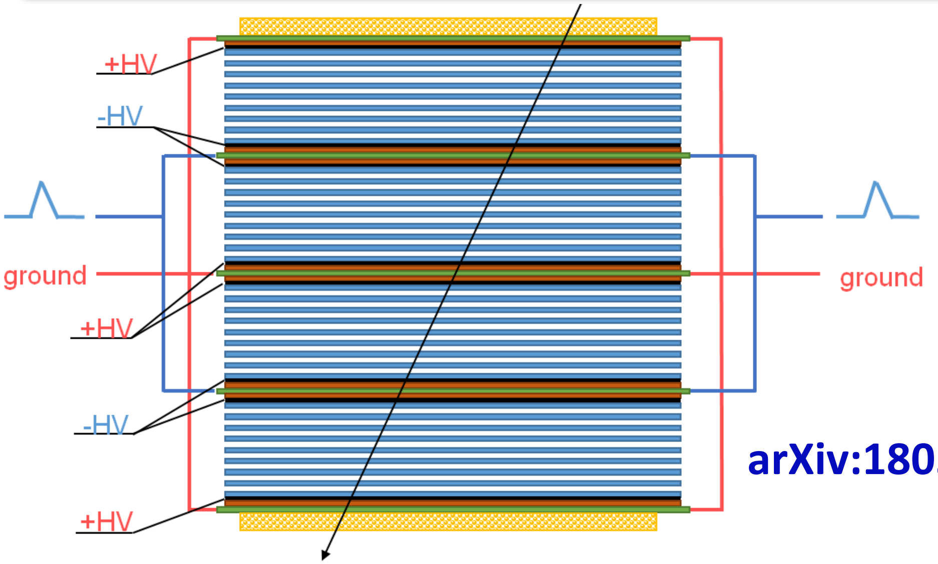


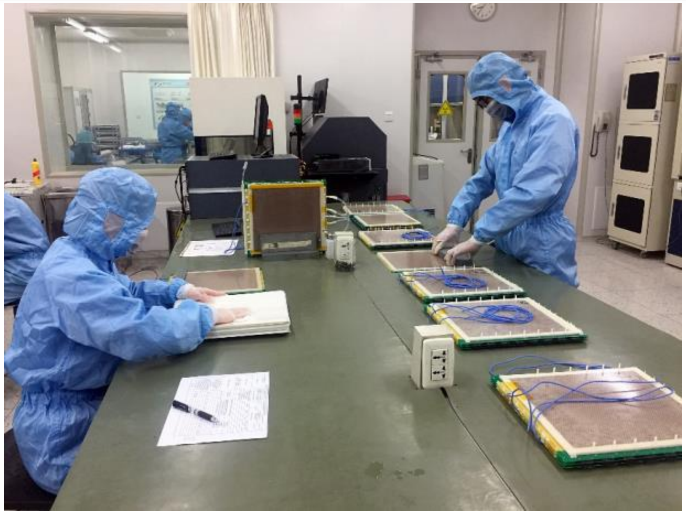




Threshold sets at 114 fC

MRPC designed by Tsinghua U.

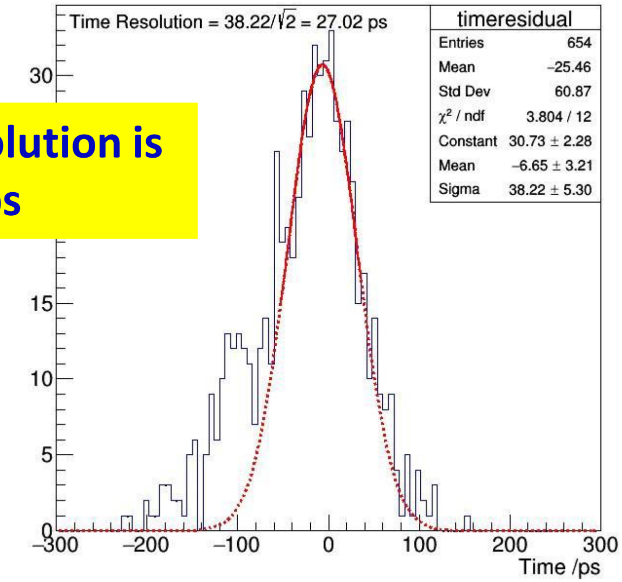




arXiv:1805.07922

Item	dimension/mm
Honeycomb	90×265×7.5
Outer PCB	120×298×0.6
Middle PCB1	120×298×1.2
Middle PCB2	120×328×1.2
Strip length	268
Strip width	7
Mylar	90×268×0.25
Glass	80×258×0.5
Carbon	72×250
Gas gap width	0.104
Number of gas gap	32

Time Resolution is about 30ps



Cost Estimation: SDHCAL

- HCAL Barrel, R_{in} = 2.3m, R_{out} = 3.34m, length = 2.67*2=5.34m, N_{layer}=40
  Area of HCAL barrel = $2*PI*[(R_{in}+R_{out})/2]*L*N_{layer}$ = 3782 m^2
- HCAL Endcap (2), R_{in} = 0.35m, R_{out} = 3.34m, N_{layer}=40
  Area of HCAL endcap = $2*PI*(R_{out}*R_{out} – R_{in}*R_{in})*N_{layer}$ = 2772 m^2

Parts	Unit Price (RMB)	Quantity	Total (RMB)
Glass	150 / m^2	2	300
Resistive Paint	1 / g	100	100
Frame	10 / m	4	40
Spacers	1	81	81
Spacer Glue	3.3 / g	30	100
Gas Connector	20	2	40
HV contacts	80 / m	0.1	8
HV connectors	50	2	100
Total cost of 1m^2 GRPC			769

Parts	Unit Price (Euro)	Quantity	Total(Euro)
Cassette plates	8 /kg	50	400
Plate machining	200	1	200
Cassette walls	8 / kg	0.8	6.4
Mylar foils	15 / m^2	2	30
Silicone glue	0.3 / ml	60	18
Bolts M2	0.02	60	1.2
Total cost of 1m^2 cassette			655.6
Readout Electronics	Unit Price (Euro)	Quantity	Total (Euro)
ASIC (64 channels)	11.5	144 (9216)	1656
ASU:PCB (8-layer)	300	6	1800
DIF (detector interface DAQ card)	285	3	855
ASU-ASU connector	11	6	66
DIF-ASU	40	3	120
Total cost for readout electronics			4497

CEPC SDHCAL: 6550 m^2
Unit Cost: 40K RMB/m^2
Total Cost: 262M RMB

Summary and Conclusion

- **SDHCAL (since 2011) is the first technological and still the unique complete prototype built for future experiments.**
- **Results of beam tests validate the concept. Many results are obtained.**
- **There is still a place for improvement by using genuine techniques (MVA, …)**

- **New features such as PCB design, timing and cooling will play important role in future colliders calorimetry R&D.**

Many thanks for great efforts from CALICE SDHCAL working group！

Backup Slides

Material	λ_I(cm)	X_0(cm)	λ_I/X_0
Fe	16.77	1.76	9.5
Pb	17.09	0.56	30.52
W	9.95	0.35	28.4

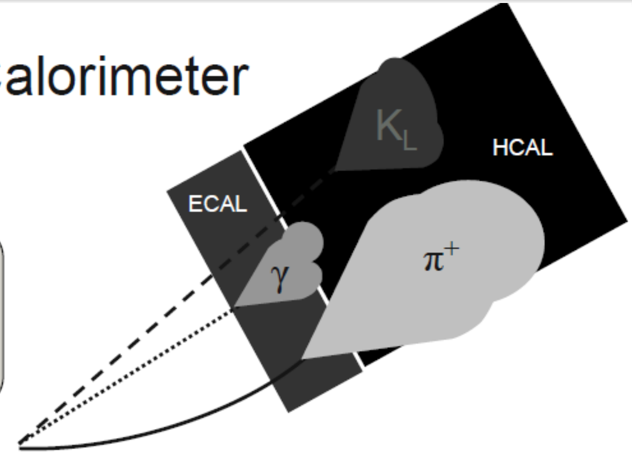
Table 1. Radiation and nuclear interaction lengths for Fe, Pb and W

Table 2. Main technology of three generation of MRPC TOF system

	Requirement	MRPC	Typical electronics	Analysis method	Typical experiment
1st TOF	Time resolution<100ps Rate<100Hz/cm^2	Gas gap:200-300 μm Electrode: float glass	NINOs +HPTDC	TOT slewing correction	RHIC-STAR LHC-ALICE
2st TOF	Time resolution<100ps Rate~30kHz/cm^2	Gas gap:200-300 μm Electrode: low resistive glass	PADI +GET4	TOT slewing correction	FAIR-CBM
3st TOF	Time resolution<20ps Rate~20kHz/cm^2	Gas gap:100-150 μm Electrode: low resistive glass	Fast amplifier + pulse shape sampling	TOT slewing correction Deep learning technology	JLab-SoLID

PFA and Imaging Calorimeter

Particle Flow Algorithms and Imaging Calorimeter



The idea…

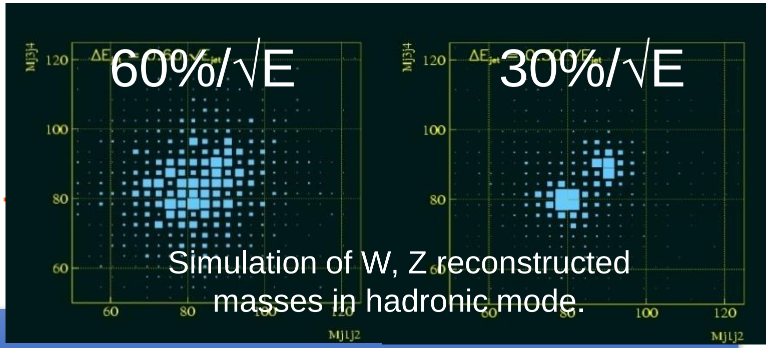
Charged particles	measured with the	**Tracker**
Neutral particles		**Calorimeter**

Particles in jets	Fraction of energy	Measured with	Resolution [σ^2]
Charged	65 %	Tracker	Negligible
Photons	25 %	ECAL with 15%/√E	$0.07^2\ E_{jet}$
Neutral Hadrons	10 %	ECAL + HCAL with 50%/√E	$0.16^2\ E_{jet}$
Confusion	Required for 30%/√E		$\leq 0.24^2\ E_{jet}$

} 18%/√E

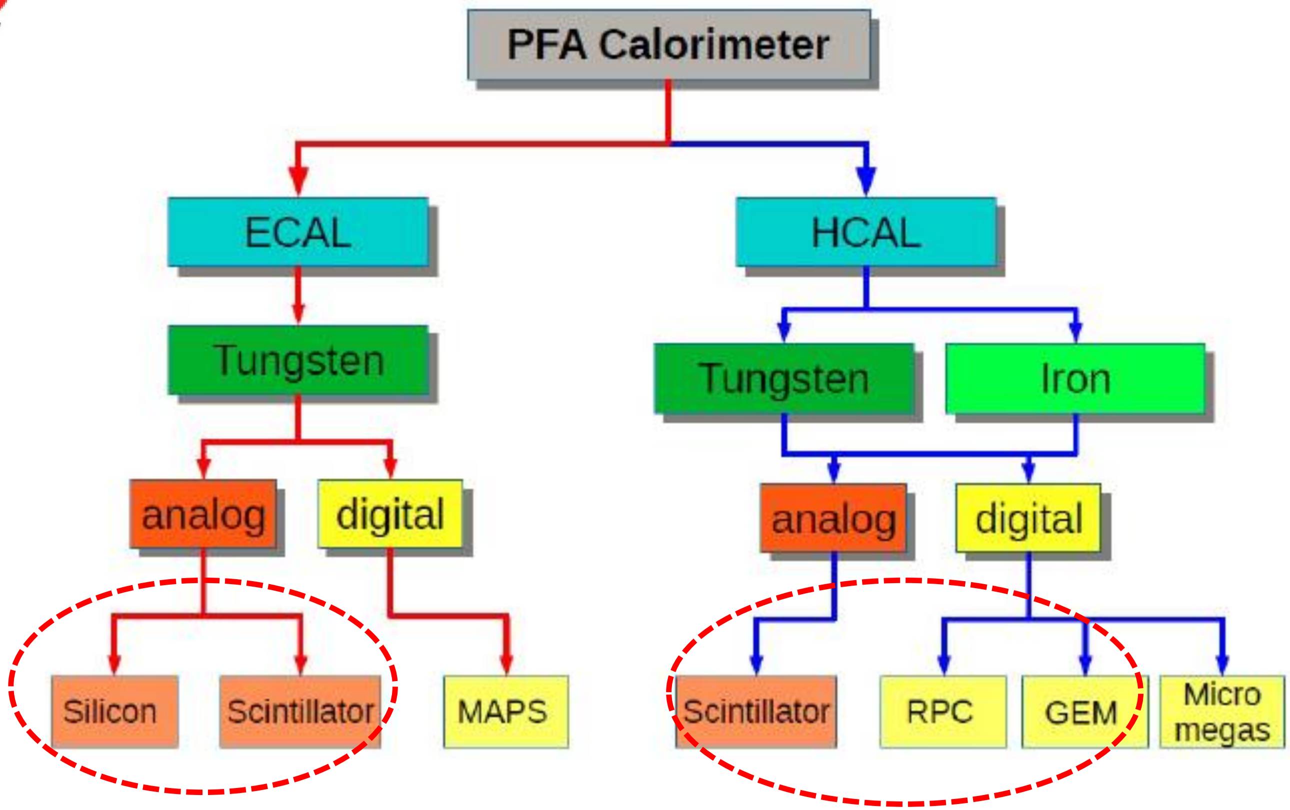
Requirements for detector system

→ Need excellent tracker and high B – field
→ Large R_I of calorimeter
→ Calorimeter inside coil
→ Calorimeter as dense as possible (short X_0, λ_I)
→ Calorimeter with **extremely fine segmentation**



CALICE: Imaging Calorimeter

https://twiki.cern.ch/twiki/bin/view/CALICE/CalicePapers

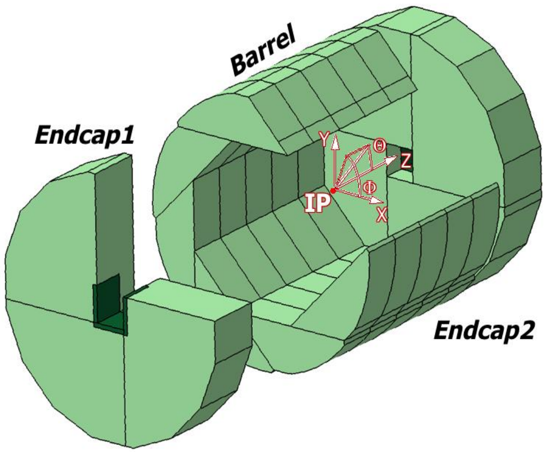


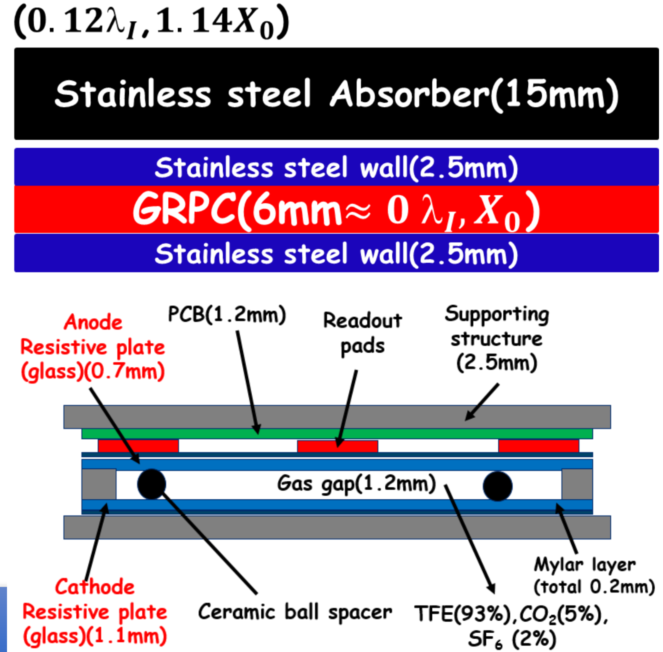
Readout cell size: 144 - 9 cm^2 → 4.5 cm^2 → 1 cm^2 → 0.25 cm^2 → 0.13 cm^2 → 2.5×10^{-5} cm^2

Technology: Scintillator + SiPM/MPPC; Scintillator + SiPM/MPPC; Gas detectors Silicon; Silicon; Silicon; Silicon (MAPS)

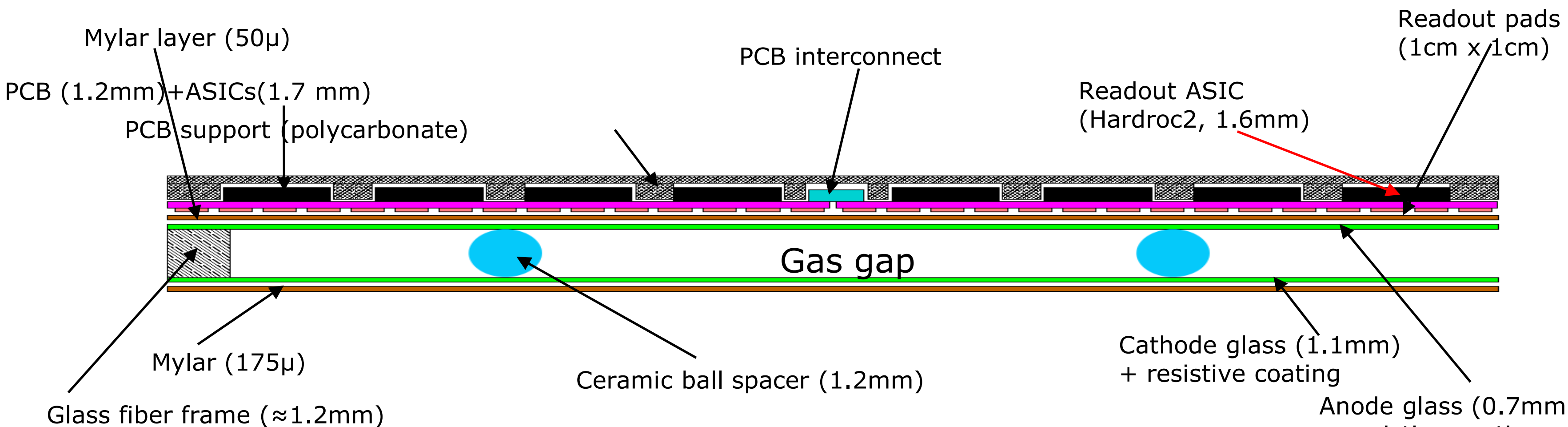
SDHCAL Prototype

- The **SDHCAL-GRPC** is one of the two HCAL options based on PFA and proposed for **ILD**. Modules are made of 48 RPC chambers (**$6\lambda_I$**), equipped with **semi-digital, power-pulsed electronics** readout and placed in **self-supporting mechanical** structure (stainless steel) to serve as absorber.
- **Proposed structure for SDHCAL:**
  - Very compact with negligible dead zones
  - Eliminates projective cracks
  - Minimizes barrel and endcap separation
- **Challenges:**
  - Homogeneity for large surfaces
  - Thickness of only a few mm
  - PCB cell size of 1cm X 1cm
  - Services from one side
  - Embedded power-cycled electronics
  - Self-supporting mechanical structure





Schematic of RPC



Ran Han (BISEE)

Haijun Yang (SJTU)

Large area gRPC:

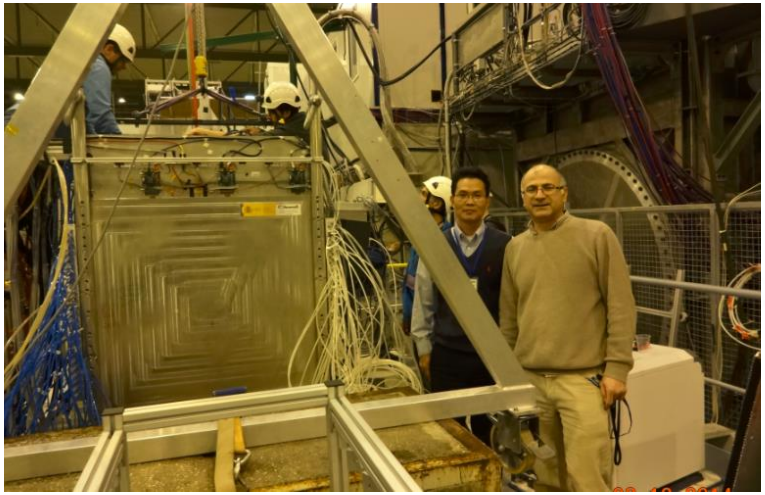
- ✓ Negligible dead zone (tiny ceramic spacers)
- ✓ Large size: 1×1 m^2
- ✓ Cost effective
- ✓ Efficient gas distribution system
- ✓ Homogenous resistive coating

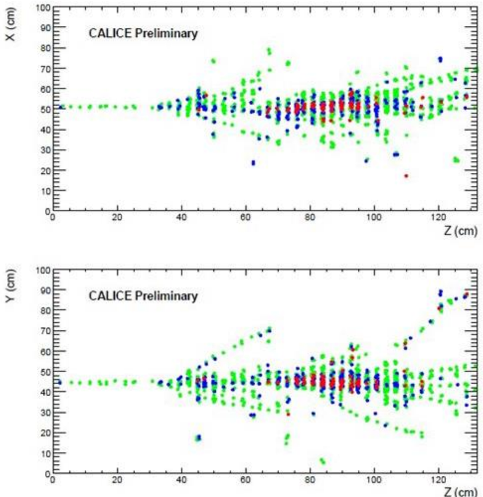
35

DHCAL with RPC

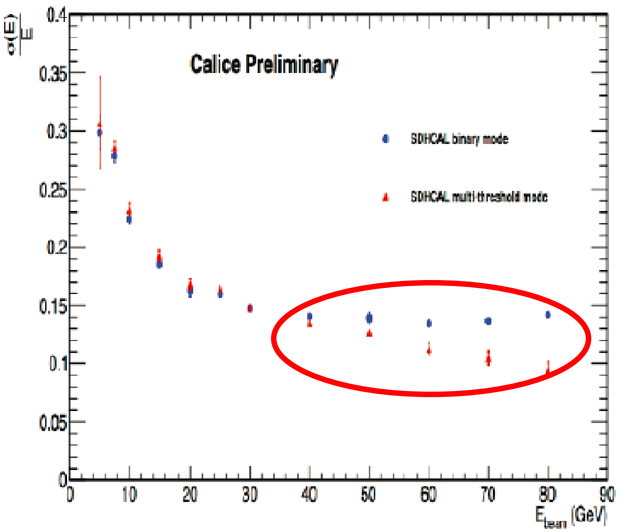
Prototypes of DHCAL based on RPC

- **ANL (J. Repond, L. Xia et.al.)**
  $1m^3$, 1 threshold, TB at CERN/Fermilab
- **IPNL (I. Laktineh et.al.)**
  $1m^3$, 3 thresholds, TB at CERN since 2012





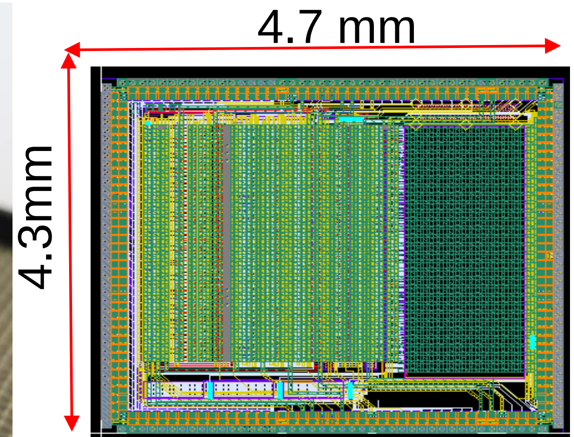
80 GeV Pion



Readout Electronics for RPC

Imad Laktineh (IPNL)

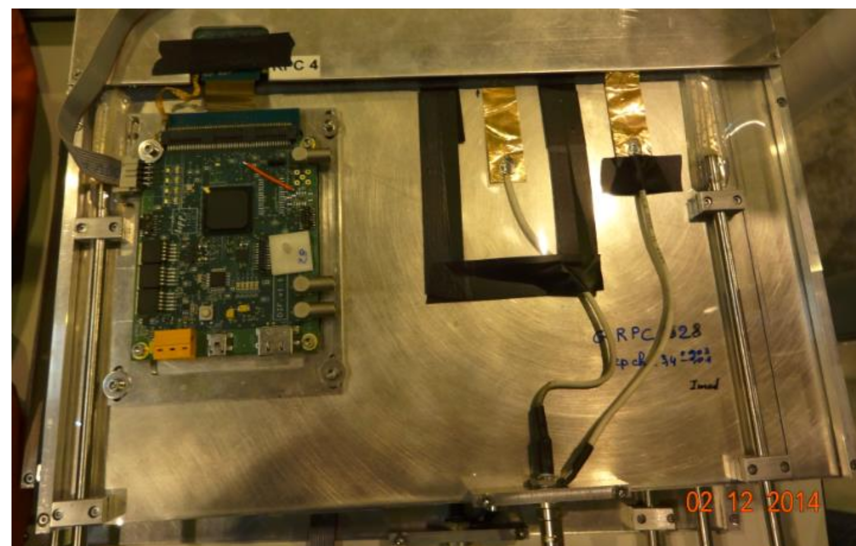
ASICs : HARDROC2
64 channels
Trigger less mode
Memory depth : 127 events
3 thresholds
Range: 10 fC-15 pC
110fC, 5pC, 15pC
Gain correction → uniformity



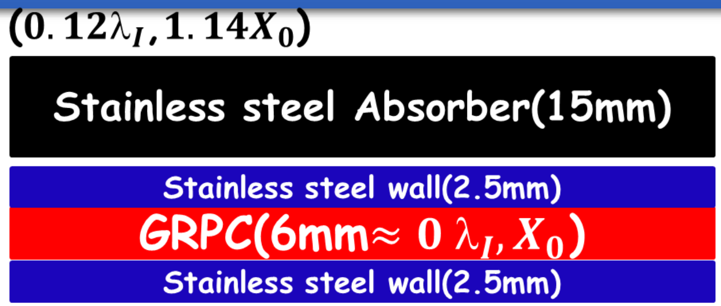
Printed Circuit Boards (PCB) were designed to reduce the cross-talk with 8-layer structure and buried vias.

Tiny connectors were used to connect the PCB two by two so the 24X2 ASICs are daisy-chained. 1×1m^2 has 6 PCBs and 9216 pads.

DAQ board (DIF) was developed to transmit fast commands and data to/from ASICs.

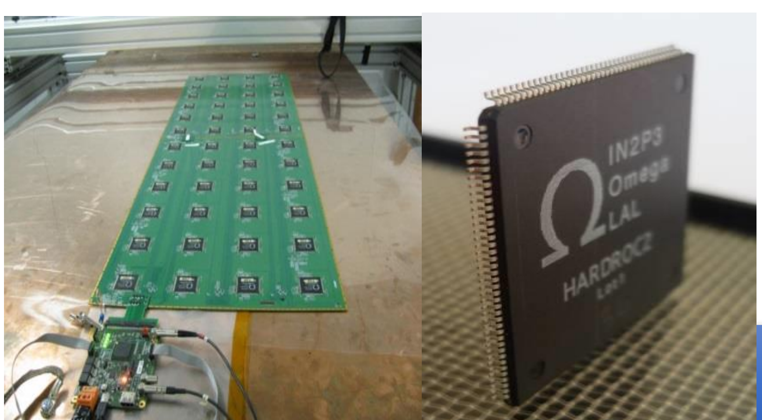


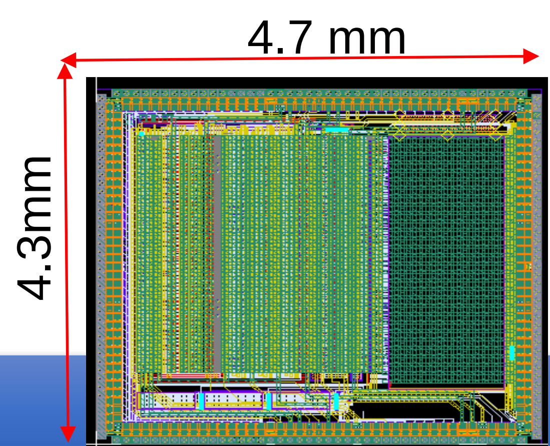
Electronics channels / m^2



- ➔ SDHCAL for CEPC has 40 layers
- ➔ Each layer: 3 mm RPC
  + 1.2 ~ 1.4 mm PCB
  + 1.6 mm ASIC (Hardroc)
- ➔ 20mm steel absorber (2.5+2.5+15mm)

- ➔ 6 PCB to cover $1m^2$ RPC
- ➔ Each PCB size: 31 cm * 50cm ~ 1536 channels
- ➔ Each ASIC chip (Hardroc) has 64 channels, size 4.3mm*4.7mm
- ➔ Each PCB with 1536-channel needs 24 ASIC chips (4*6)
- ➔ Power: 1.4mW/ch * 64 ch = 90 mW/Chip
- ➔ Power: 1.4mW/ch * 6*24*64 ch = 1.4mW/ch*9216ch/m^2 = 13W/m^2

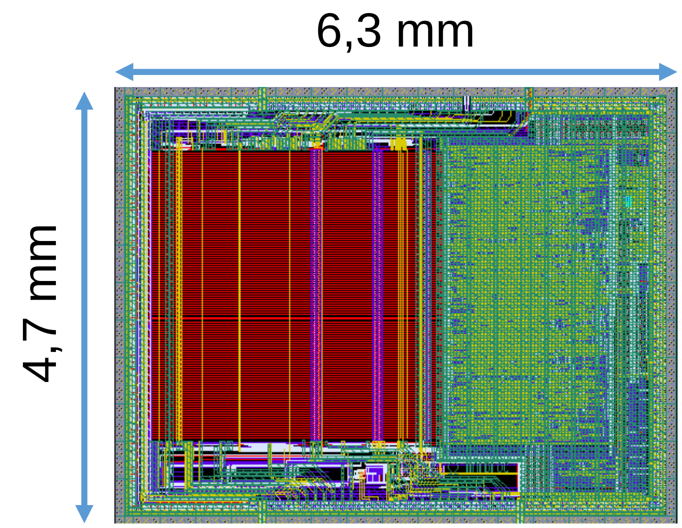




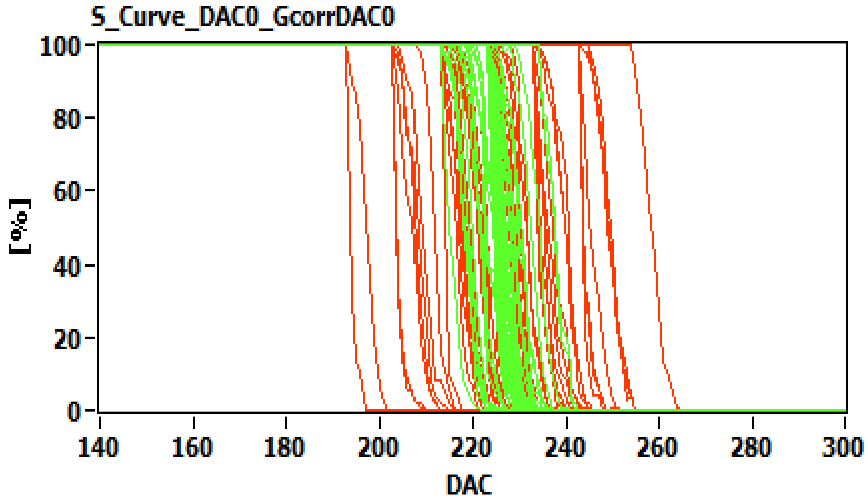
New Electronics: ASIC

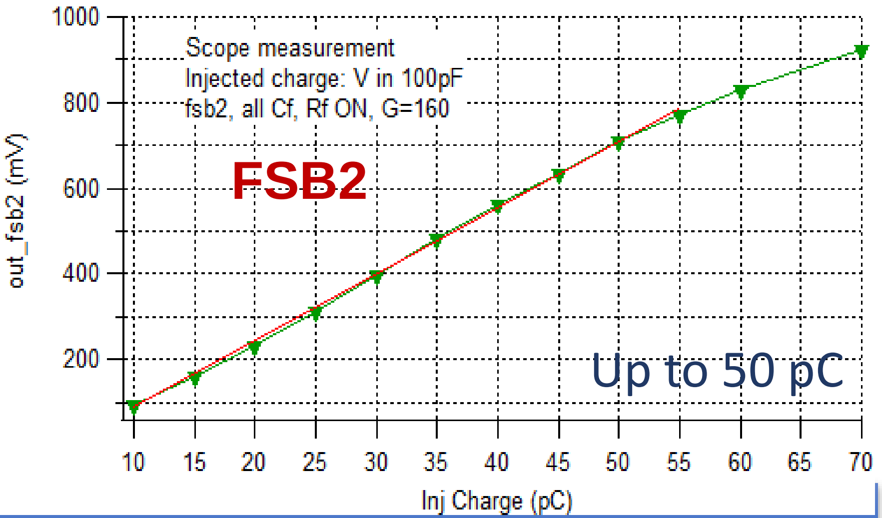
HARDROCR3 main features:

- Independent channels
- Zero suppress
- Extended dynamic range (up to 50 pC)
- I2C link with triple voting for slow control parameters
- packaging in QFP208, die size ~30 mm^2
- Consumption increase (internal PLL, I2C)



H3B TESTED : 786, Yield : 83.3 %





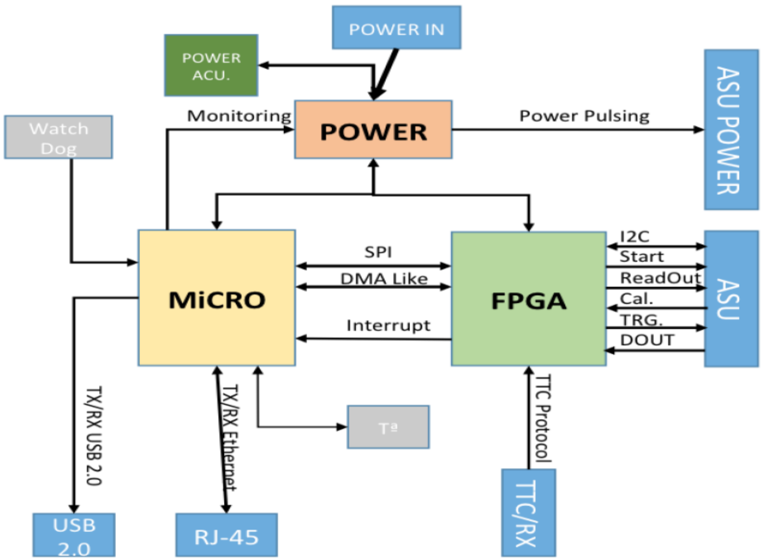
ASU (Active Sensor Unit)

One important challenge is to build a PCB up to 1m length with good planarity to have a homogeneous contact of pads with RPCs in order to guarantee an uniform response along all the detector. After investigation in some companies, ***1x0.33 m2 with 13 layer ASUs*** have been built.

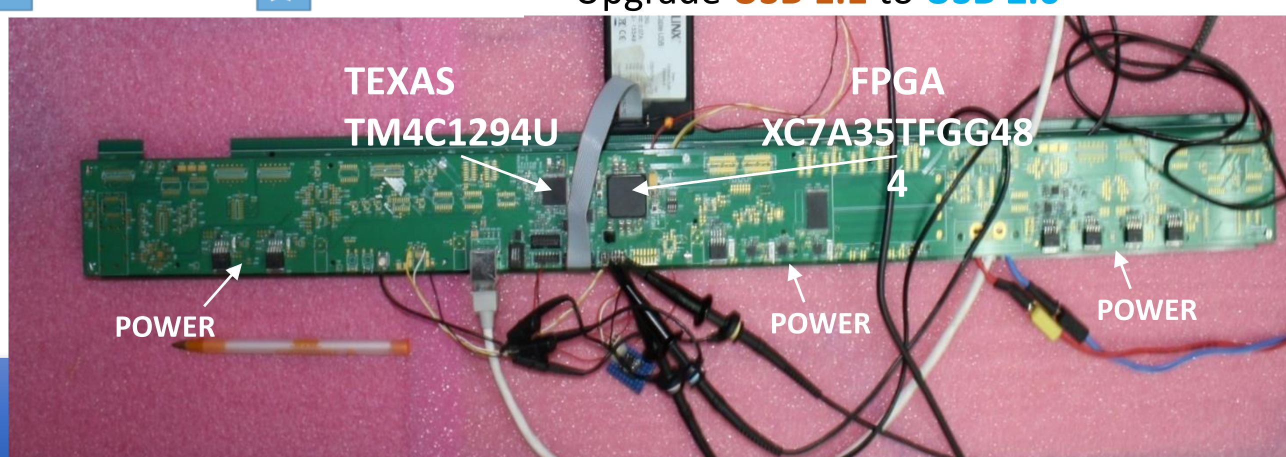
The ASU-ASU (= ASU-DIF) connections also produced

New Electronics: DIF

DIF sends DAQ commands (config, clock, trigger) to front-end and transfer their signal data to DAQ. It controls also the ASIC power pulsing



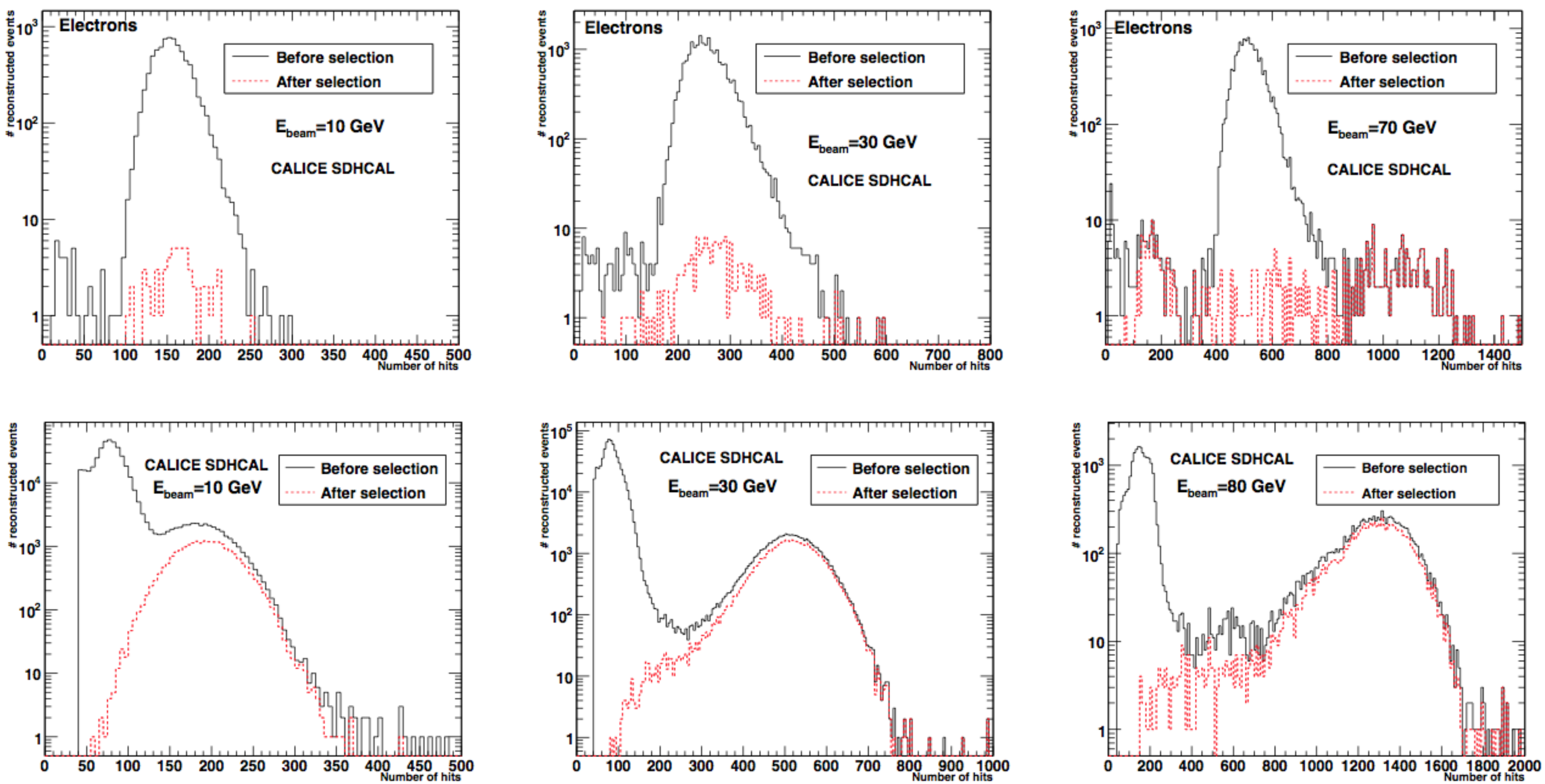
- Only **one DIF per plane** (instead of **three**)
- DIF handle up to **432 HR3 chips** (vs **48 HR2** in previous DIF)
- HR3 **slow control** through **I2C bus (12 IC2 buses).** Keeps also **2 of the old slow control buses as backup & redundancy**.
- **Data transmission to/from DAQ** by **Ethernet**
- **Clock and synchronization** by **TTC** (already used in LHC)
- **93W Peak power supply** with super-capacitors (vs **8.6 W** in previous DIF)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- Upgrade **USB 1.1** to **USB 2.0**



Event Selection of Hadron Beams

Electron rejection	Shower start ≥ 5 or $N_{layer} \geq 30$
Muon rejection	$\frac{N_{hit}}{N_{layer}} > 2.2$
Radiative muon rejection	$\frac{N_{layer} \backslash RMS>5cm}{N_{layer}} > 20\%$
Neutral rejection	$N_{hit \in First\ 5\ layers} \geq 4$

- No containment selection.
- No Cerenkov detector
- Triggerless mode
- Power pulsed mode



Energy Reconstruction (χ^2)

JINST 11 (2016) P04001

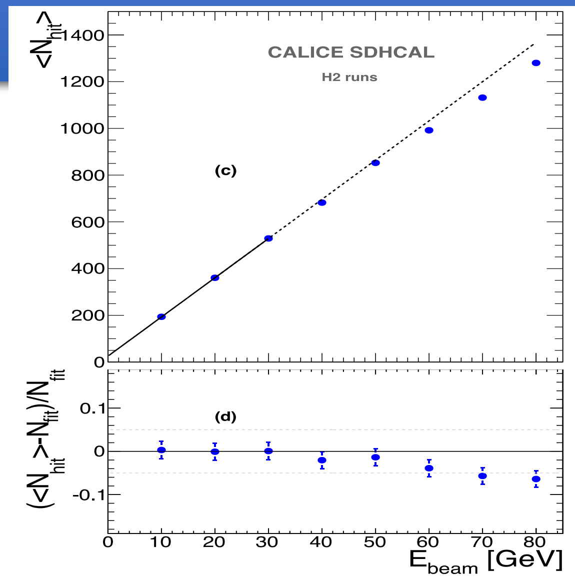
$$E_{rec} = \alpha \times N_1 + \beta \times N_2 + \gamma \times N_3 \qquad (1)$$

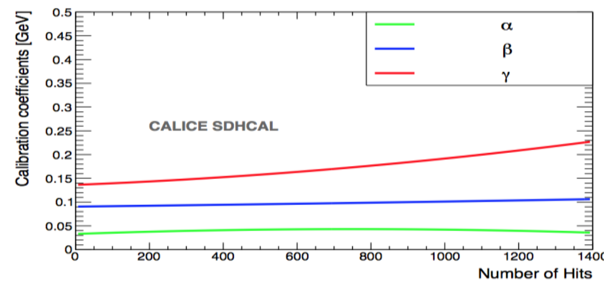
where α, β and γ are three weight parameters treated as a function of the total hits counted with notation N_{total}, in which $N_{total} = N_1 + N_2 + N_3$. And we extend relations between these parameters and N_{total} to second order polynomial as:

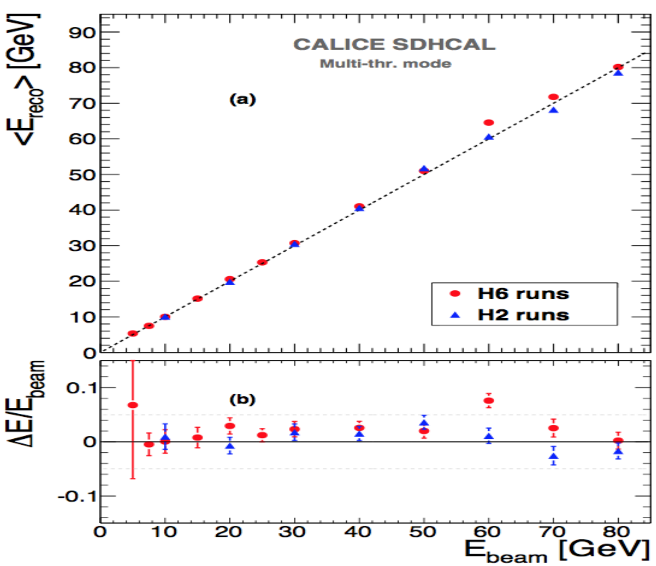
$$\begin{aligned} \alpha &= \alpha_1 + \alpha_2 \times N_{total} + \alpha_3 \times N_{total}^2 \\ \beta &= \beta_1 + \beta_2 \times N_{total} + \beta_3 \times N_{total}^2 \qquad (2) \\ \gamma &= \gamma_1 + \gamma_2 \times N_{total} + \gamma_3 \times N_{total}^2 \end{aligned}$$

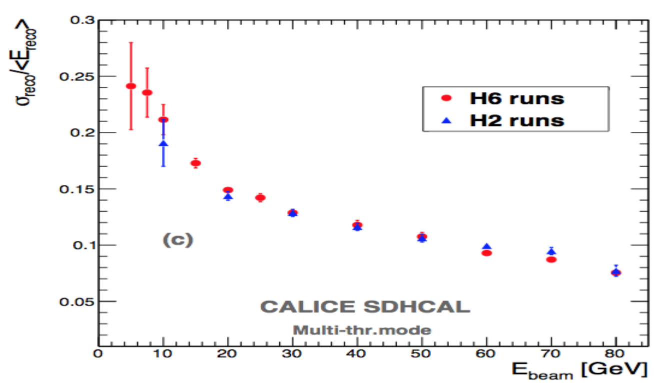
We can obtain nine parameters from the simulated samples by minimizing the χ^2 function, which reads:

$$\chi^2 = \sum_{i=1}^{N} \frac{(E^i_{beam} - E^i_{rec})^2}{\sigma_i^2} \qquad (3)$$

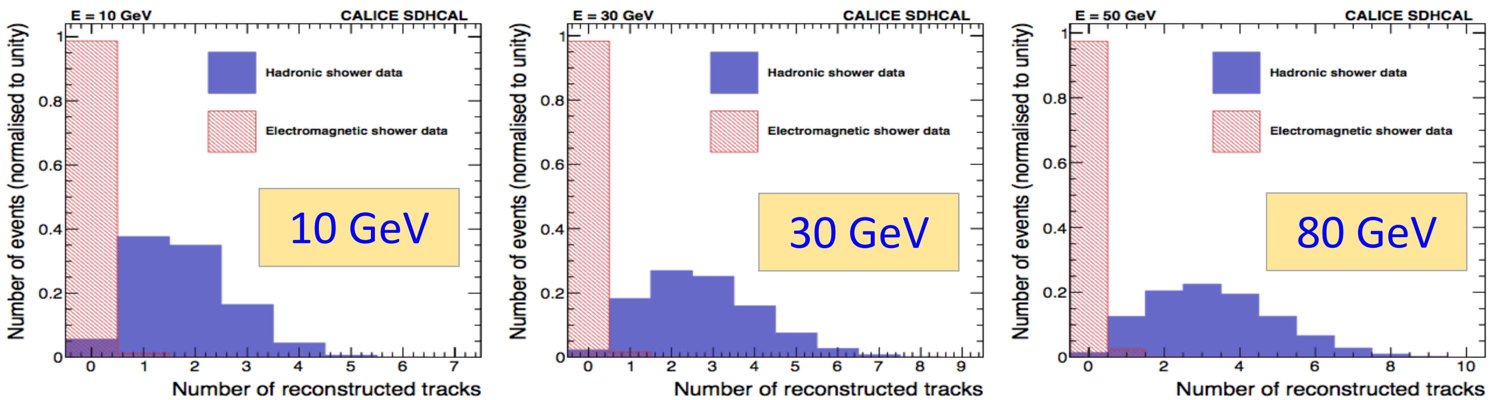




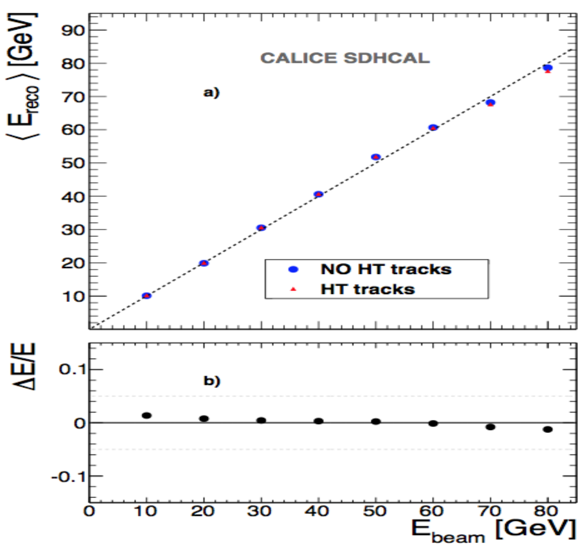


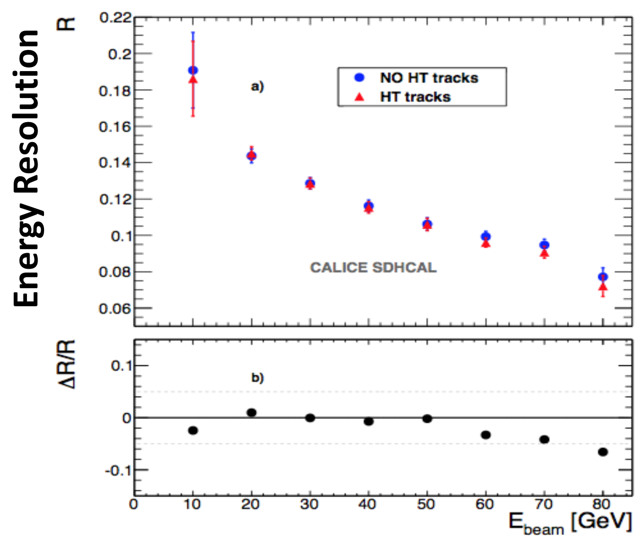


Separation of electron/hadron



It improves on the **energy reconstruction** by dealing with the hits belonging to the track segments independently of their threshold.





The technique could be extended to hadronic showers in magnetic field.

JINST 12 (2017) P05009

Arbor PFA

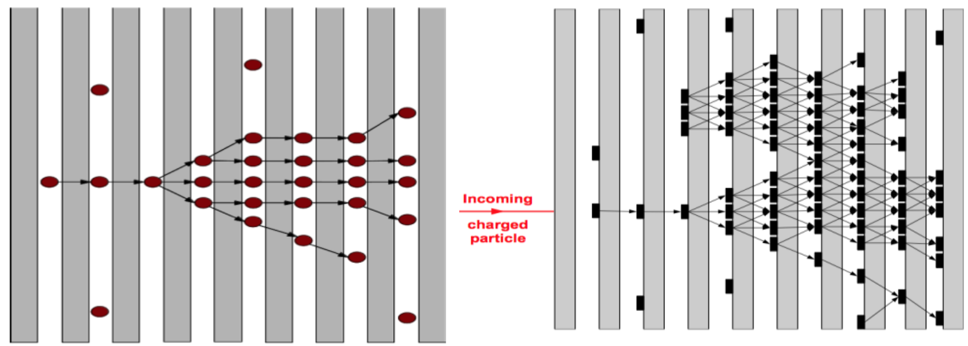
CALICE note CAN054

SDHCAL high granularity is desirable

It helps to optimize the connection of hits belonging to the same shower by using the topology and energy information

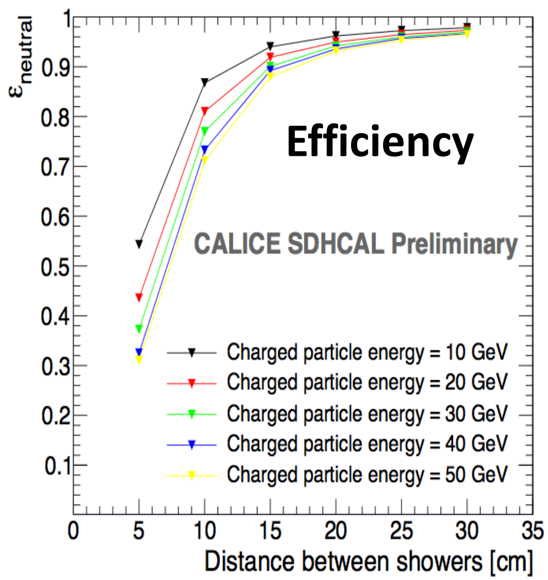
ArborPFA algorithm:

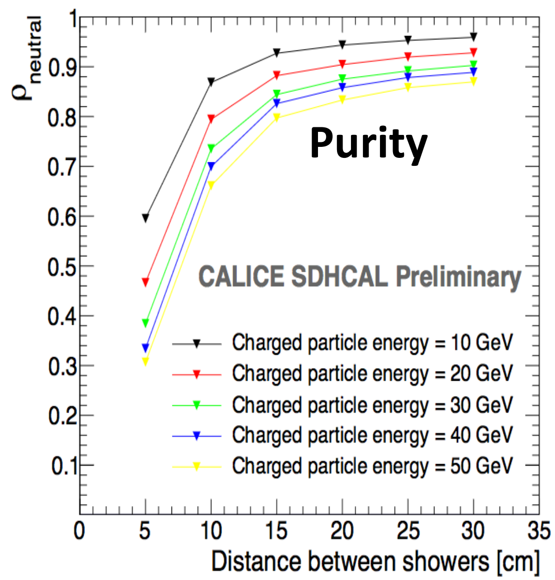
It connects hits and clusters using distance and orientation information, then correct tracker momentum information.

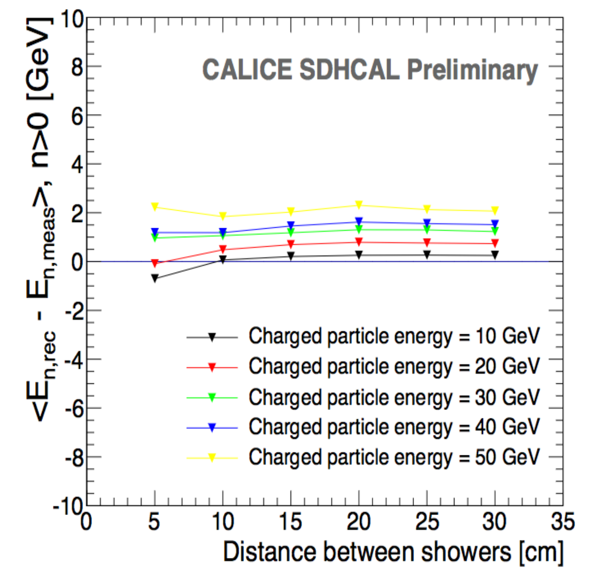


$$\epsilon = \frac{Nhit_{good}}{Nhit_{ini,tot}}$$

$$\rho = \frac{Nhit_{good}}{Nhit_{rec,tot}}$$







Pion eff. vs Backgrounds eff.

- For same Pion efficiency, we compare electron & muon efficiencies from "simple cut" and "BDT" methods.
- BDT has modest improvement for electron suppression and significant improvement for muon suppression.

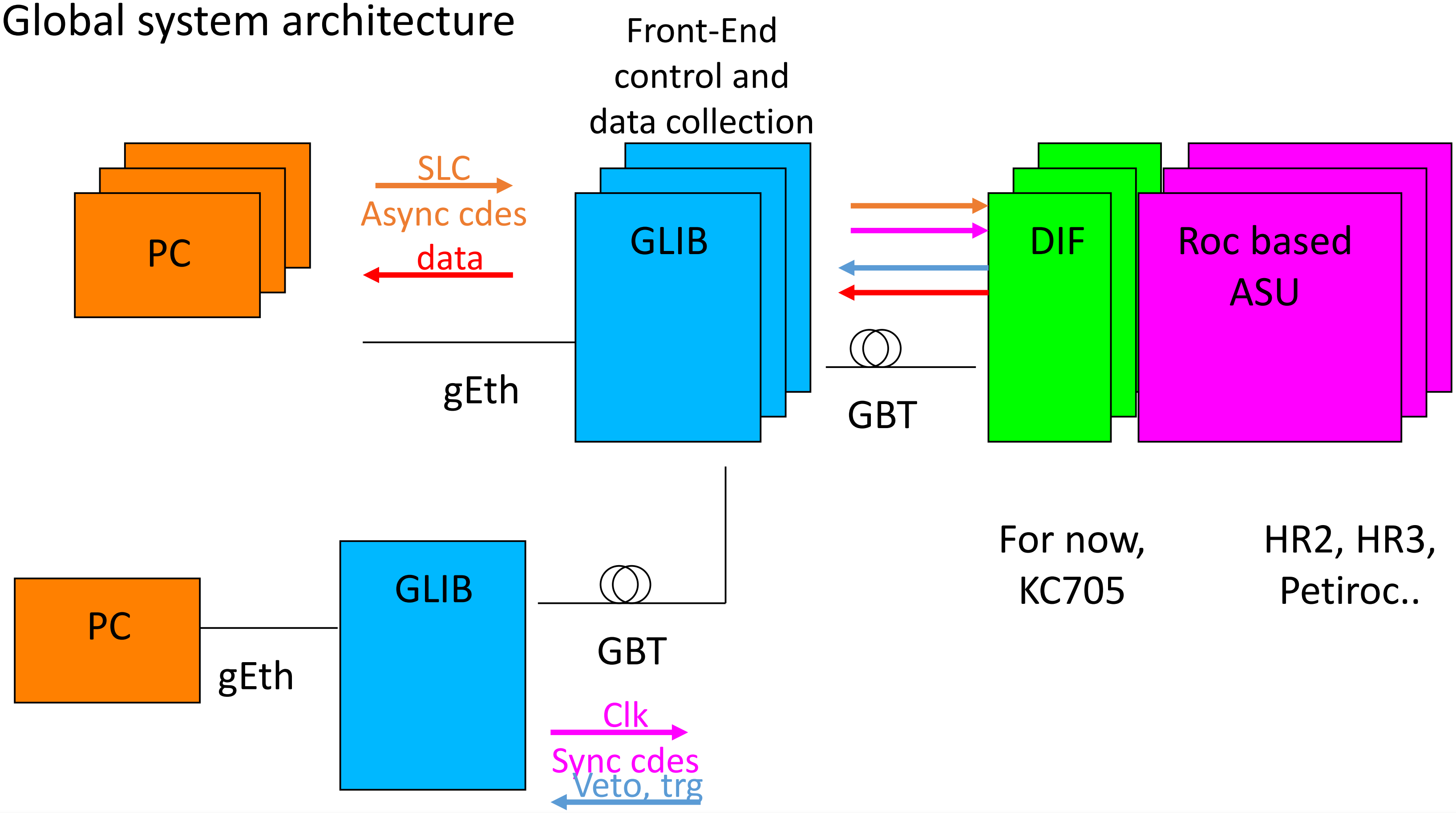
Energy	simple cut			BDT		
	eff_{pion}	$eff_{electron}$	eff_{muon}	eff_{pion}	$eff_{electron}$	eff_{muon}
10GeV	55.7%	0.0%	0.1%	55.7%	0.0%	0.0%
20GeV	70.5%	0.0%	0.3%	70.5%	0.0%	0.0%
30GeV	80.9%	0.0%	0.6%	80.9%	0.0%	0.1%
40GeV	87.2%	0.1%	0.6%	87.2%	0.0%	0.1%
50GeV	90.6%	0.1%	0.9%	90.6%	0.1%	0.1%
60GeV	93.0%	0.2%	1.0%	93.0%	0.2%	0.2%
70GeV	94.7%	0.3%	1.2%	94.7%	0.2%	0.2%
80GeV	95.7%	0.3%	1.1%	95.7%	0.2%	0.2%

CALICE note CAN059

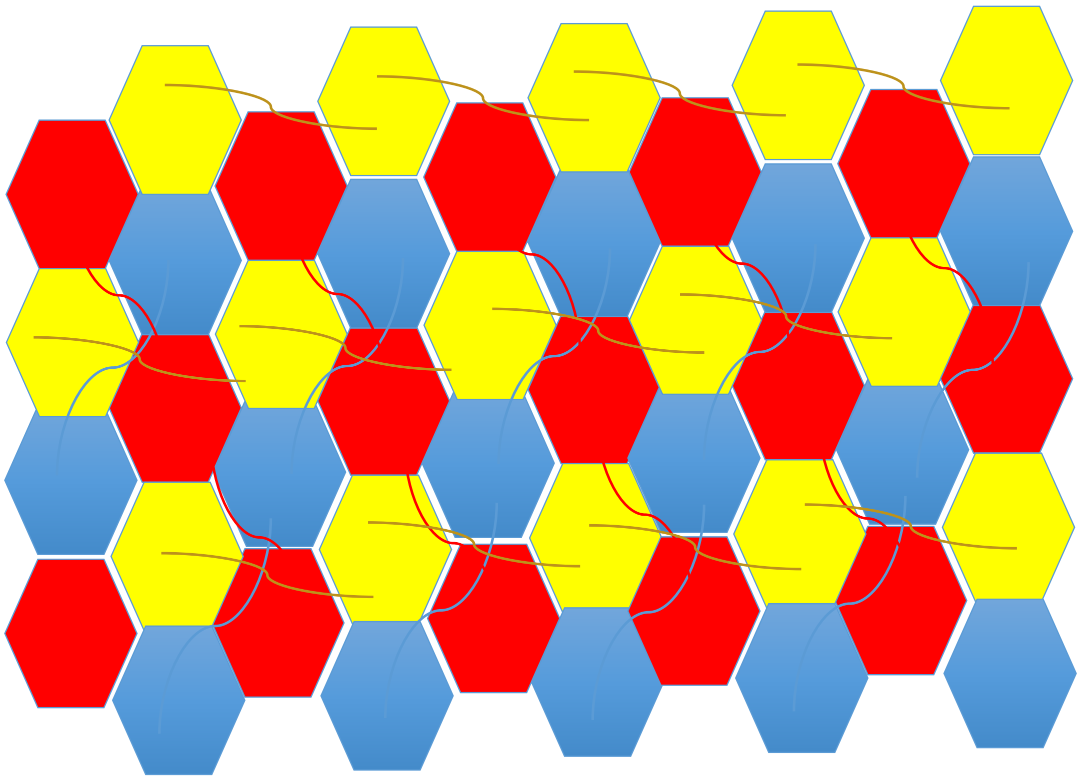
DAQ System

Implementation of a GBT-based communication system for ROC chips. This aims to reach higher performance using robust and well maintained system in the future

Global system architecture



New PCB Design



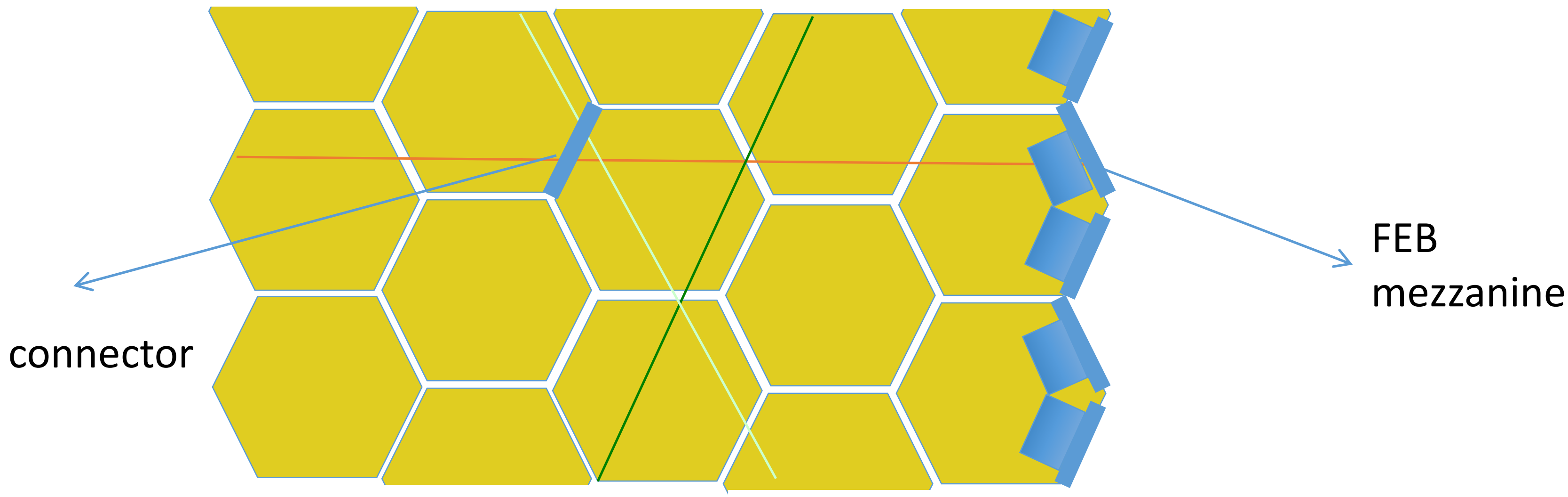
- ❑ Several shapes of pixels/pads can be used: triangles, lozenges, pentagons, hexagons the most convenient is the triangular shape
- ❑ The pixel/pad size should be a slightly smaller to charge extension to feed at least two
- ❑ Having 3 or more directions allow one to eliminate ambiguities (ghost particles)

Ongoing work

How to build larger PCB?

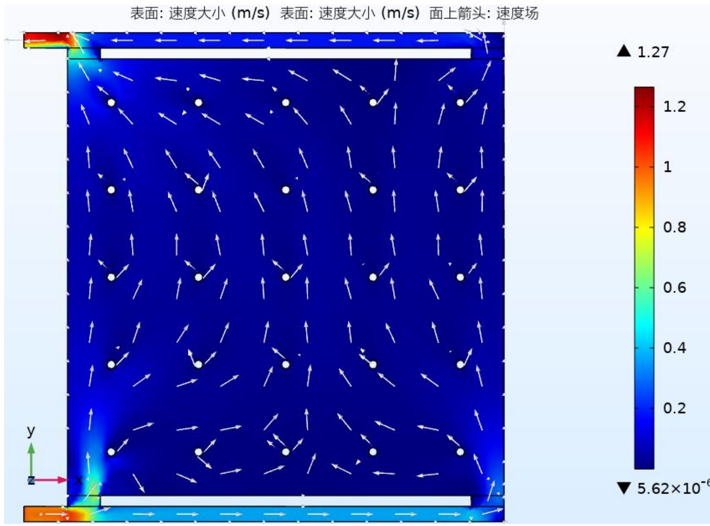
Using PCB-unit, A PCB-unit will be equipped with connectors allowing:

- ❑ Either to connect two PCBs
- ❑ Or to plug a mezzanine that host the ASICs and the DIF's FPGA as well as Ethernet or wireless communication protocols

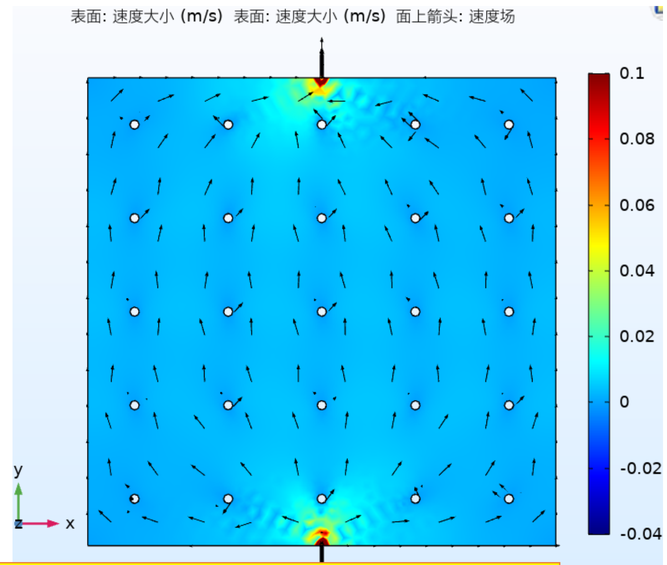


The connector should have a low inductance. In this case long strips of several meters (maybe tens of meters) could be used as far as the signal reduction is acceptable. This will represent a huge reduction of electronic channels.

More Gas Flow Simulation



In Progress



to optimize RPCs gas distribution system