ATLAS High Granularity Timing Detector (HGTD)

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Organization issues

- Need to organize for new TDR timescale
  - Critical issues to be addressed
  - We are essential for the successful approval of HGTD
- New email list: atlas-hgtd-ihep@mailist.ihep.ac.cn
  - Everyone from IHEP HGTD should be on this email list
- New location for HGTD meetings:
  - https://indico.ihep.ac.cn/category/67/
  - Need module and sensor meetings
  - Regular common meeting?

Projects to work on (email from 3 weeks ago)

- **1) Bump bonding tests and ALTIROC1 chips.**
  - USTC might do this with dummies but we were asked to make tests with our BB company using real chips. There are chips and sensors at IHEP already. We need someone to volunteer to organize and pursue this.
  - Timescale: Now
- **2) Review and possible update of flex cable.**
  - Currently there are many versions of modules because they are attached to different length cables. This is really undesirable and Sebastian would like to try to make things uniform. This means, we could look into having one single common module design, plus a connector that would connect to flex cables of different length. There are also issues related with the design, number of layers, cost, etc... People working on this are not experts, so an alternative design would be welcome.
  - Timescale: Now
- **3) Dummy sensor heaters and ladders**
  - This is potentially design and build small sensors that incorporate a resistor. These sensors can mimic the real sensors and produce heat. We can use these to study the module assembly, ladder assembly and cooling. This is an important step in the design and somewhat cool. We would need a person to lead this. The work could be done together with Barcelona.
  - Timescale: Start soon. The earlier the better.
- **4) DAQ for ALTIROC2**
  - Develop a simple DAQ system based on FPGA for testing of the chip, and later for testing of the modules.
  - Sebastian can provide most of the firmware but the board needs to be made to work. This can also help provide input regarding the ALTIROC2 chip design.
  - Timescale: Later in the year.

Critical Issues for TDR

- Sensors

1. Ensure that irradiation tests cover the full spectrum of particle types and energies expected as a function of radius in ATLAS, including TID to 500 MRad and NIEL to 5x10^15, since LGADs may not completely follow the NIEL hypothesis. In particular, completing the irradiations up to 6x10^15 NIEL, and carrying out p irradiations for the two most promising sensor prototypes (FBK C-diffusion and HPK 3.2 B-enhanced) should be the priority, along with further comparisons of the charge collection and time resolution arising from protons compared to neutrons as a function of fluence and also beam energy. Pure TID irradiations (electrons or X-rays) may provide additional insight. Should also understand why modest over-voltages can "kill" sensors, and consider mitigations to ensure this cannot happen during HGTD construction and operation.

2. Develop R&D Plan in detail for completing sensor R&D phase (including critical date for PDR => sensor baseline). It now appears that the most promising directions are improved depth and dose for the B implants, and the addition of diffusion/implantation of C. The R&D plan needs to cover submission/characterization schedule, and how the work will be distributed across the three vendors, as well as technology convergence to common designs.

Critical Issues for TDR

- Sensors

3. Develop a procurement model and schedule. Is this a CERN procurement ? Will there be a Market Survey process (either CERN or national) ? Will only the present three vendors be included in the process (or only a subset of these vendors) ? What is the target production plan for the vendors ? Build up a schedule for the required procurement steps and use it to provide critical milestones for the sensor R&D program.

4. Develop mitigation strategies in case sensor development only allows reaching 2-3x10^15 NIEL fluences (as observed today with the most promising sensor candidates). This may include geometry changes (e.g. larger inner radius ? more frequent replacement of inner region ?) or any other relevant changes.

Critical Issues for TDR

- Modules

1. Urgently need to develop detailed thermal model of the module, both static (what will the sensor temperature be as a function of irradiated sensor leakage currents and bias voltages ?) and dynamic (is the thermal impedance from the sensor to the cooling structures low enough to avoid thermal runaway ?). This requires detailed modeling of the thermal impedance through the bump-bonded interface between the sensor and the FE ASIC - for now this could be done with IFAE bumping technology. This will define an achievable sensor temperature during operation, and ensure stable operation is possible throughout the detector lifetime. Should include the possibility that the gain reductions at high fluence observed in the present prototype sensors are improved, leading to still larger leakage current power at the highest fluences => establish significant margin.

2. This must be urgently followed by ALTIROC1 "mini-modules" (hybridization "in-house") made with 5x5 sensors, and then the ASIC+Sensor assembly needs to be irradiated (with p and n sources) and characterized in testbeams. One critical issue is to determine the time resolution (jitter) as a function of p and n fluences, as the sensor gain mechanism evolves, large sensor leakage currents appear, and the preamp performance degrades. Very significant risk remains in the project until these milestones are achieved.

Critical Issues for TDR

- Modules

3. Need to develop and execute more detailed plan for bump-bonding: identify vendors and launch prototype and qualification work, define procurement strategy (hybridization involves UBM, bump deposition, and flip-chip steps - vendors may be different), etc. Need dummy assemblies to characterize production thermal performance, as well as establish collaborative workplan with vendors.

4. Need to develop a much more detailed production plan for the ~10K modules needed - bottom-up time to assemble and test modules => number of assembly and testing sites => how much time and manpower is required to build and test ~10K modules ? Historically, the testing development is complex and requires significant specialized hardware, and the time required in production for testing is significantly underestimated.

Critical Issues for TDR

- Electronics

1. Present HGTD design relies heavily on high efficiency and low jitter measurements of charges in the range 2.5-10 fC, where the jitter performance is significantly reduced in the ALTIROC1 prototype. As the importance of the low-charge region has become clearer with the ongoing sensor R&D program, it is essential that the ASIC front-end is fully optimized for this very difficult regime. If there are further design optimizations possible, consider additional prototyping activities.

2. Need to carry out TID and NIEL testing of ASICs and assess process changes and impact on ASIC performance for existing ASICs. Results should be compared to best available device models for radiation effects. Establish impact of low-dose-rate effects and temperature/annealing effects on ASICs. Similar efforts are needed for SEU testing in order to prepare the path for ALTIROC2 SEU-hardening.

3. Strengthen the ASIC design team and appoint a lead engineer to oversee the full design effort and schedule. Increase emphasis on critical radiation-tolerant design, especially in the digital domain, to achieve reliable performance up to the nominal 500 MRad requirement. This will require improved modeling with radiation corners for digital synthesis. The ASIC is the critical path for this project for the foreseeable future and must receive the highest priority. Without a stronger team, the required schedule will not be reliably achieved.

Critical Issues for TDR

- Electronics

4. The detailed specifications for the ALTIROC2 final prototype ASIC are urgently needed. They will then be reviewed in a Specification review, leading to a PDR before submission. A detailed schedule for all of the components of this submission is urgently needed. This ASIC will be the equivalent of the RD53A ASIC for the ITk Pixel project, and must include essentially all of the features of the final design, and must undergo extensive verification before submission to ensure a very high quality ASIC.

5. A detailed overall grounding and powering plan is needed for the full electronics system of HGTD. There should be an overall electronics coordinator for the project with extensive experience in large and complex electronics systems. A technical review of this area should be carried out in the near future.

Critical Issues for TDR

- Demonstrator

1. Critical to launch this activity based on fabrication of a significant number of ALTIROC1 "mini-modules" and taking them through a comprehensive characterization process. Then a larger scale ALTIROC2 program will be needed (should be order of 100 modules or more), before proceeding to pre-production. Appropriate infrastructure and test systems must be developed for each step of this plan (this should also include the probe-station testing of the FE ASICs). Larger scale plans for system test (first stave-like or disk-like multi-module systems) and surface commissioning (qualifying large fractions of HGTD in dedicated surface test setup to ensure HGTD works in ATLAS) are needed. The time required along with infrastructure, space, and components needed to be factored into the project planning (cost, schedule, resources).

Critical Issues for TDR

- Global

1. In general for a TDR, there should be a modest number of "options", where a decision between two competing options will be made later in the project after more R&D. However, it is essential that for each of the option areas that a baseline has been defined, which can then be evaluated for cost, schedule, risk, etc. A key goal for the TDR is then to provide all available information to demonstrate that the baseline is technically feasible.

2. Current plan for review milestones needs to be updated: dates for ASIC reviews are not credible, and all other milestones need to be synchronized. Need to include specification reviews as well. ATLAS should consider inserting "Intermediate Design Reviews", similar to those used for the ALTIROC ASICs, into the schedule for other critical areas discussed above (sensors, modules, grounding and powering, etc.) This can help transfer decades of expertise from ITk experts into the HGTD project.

3. It is essential to begin the preparation of the UCG material. The key components are detailed costing with BoE back-up documentation, detailed schedules for each WBS area, including all necessary cross-links to capture dependencies between tasks, WBS-level assessments of required and available manpower per year, and detailed risk analysis including cost, schedule, and technical risks. The TDR review process and the UCG review process are coupled in a combined review, and the UCG material needs to be available roughly 4-6 weeks after the TDR submission.

Summary

Summary

1. In several key areas, these demonstrations are incomplete (sensors which meet fluence requirements, ASICs which meet dose requirements, modules which meet requirements after testing with full TID/NIEL).

2. Tentative proposal for work towards TDR and UCG Material:

- Sensors: Items 1-4 should be largely completed with the priorities given above.
- Electronics: Items 1 and 3 should be largely completed and item 2 should be advanced with detailed planning

- Modules: Item 1 must be completed, item 2 should be well-advanced with initial results, items 3 and 4 need to be advancing with a clear plan and overview.
- Demonstrator is largely a planning exercise plus good progress on modules item 2.
- Global: Items 2 and 3 are critical for the UCG Review, and item 1 is a reminder of the primary goals for a TDR.

HGTD LHCC/UCG Review process:

Conclusions: propose to delay TDR/UCG material submission dates by ~6 months (early Oct TDR submission, UCG submission ~2 weeks before 18 Nov LHCC Week) in order to address TDR concerns and develop detailed UCG material. Anticipated approval would then be in Mar 2020.

- Proposed new dates:
  - ✦ TDR Approval @ USC, EB: September 26, 27
  - ✦ **TDR Submission: September 30/October 1st**
  - ✦ **LHCC Kickoff: October 26 (Vidyo, afternoon)**
  - ✦ LHCC Iteration: Nov 10 (Vidyo, afternoon)
  - ✦ *LHCC iteration 2 (if needed): Nov 22 (Vidyo, afternoon)*
  - ✦ LHCC Review: Dec 4 (CERN, morning)

  - ✦ **UCG Package submission: Nov 16**
  - ✦ UCG Kickoff: Dec 6 (CERN, afternoon)
  - ✦ UCG Iteration: Jan 16 (Vidyo, afternoon)
  - ✦ *UCG Iteration 2 (if needed): Jan 29 (Vidyo, afternoon)*
  - ✦ UCG Review: February 24-25
  - ✦ *LHCC Week: March 2 (TBC)*
  - ✦ *Research Board: March 9 (TBC)*

Previous TDR Schedule

HGTD LHCC/UCG Review process:

- **Original dates confirmed by F. Simon:**
  - **TDR Submission: April 5 ok**
  - **LHCC Kickoff: April 26 (Vidyo, afternoon)**
  - LHCC Iteration: May 10 (Vidyo, afternoon)
  - *LHCC iteration 2 (if needed): May 22 (Vidyo, afternoon)*
  - LHCC Review: June 4 (CERN, morning)

  - **UCG Package submission: May 16**
  - UCG Kickoff: June 6 (CERN, afternoon)
  - UCG Iteration: July 16 (Vidyo, afternoon)
  - *UCG Iteration 2 (if needed): July 29 (Vidyo, afternoon)*
  - UCG Review: September 9 and 10 (CERN, plenary 09.09 late morning, parallel & closeout 10.09 morning)
  - *Research Board: September 18*

HGTD Schedule in ATLAS

HGTD schedule (Figure 64 of TP)