Research of high precision time measurement electronics

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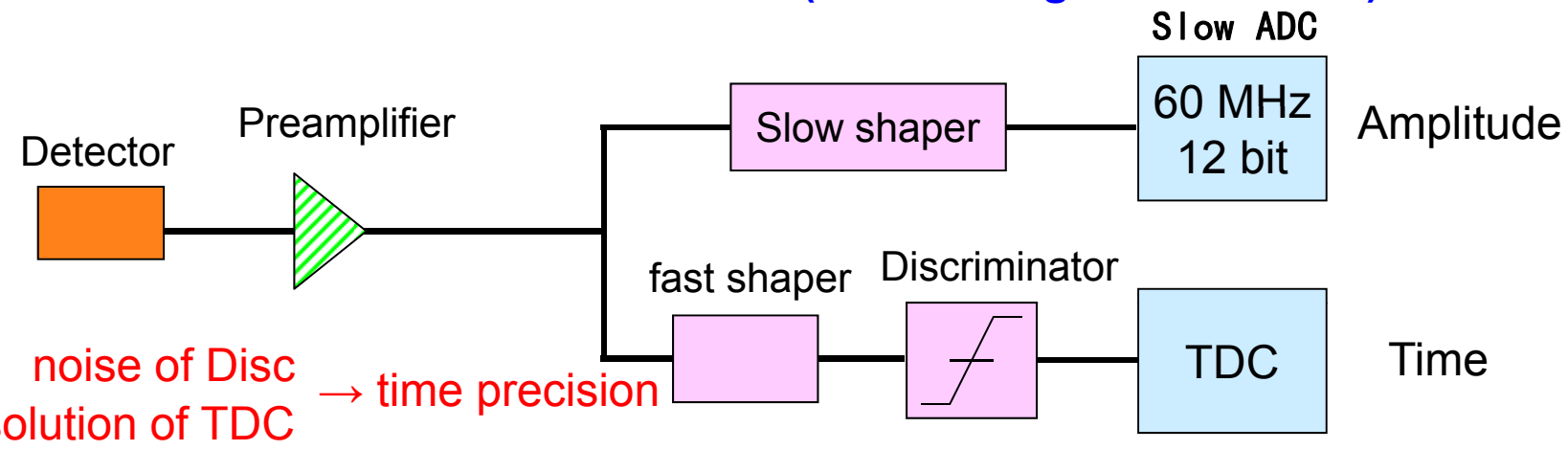
Contents

- Methods for time measurement
- Method 1: discrimination + TDC
- Method 2: waveform digitization based on SCA
  - verification based on TARGET7
  - verification based on DRS4
  - verification using another time calibration method
- Design of a 16 chl waveform digitizer for nMRPC

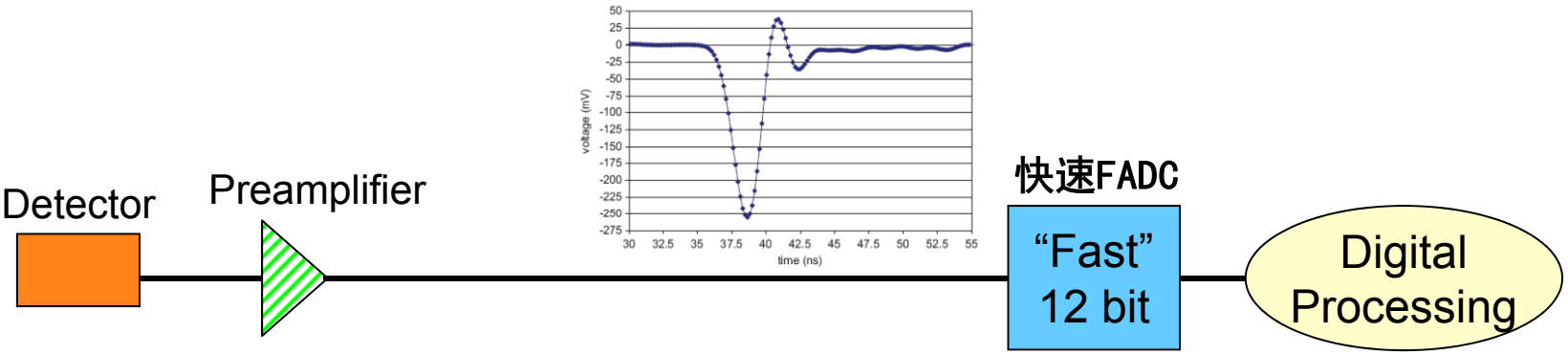
Two methods for time measurement

Method 1: Time discrimination + TDC(Time-to-Digital Converter)



noise of Disc
resolution of TDC → time precision

Method 2: Waveform digitization + Digital processing



Flash ADC → Power consumption, density, cost

→ Switched Capacitor Array (SCA)

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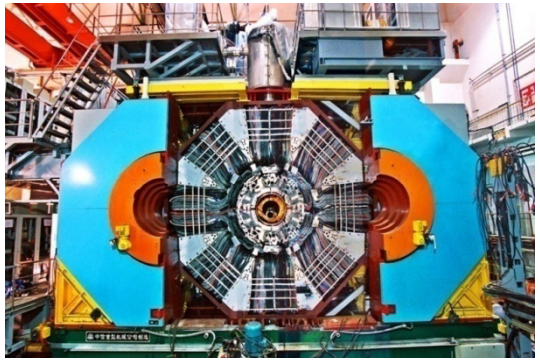
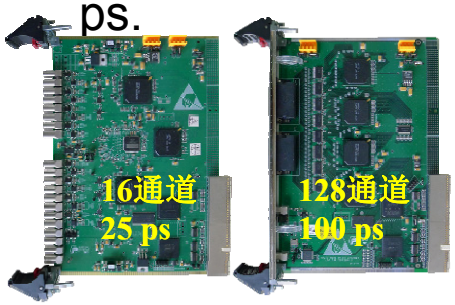
Time measurement in two projects

- In BESIII，the readout electronics of the Time-Of-Flight (TOF) detector is based on discrimination and HPTDC, and achieves a time resolution of better than 25 ps.

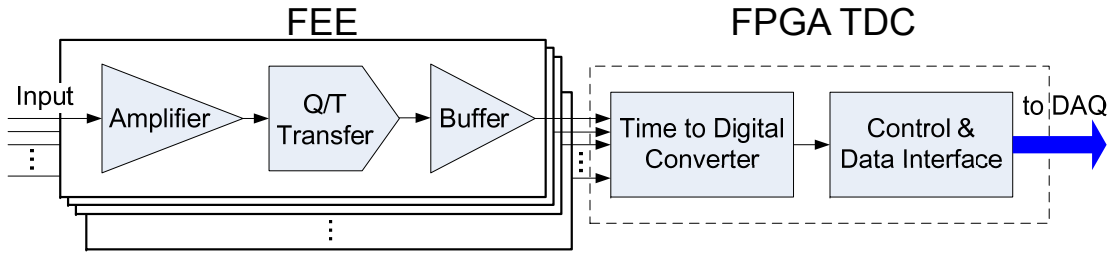


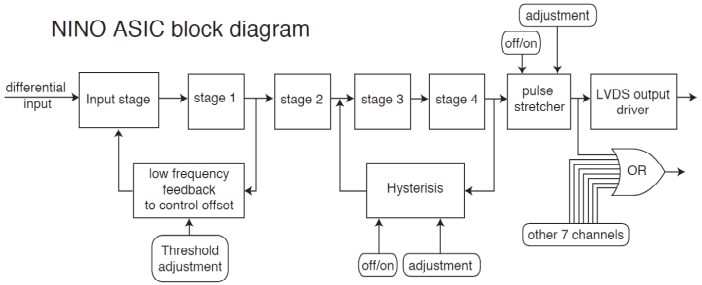
- In the readout electronics of the external target experiment of CSR in Heavy Ion Research Facility in Lanzhou (HIRFL), time measurement is also based on discrimination and TDC. Time resolution of the electronics is better than 25 ps.

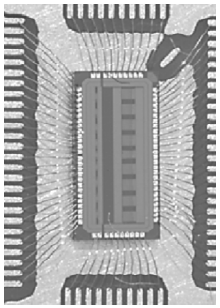


探测器	通道数	单模块通道数	时间精度
MWDC	3000	128	100 ps
TOF Wall	360	16	25 ps
Neutron Wall	504	16	25 ps

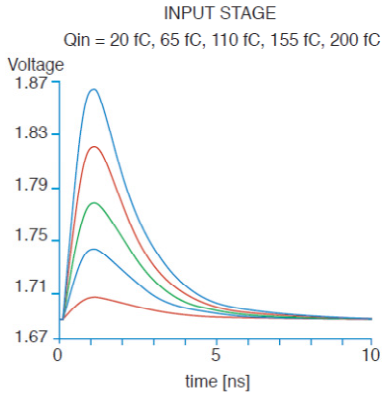
MPRC readout based on NINO+TDC

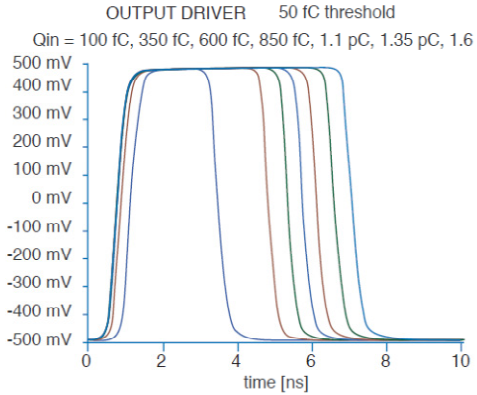


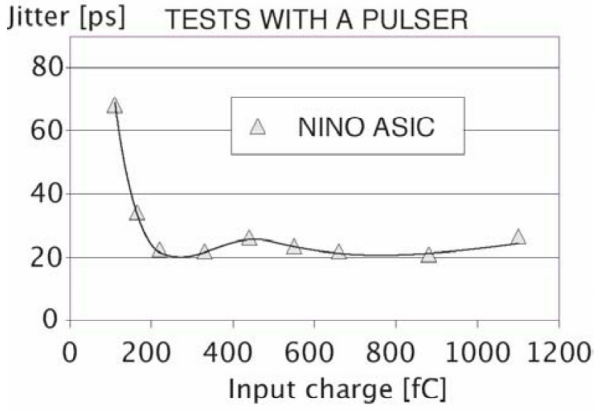




Parameter	Value
Peaking time	1ns
Signal range	100fC-2pC
Noise (with detector)	< 5000 e- rms
Front edge time jitter	< 25ps rms
Power consumption	30 mW/ch
Discriminator threshold	10fC to 100fC
Differential Input impedance	40Ω< Zin < 75Ω
Output interface	LVDS



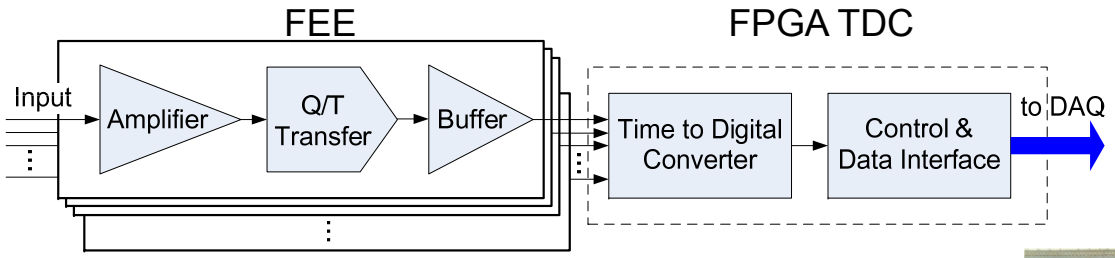


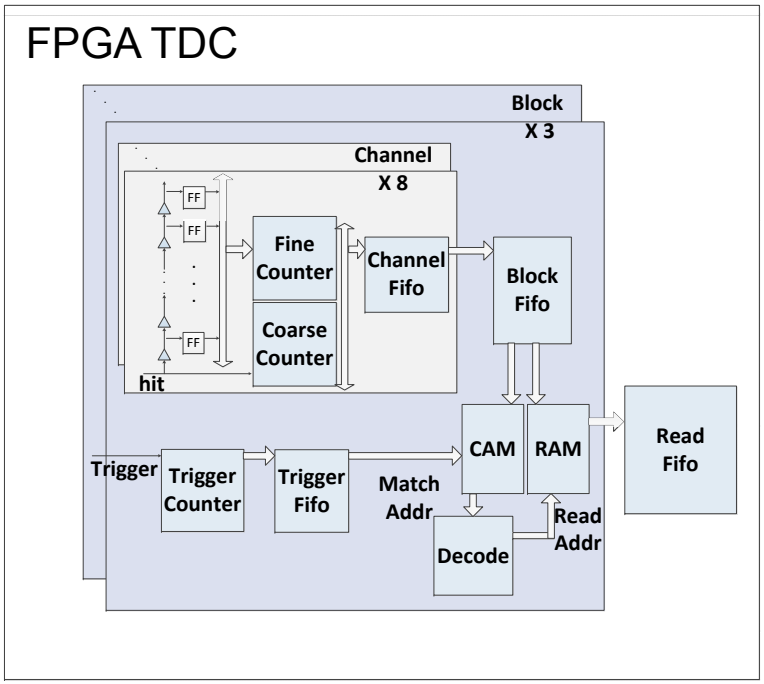


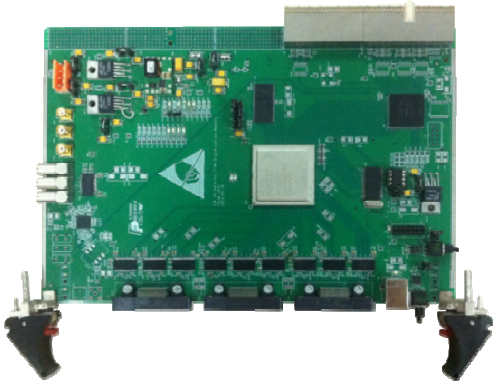
By F. Anghinolfi, et. al.

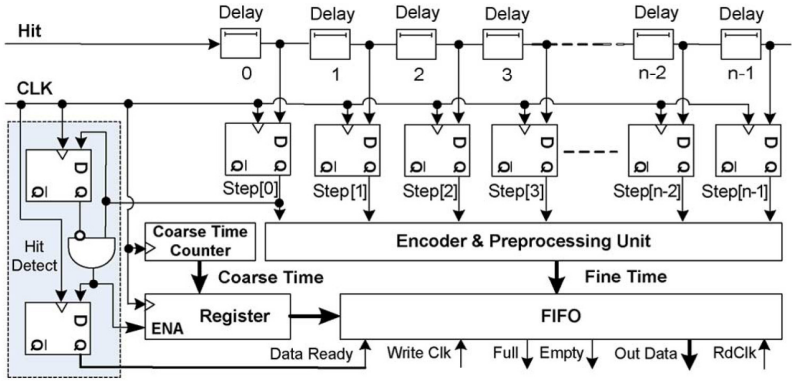
MPRC readout based on NINO+TDC

Readout electronics of External Target Experiment of CSR in HIRFL

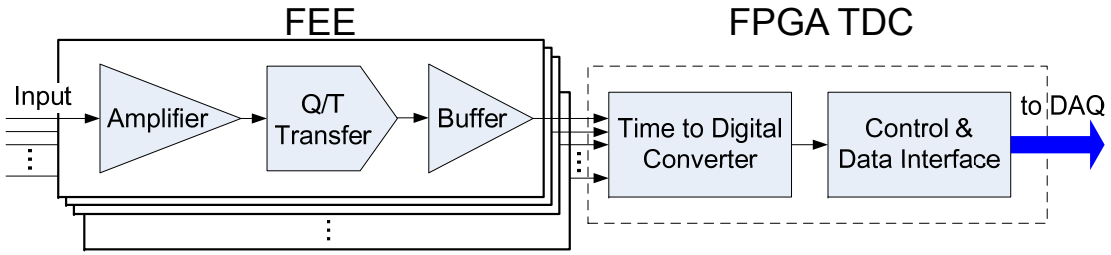


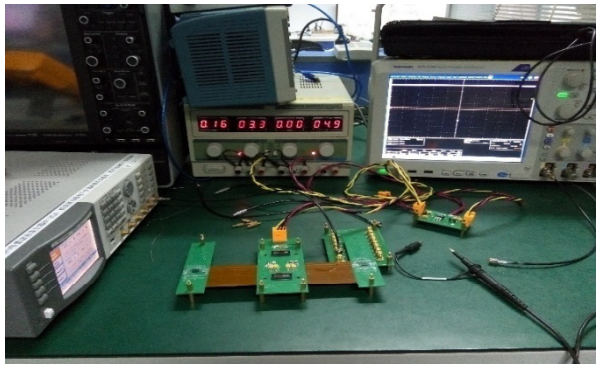


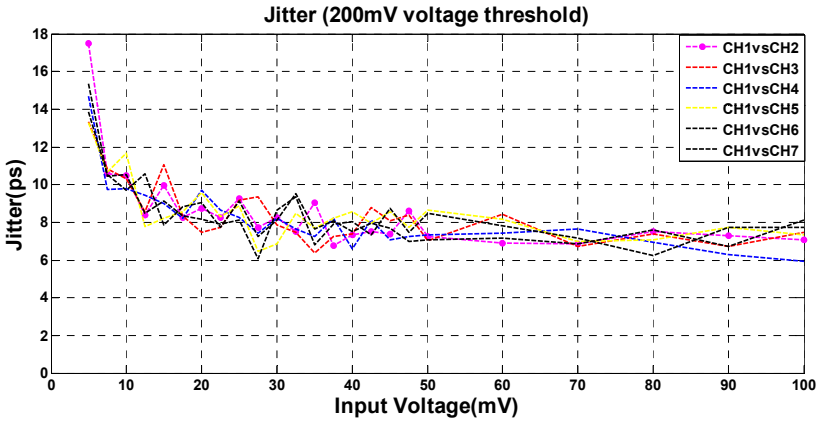


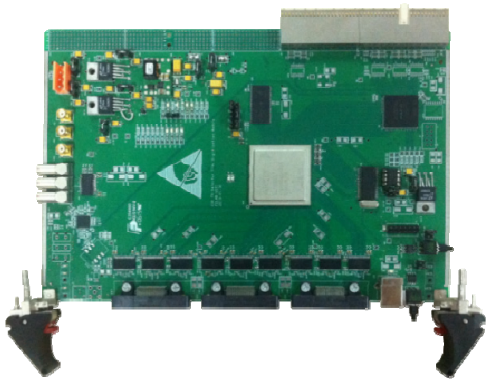


MPRC readout based on NINO+TDC

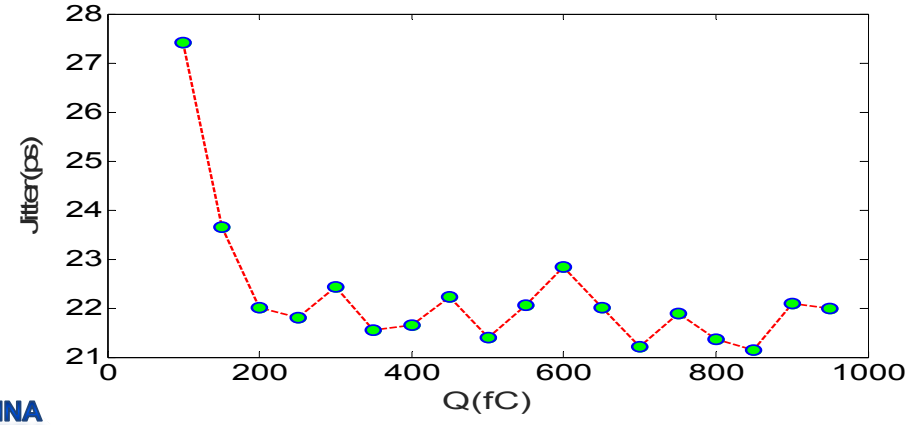




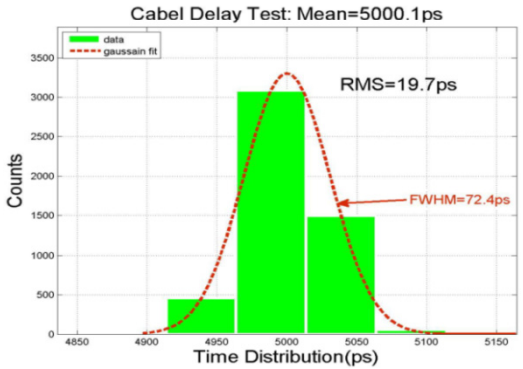




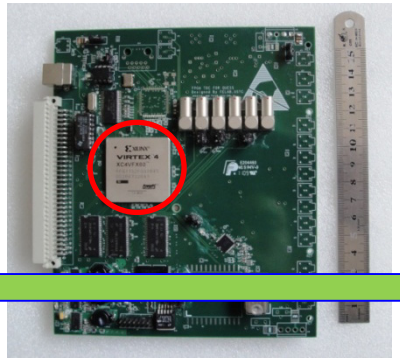
TDC bin size~30 ps, RMS ~ 20 ps

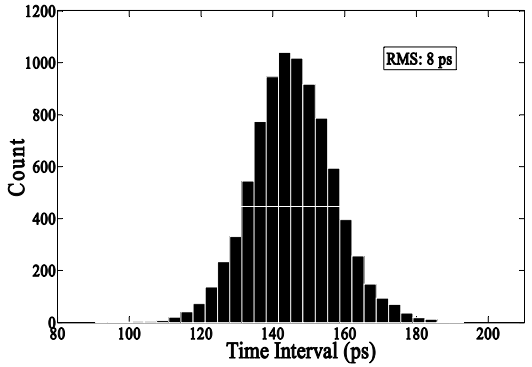


FPGA TDC Design

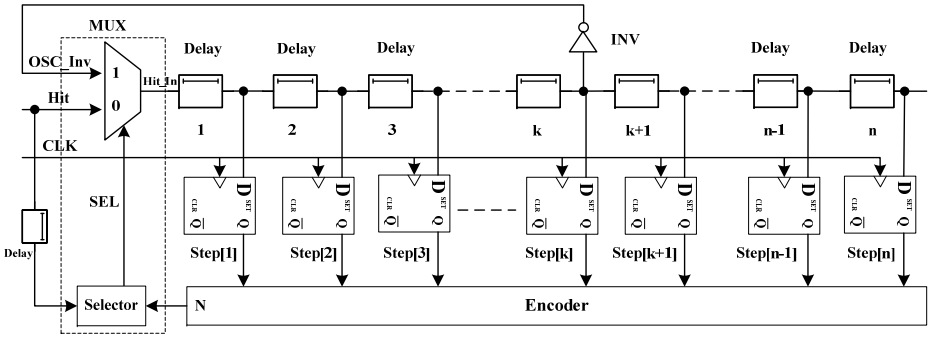


RMS ~ 25 ps





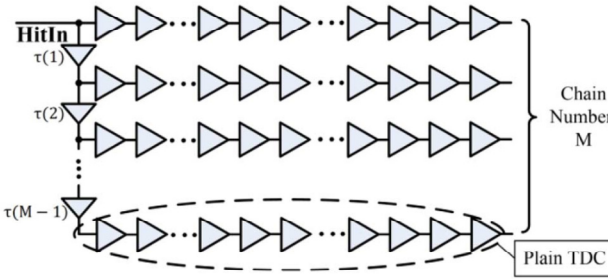
RMS ~ 8 ps

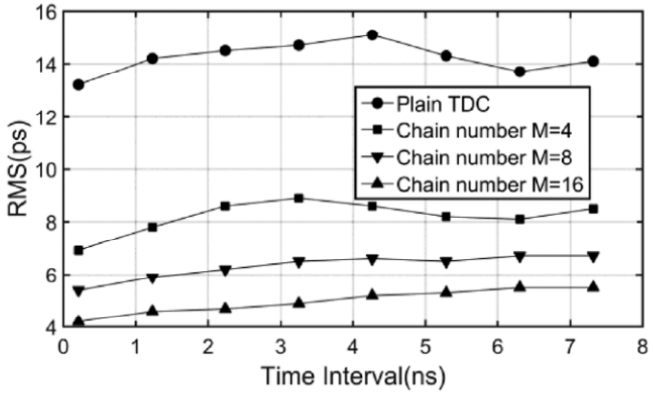


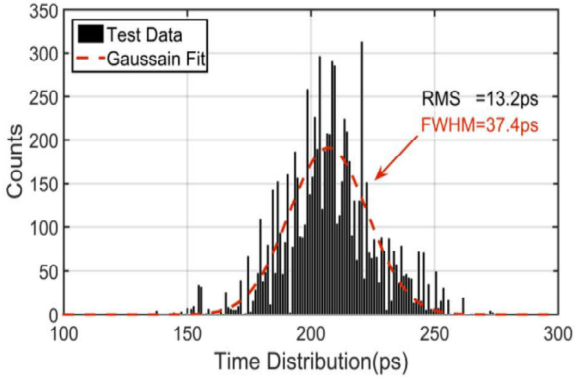
Based on Wave-union method, the bin size and RMS resolution can be effective enhanced.

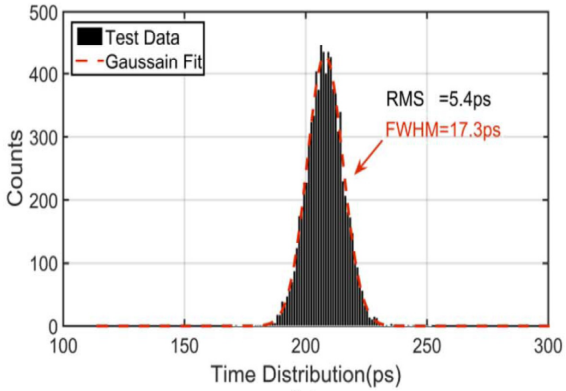
FPGA TDC Design

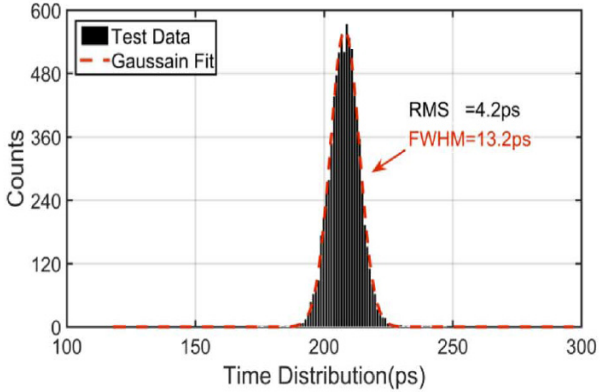
Bin size ~ 1.7 ps, RMS ~ 4.2 ps











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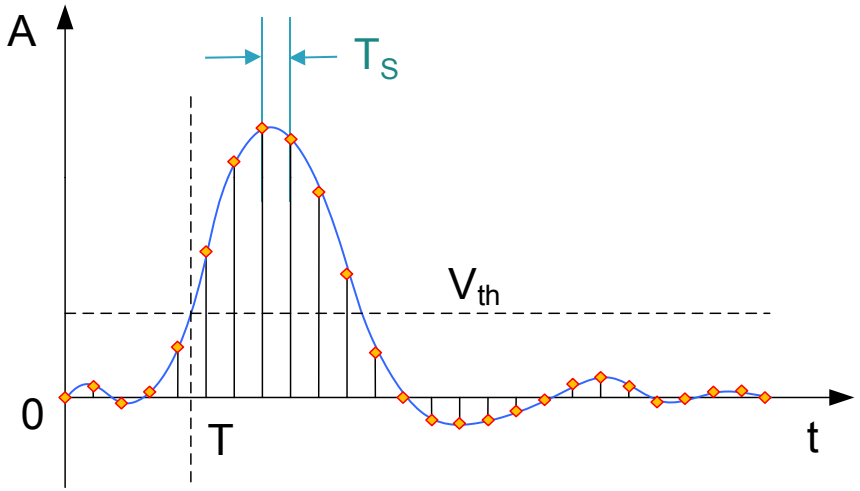
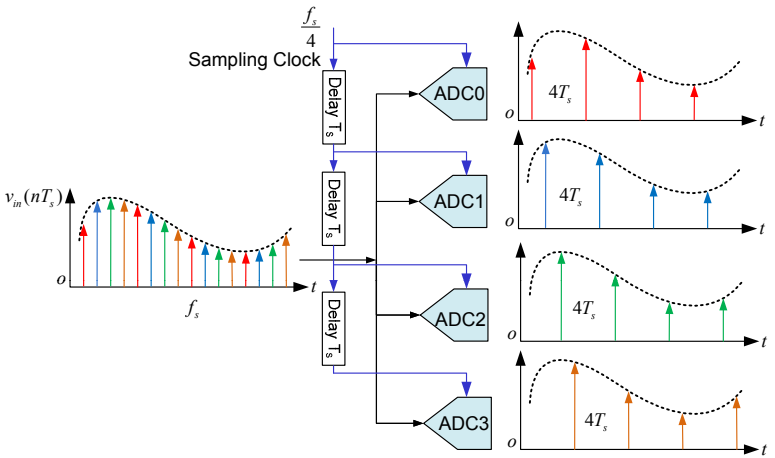
Time measurement based on waveform digitization

- The basic idea is to sample the signal with a very high speed, then compute the time using the digitized waveform in digital signal processing domain.



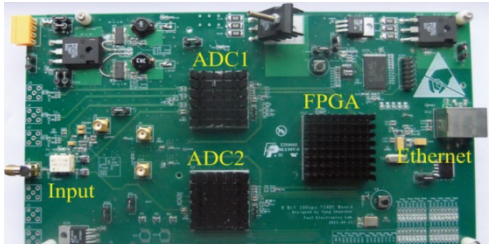
- Since full waveform is digitized, charge information can be calculated, and time walk is not a problem.
- By increasing the sampling frequency f_S, the time resolution of the electronics can be enhanced, far beyond the sampling period ($T_S=1/f_S$) through digital processing such as fitting.

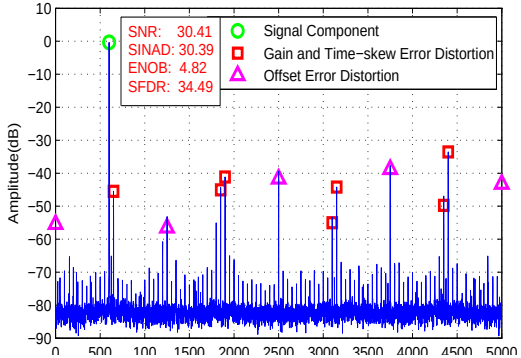
Waveform digitization based on TIADC



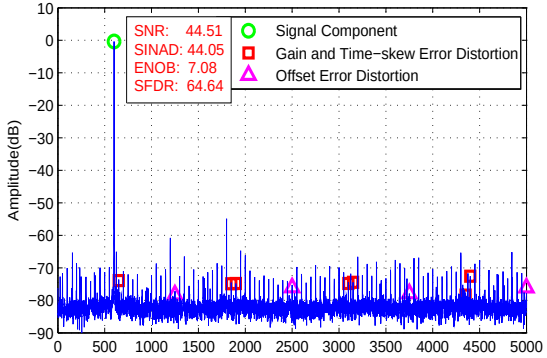
- High speed waveform digitization can be achieved based on Time Interleaving A/D Conversion (TIADC) technique.
- We achieved mismatch error correction using digital signal processing algorithms, and good resolution can be achieved.

10 Gsps, 8 bit



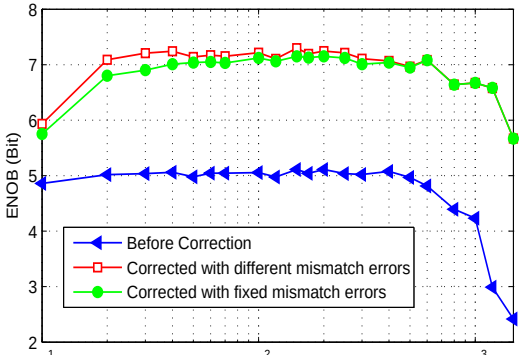


before correction



after correction

Frequency spectrum



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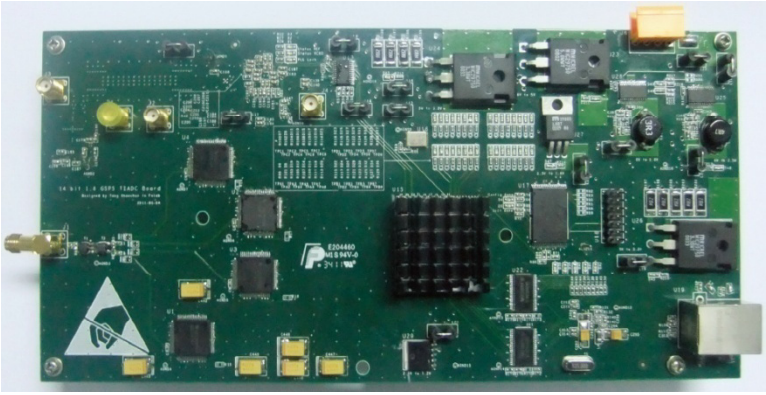
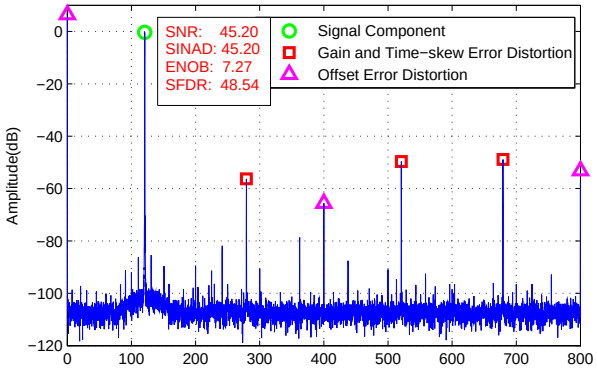
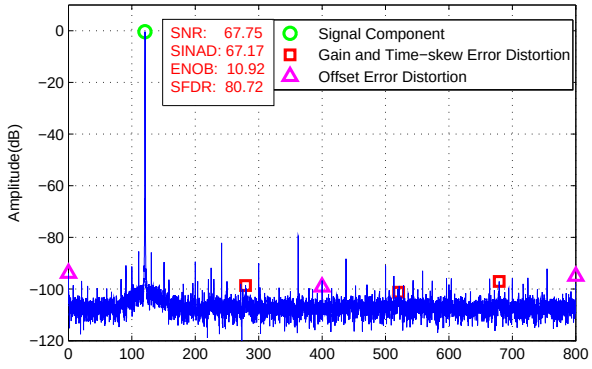
Waveform digitization based on TIADC



1.6 Gsps 14 bit TIADC with real-time correction

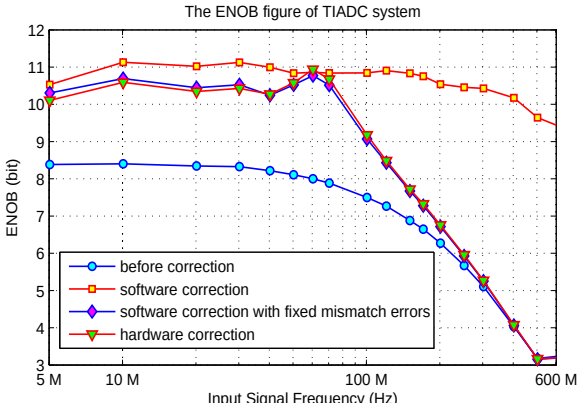


before correction



after correction

Frequency spectrum



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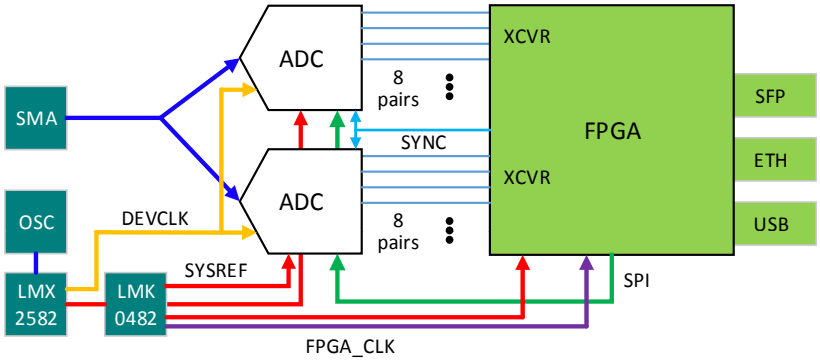
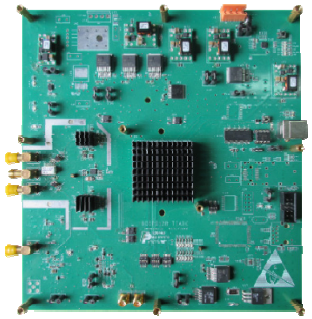
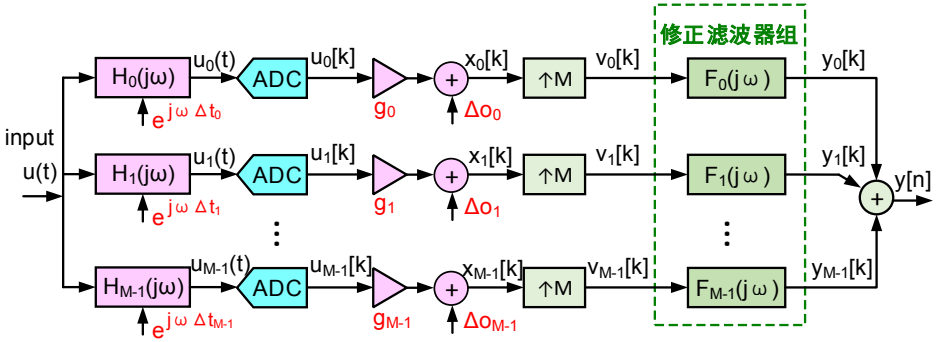
Waveform digitization based on TIADC

- We have also designed a 8 Gsps, 12 bit TIADC module.

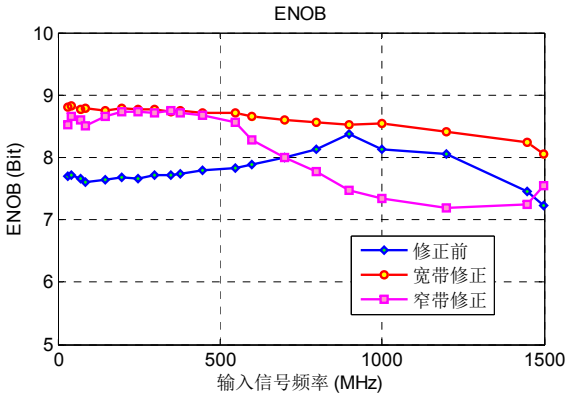




- The mismatch errors can be corrected over a wide input signal frequency range, and real-time correction algorithm is successfully implemented in the FPGA device.



Correction algorithm



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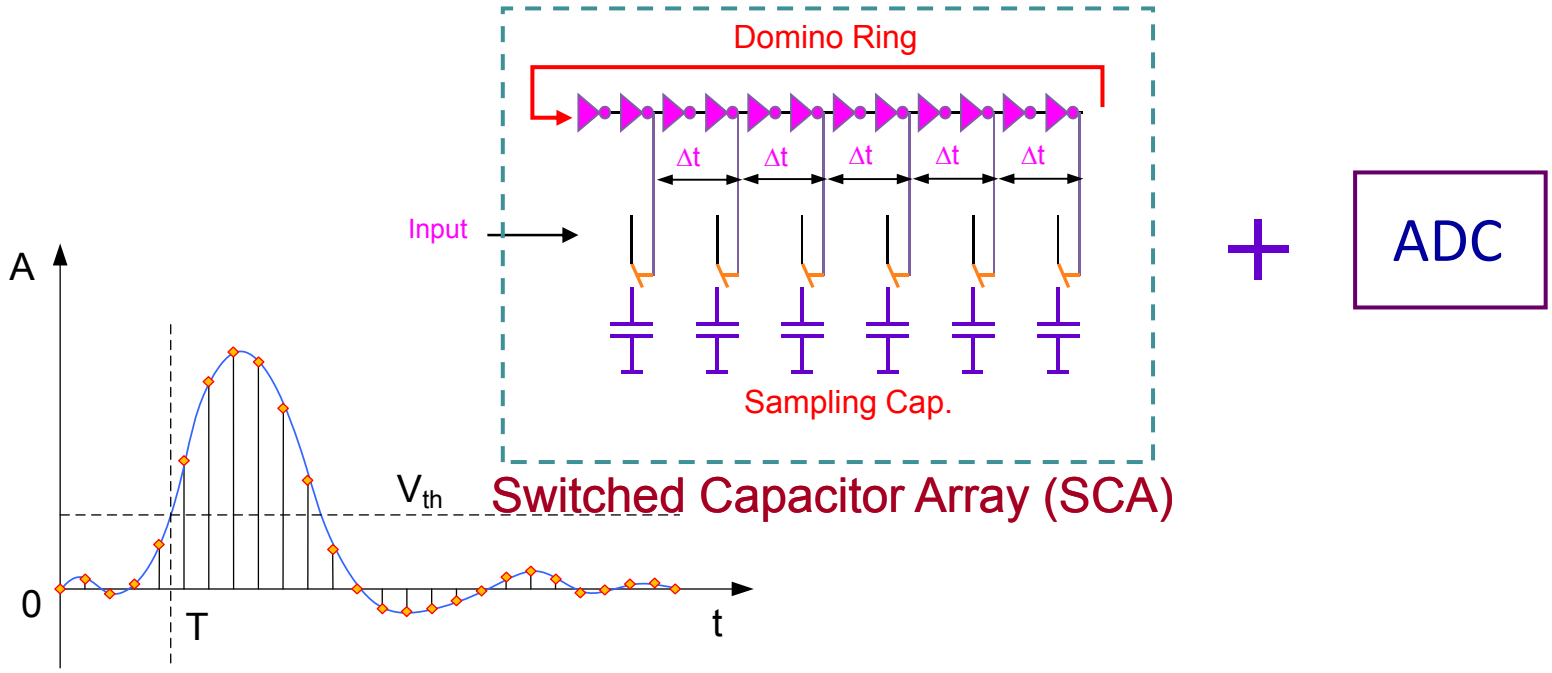
SCA based waveform digitization

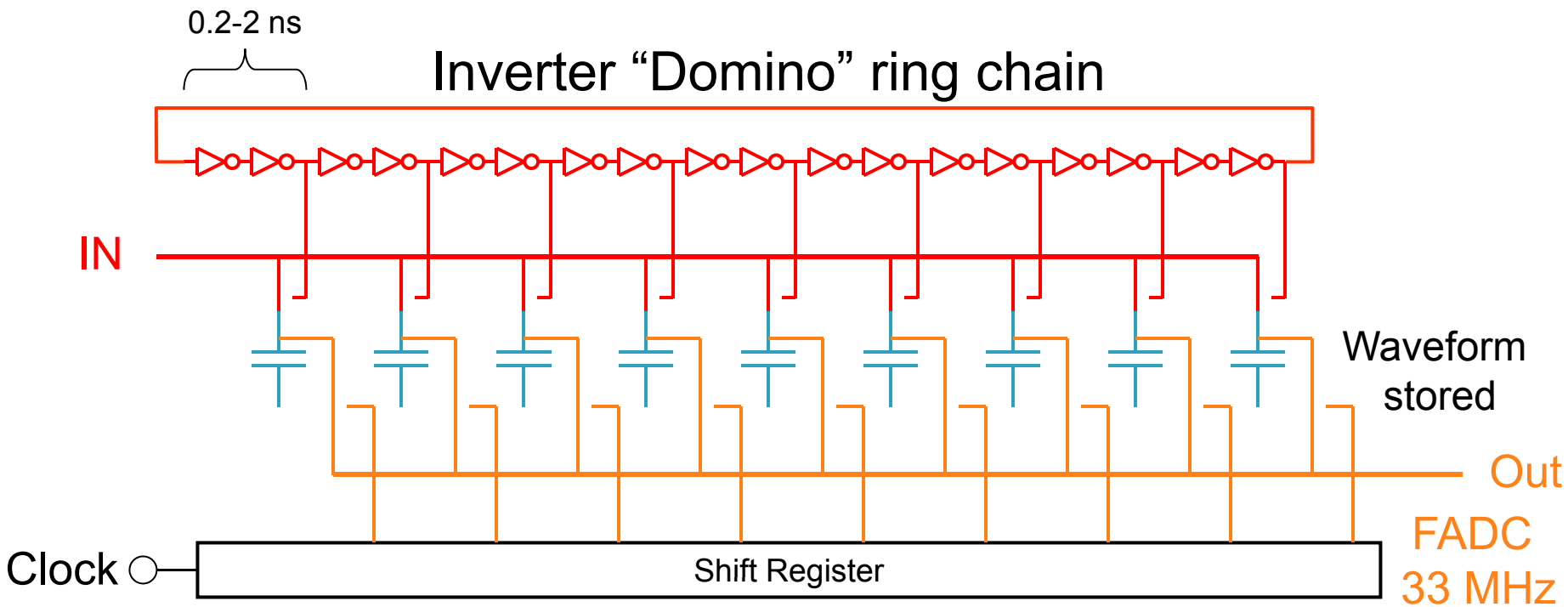
High speed analog transient signal sampling & storage ＋ ADC （SCA + ADC）

high speed sampling

Slow A/D conversion



Basic mechanism of SCA functionality



By Dr. Stefan Ritt

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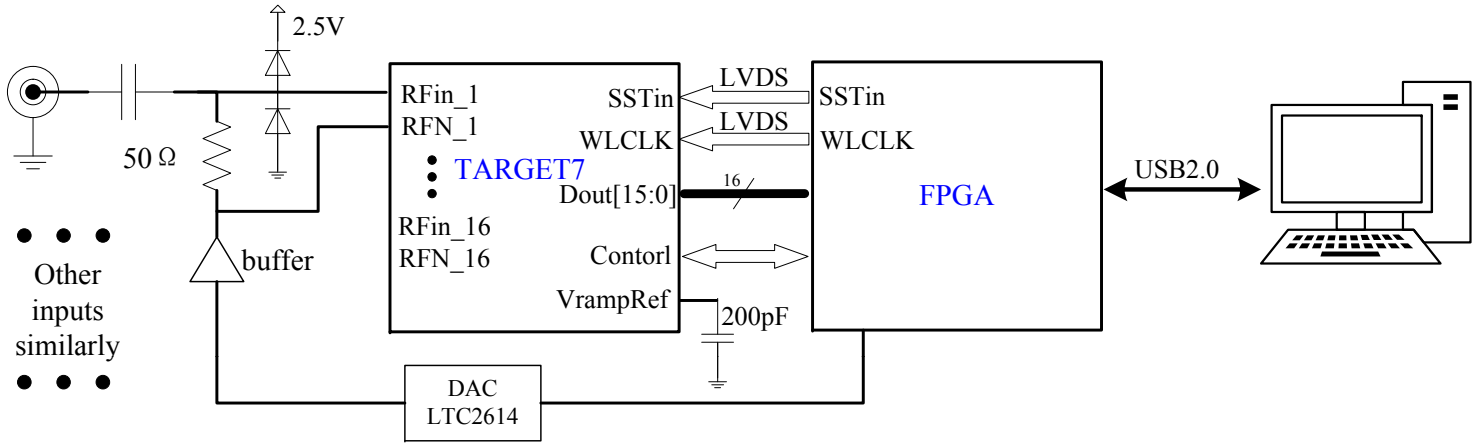
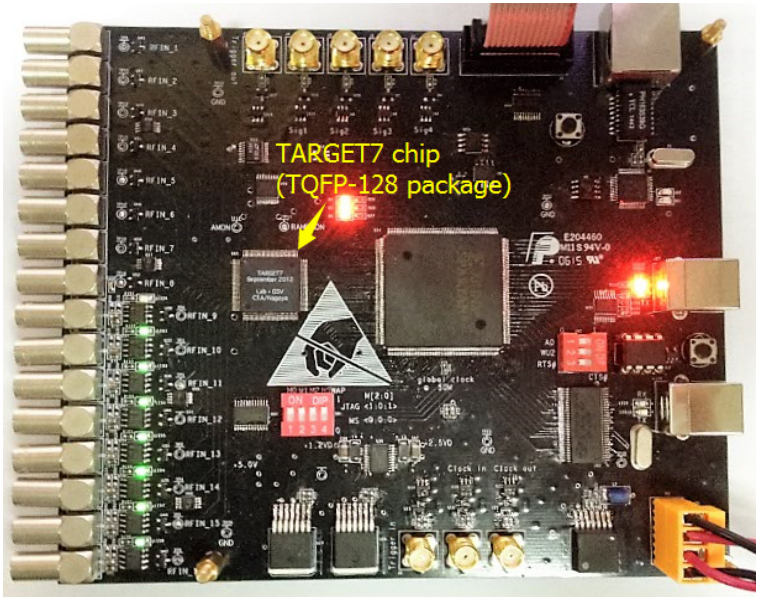
Verification based on TARGET7

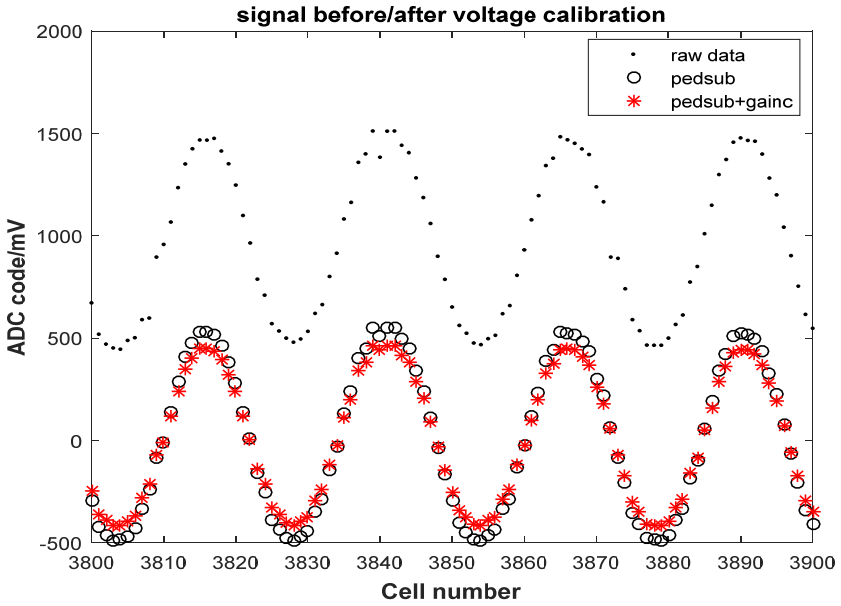


- 16 chl / chip
- Power consumption: (<10mW/chl)
- Sampling rate: ~ Gsps
- 16384 cells / chl
- wilkinson ADC inside for each chl

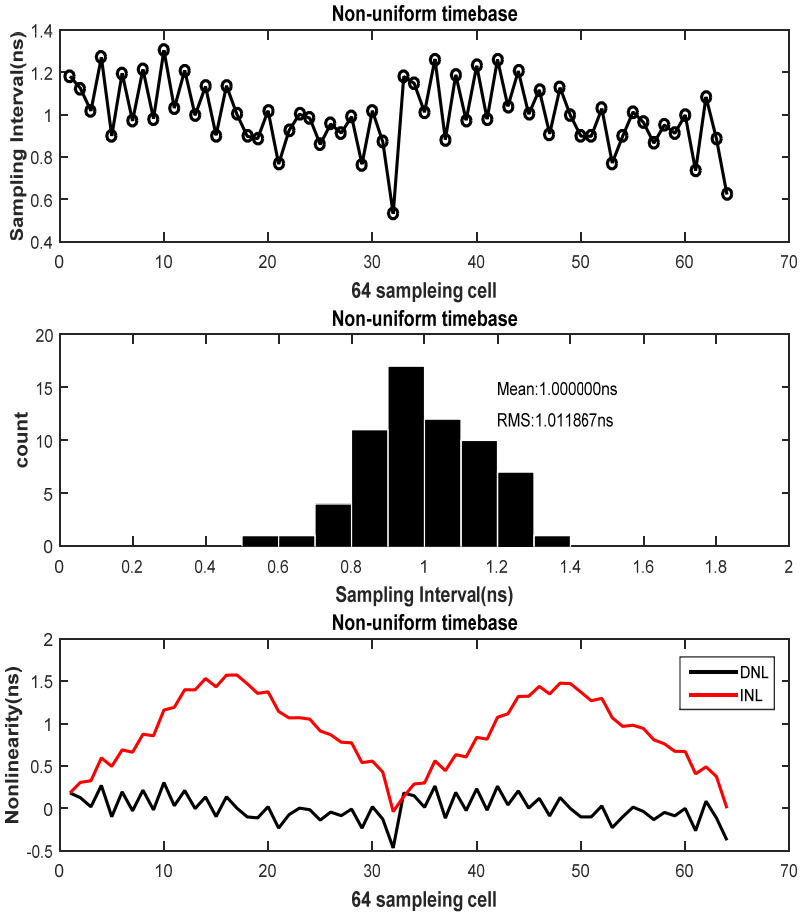


Verification based on TARGET7

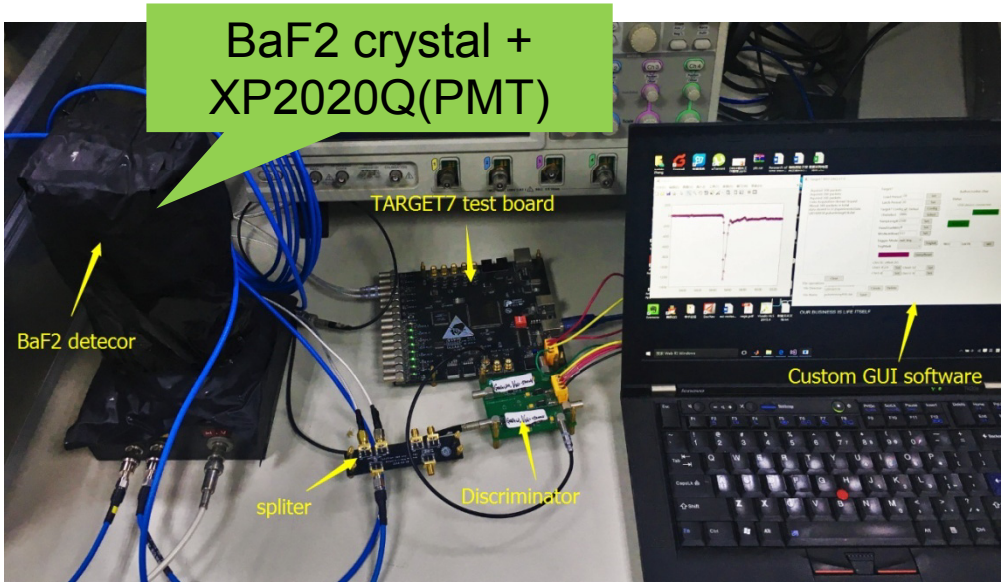
Voltage calibration

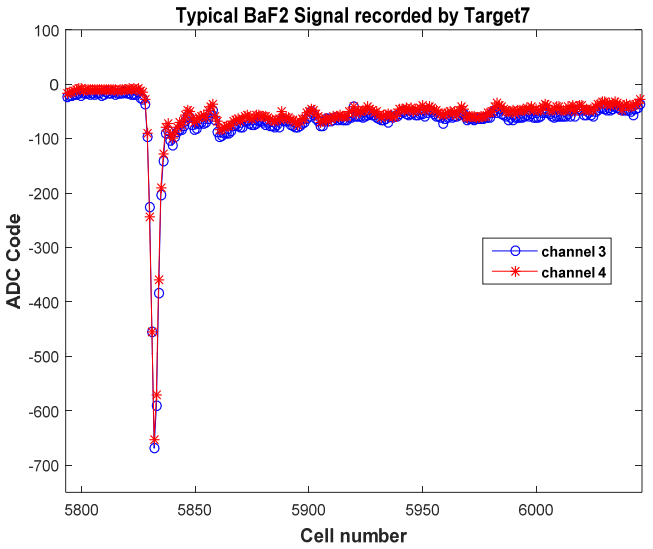


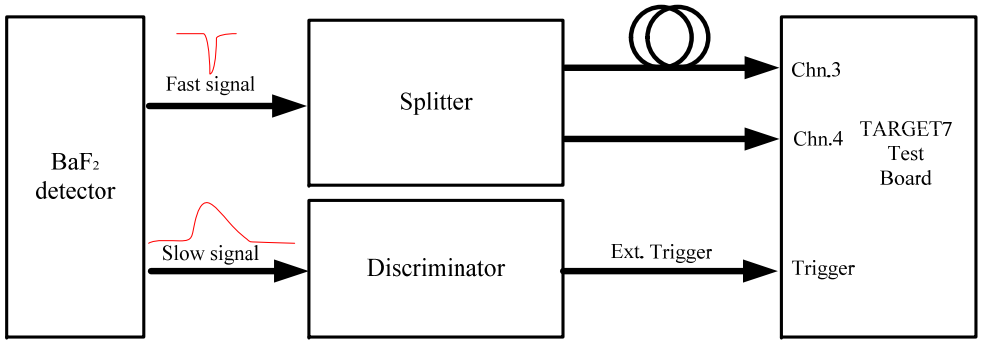
Uneven sampling interval calibration

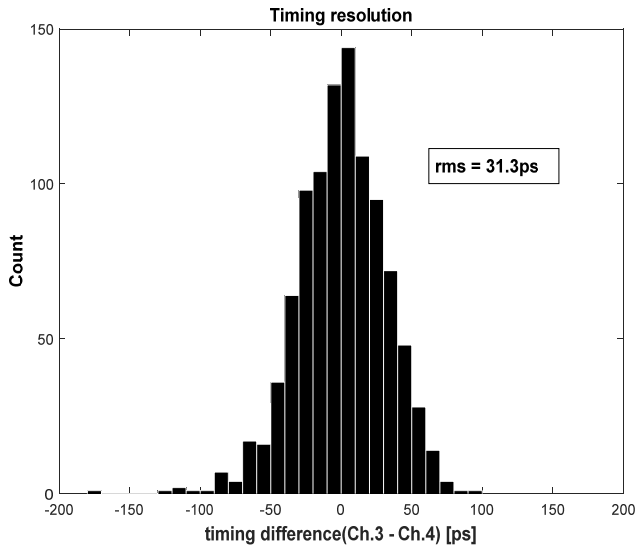


Verification based on TARGET7









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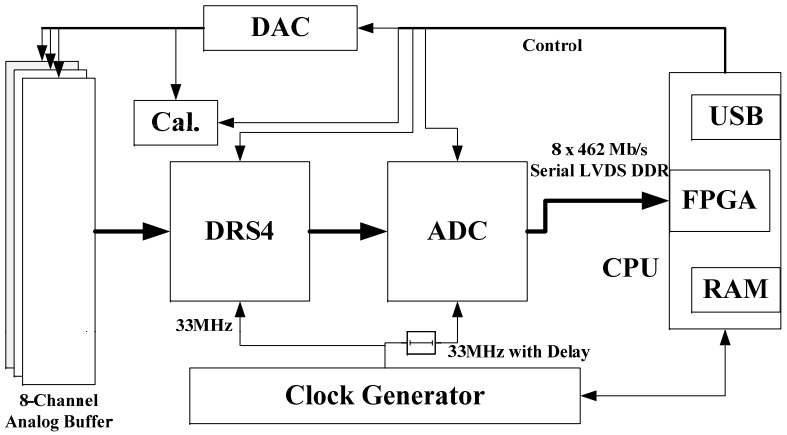
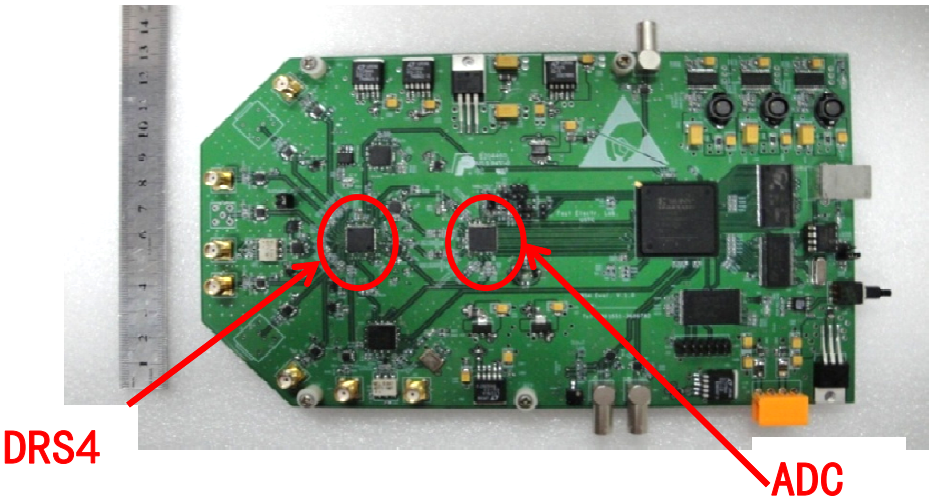
- Design of a 16 chl waveform digitizer for nMRPC

Verification based onDRS4

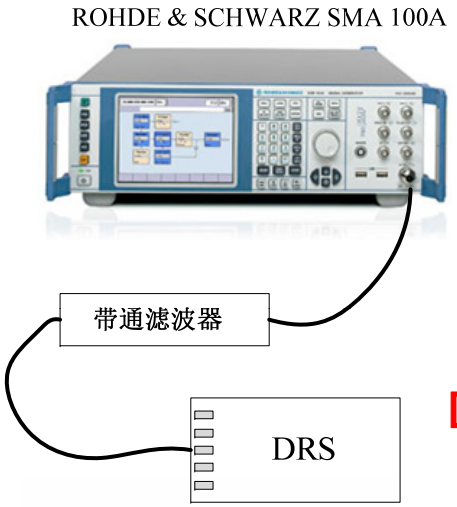




Parameter:
- 8 Chnl.
- 5GS/s (max.)
- ~300 MHz BW (Passive Input)

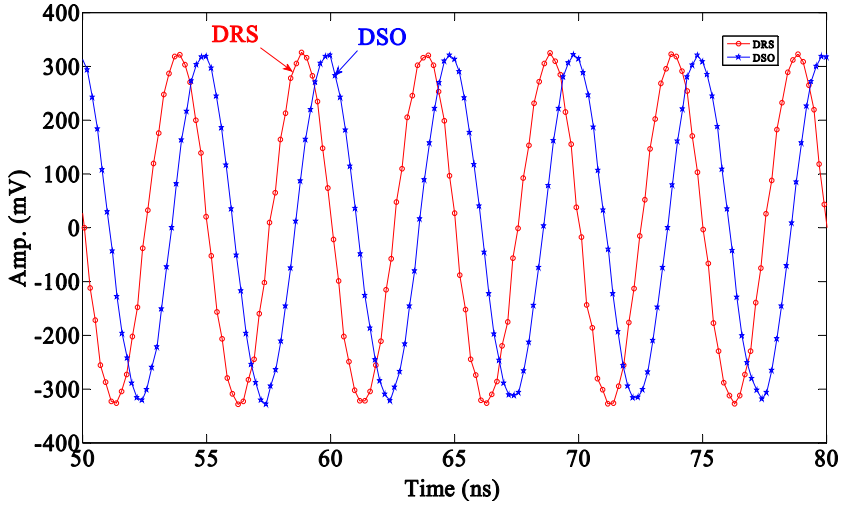
Focusing on:
- Study of DRS4
- Prototype design
- Calibration & correction study:
  - DC offset correction
  - Time error correction

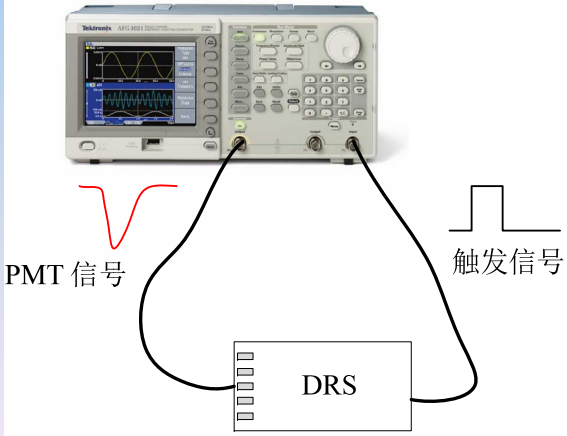
Waveform tests



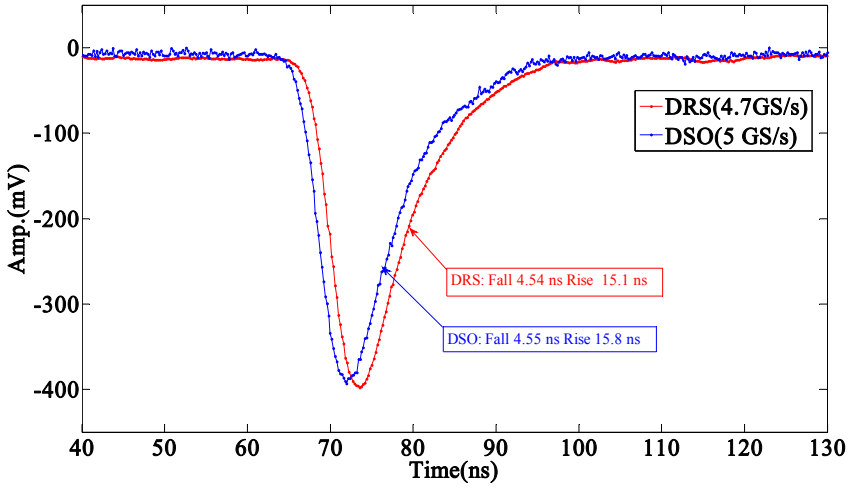
200 MHz Sine

DRS4: 4.7 GS/s



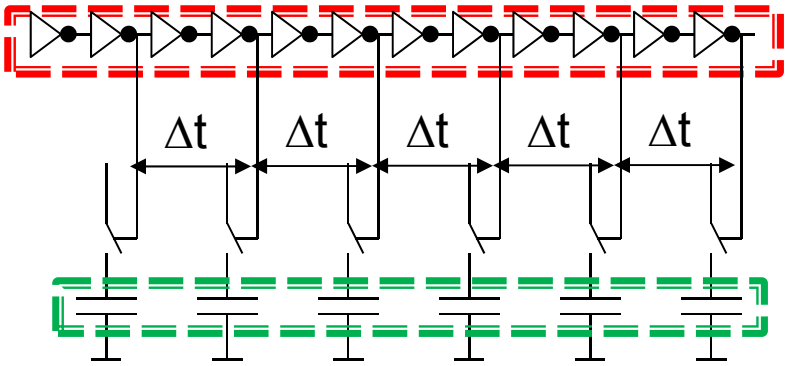


PMT output like signal

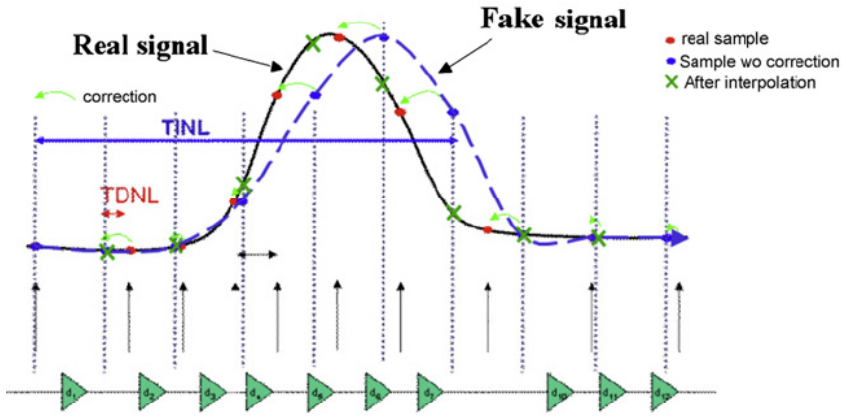


Calibration & correction

- (1) DC Offset Variation Error

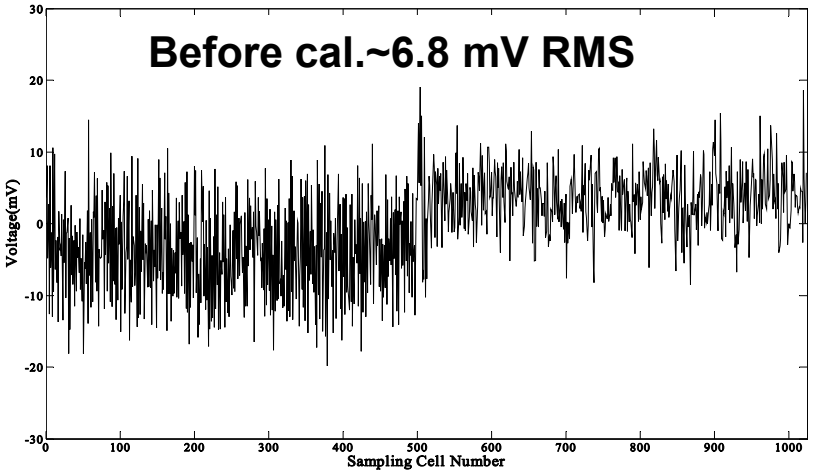


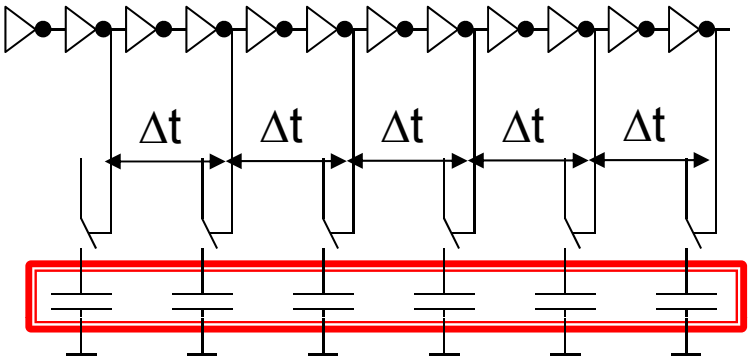
- (2) Uneven Sampling Intervals



NIMA :629 (2011) 123-132

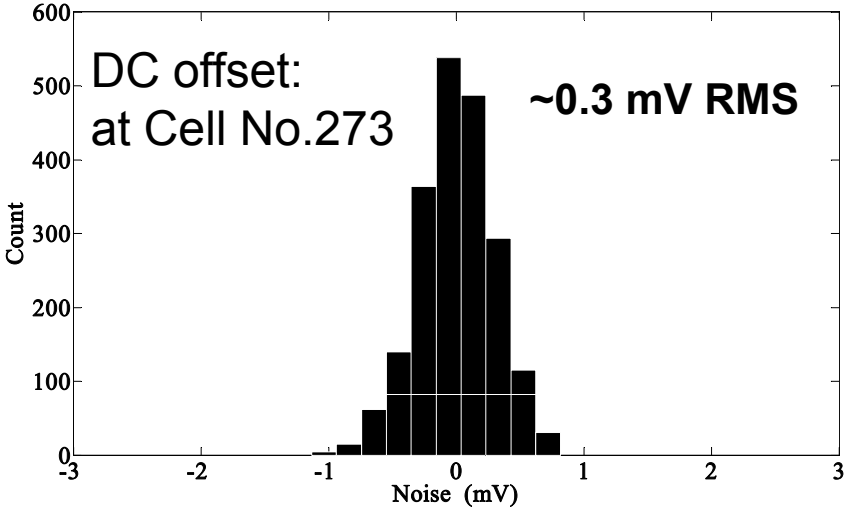
Calibration of DC offset

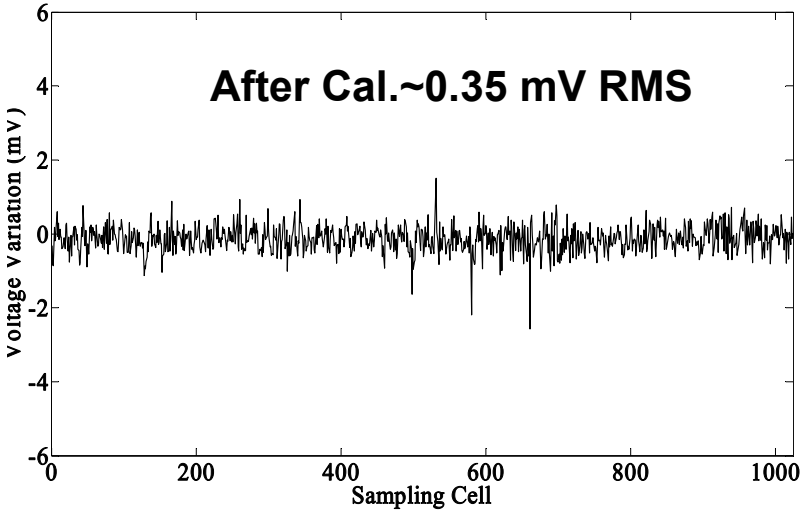




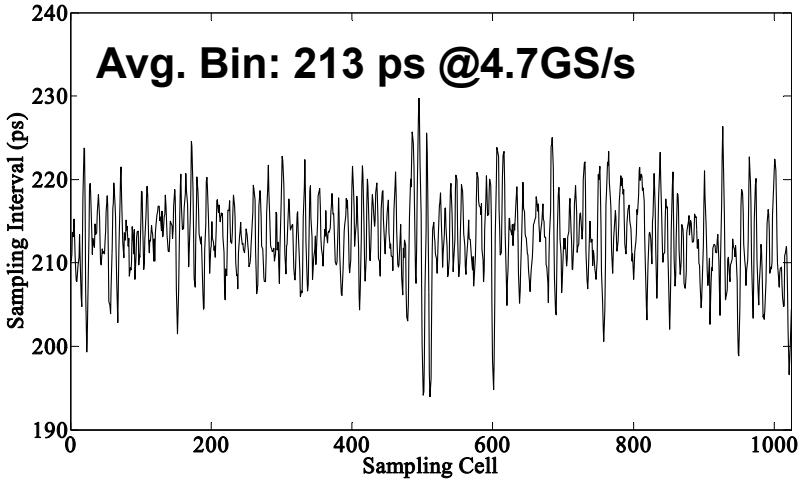
Cell to cell Variation

DC offset: Cell-to-Cell Variation

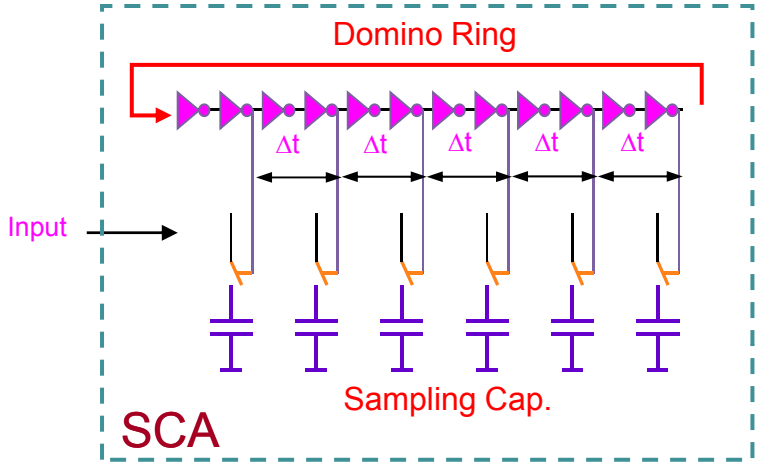


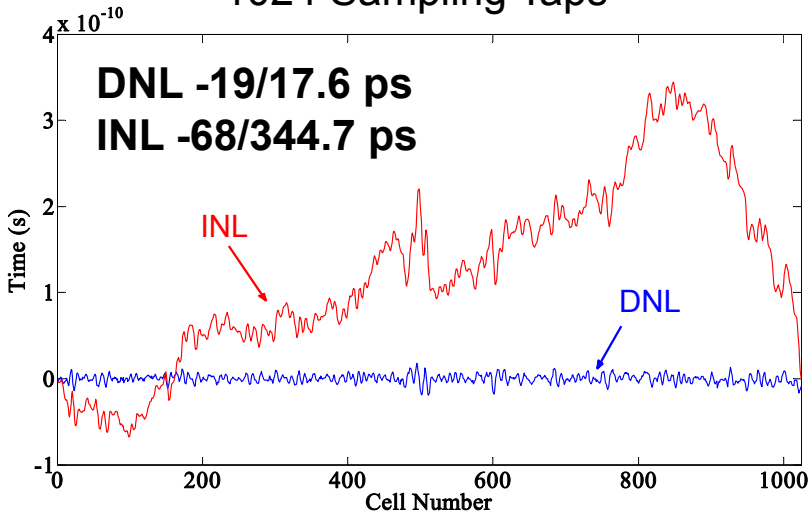


Calibration of Uneven Sampling Interval

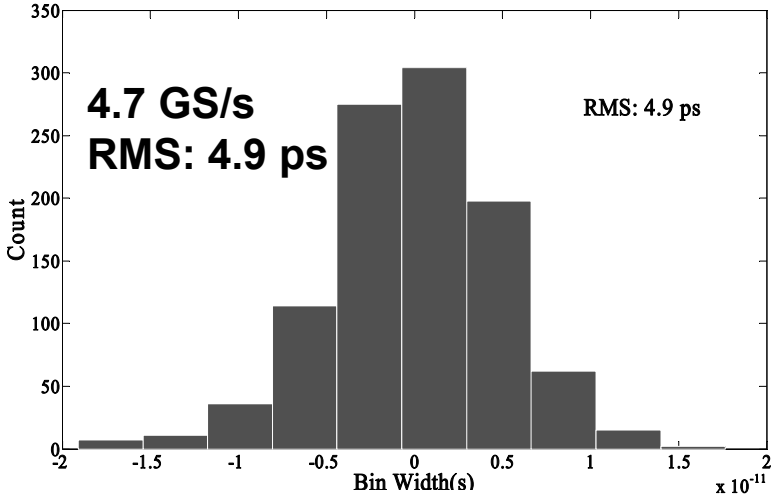


1024 Sampling Taps



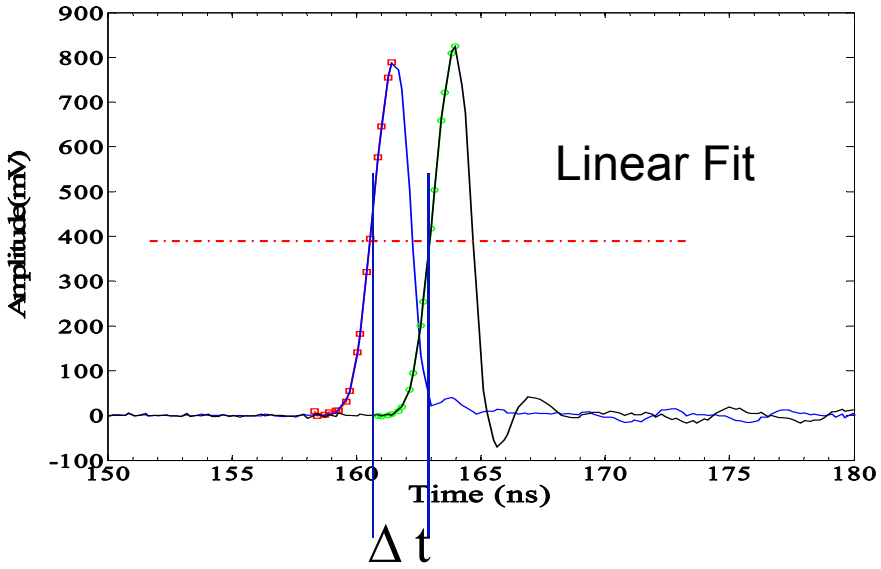


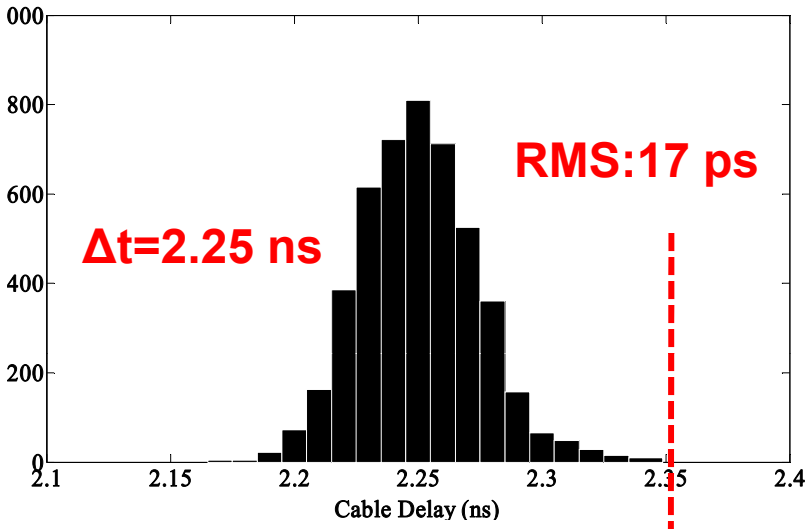
DNL & INL



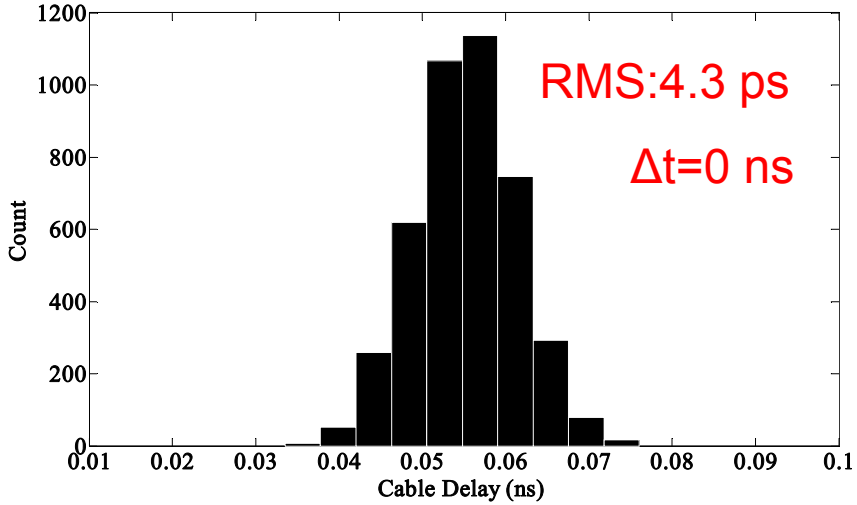
Distribution of Bin width

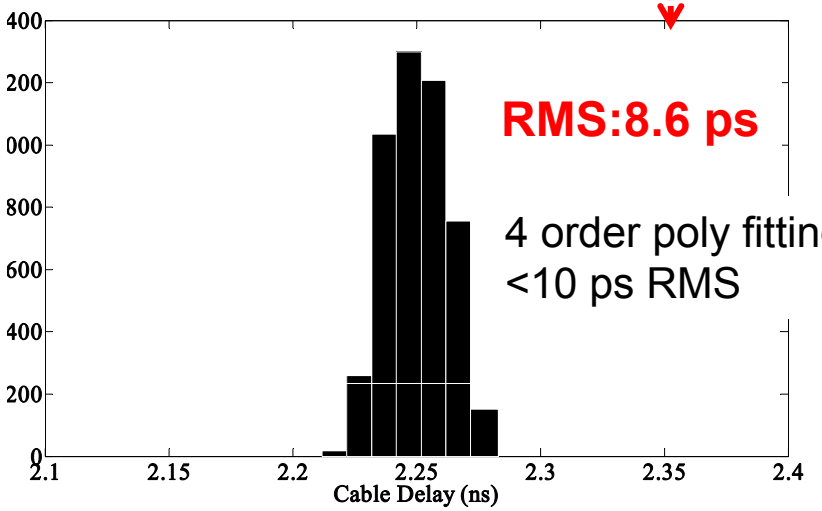
Pulse Fitting





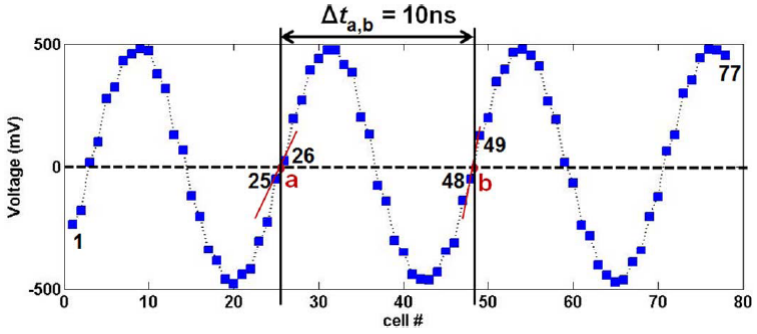
after correction

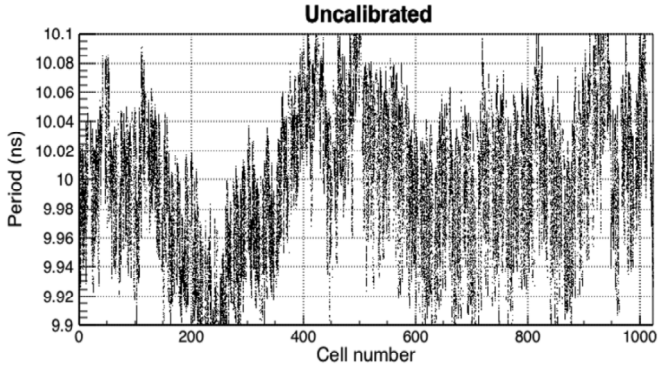


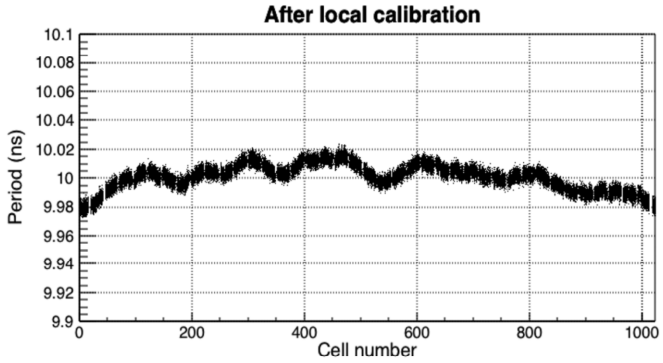


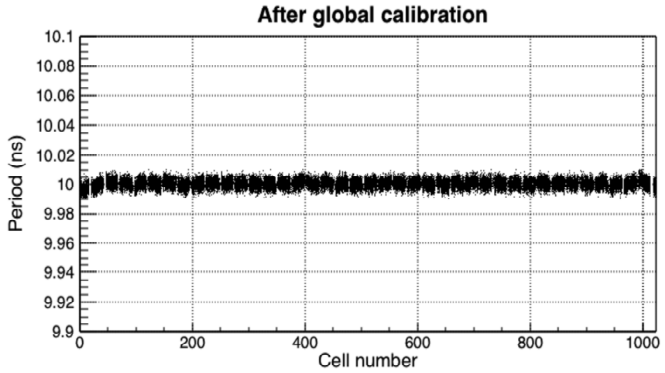
DRS4 time calibration

Global calibration









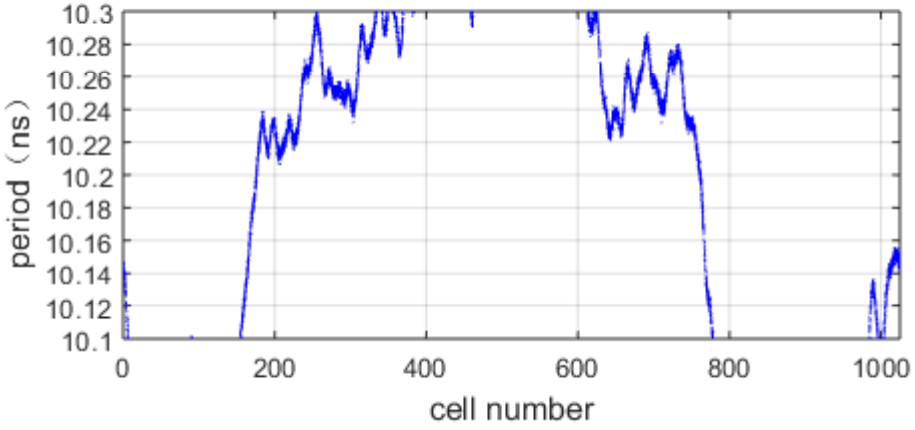
↓ Differential Non-Linearity (DNL)

↓ Integral Non-Linearity (INL)

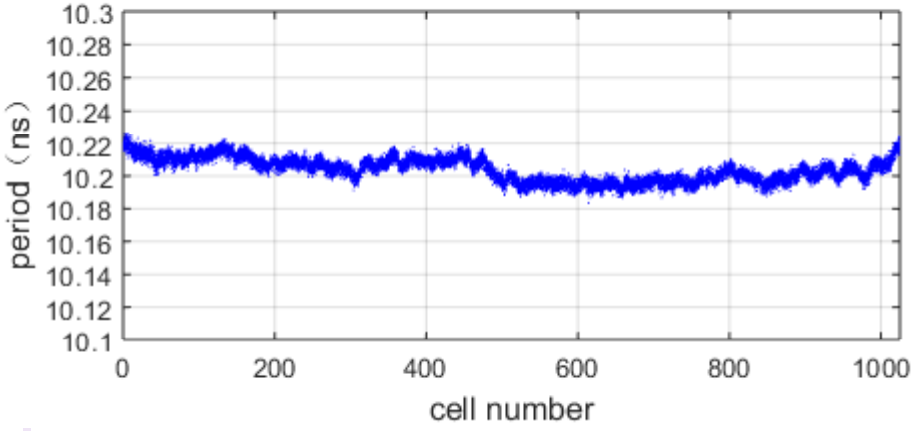
By D. Stricker-Shaver, S. Ritt

Time calibration

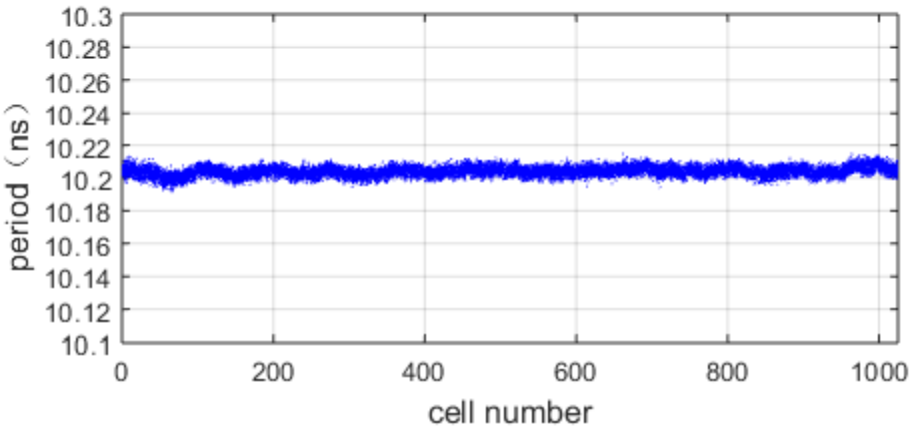
Before calibration



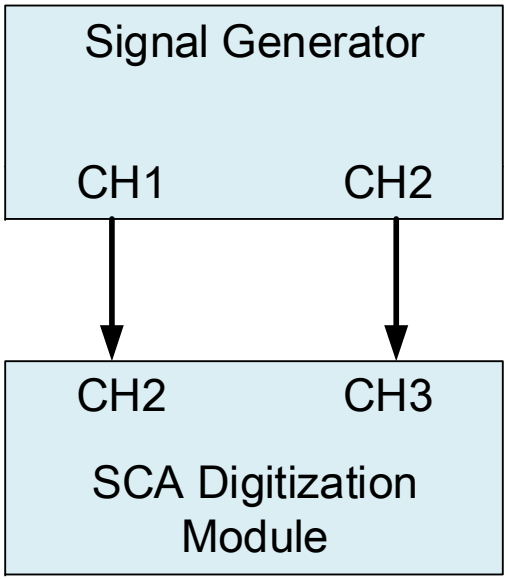
Local calibration



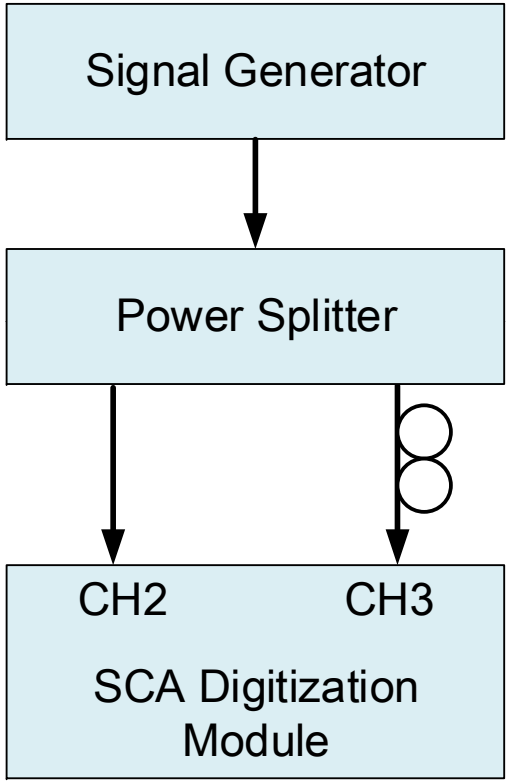
Global calibration



Test in the Lab



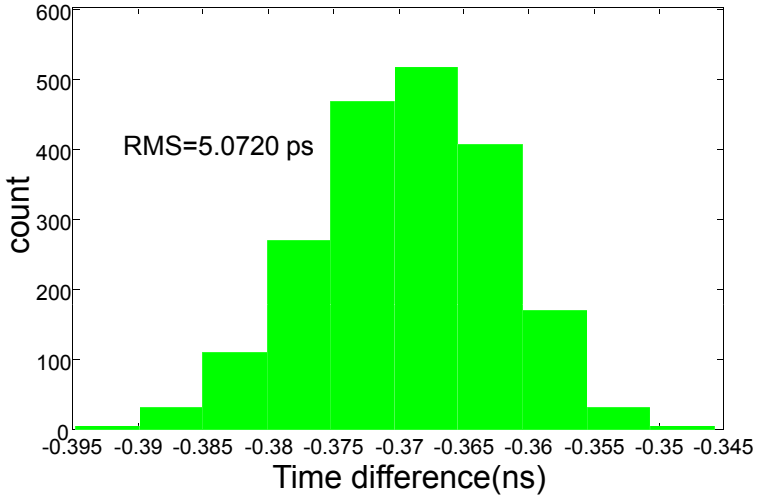
Time Sweep



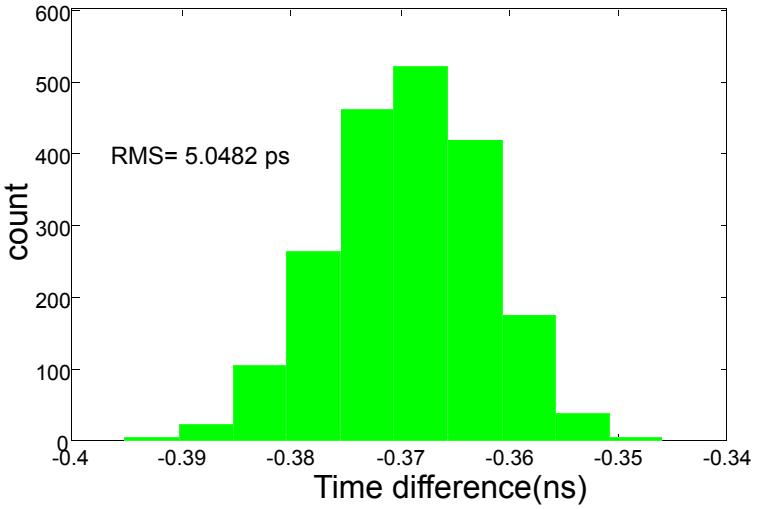
Cable Delay

Time resolution test

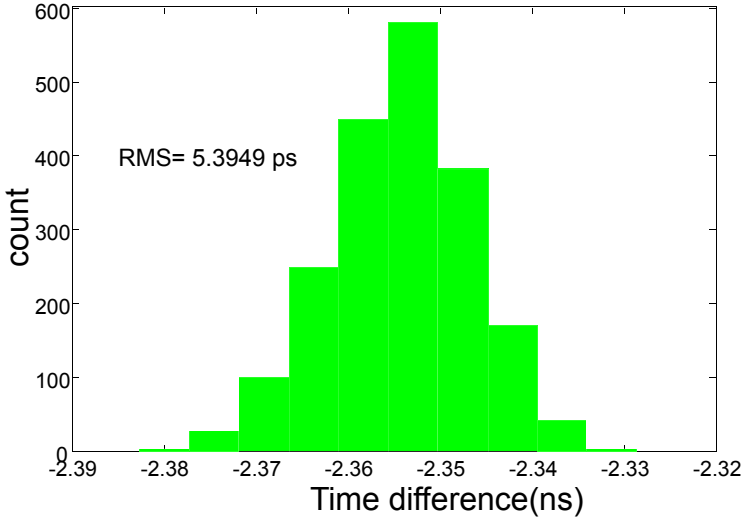
Local calibration

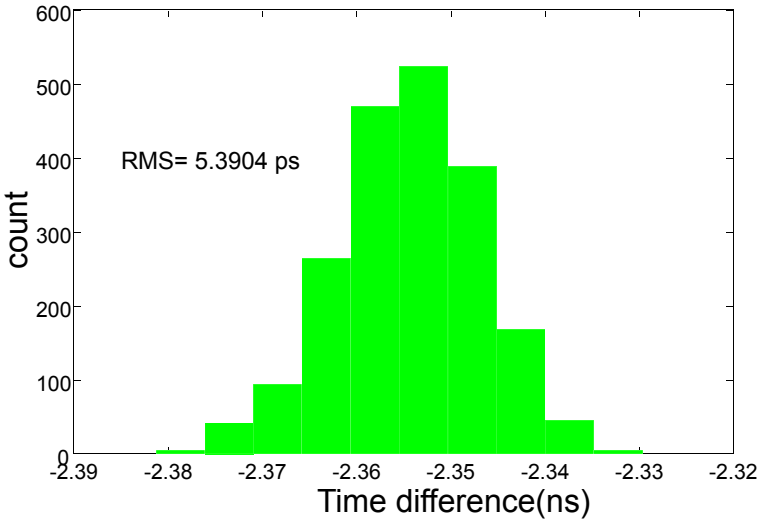


Global calibration



0 ns

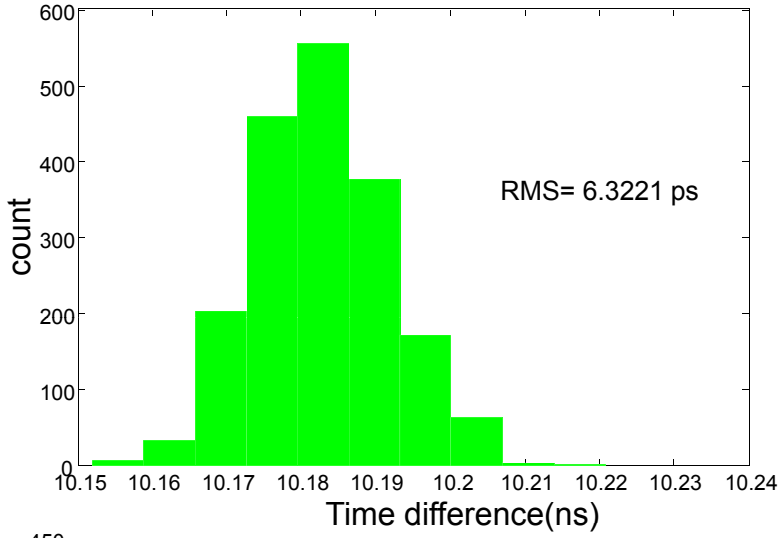




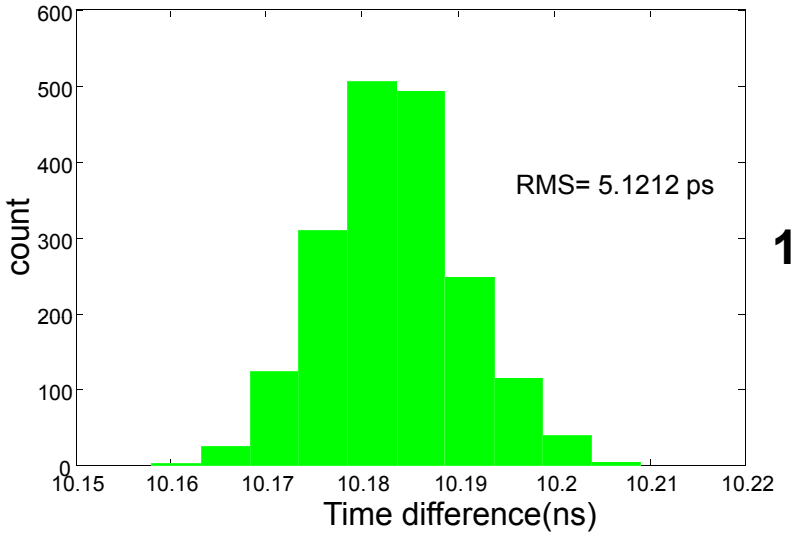
2 ns

Time resolution test

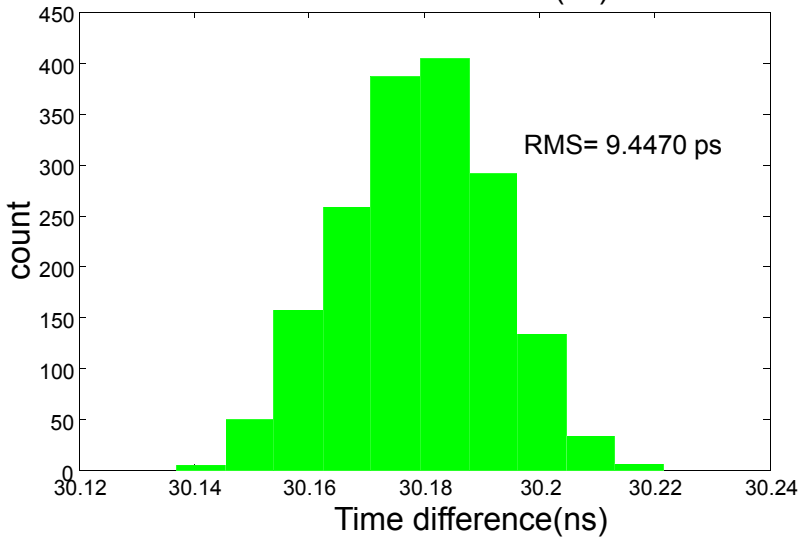
Local calibration

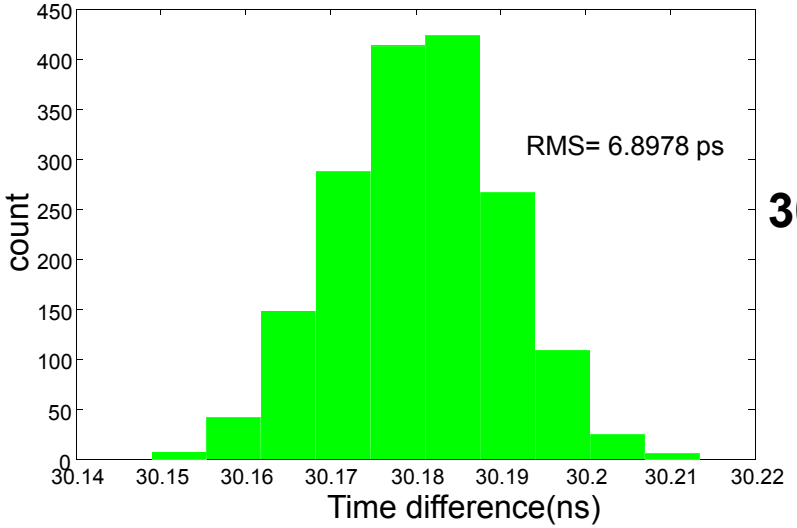


Global calibration



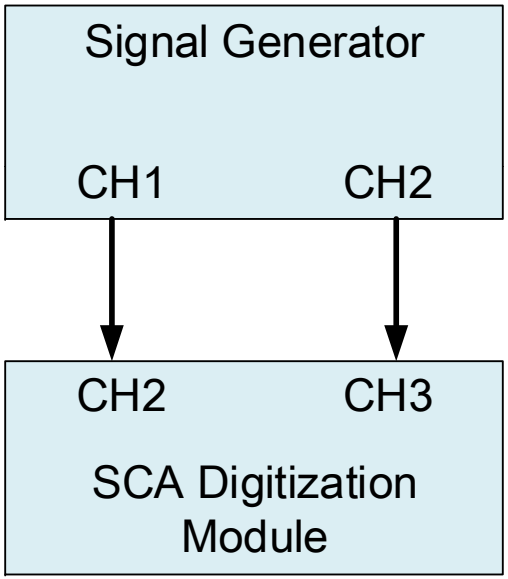
10 ns



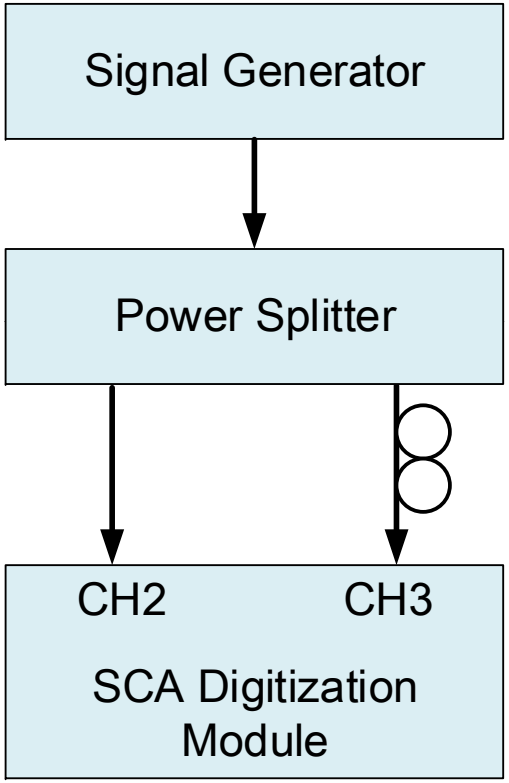


30 ns

Test in the Lab



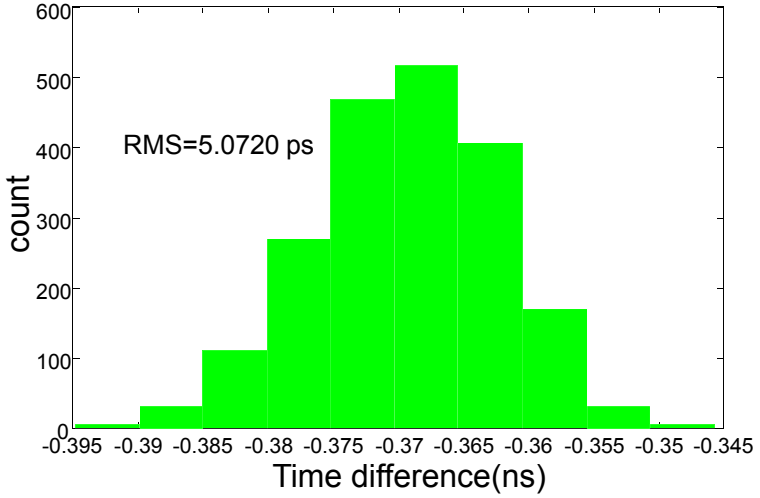
Time Sweep



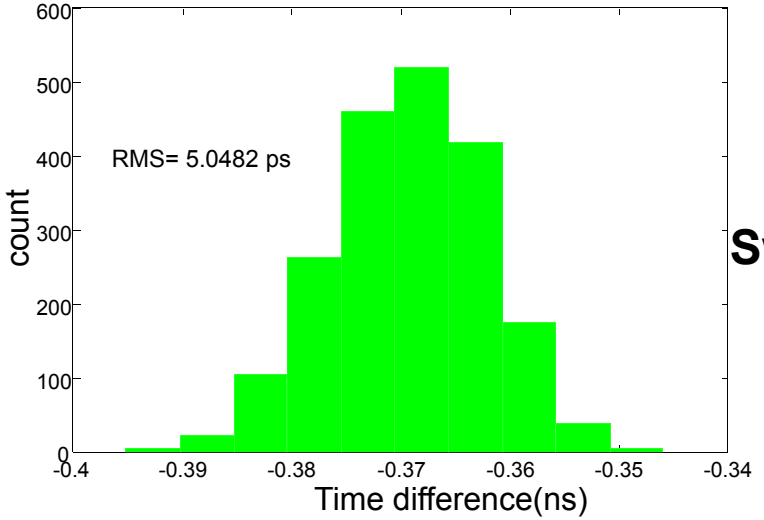
Cable Delay

Time resolution test

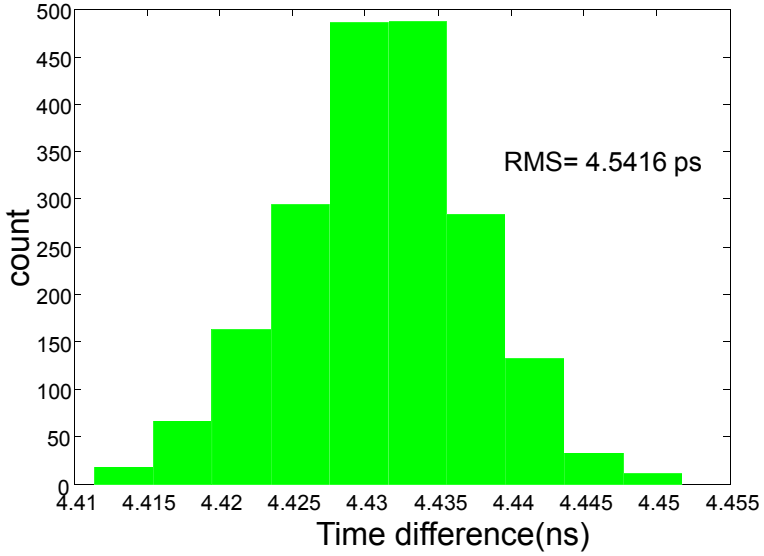
Local calibration

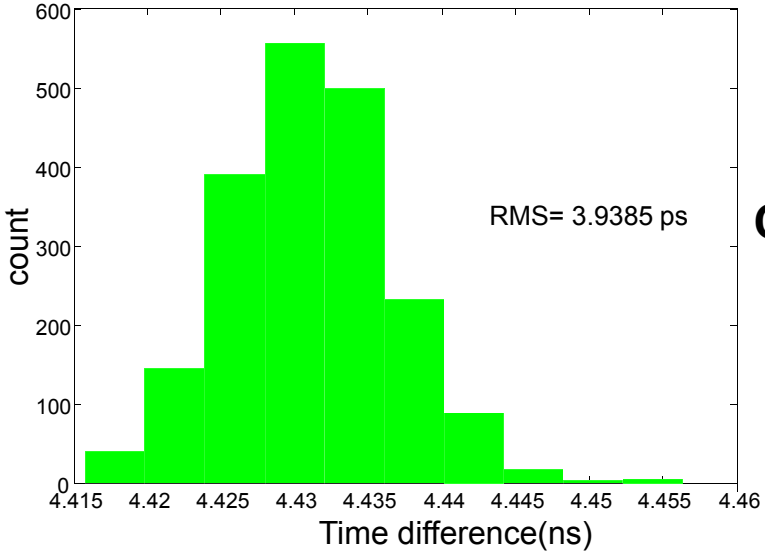


Global calibration



Sweeping





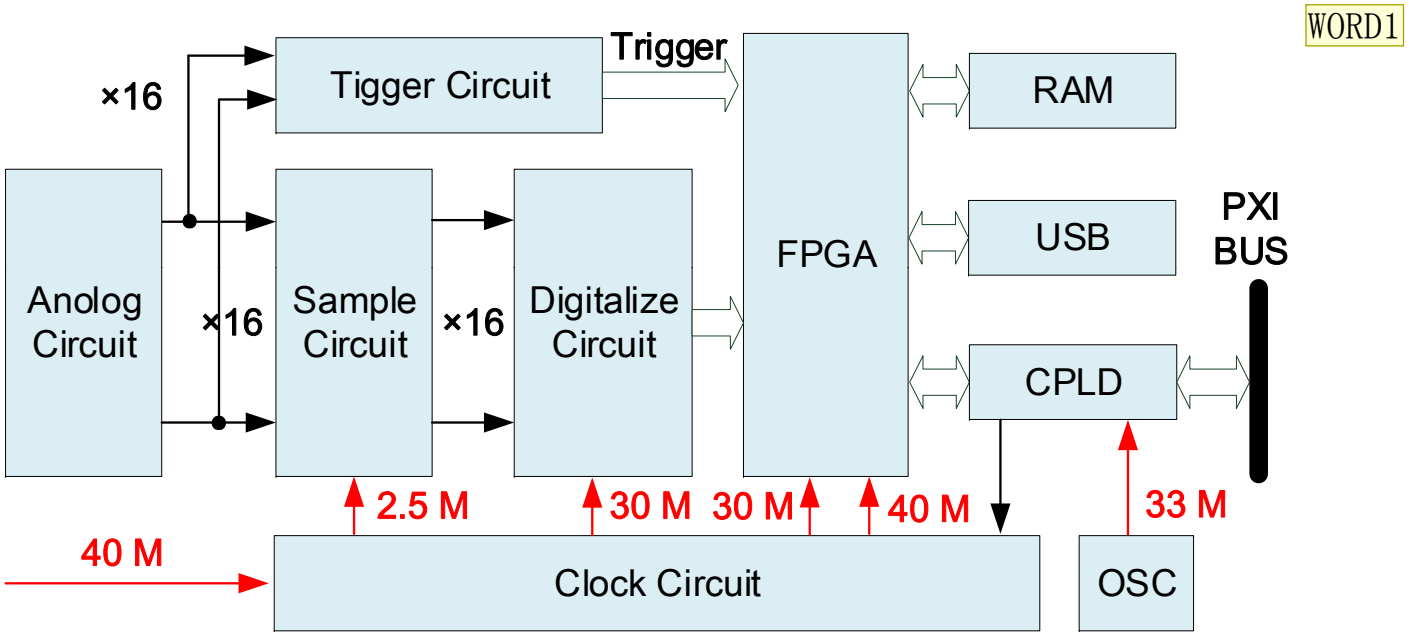
Cable

Contents

- Methods for time measurement
- Method 1: discrimination + TDC
- Method 2: waveform digitization based on SCA
  - verification based on TARGET7
  - verification based on DRS4
  - verification using another time calibration method
- Design of a 16 chl waveform digitizer for nMRPC

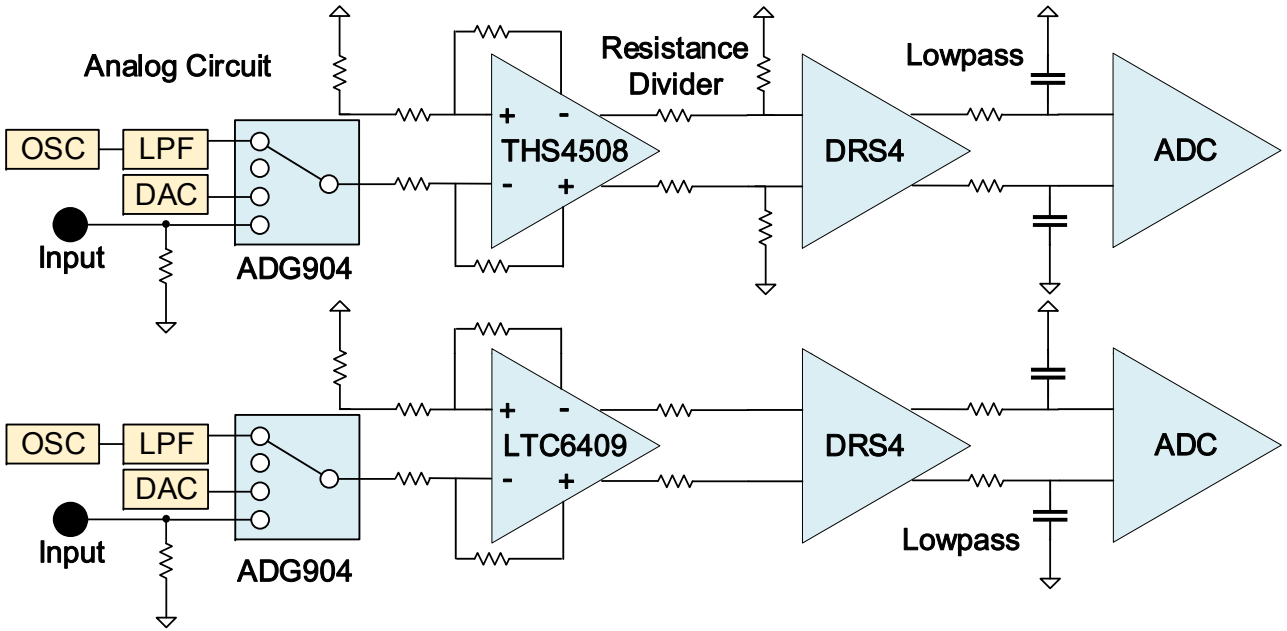
Design of a 16 chl waveform digitizer

- Block diagram:



- 16 channels per module
- Analog circuits: buffering for input signals, calibration signal generation
- Self Trigger Circuits: discrimination, self trigger signal for SCA readout
- Data Readout： USB or PXI interface

Analog Front End



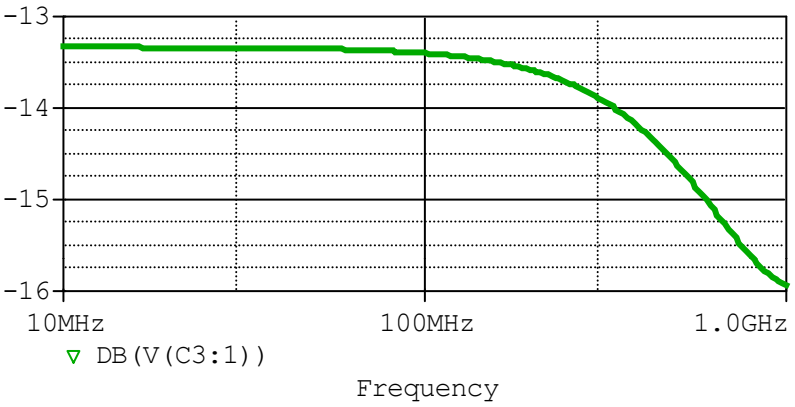
- Two amplifiers are employed for comparison
- Using switches to select among:

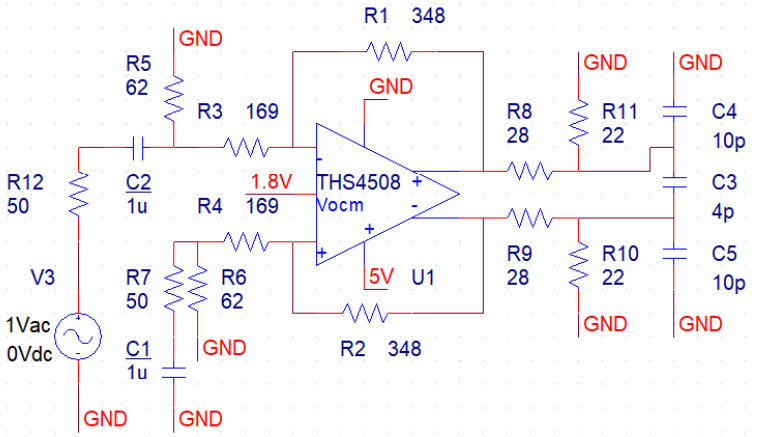
① Analog input signal
② DC voltage from DAC for calibration
③ Sine wave signal for calibration

Analog Front End

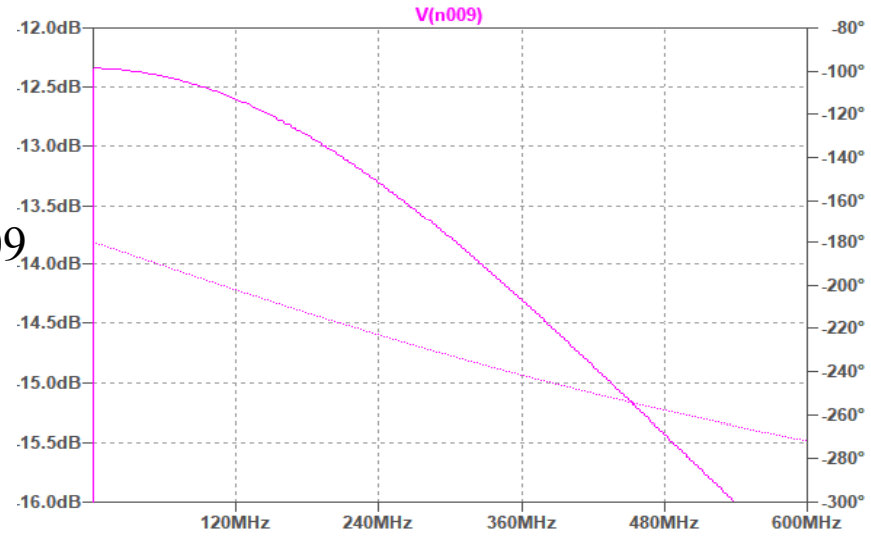
- Simulation results of bandwidth

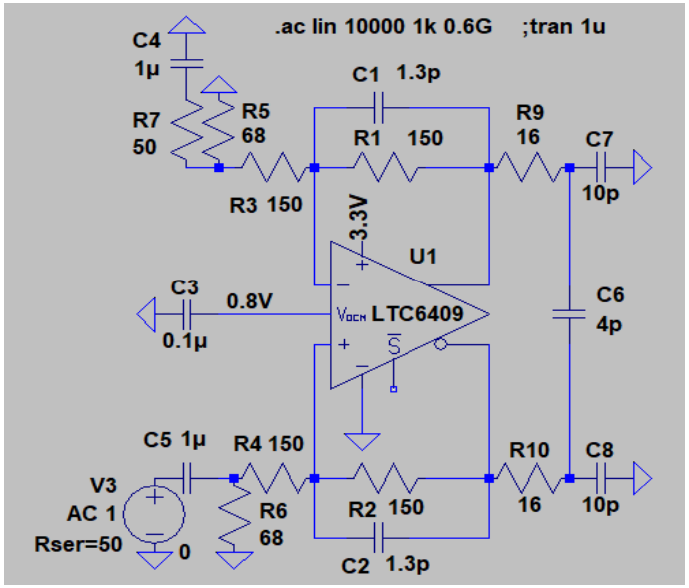
THS4508



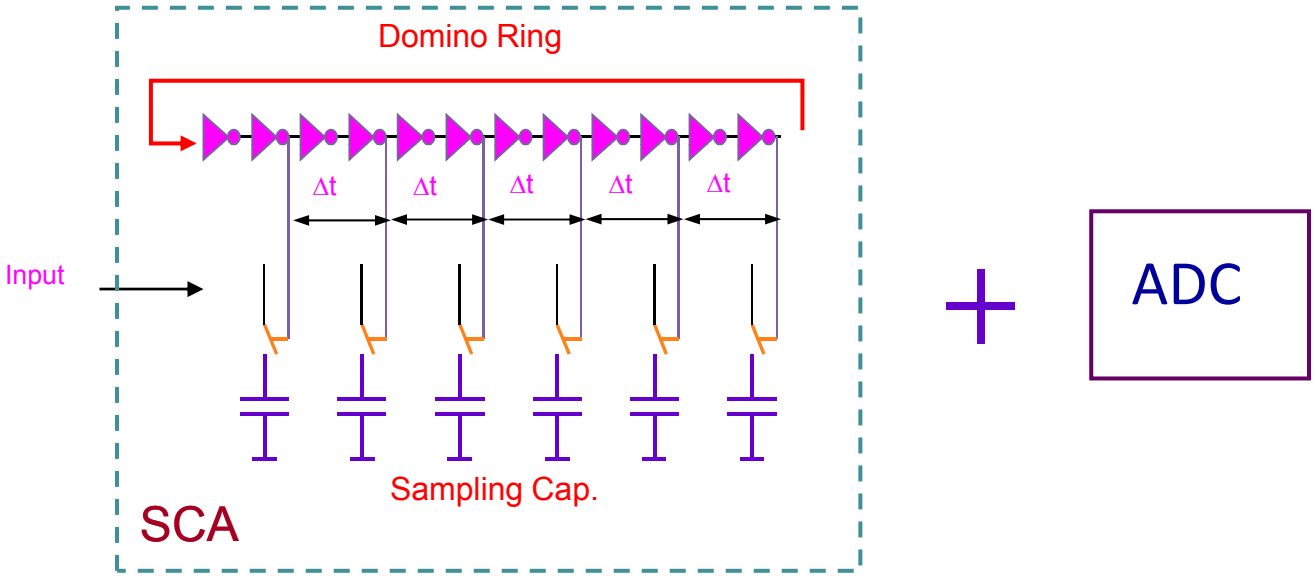


LTC6409

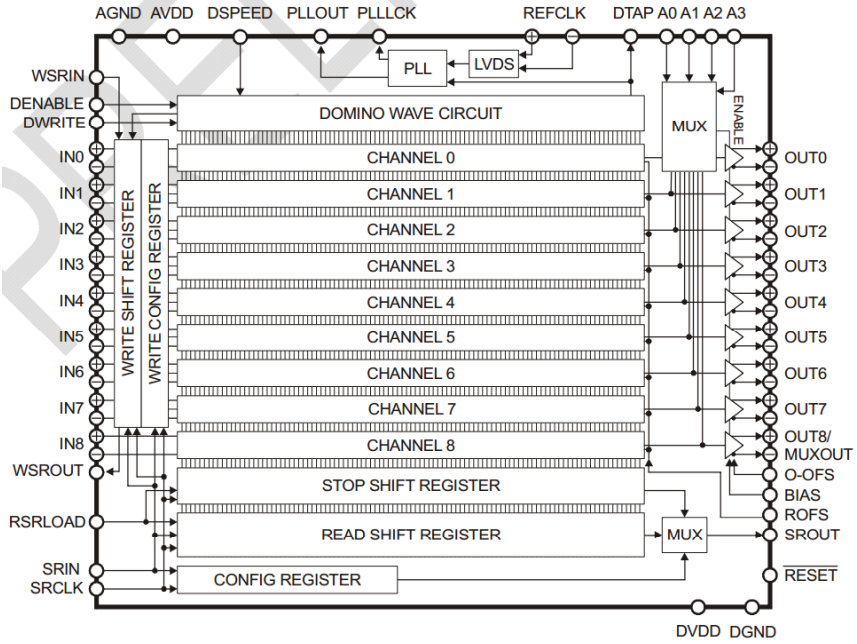




Digitization circuits

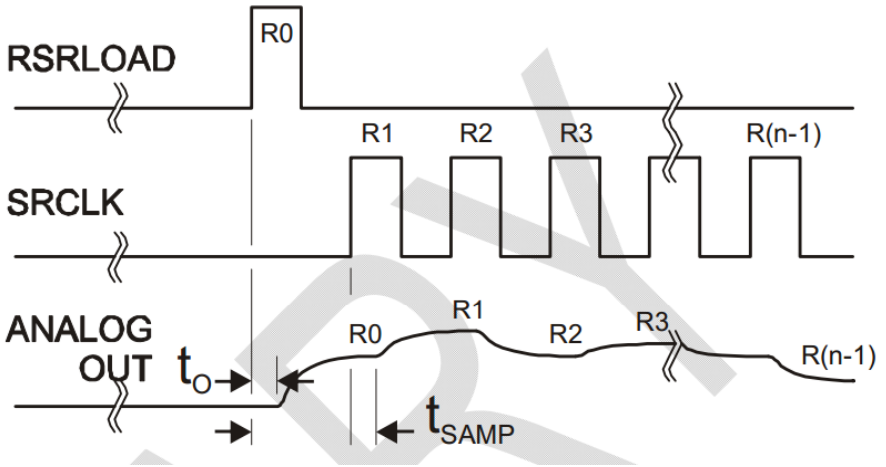


Sampling: SCA – DRS4



Parameter	
Channel no	8+1
-3dB BW	950 MHz
Sampling speed	0.7 Gsps ~ 5Gsps
Readout frequency	30~40 MHz
noise	0.35 mV RMS
Diff input range	< 1 Vpp

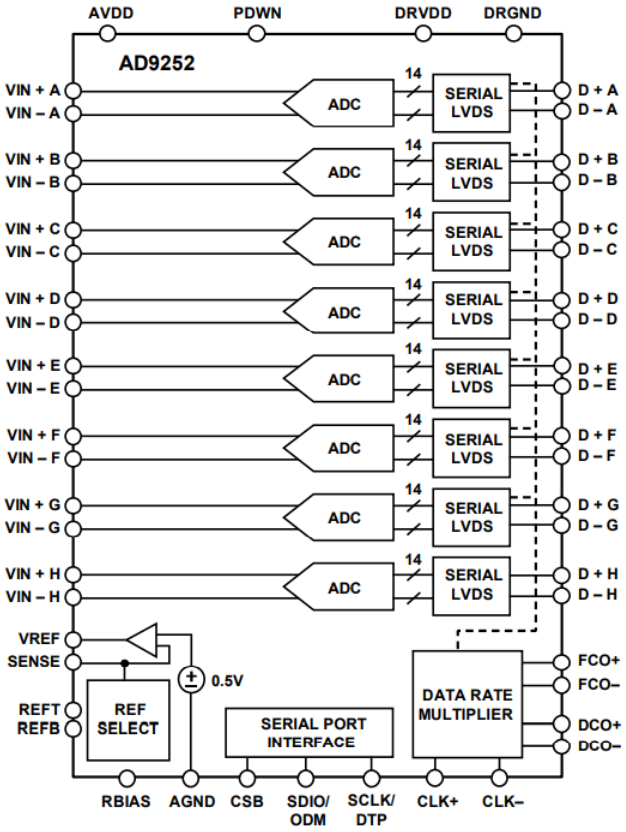
DRS4 output waveform



Quantization

8 chl ADC

AD9252



Parameter	
Channel no	8
-3dB BW	325 MHz
Sampling speed	50 Msps
resolution	14 bits
ENOB	11.8 bits
FSR	< 2 Vpp

ADC output data

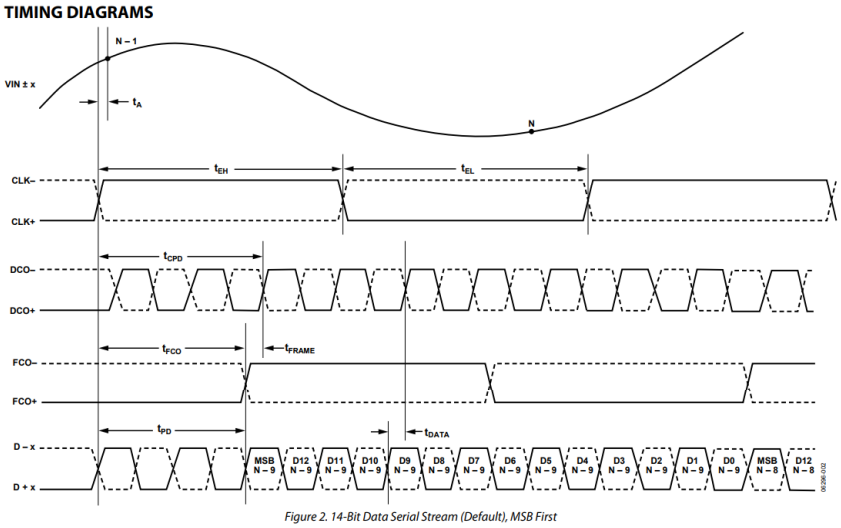
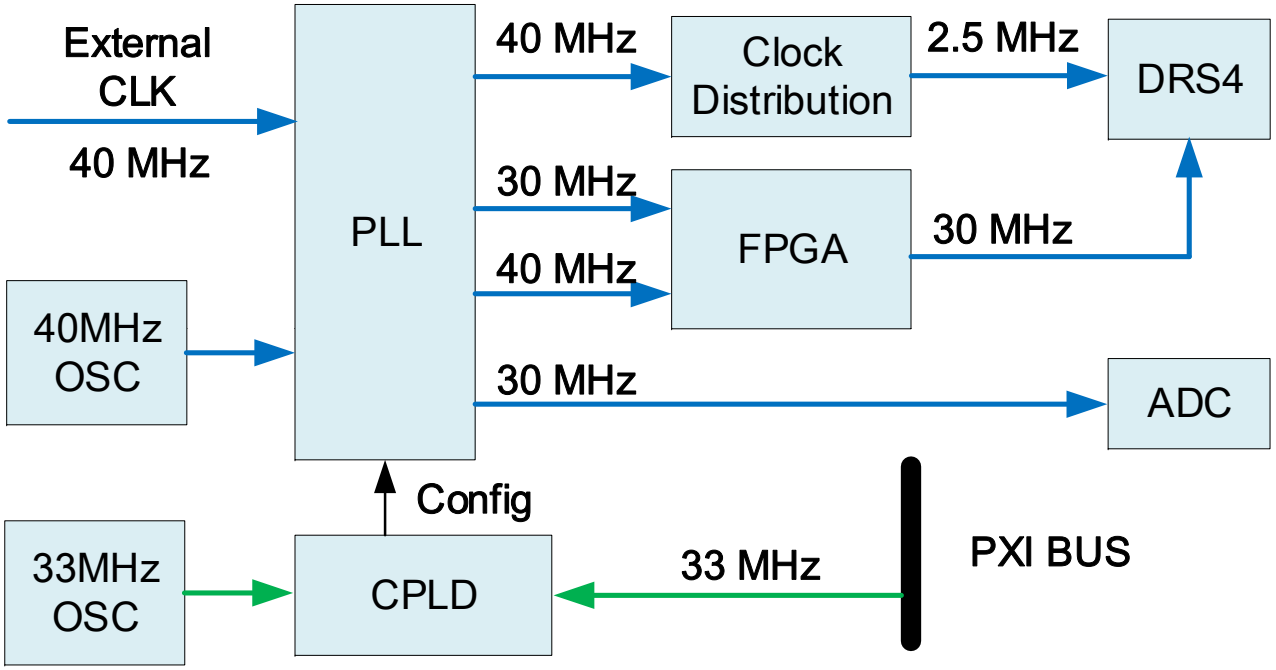


Figure 2. 14-Bit Data Serial Stream (Default), MSB First

Clock circuits



- Main Clock

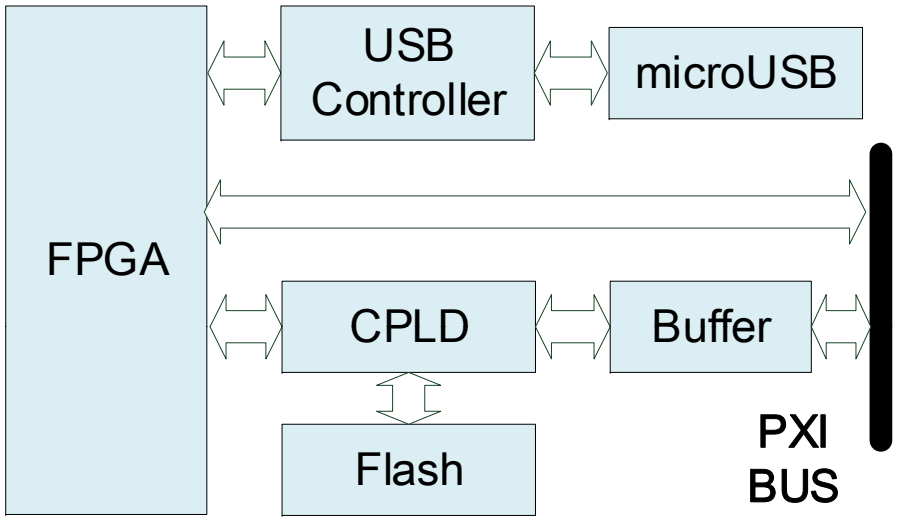
① 40MHz External clock input

② Ref clock for generating the sampling clock & ADC sampling clock are both synchronized with it

- PXI Clock

Used for data transfer based on PXI bus, provided by the backplane of the crate

Data Interface



- PXI interface

① CPLD functions as PXI interface, responsible for data & command transfer, online update of the FPGA logic

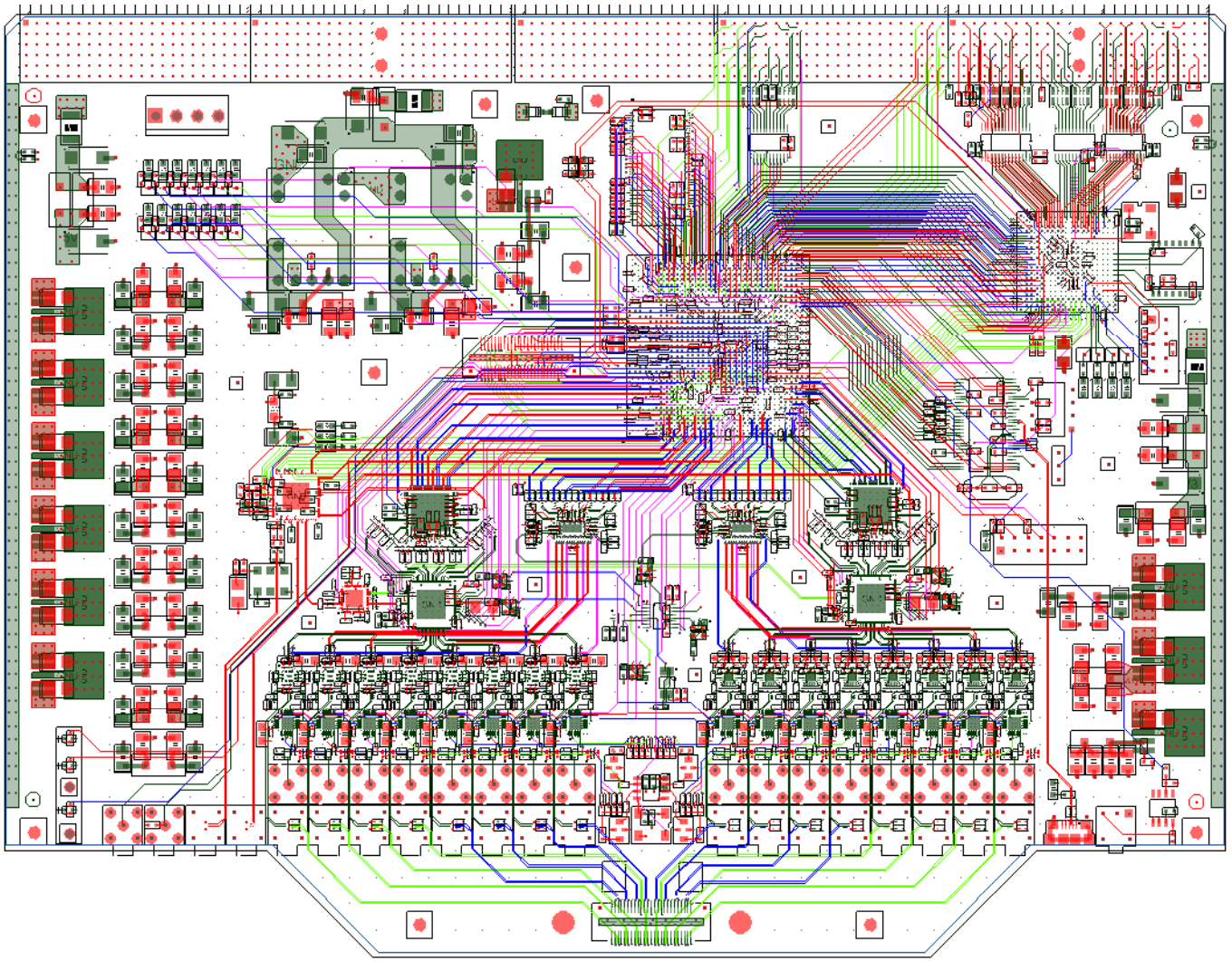
② Trigger signal receiving from the start trigger bus

- USB interface

① Used in debugging mode

② Using CY7C68013A as the USB controller

PCB Layout



Thanks