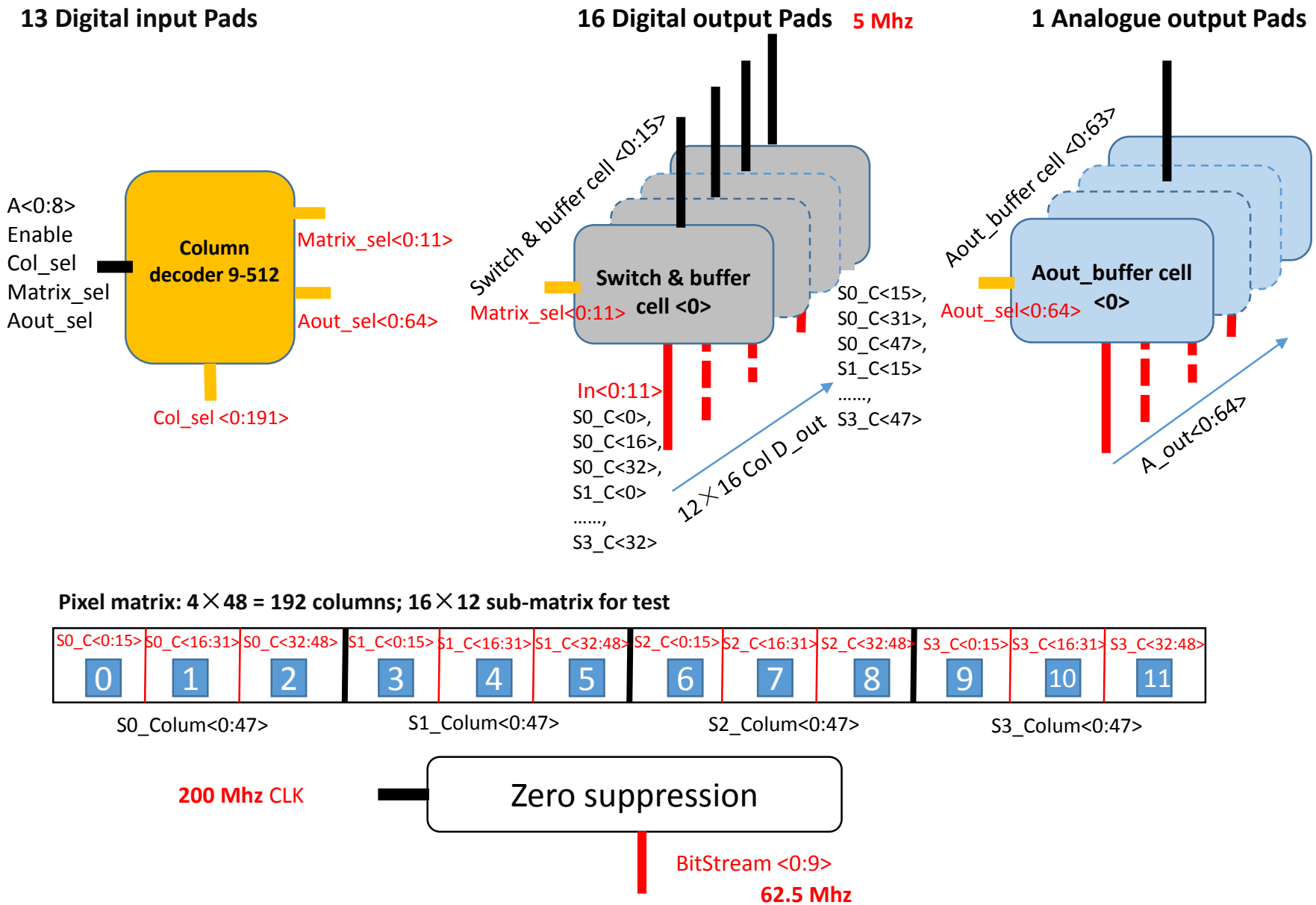
部分可测试性方案设计：


13 Digital input Pads
A<0:8>
Enable
Col_sel
Matrix_sel
Aout_sel
Column decoder 9-512
Matrix_sel<0:11>
Aout_sel<0:64>
Col_sel <0:191>
16 Digital output Pads
5 Mhz
Switch & buffer cell <0:15>
Switch & buffer cell <0>
Matrix_sel<0:11>
In<0:11>
S0_C<0>,
S0_C<16>,
S0_C<32>,
S1_C<0>
……,
S3_C<32>
S0_C<15>,
S0_C<31>,
S0_C<47>,
S1_C<15>
……,
S3_C<47>
12×16 Col D_out
1 Analogue output Pads
Aout_buffer cell <0:63>
Aout_buffer cell <0>
Aout_sel<0:64>
A_out<0:64>
Pixel matrix: 4×48 = 192 columns; 16×12 sub-matrix for test
S0_C<0:15>
S0_C<16:31>
S0_C<32:48>
S1_C<0:15>
S1_C<16:31>
S1_C<32:48>
S2_C<0:15>
S2_C<16:31>
S2_C<32:48>
S3_C<0:15>
S3_C<16:31>
S3_C<32:48>
0
1
2
3
4
5
6
7
8
9
10
11
S0_Colum<0:47>
S1_Colum<0:47>
S2_Colum<0:47>
S3_Colum<0:47>
200 Mhz CLK
Zero suppression
BitStream <0:9>
62.5 Mhz

关键数据端口仿真结果：时钟输入需要LVDS receiver， 数据输出可以直接用Digital pads