中国科学院高能物理研究所
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PixelArray Status & Layout Tips

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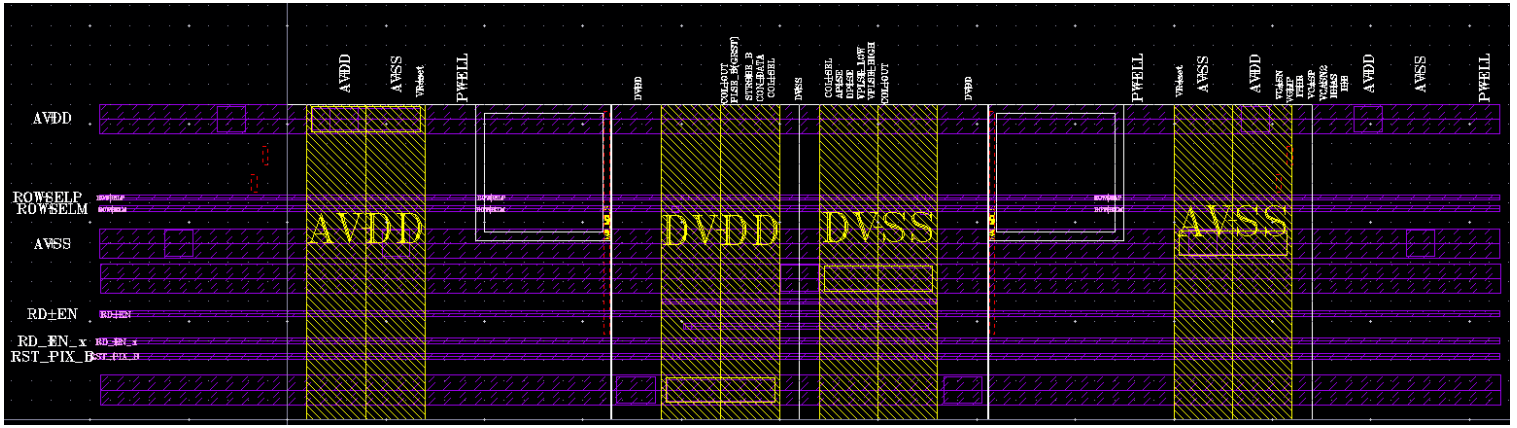
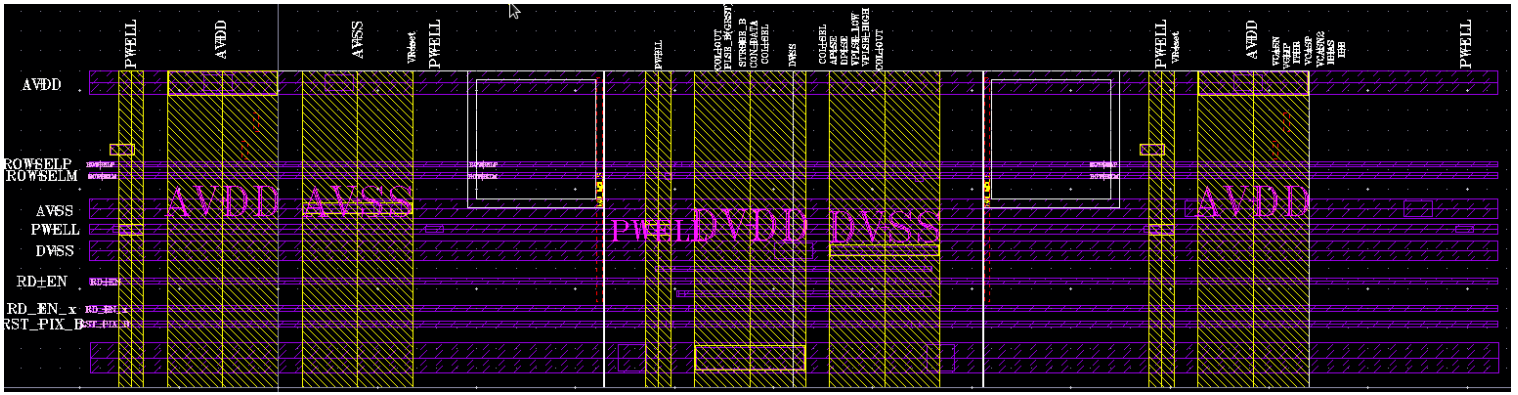
PixelArray_S0

- 新版PixelArray_S0_V1:在之前S0(DG_V0+FE_S0)基础上，使用Front_end_S0_V1及DG_V0



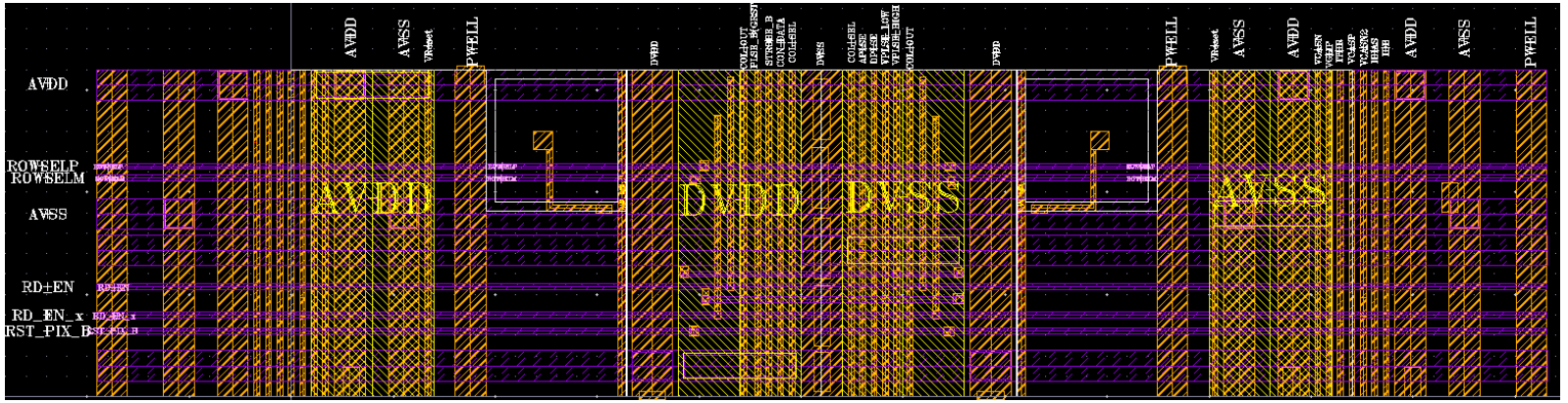
旧版Power mesh



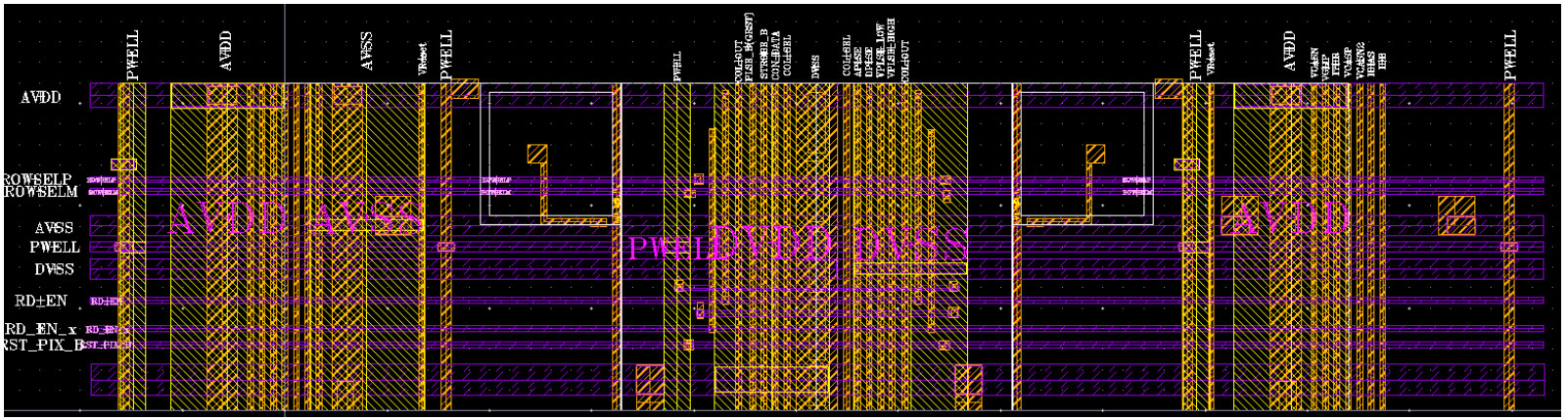
新版Power mesh

PixelArray_S0

- 新版PixelArray_S0_V1:在之前S0(DG_V0+FE_S0)基础上，使用Front_end_S0_V1及DG_V0



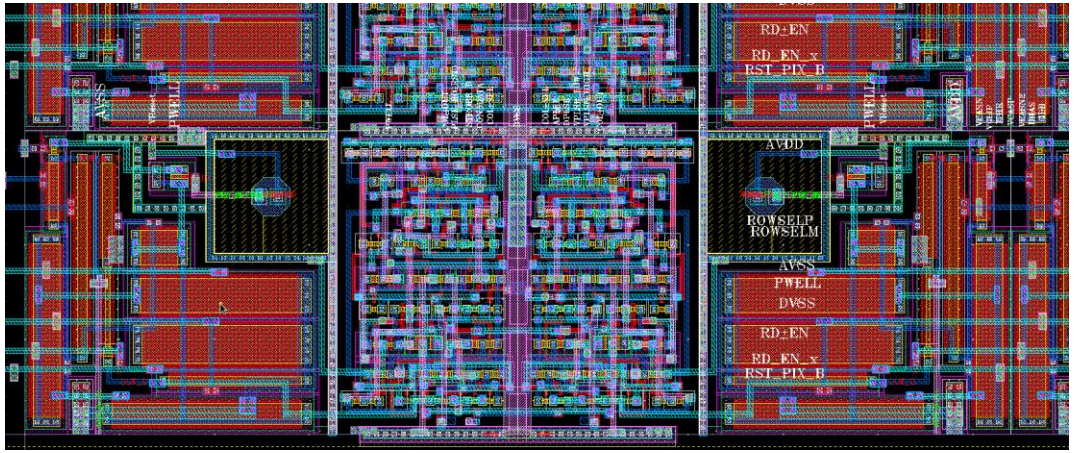
旧版

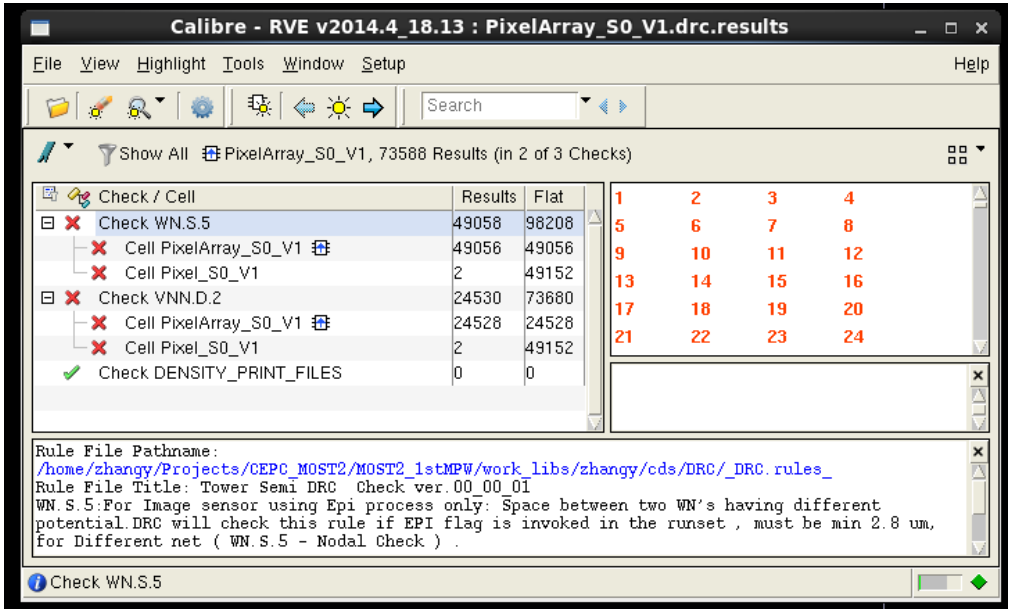


新版

PixelArray_S0

- 通过DRC及LVS验证





PixelArray_S3

- **Pixel_S3 = FE_S3+DG_V0: 26 um × 16 um**
- **Pixel 1x2已完成，采用PixelArray_S0_V1新版布线**
- **PixelArray_S3今天可完成**

Layout Tips

Referenced documents

- **DR2 0018 SL.pdf, DR TS18 IS HR.pdf, Design Rules for TS18 Image Sensor Process.pdf**

- **WPD (Deep P-Well) must cover the whole CMOS Area, excluding:**
  - Deep N-Wells (WB)
    - A fixed distance of 1 [um] between WPD to any WB must be kept
  - Pixel ARRAY_AREA (80dt72)
  - Pixel Array N-Well Guard Ring (77dt106)

WB的用法

- 因为P-SUB 要接负电压（-1 V~ -6 V），阵列外的版图NMOS 管要放在深N阱（WB）中，为了将NMOS 管的衬底和P-SUB 隔绝，隔绝后NMOS 管的衬底可以和VSS 连接在一起接地

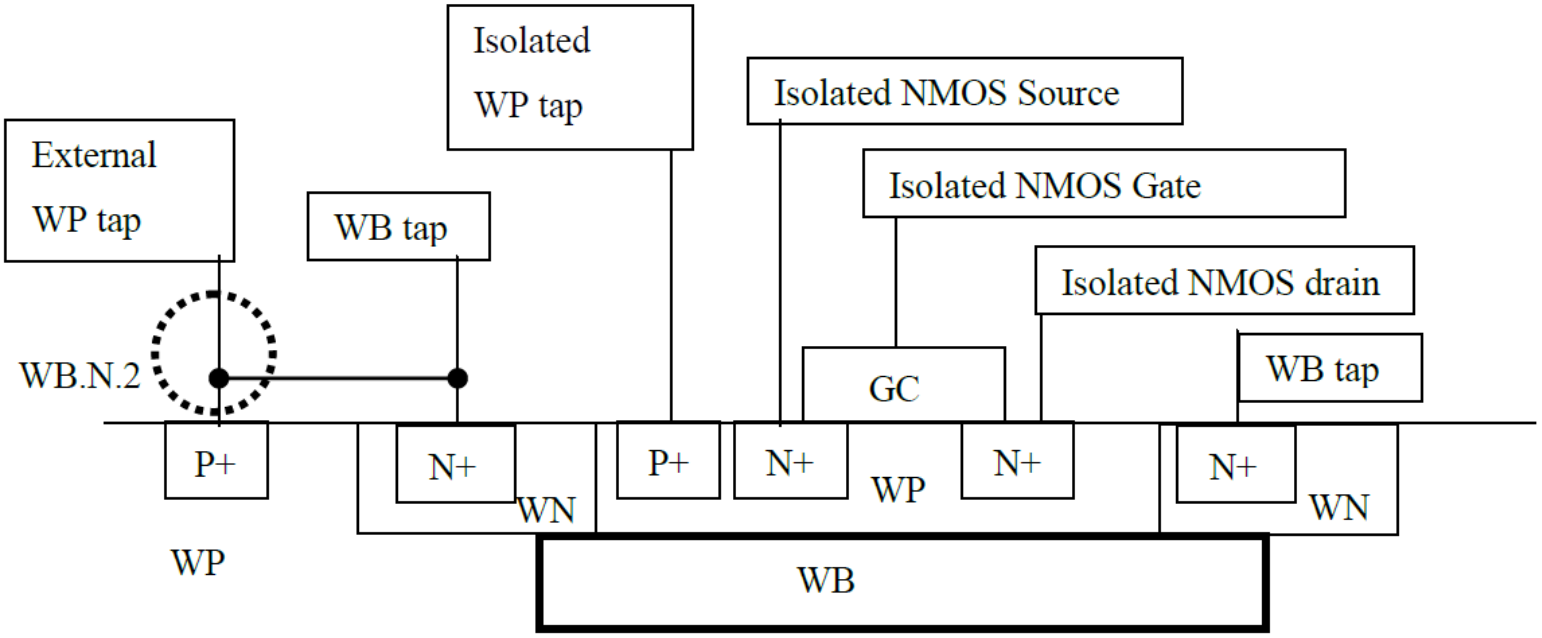


Figure 7-25: Cross Section of WB Region with the Electrical Connections

- 具体DRC rule 参见DR2 0018 SL.pdf （p122-p124）
  - 增加WB后，会产生寄生二极管，过LVS时需要在原理图上添加寄生二极管器件（ddwnpw18，ddwnps18）才能过 LVS

外围电路中PMOS的画法

- **NMOS，PMOS均画在WB中**
  - 单个模块正常版图画好后，整体加入WB
  - 基本版图画法无需改变，方便、画法简单，
- **PMOS放在另外的WN（N阱）中，需要被WPD覆盖。WN与NMOS的WB/WN有间距要求，WPD和VNN需要在每个block的版图中加**

WB的用法

- WB/WN外围一圈VNN（没有P型注入），为了消除WB/WN和WPD/substract 之间的寄生二极管，防止衬底负偏压影响各个阱电位，影响mos 管工作。VNN 外再加WPD和P+ SUB 接触；