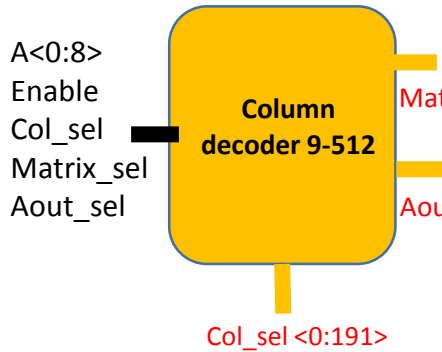
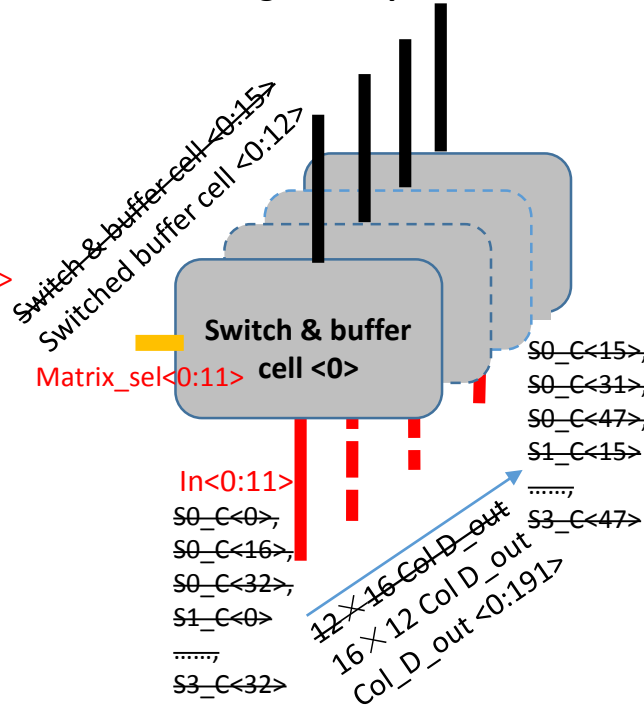


部分可测试性方案设计修改:

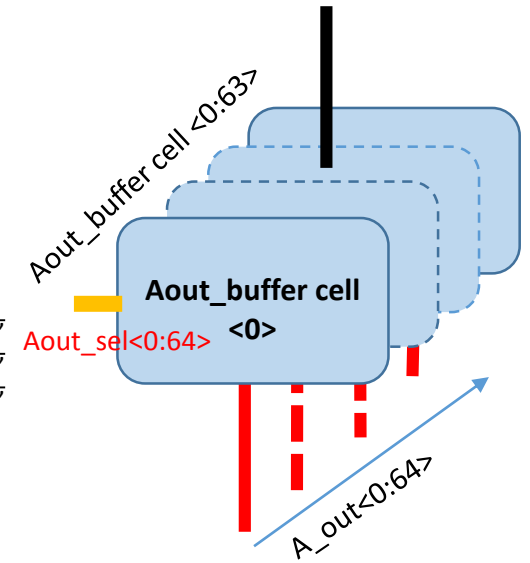
13 Digital input Pads



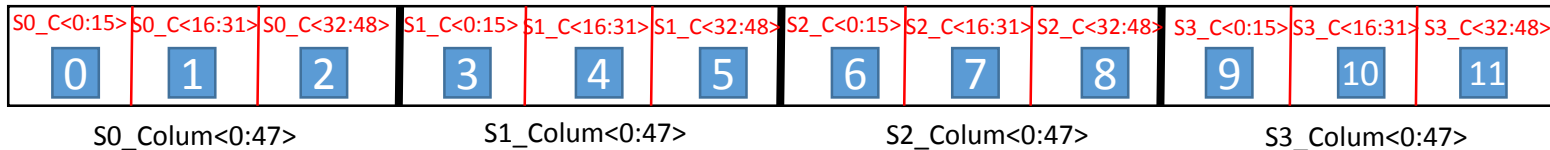
16 Digital output Pads 5 Mhz



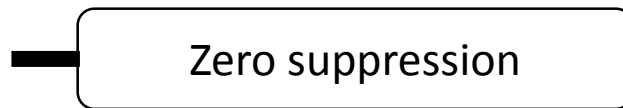
1 Analogue output Pads



Pixel matrix: 4 × 48 = 192 columns; 16 × 12 sub-matrix for test



200 Mhz CLK

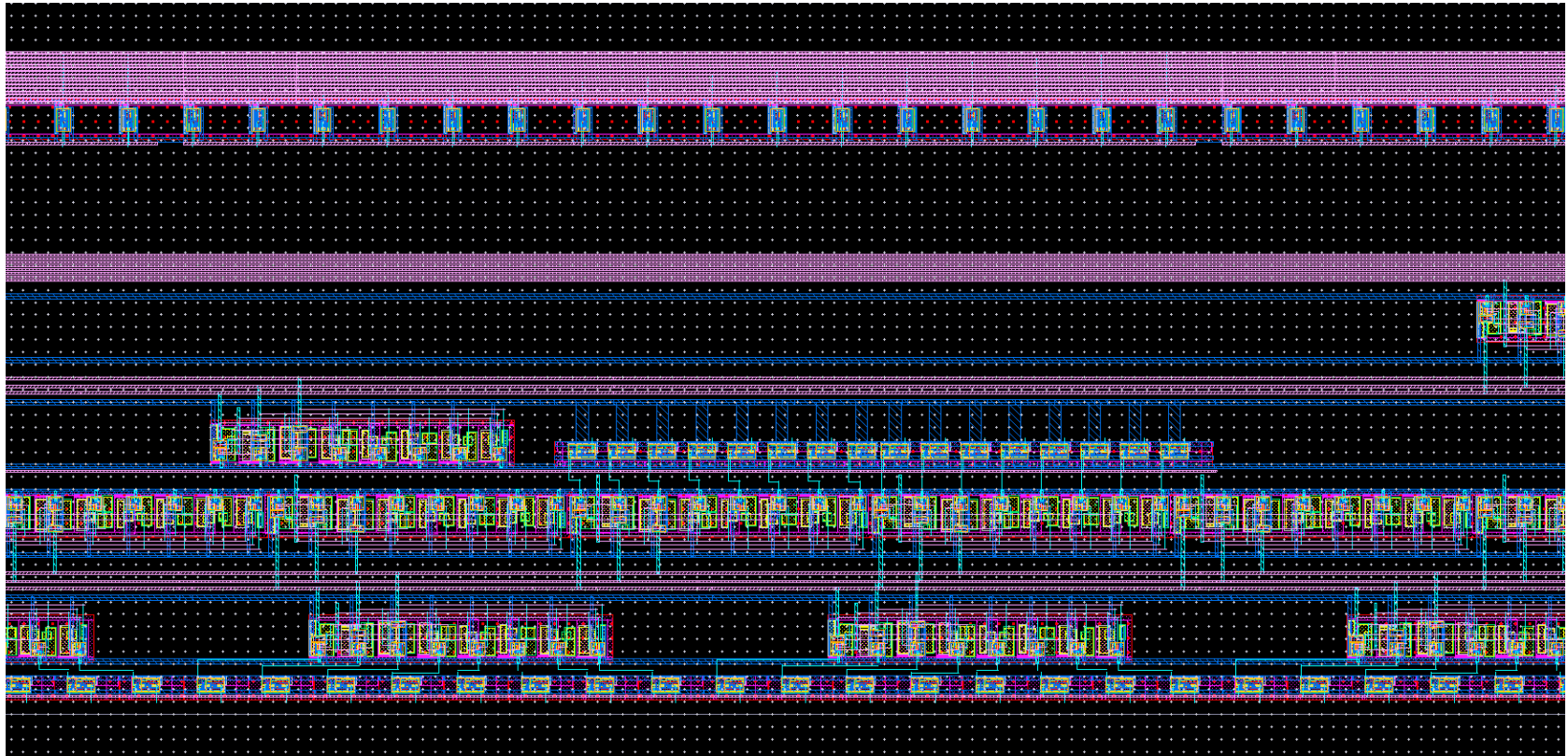


BitStream <0:9>

62.5 Mhz

Col_Decoder及可测试性模块版图进度:

- 基本模块完成, 版图尺寸: 大约 $300\text{ um} \times 4900\text{ um}$ (宽度与像素一一对应)
- 等待像素面阵完成后与各列级信号线位置匹配连接;



Questions:

- 像素外围所有模块的Deep-nwell, 各个小模块单独完成 or 整体放在一个深井里?
- 像素面阵之外的所有部分, 全deep-nwell覆盖 or 电路部分各模块deep-nwell覆盖+其余部分不覆盖 or 电路部分各模块deep-nwell覆盖+其余部分deep pwell覆盖?
- deep-nwell外围加一层VNN环绕, 是否需要违反DRC规则? (距离nwell $0.16\text{ or }0.05\text{ or }0\text{ um}$?)