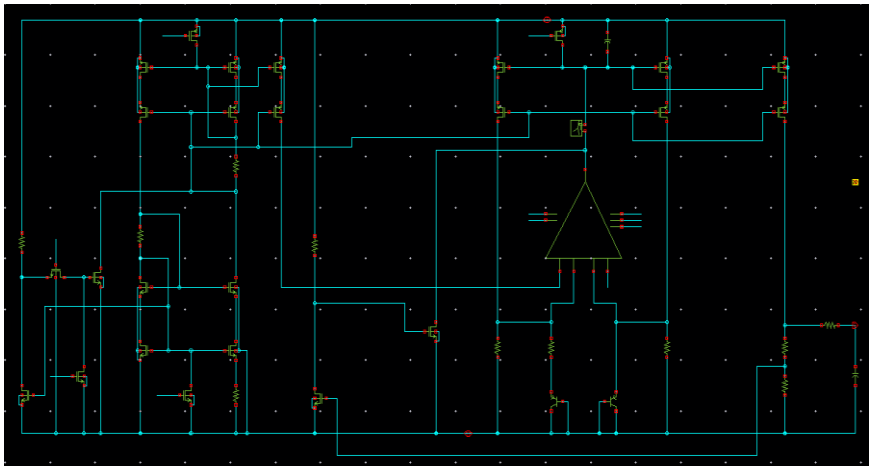
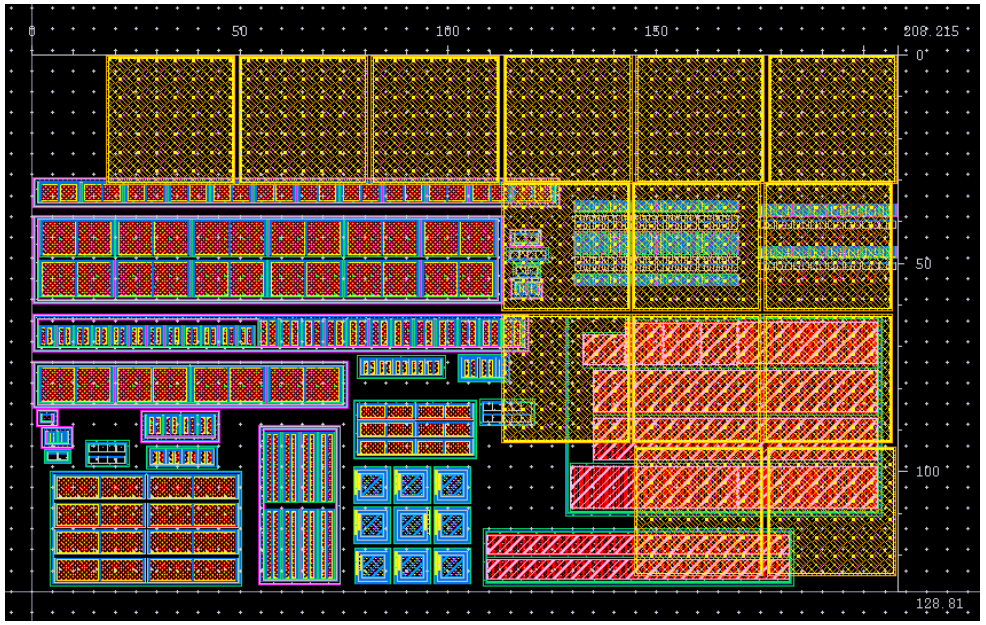
Bandgap 1.2V @ 1.8V power supply



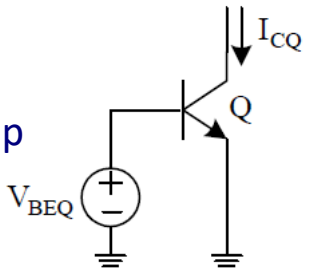
Schematic



Layout: 130 x 210 μm^2

- **Concept of V_{REF}**
  - V_{BE} decreases slight non-linearly with temperature
  - V_T （~kT/q） increases linearly with temperature
  - $\Delta V_{BE} = V_T \cdot \ln(N) = V(T)$
  - Weighted sum of V_{BE} and V_T results in low-temp dependence reference voltage
  - $V_{REF} = V_{BE} + V(T) \uparrow \approx 1.205V@27°C$ ($V_T \approx 26$ mV)

    a small and temp-dependent voltage



$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \quad (1)$$

$$V_{BE} = \frac{KT}{q}\ln\left(\frac{I_C}{I_S}\right) \quad (2)$$

芯片减薄

1. 减薄的die size ≥ 1mm x 1mm;

2. die能做到的最小减薄: 50um;

3. 8寸wafer级减薄能够做到的最小减薄: 60um左右；

4. 公司做过的最小减薄为30um，但是成品率比较低；

5. die减薄费用20K RMB起，wafer级减薄费用根据尺寸、材料和具体需求计算。