Research Activities in ECOPICS

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on behalf of the ECOPICS project (IPHC, IHEP, SDU, CCNU)

Outline

- Part of research activities in ECOPICS (Electron collider oriented pixelated CMOS sensor development)
- A CMOS pixel sensor (CPS) detector prototype study
- CMOS pixel sensor design and planed MPW run with IPHC

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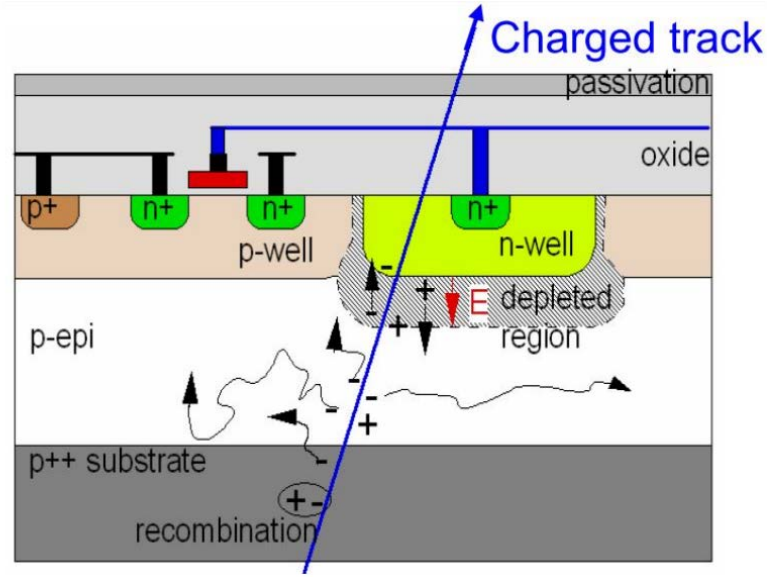
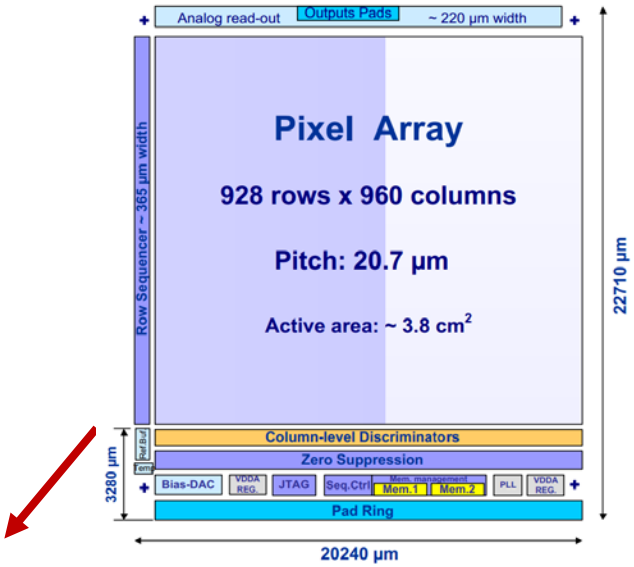
CPS and prototype for BESIII MDC Upgrade



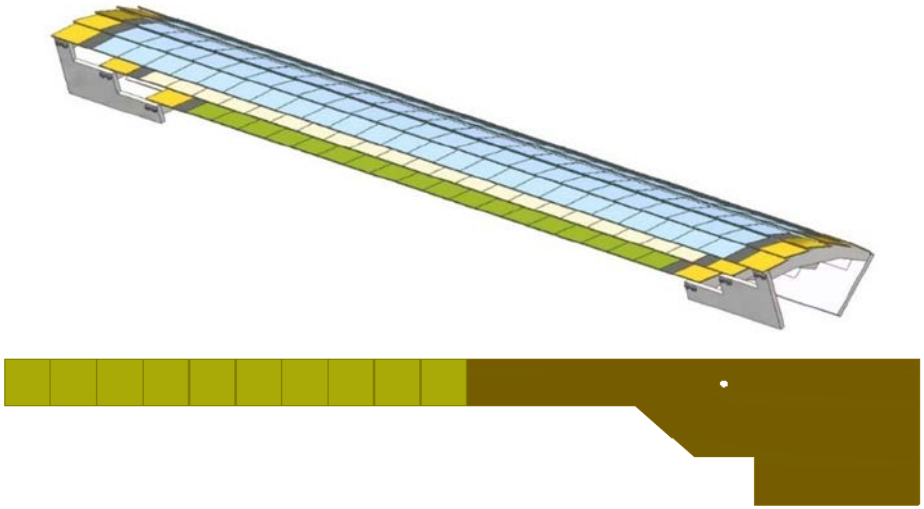


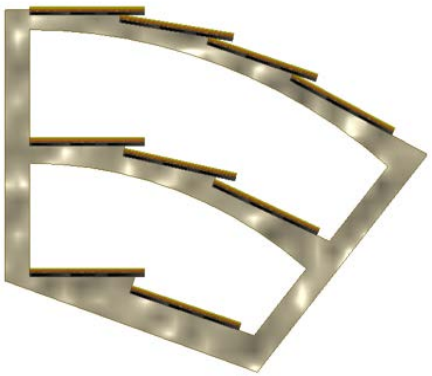
- CMOS pixel sensors have attractive features: low material budget, low power consumption, high spatial resolution and low cost
- Initiated by IPHC in Strasbourg
- Used for the STAR pixel detector, the ALICE ITS upgrade and the CBM MVD.
- Also for ILC, CEPC, …. R&D

A MIMOSA28 sensor designed for the STAR PXL detector is selected as one of the prototype schemes for the inner MDC upgrade

- Density: 20.7µm pixel pitch, ~0.9Mpixels/chip
- Spatial resolution: ~3.5µm
- Rating capability: ~10^6Hz/cm^2
- Material budget: ~50µm thick
- Radiation tolerance: ~1 MRad, 10^{13} n_{eq}/cm^2
- Room temperature operation

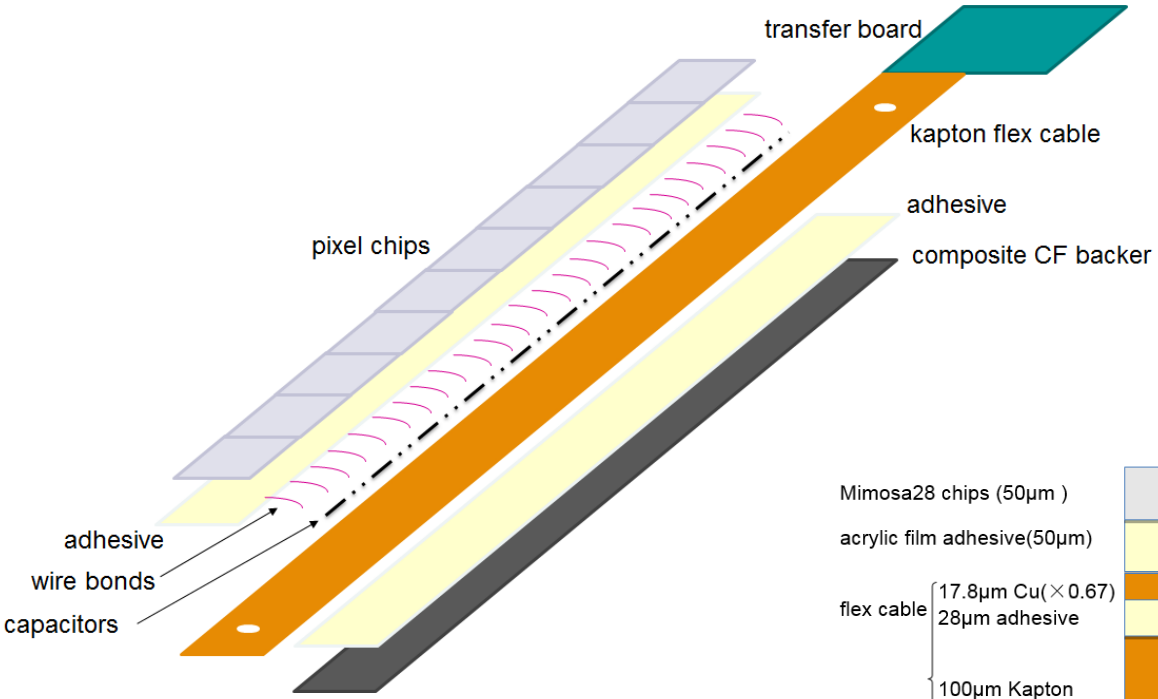
R&D target: a CPS Prototype

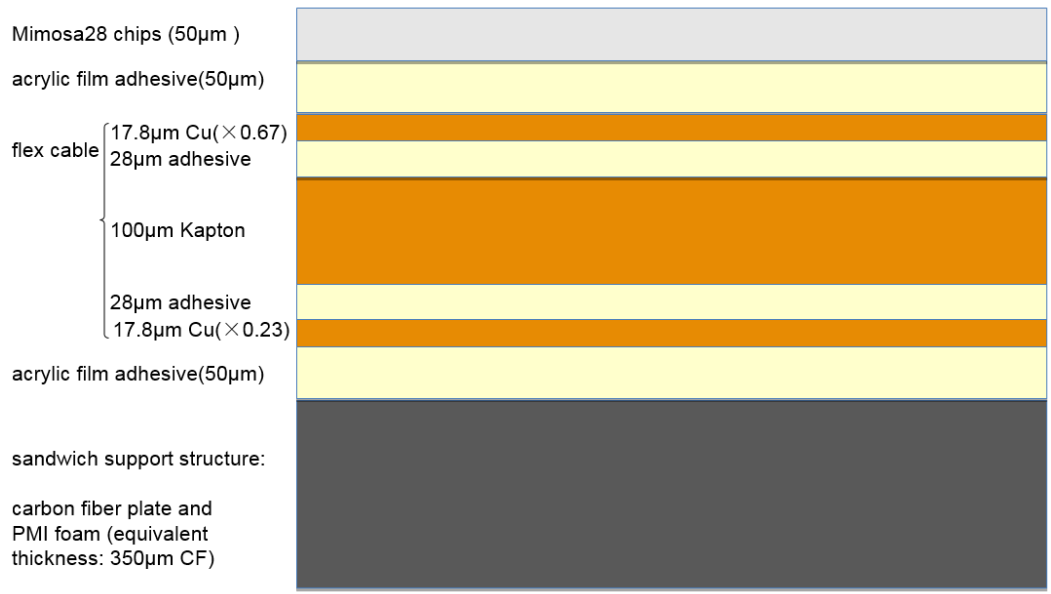




- A CPS detector prototype
  - 1/10 Coverage of the inner tracker (~ 720cm^2→180 chips→180M pixels)
  - ϕ direction: 2 , 3 and 4 ladders for the 1st, 2nd and 3rd layer respectively
  - Z direction: 2 sets of ladders each layer
  - 10 Mimosa28 chips with dimension of 2cm×2cm in each ladder

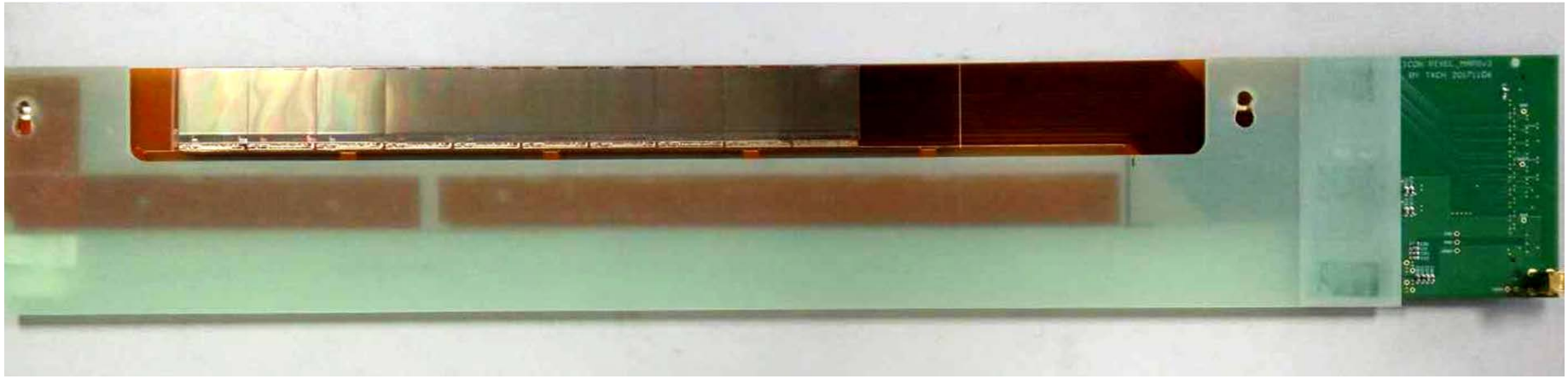
Ladder Design



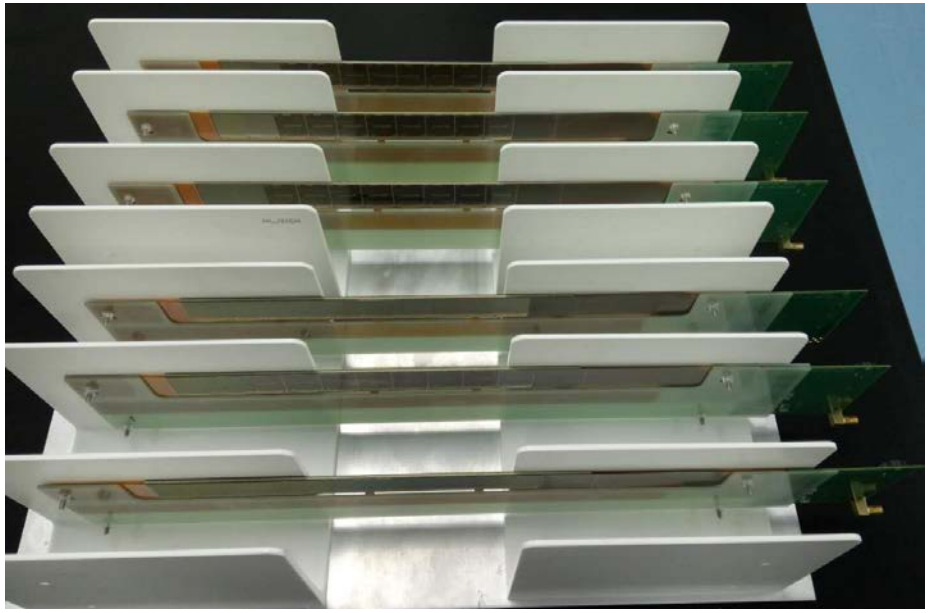


- Ladder: basic building and functional block of the detector, key issue for the prototype
  - 10 Mimosa28 chips (50μm)
  - Flex cable
  - Carbon fiber mechanical support

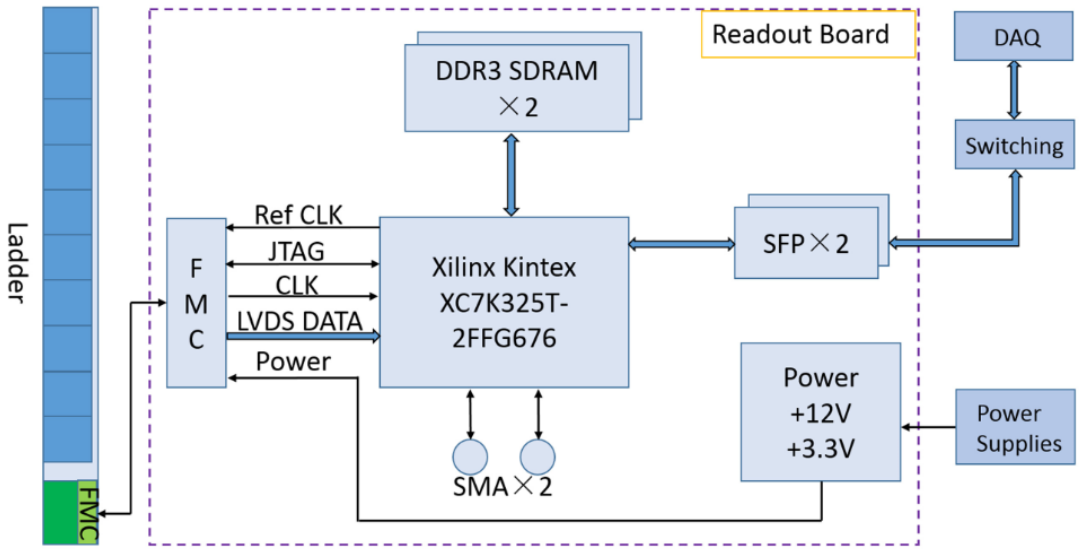
Ladder Assembly



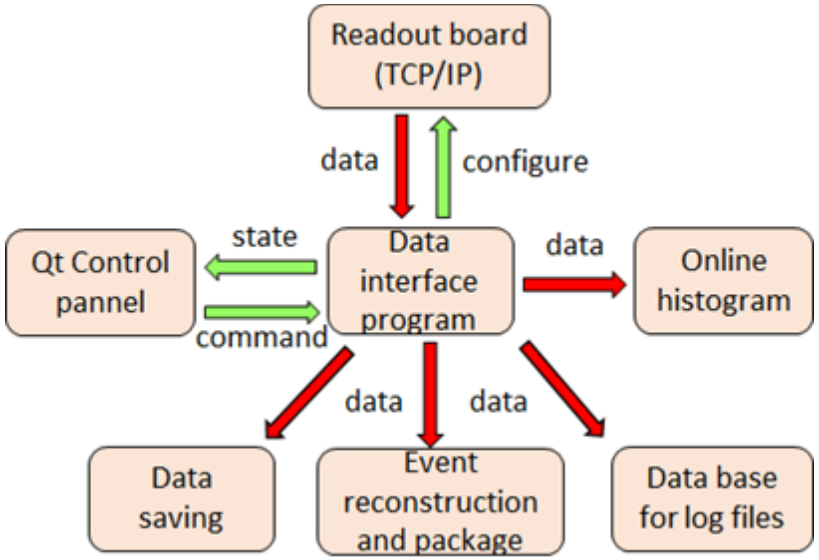
- Ladder assembly was operated at a dedicated jigs to ensure the location accuracy of the chips
- Material budget of the ladder by calculation: 0.37% X_0 /ladder
- Chip location accuracy measured by imaging machine: < 10μm



Readout Electronics and DAQ



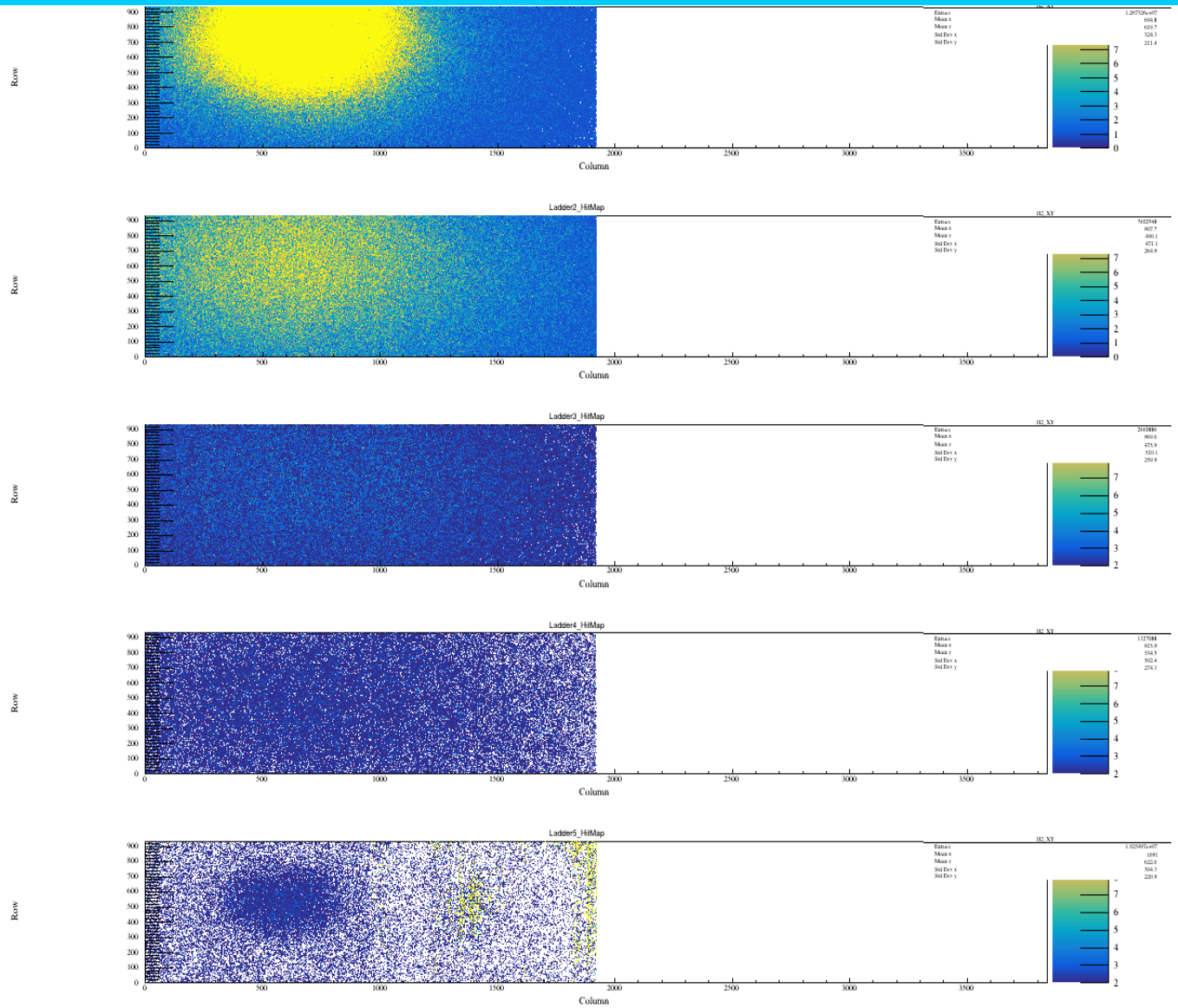
- Distributed system
- Ladder → FCB → Readout Board → Switching → PC
- SiTCP : high-speed and highly reliable data transmission
- Readout speed: 30~40MB/s/ladder



Test in IPHC

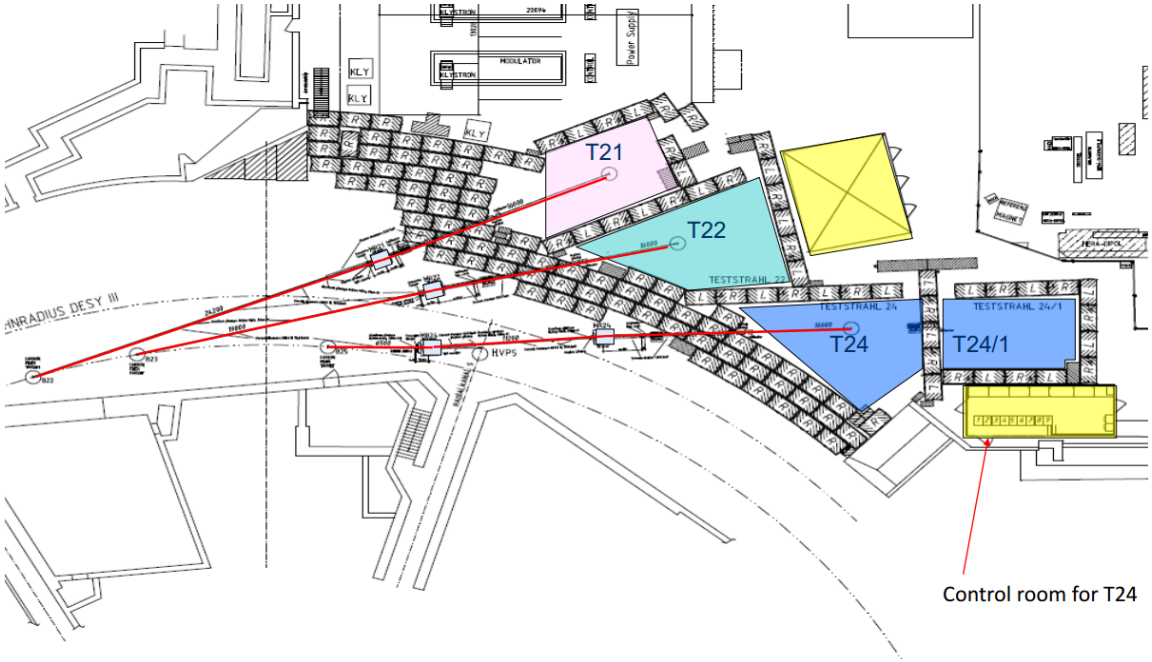
- Test system was shipped to IPHC in October, 2018
- We did noise test, threshold scan, radioactive source test, stability test, … to make sure the system works well in beam
- We also discussed and determined the beam test plan in DESY

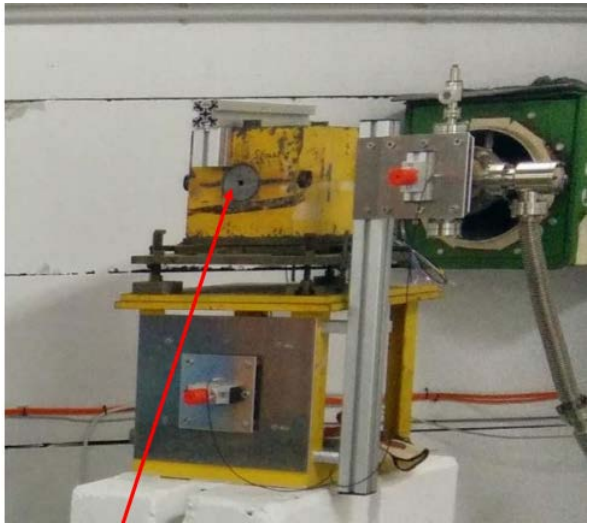
Test in IPHC



- Test with Sr-90 source. Chips response by using a collimator

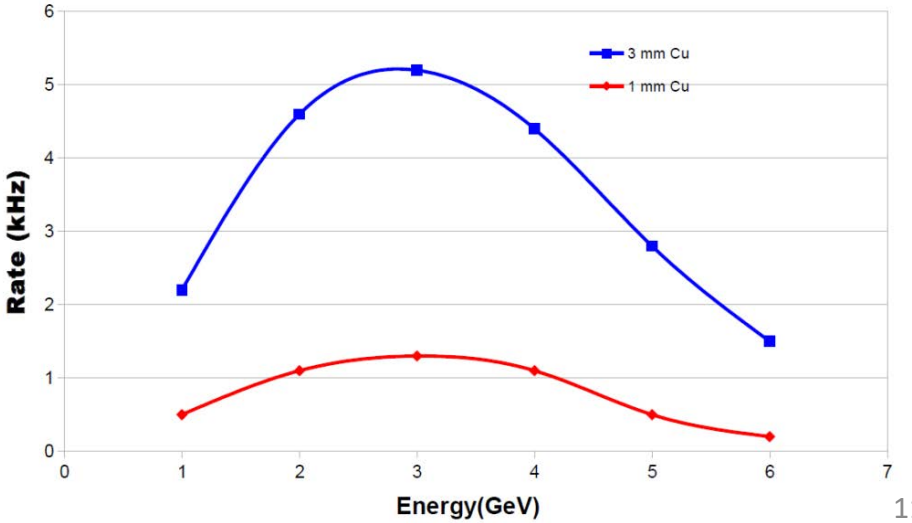
Beam Test in DESY





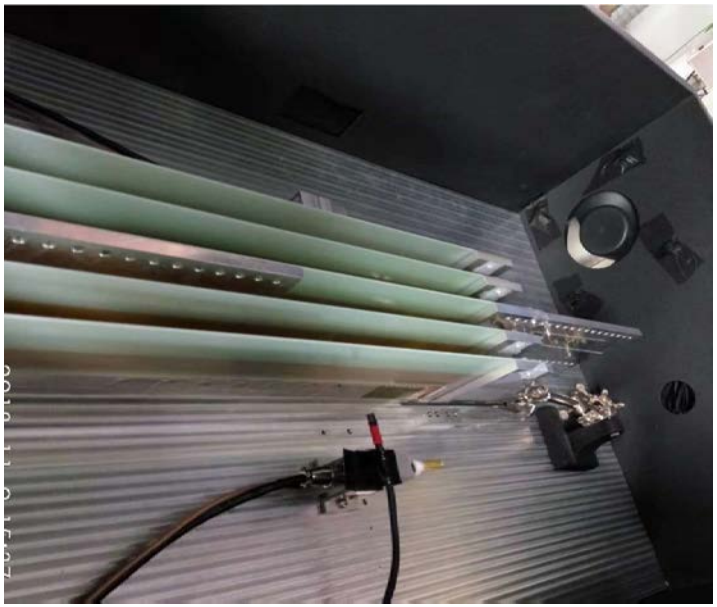
lead collimator

- T24 testbeam
- PICSEL group from IPHC, Strasbourg and Chinese group from IHEP
- November 5-11, 2018

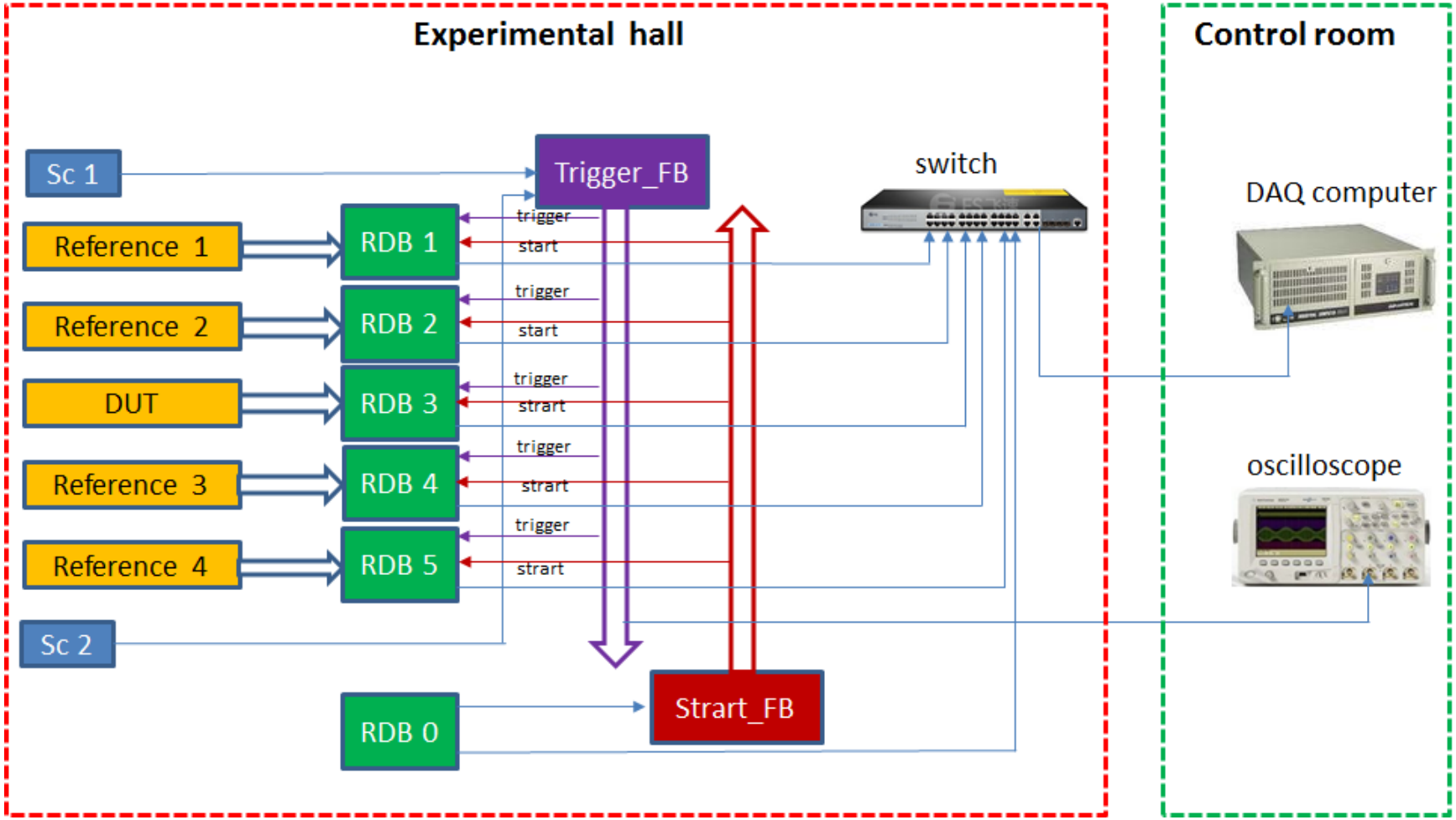


Beam Test in DESY

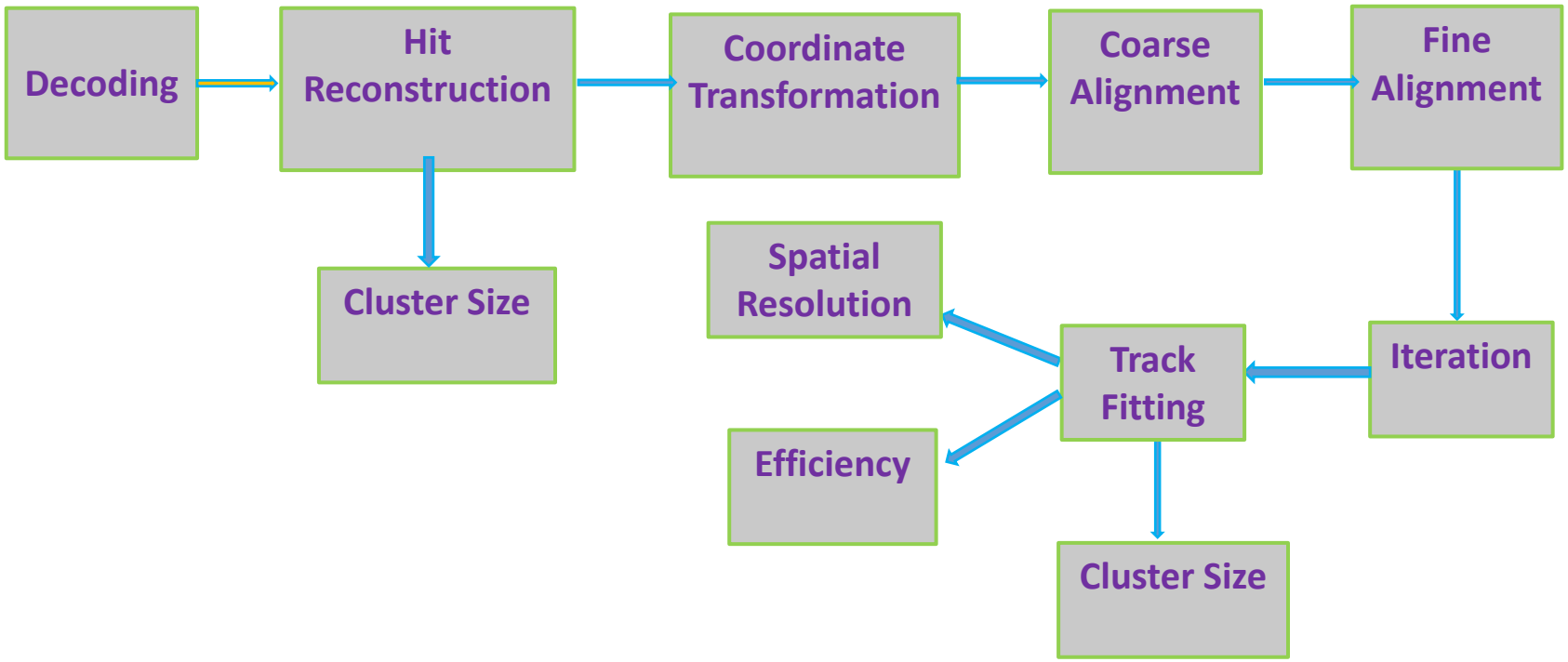
- Energy Scan
- Ladder scan
- Threshold scan
- Gap between the neighboring chips
- Material budget test
- Target scattering test
- Cooling air flow



System Setup

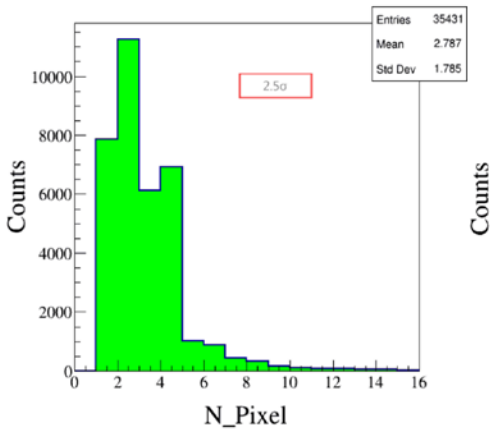


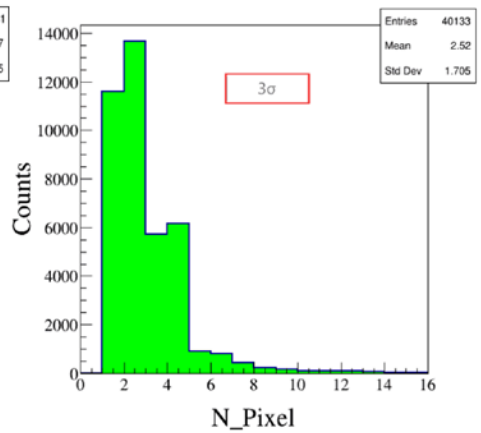
Analysis Software Framework

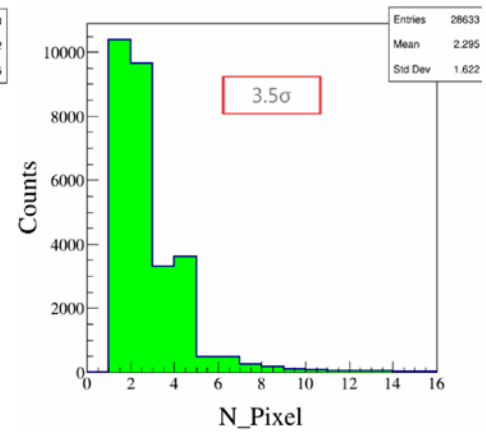


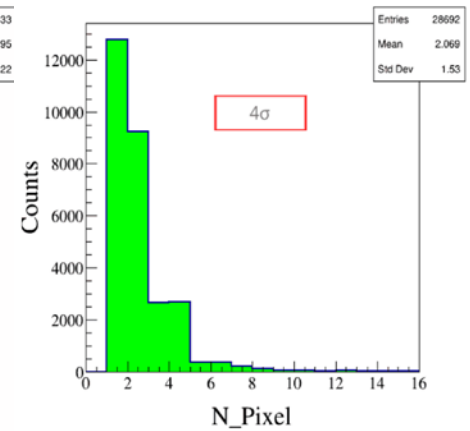
- Hit reconstruction : cluster size, digital signal, no seed
- Alignment: high precision
- Tracking:

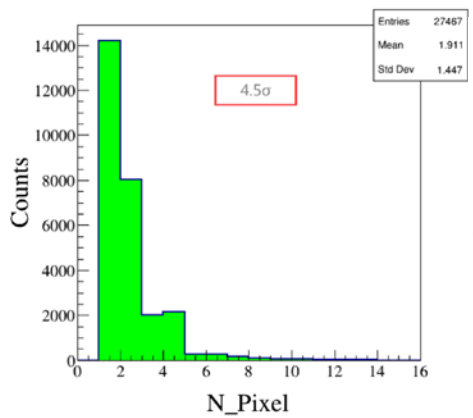
Cluster Size Analysis

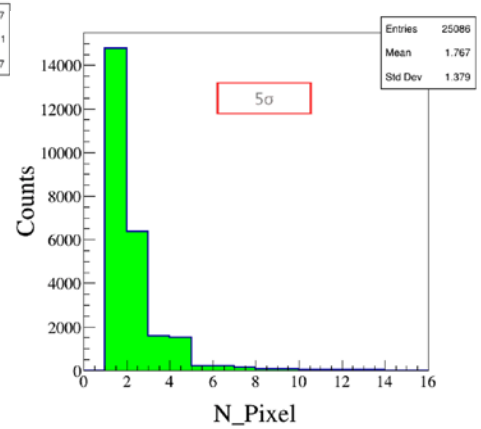


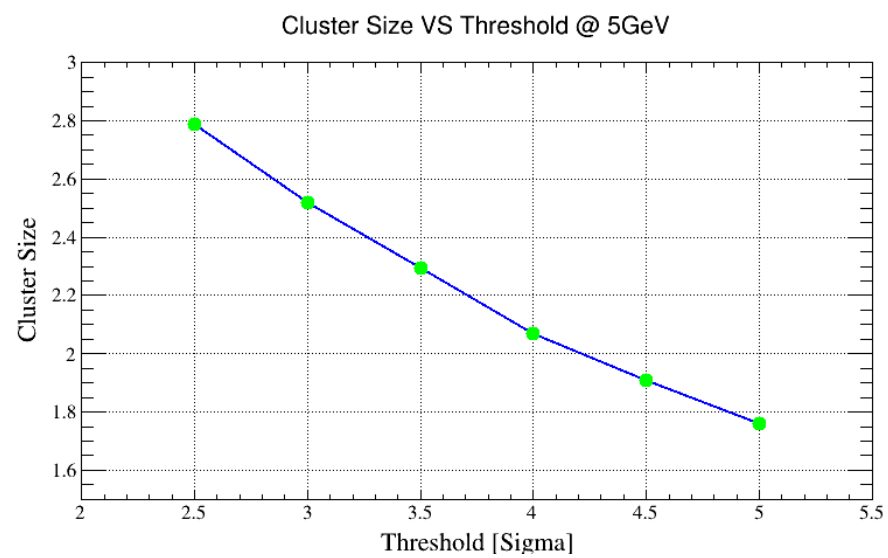






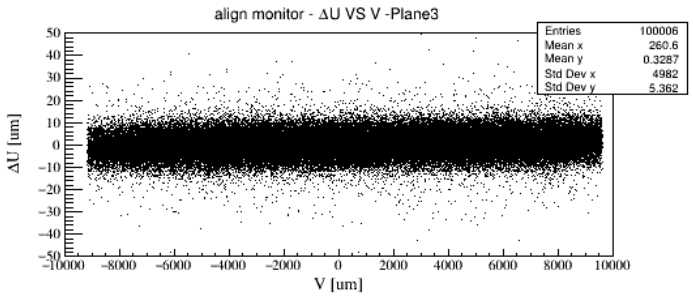


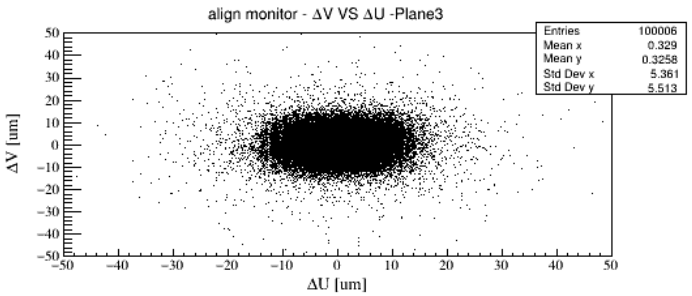


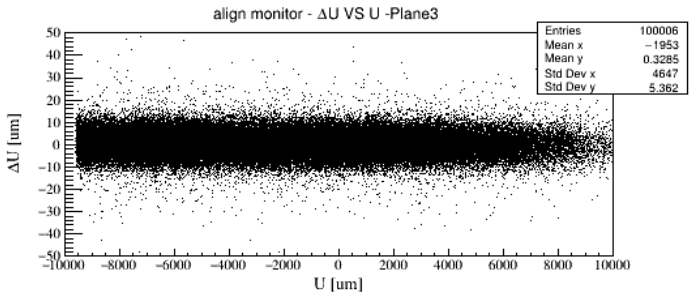


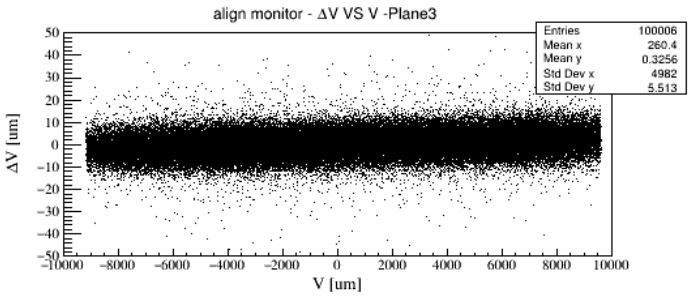
- Charge collection by thermal diffusion
- Charges sharing: one hit can lead to several fired pixels, be benefit to spatial resolution
- Reconstruction algorithm

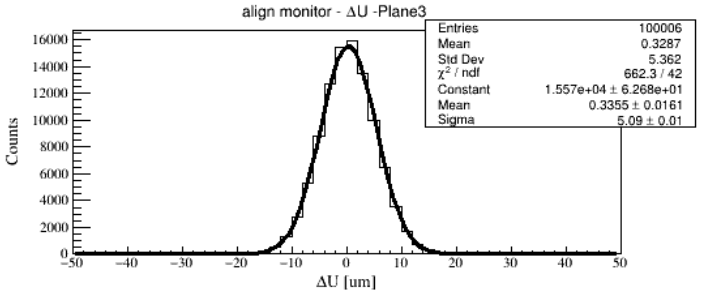
Alignment Results

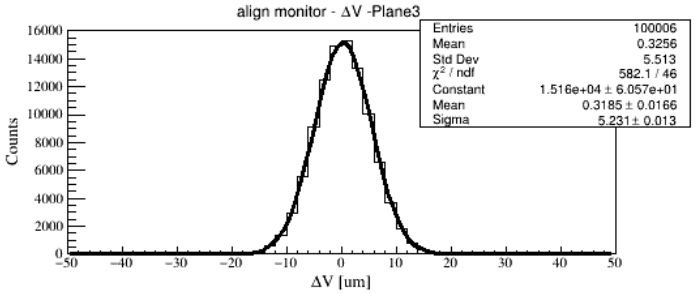


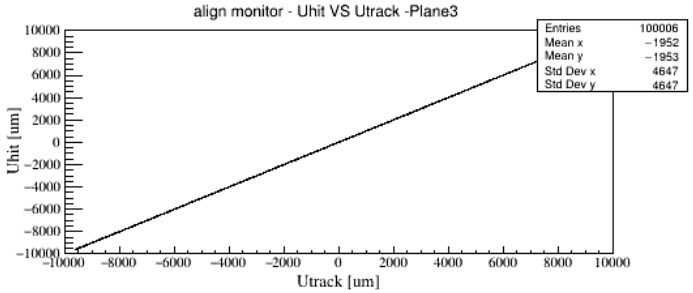


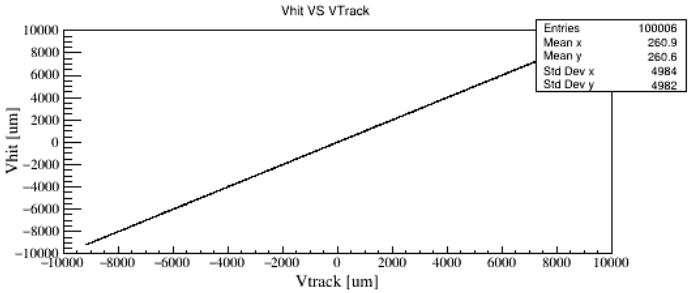




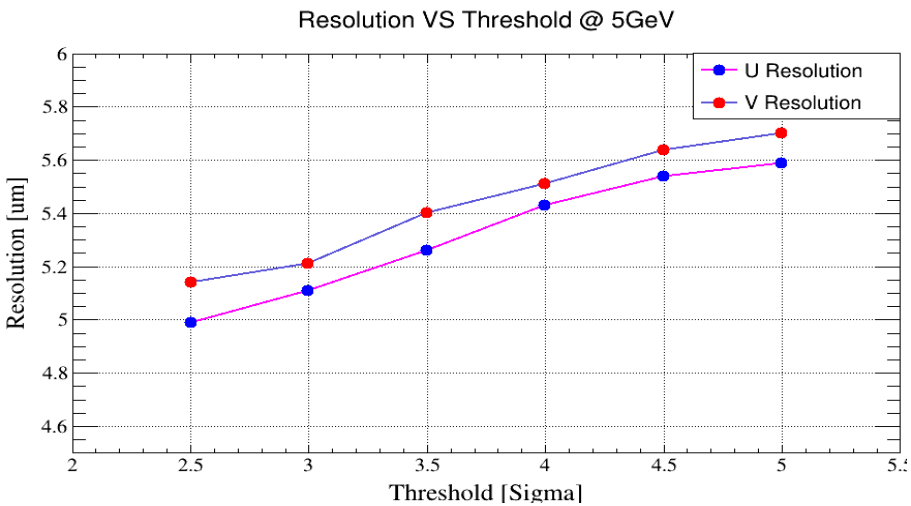




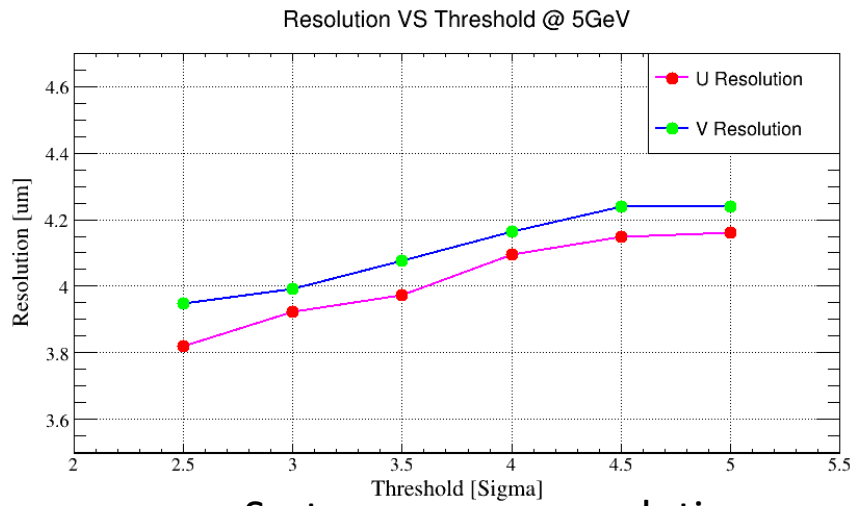




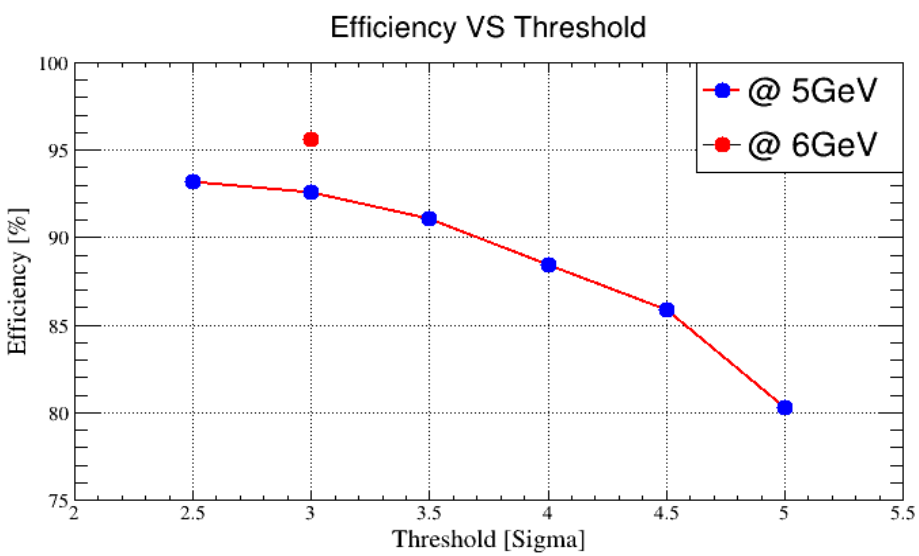
Spatial Resolution and Efficiency



DUT resolution

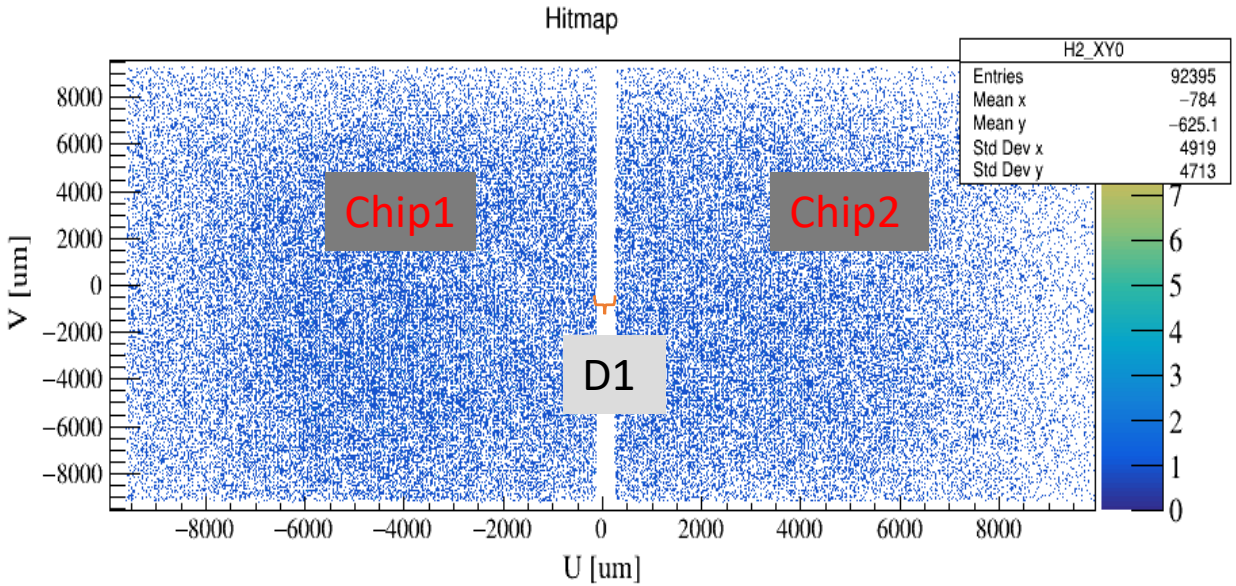


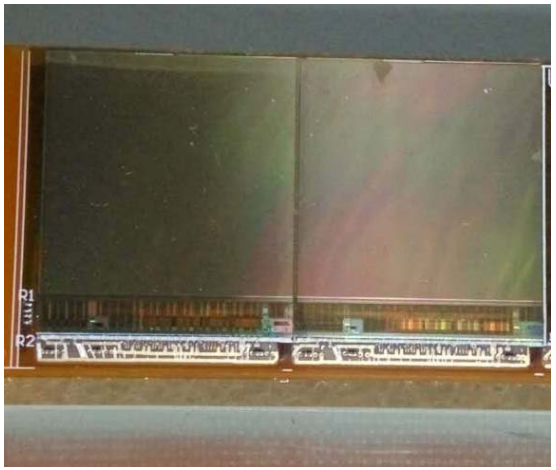
System average resolution

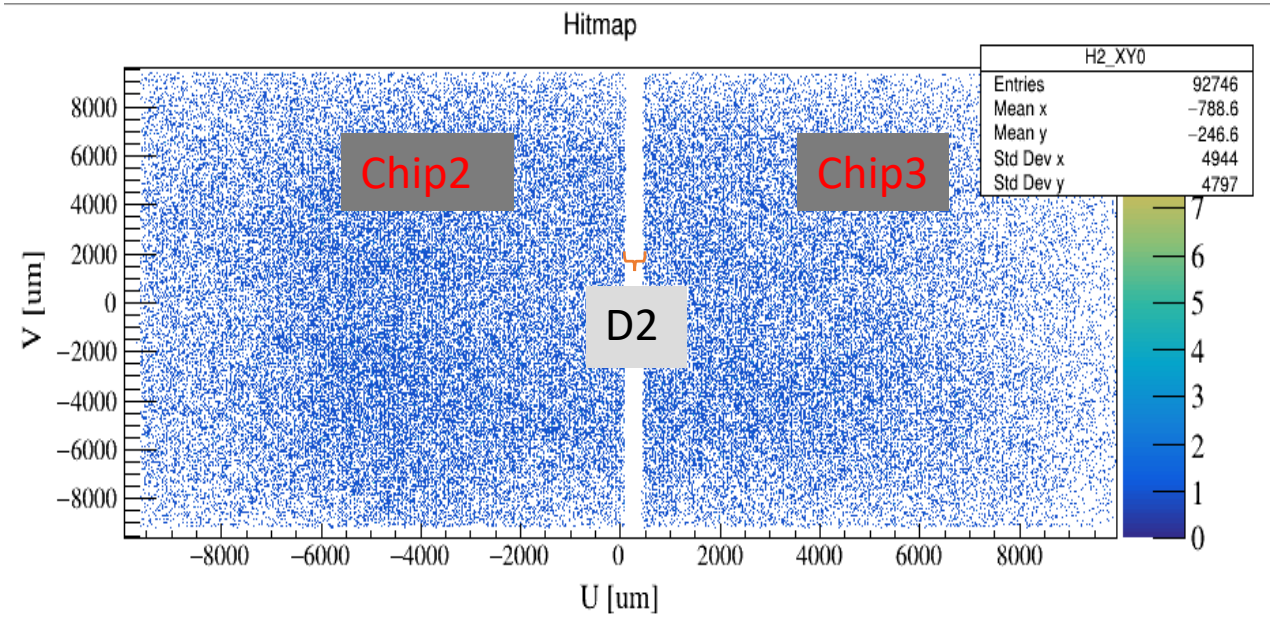


- The efficiency of MIMOSA28 was near 100%.
- The lose of ~4% of the efficiency in this test is due to the readout and DAQ system
- The readout and DAQ system will be updated and tested

Gap between two chips





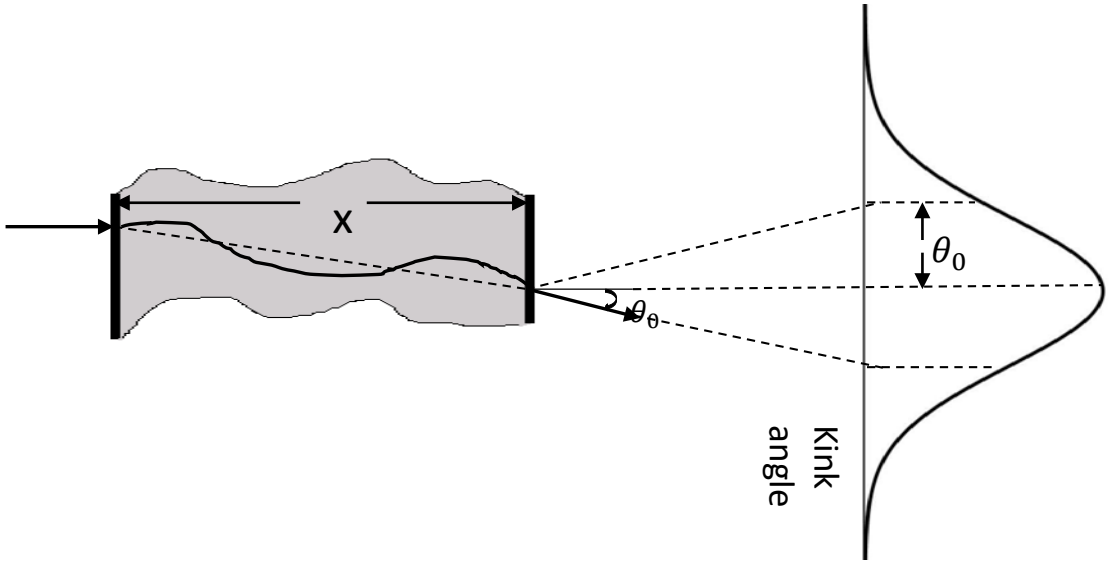


- D1≈D2 ≈ 340μm
- Average gap between neighboring chips is 340μm
- Take into account the row sequencer on the chip, chip location accuracy is better than 10μm

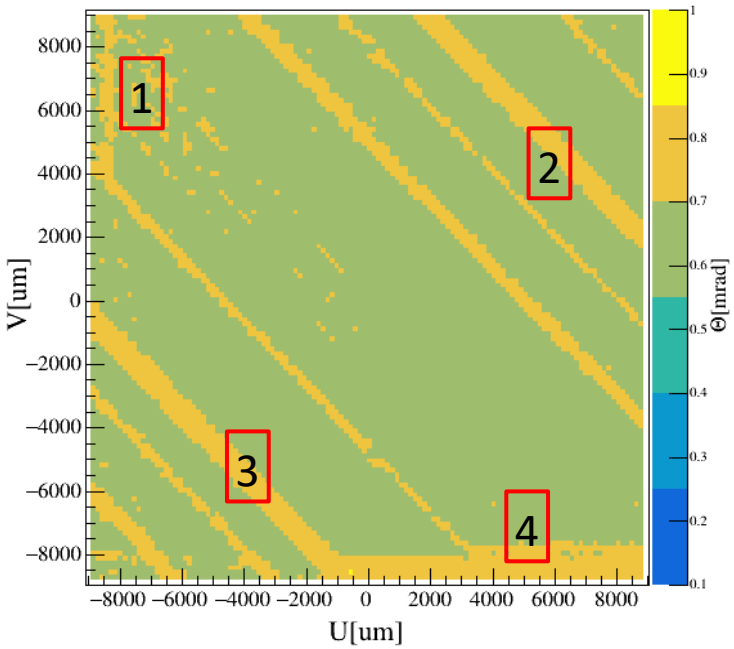
Multiple Scattering

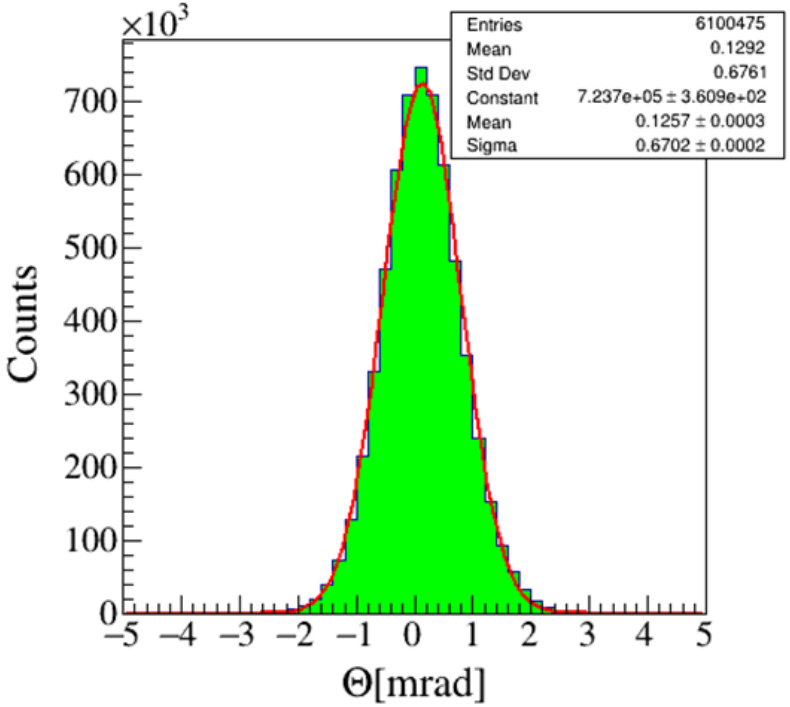
- High-energy particles undergo **multiple coulomb scattering** when passing through the material;
- Kink angle depends on **material budget (x/X_0);**
- The **width of the gaussian-like center** is well predicted by the Highland formula;
- Highland formula: $\theta_0 = \frac{13.6MeV}{\beta cp} Z \sqrt{\frac{x}{X_0}} \left(1 + 0.038 \ln\left(\frac{x}{X_0}\right)\right)$

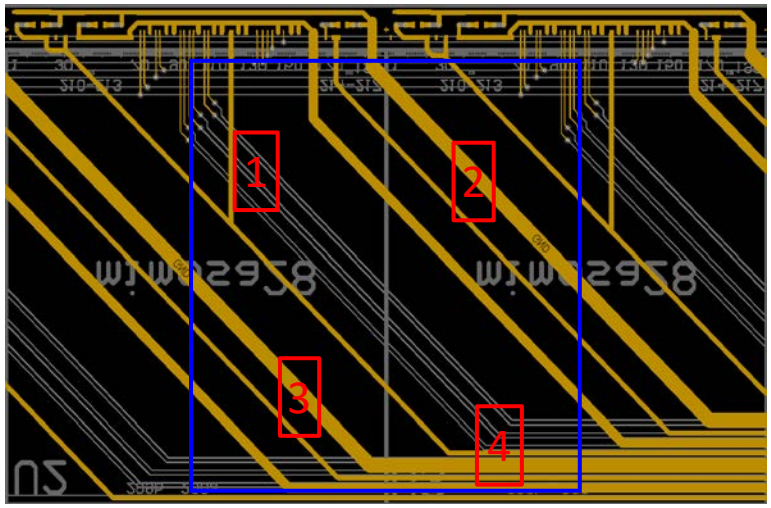
θ_0= RMS of scattering angle
z = charge of incident particle
x = material thickness
X_0 = radiation length



Material budget







$$\theta_0 = \frac{13.6MeV}{\beta cp} Z \sqrt{\frac{x}{X_0}} \left(1 + 0.038 \ln\left(\frac{x}{X_0}\right)\right)$$

θ_0=0.0006702 rad

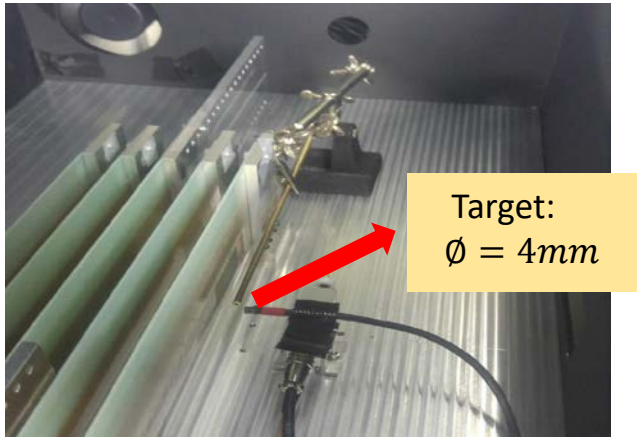
P =1GeV

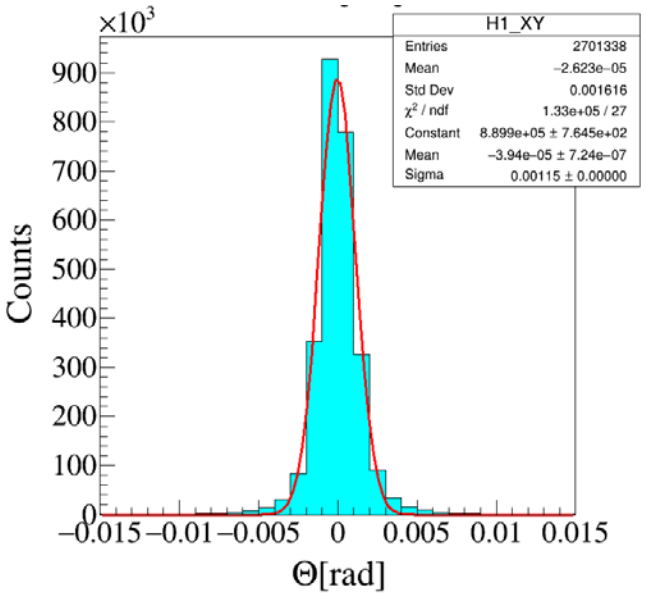
$$\frac{x}{X_0} = 0.39\%$$

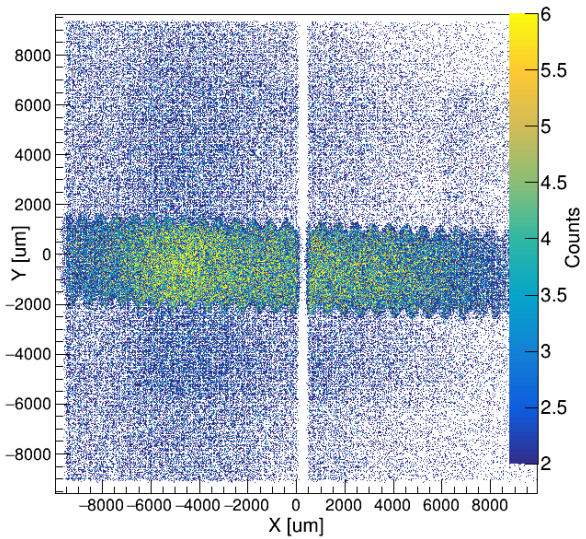
- Be consistent with the calculation result

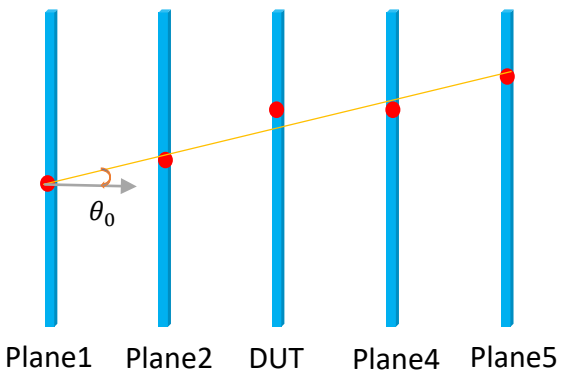
Target Test

- **Goal :Getting the target image according to multiple scattering.**
  - Target in front of plane 1.
  - Target1: A copper screw ($\emptyset$=4mm).
  - Target: An Aluminum plate ($thickness$ =1mm)









For the copper screw target , $\frac{x}{X_0}|_{\text{theoretical}}$=21.97% X_0

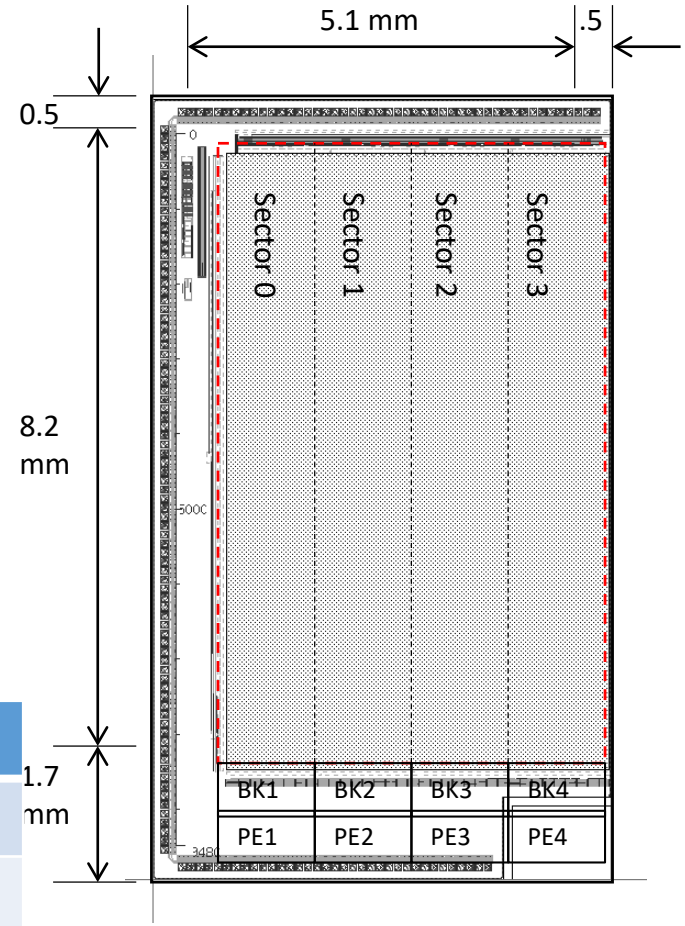
θ_0=0.00115 rad, P =5GeV ⇒ $\frac{x}{X_0}$ =20.259%

Outline

- Part of research activities in ECOPICS (Electron collider oriented pixelated CMOS sensor development)
- A CMOS pixel sensor (CPS) detector prototype study
- CMOS pixel sensor design and planed MPW run with IPHC

CMOS Pixel Sensor design variants

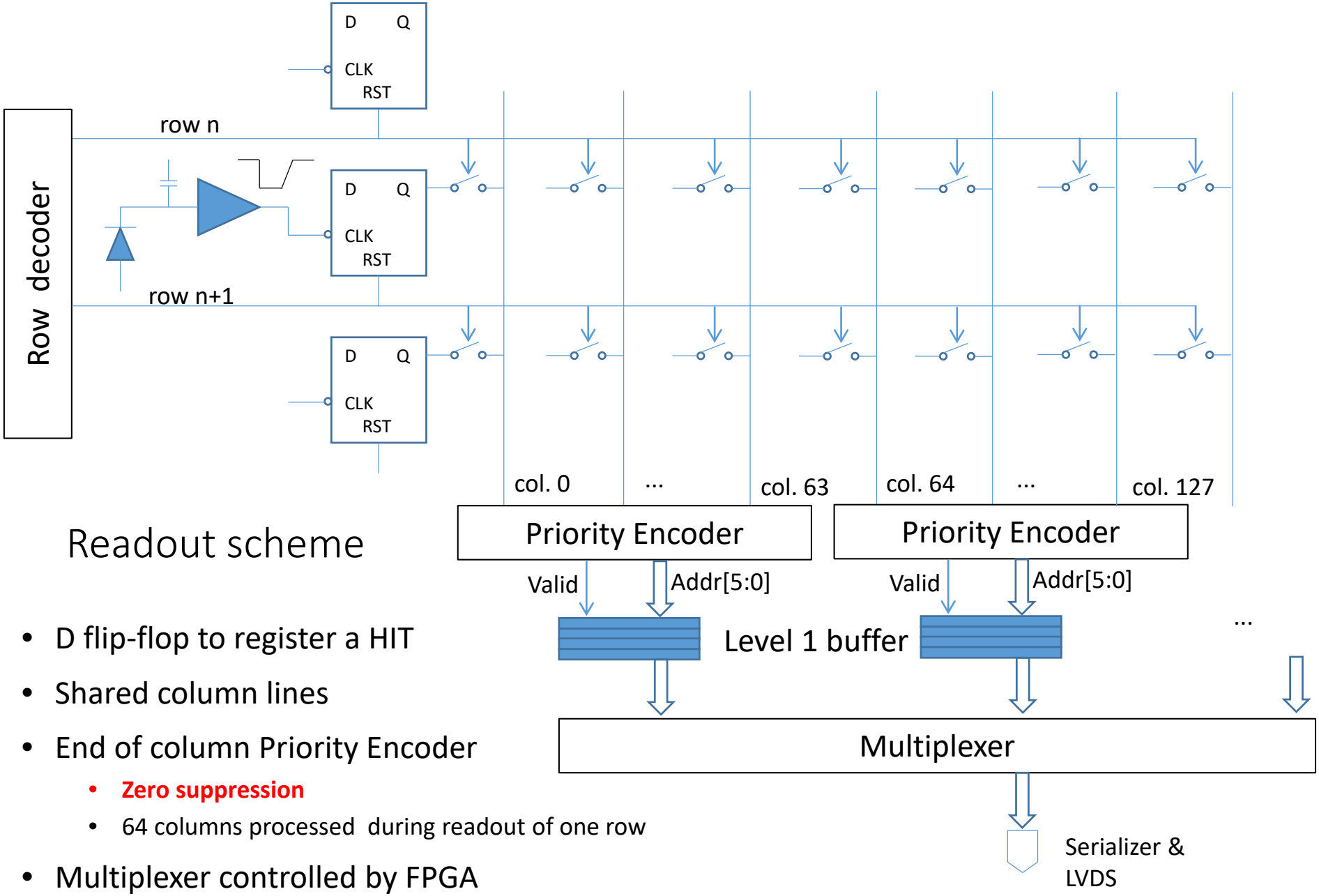
- Designed in TJ 0.18 µm CIS technology
  - The 3rd common submission with IPHC
- Diode, minimum size
- Front-end, 2 versions
  - FE_V0, FE_V1 (20nA, 60nA)
- Pixel digital, 3 versions
  - DGT_V0， DGT_V1， DGT_V2
- Pixel area
  - 16×26 µm^2
  - 16×23.1 µm^2



Four Pixel design variants

Sector	Diode	Front-end	Pixel digital	Pixel layout
0	2 + 2 µm	FE_V0	DGT_V0	16×**26** µm^2
1	2 + 2 µm	FE_V0	DGT_V1	16× **26** µm^2
2	2 + 2 µm	FE_V0	DGT_V2	16× **23.11** µm^2
3	2 + 2 µm	FE_V1	DGT_V0	16×26 µm^2

Readout scheme



- D flip-flop to register a HIT
- Shared column lines
- End of column Priority Encoder
  - **Zero suppression**
  - 64 columns processed during readout of one row
- Multiplexer controlled by FPGA
  - Flexible readout control

Summary

- A detector prototype system was set up and tested at T24 beam line in DESY
- Good performance have been obtained: spatial resolution: 5μm, efficiency : 96%, high location accuracy of the chips: 10μm, low material budget: 0.39% X_0
- CMOS Pixel Sensor design and planed MPW run with IPHC

Thanks for your attention !