ATLAS Silicon Detector R&D

-CPPM /ACC perspective-

12^{th} FCPPL workshop in Shanghai Jiao Tong University
April 24^{th}, 2019

Marlon Barbero / CPPM

CPPM / ATLAS Chinese Cluster Collaboration

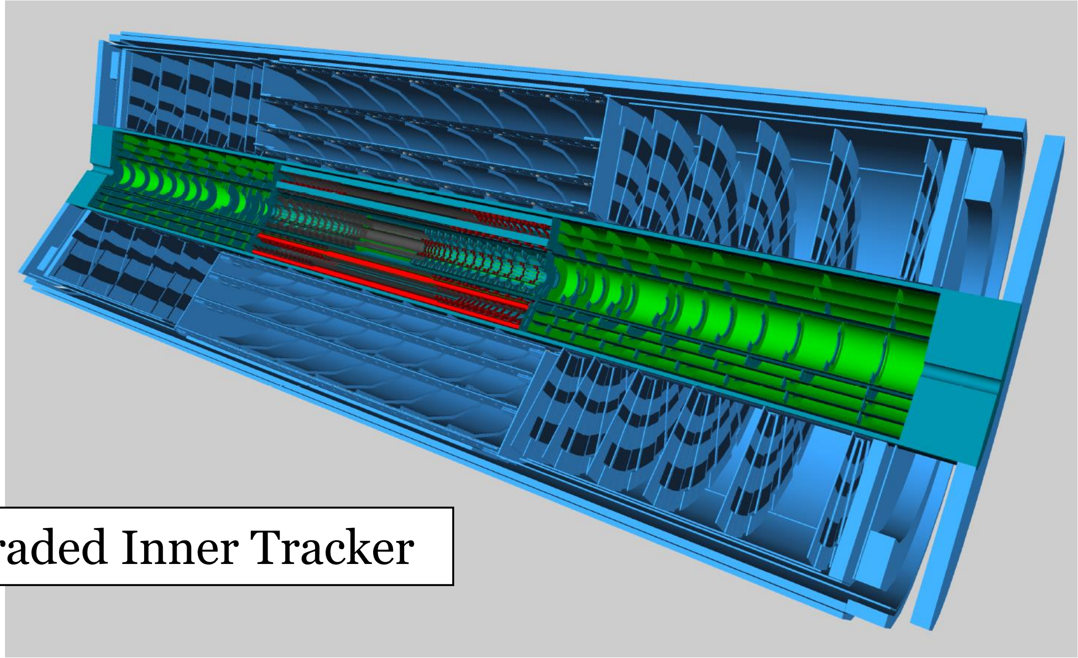
- CPPM / ACC collaboration for design and test of Front-End pixel electronics for ATLAS phase II upgrade.

- Scientific cooperation supervised by Pr. Xinchou LOU, Dr. Zheng WANG and Pr. M.B., derived from ACC / ATLAS CPPM project (Pr. Jin SHAN / Dr. Emmanuel MONNIER)

…involving IHEP, SDU (Pr. Meng WANG) and CPPM

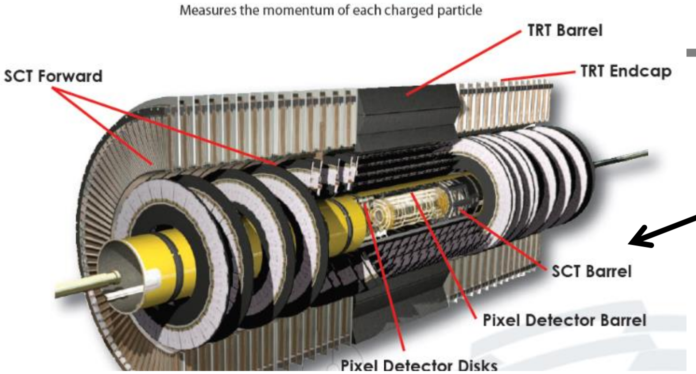
Plan

- Current detector:
  - Original ATLAS 3-pixel layers + IBL in 2014.
- ITk and new developments.
  - Why the ATLAS Inner Tracker (ITk) upgrade?
  - Front-End electronics
  - Depleted CMOS sensors
  - Current challenges
- Conclusion

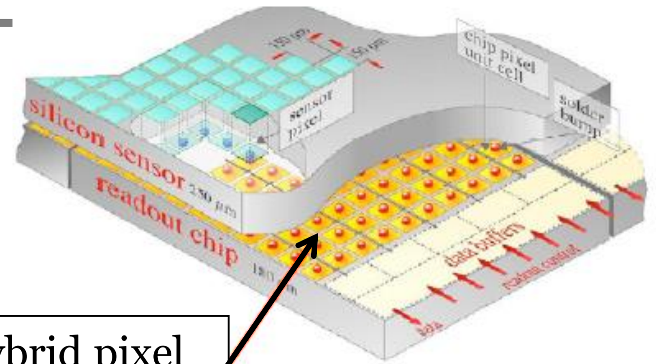


ATLAS Upgraded Inner Tracker

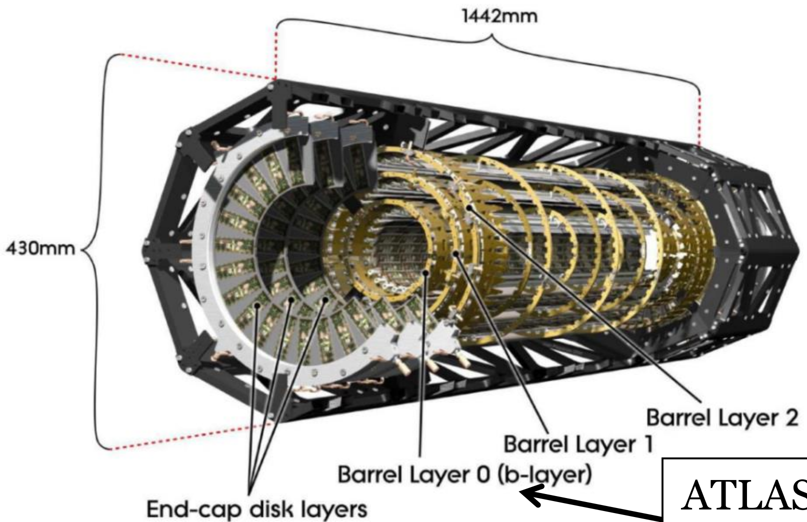
Original pixel detector



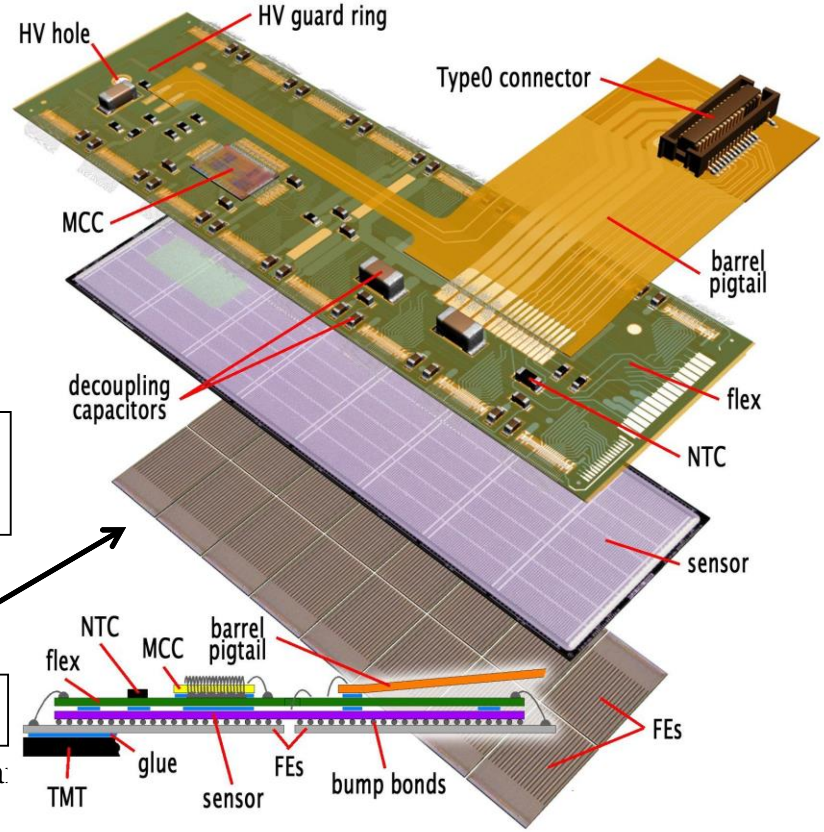
ATLAS Tracker (<2014)



Hybrid pixel



ATLAS Pixel detector (<2014)



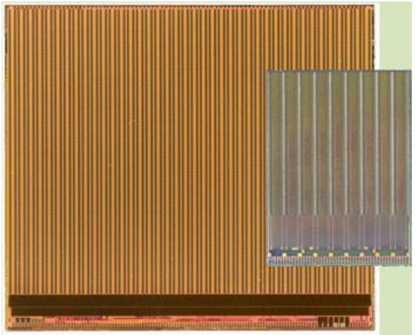
The initial ATLAS pixel detector: 87 millions pixels of size 50×400μm^2, in a 3-layer cylinder, cooled down at -15^{o}C, measuring particle crossing 40 millions times per second!

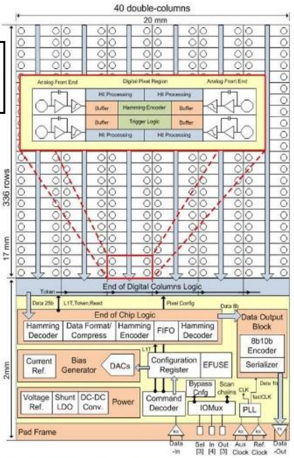
Original hybrid module

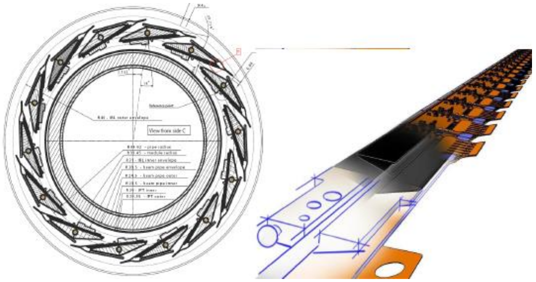
2014: ATLAS Pixel IBL

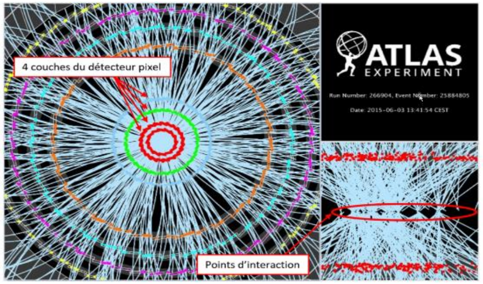
- Motivations:
  - Improves b-tagging performances
  - Increased robustness of pattern recognition
- How:
  - New innermost layer inserted into initial inner layer at r~3,7 cm. 2 mm clearance for insertion!

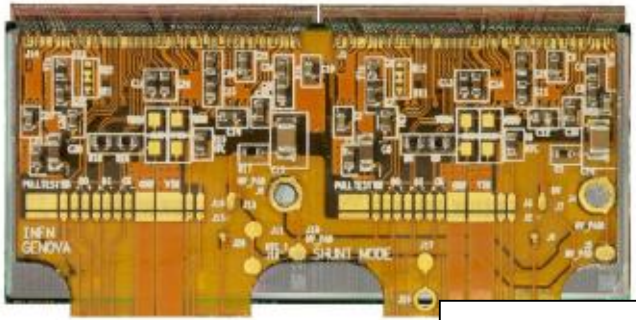
FE-I4, ROC for IBL





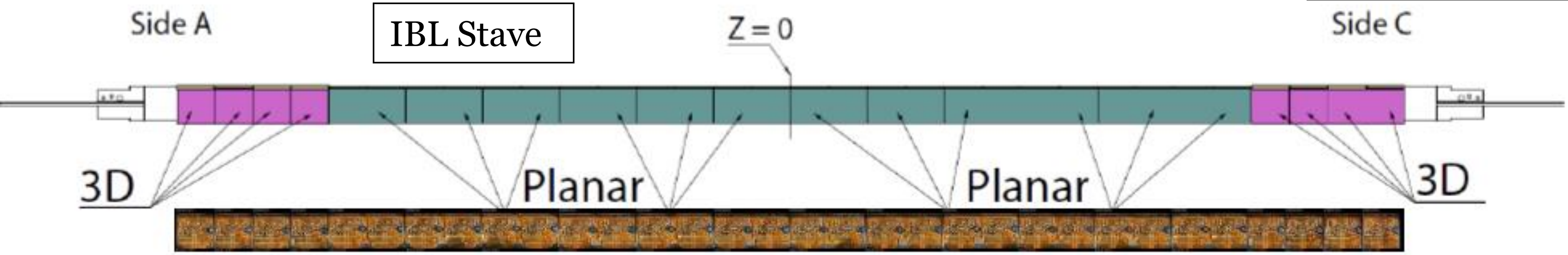






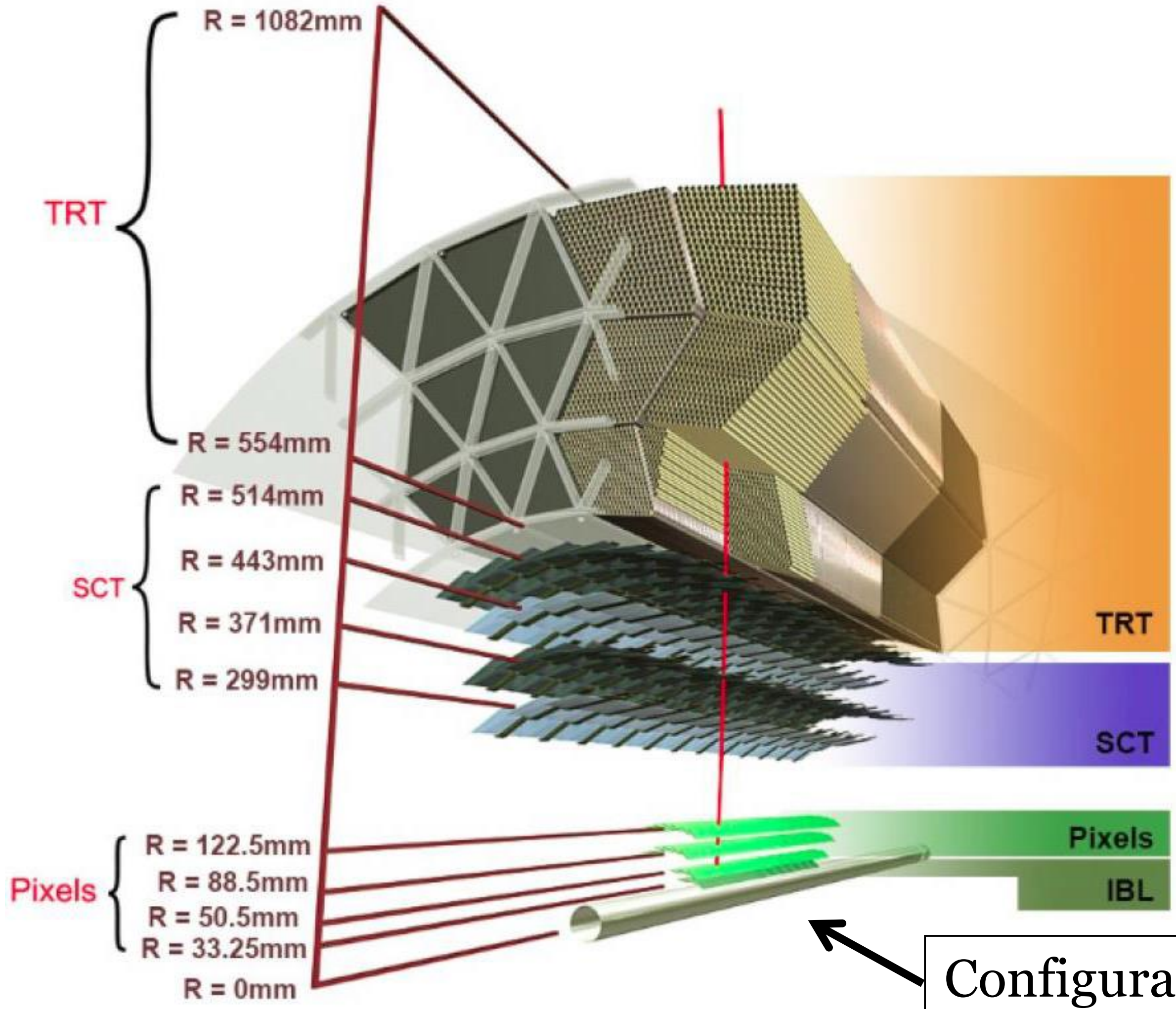
2-ROC module

- IBL staves rely on sensors developed in 2 technologies (planar n-in-n / 3D) + ROC 130nm



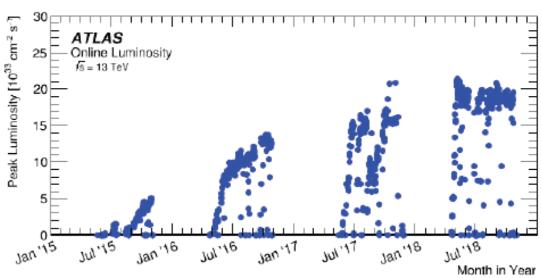
IBL Stave

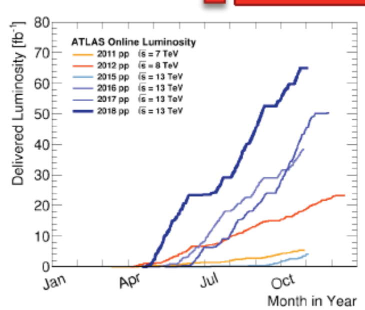
ATLAS tracker (present: 10m² silicon→ ~200m² for ITk!)



Configuration for Run II and Run III → 2023

Upgrade of the LHC





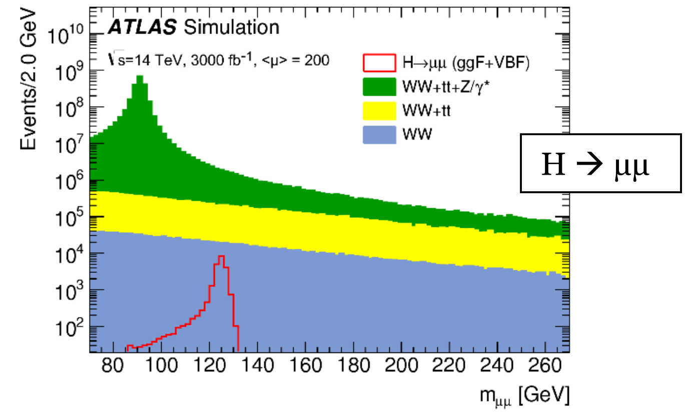
Current pixel detector
$L = 2\times10^{34}\ cm^{-2}s^{-1}$
$\int L = 300\ fb^{-1}$

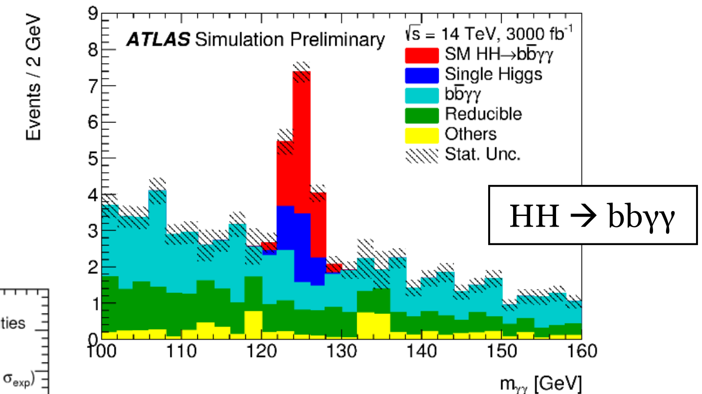
ITk pixel detector
$L = 7\times10^{34}\ cm^{-2}s^{-1}$
$\int L = 4000\ fb^{-1}$

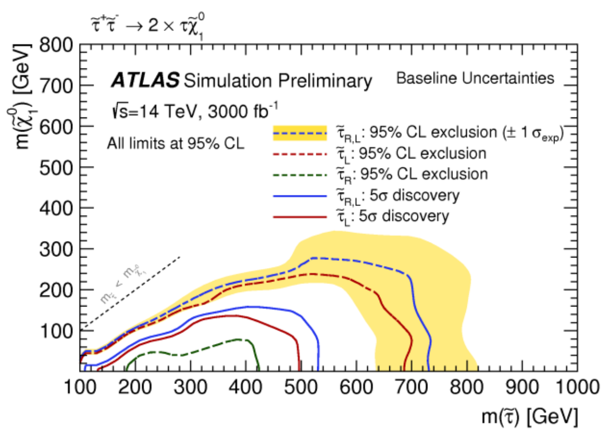
HL-LHC physics program

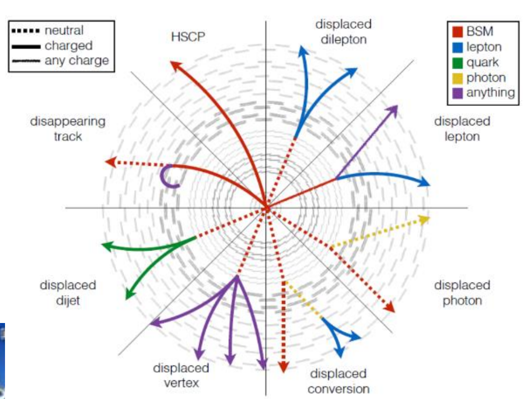
- The program includes:
  - Precision SM measurements:
    - Higgs boson: coupling, rare processes, Higgs auto-coupling
    - Vector boson scattering
  - Beyond SM searches:
    - New resonances
    - Susy
    - Dark Matter
    - Long Lived Particles
- See yellow report vol.2

https://arxiv.org/abs/1902.10229





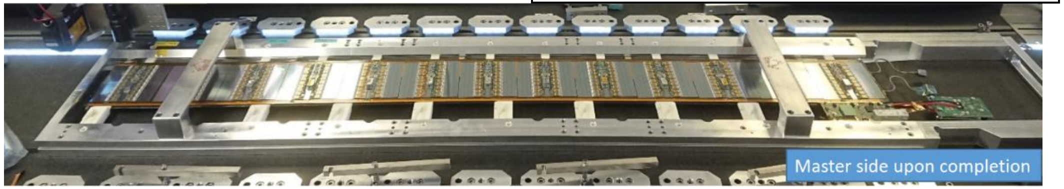




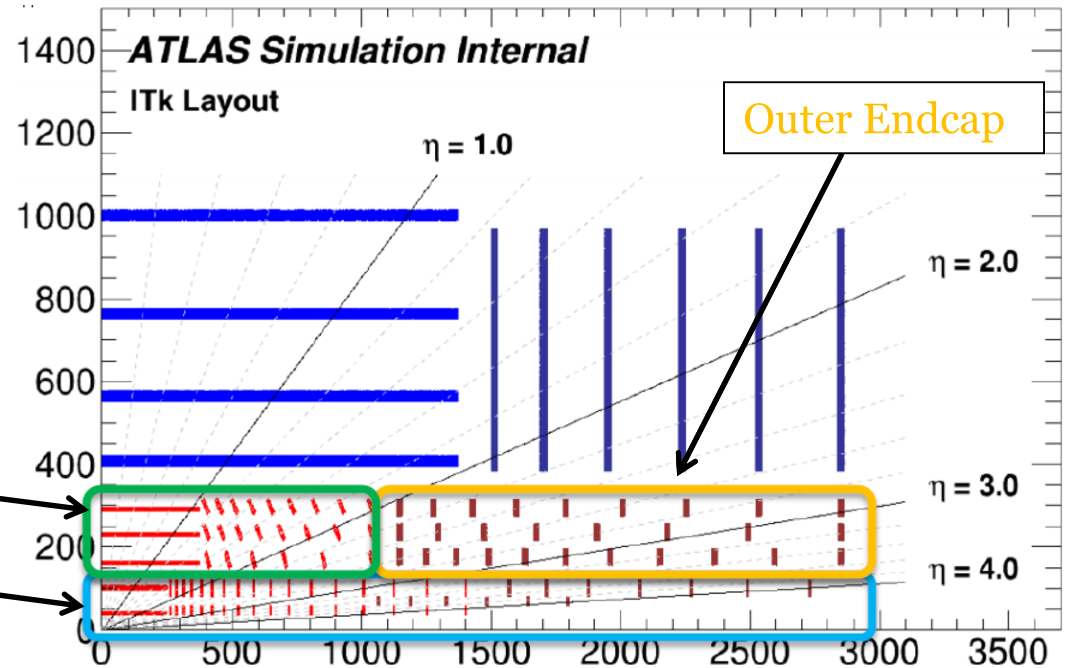
The Inner Tracker Upgrade -ITk- ATLAS biggest upgrade project

- An all silicon tracker, covering up to radius approx. 1m and extended tracking coverage $\eta = 4$.
- Reduced material (<1 X0 up to $\eta \sim 3$)

Prototype double sided strip stave

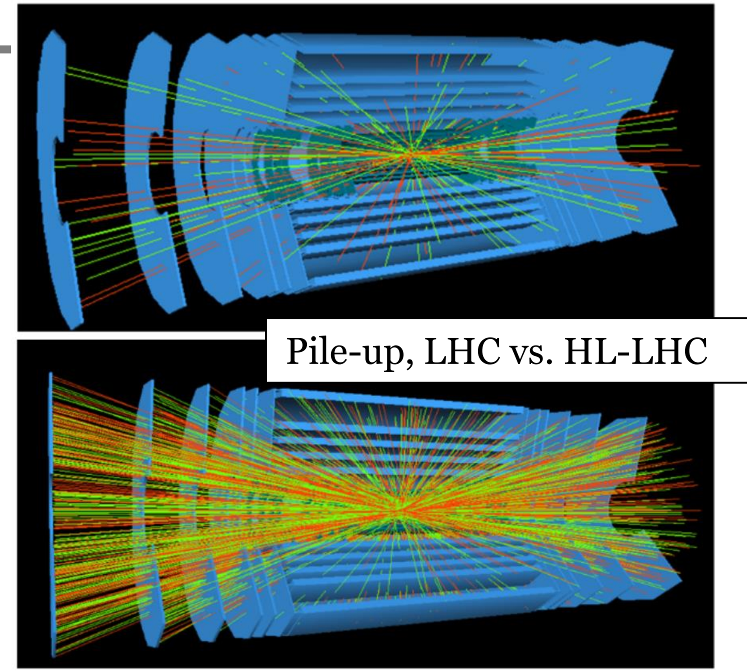


- **Silicon strip**:
  - 4 layers Strip Detector.
  - n^+-in-p FZ and ABC130 ASIC
- **Pixel detector**:
  - 5 layers Pixel Detector.
  - Features:
    - Replaceable inner system.
    - Serial Powering.



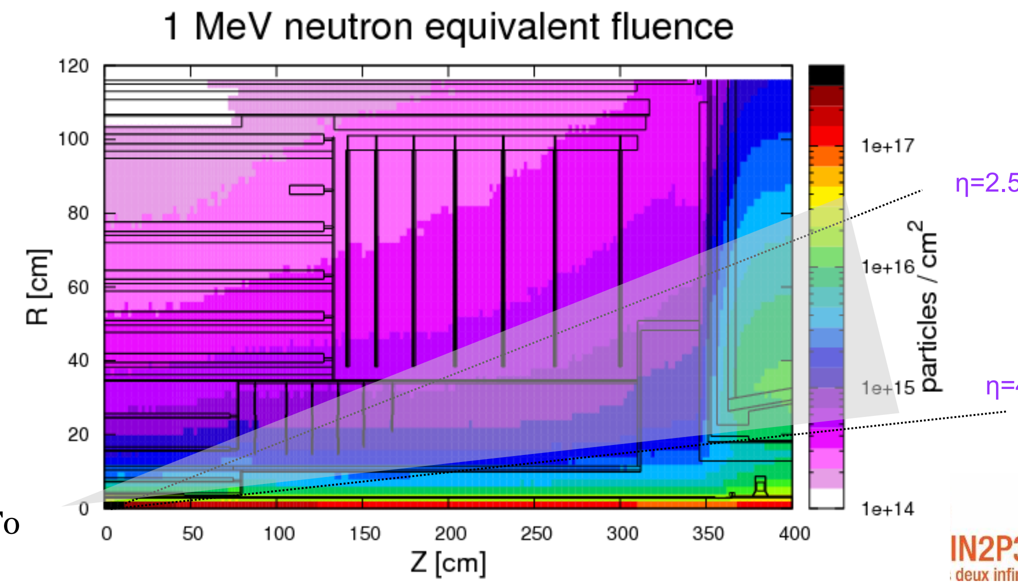
Why a new tracker?

- A huge pile-up: 200 interactions per beam crossing!
  - ATLAS designed for 25 interactions
  - The new detector will allow to keep current performances in terms of tracking and vertexing, b-tagging…



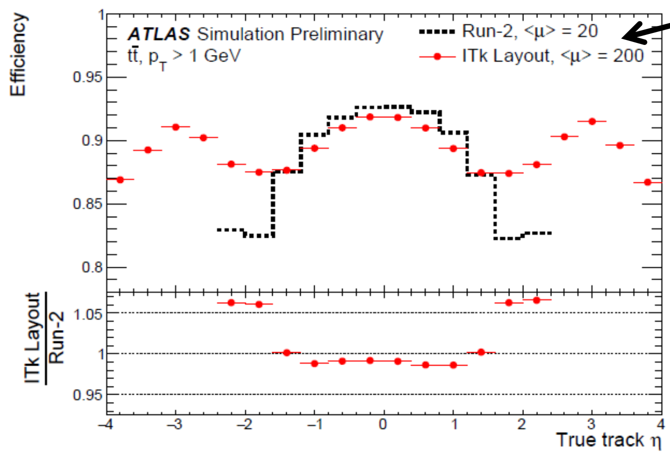
- More difficult radiation environment:
  - Central layers should cope over lifetime with > 2.10^{16} n_{eq}/cm^{-2} / > 1 Grad!
  - vs. 100-200 Mrad design for current inner layers

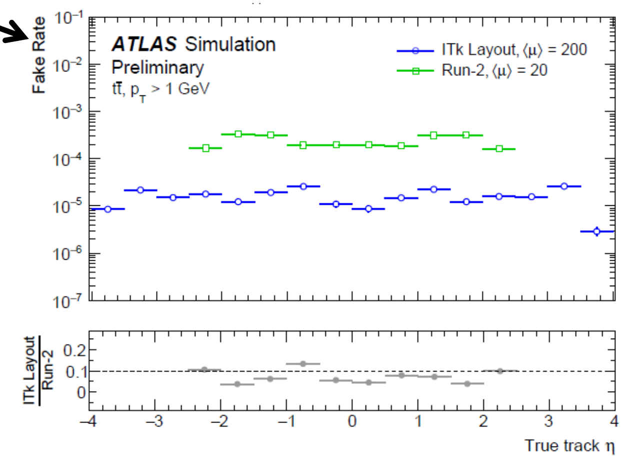
- Better η coverage:
  - η = 2.5 → 4.0
  - higher lepton acceptance
  - better pile-up rejection



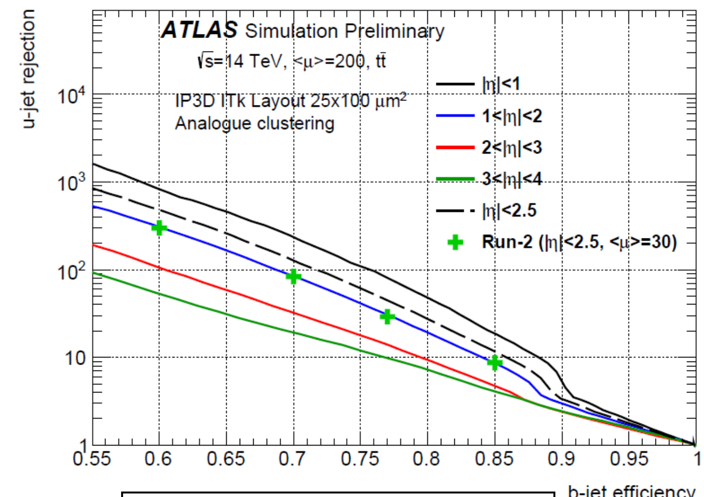
ITk performances

Track reconstruction efficiency and fake rate (tt sample with <μ> = 200, ITk vs. Run2)





See: http://cdsweb.cern.ch/record/2669540/files/ATL-PHYS-PUB-2019-014.pdf



Light jet rejection vs. b-tagging efficiency (IP3D algo)

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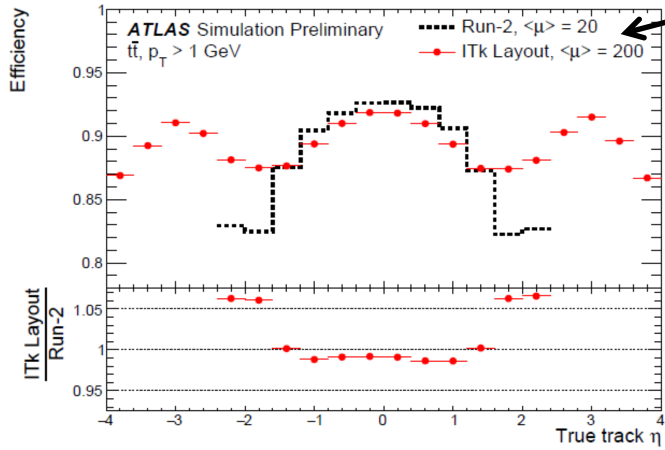
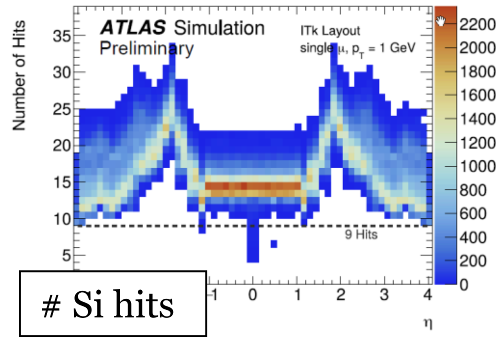
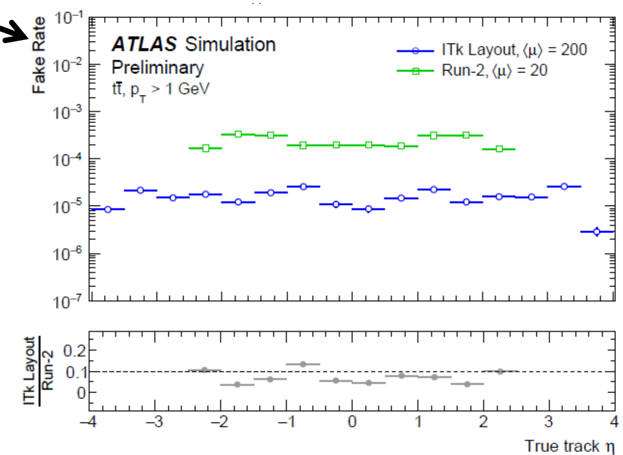




Si hits



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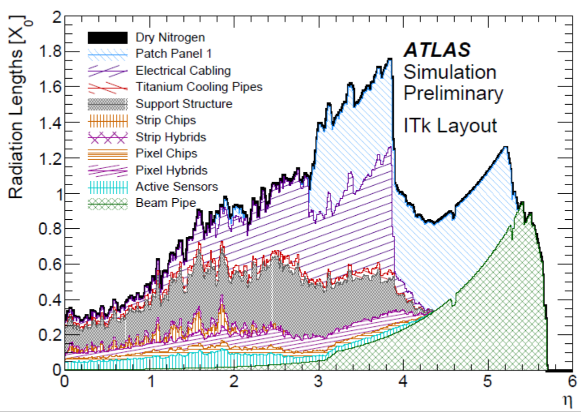
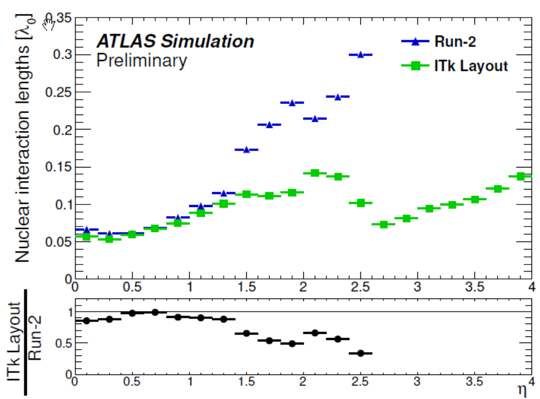
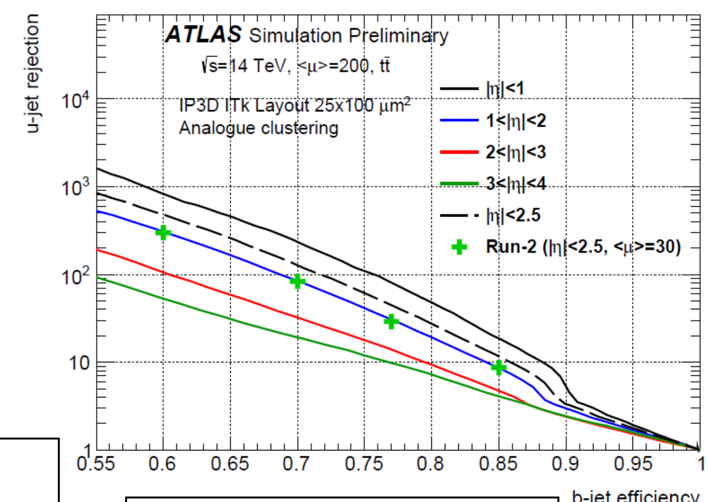


Radiation length vs pseudorapidity (ITk layout)



# of interaction length vs η (ITk vs. Run2 up to reconstruction requirement for # of hits fulfilled)



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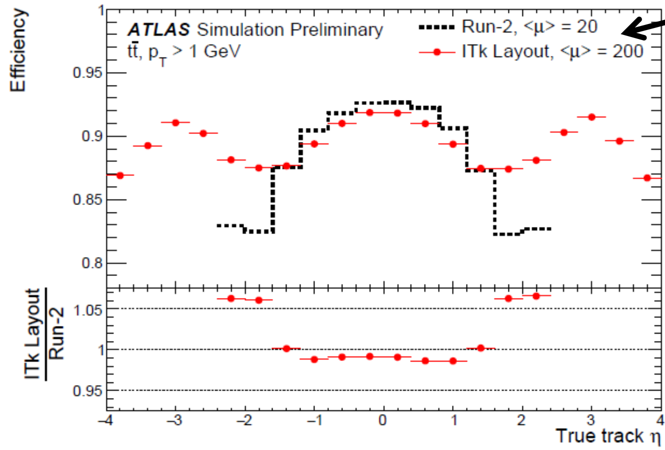

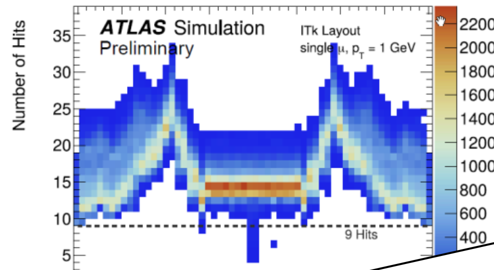

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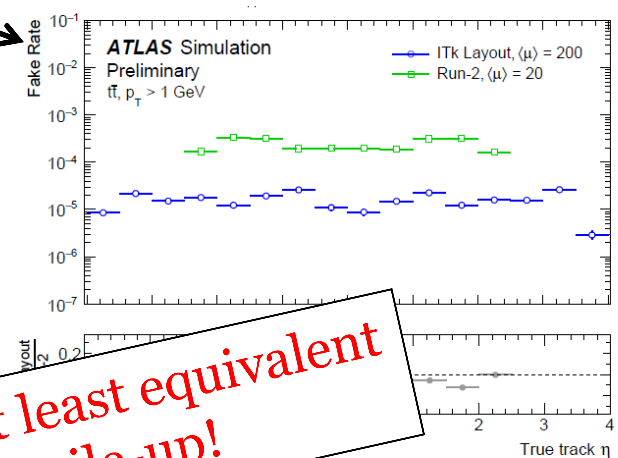
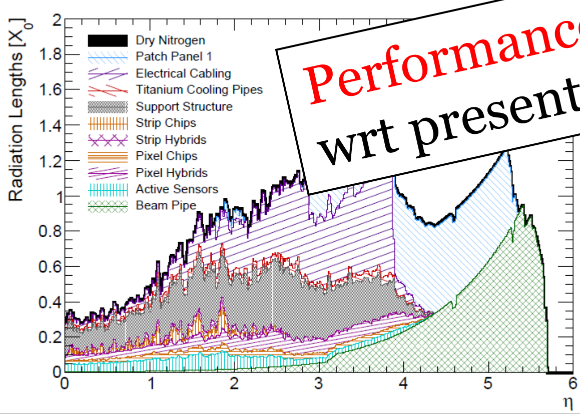


See: http://cdsweb.cern.ch/record/2669540/files/A...

Performances with the ITk should be at least equivalent wrt present tracker with 5-7 times more pile-up!



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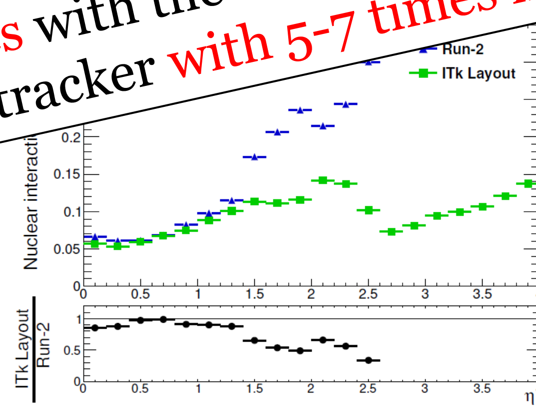

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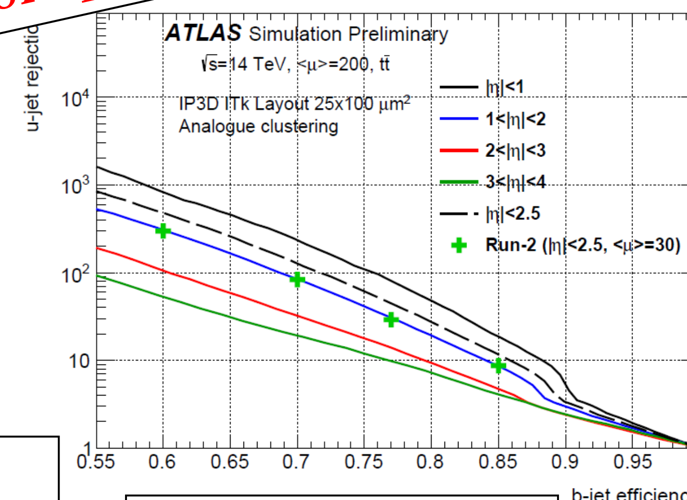
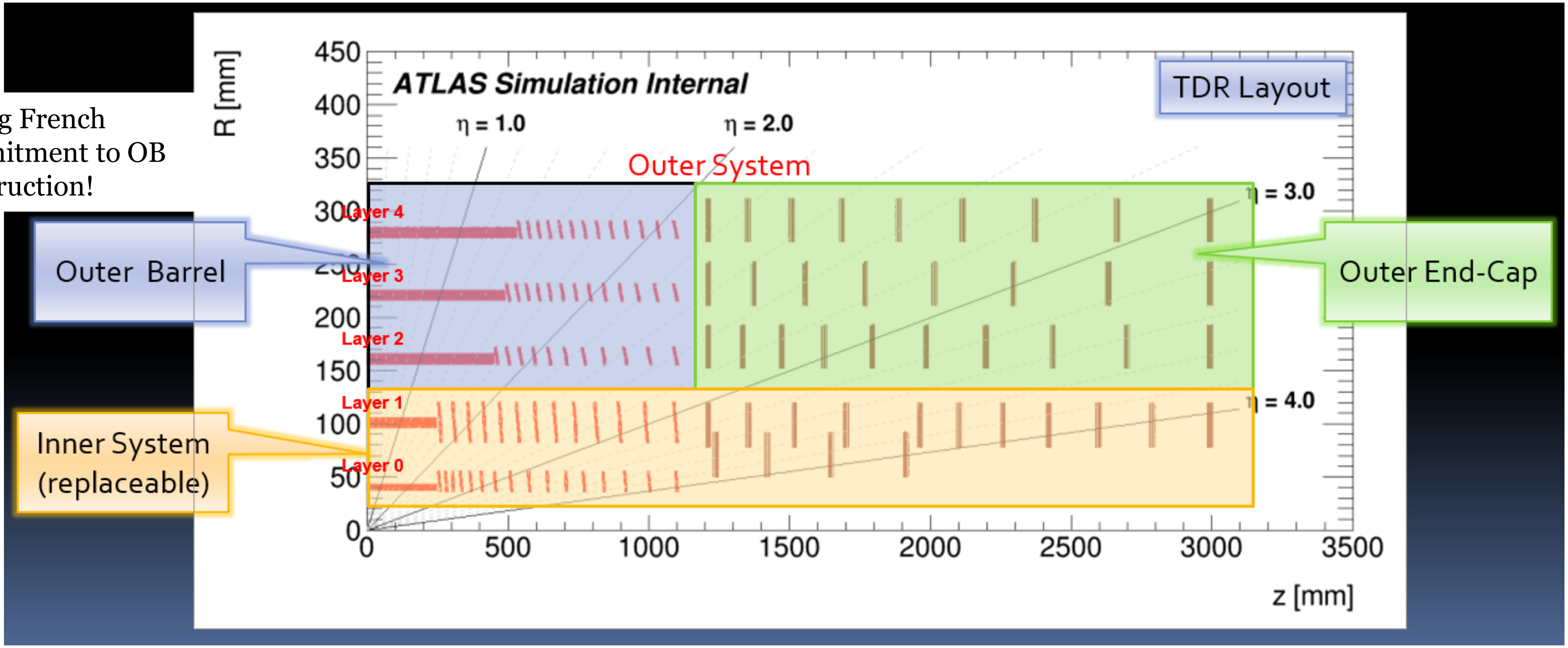


Light jet rejection vs. b-tagging efficiency (IP3D algo)

ITk Pixel Detector

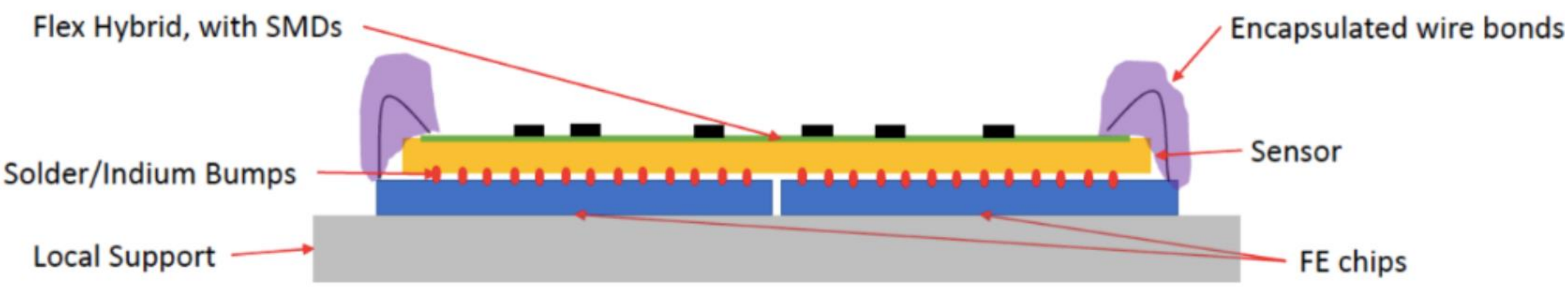
- 5 layers, >12 m², ~10k modules, ~5.10⁹ channels.
- Inner layer at 39 mm / pixel size 50×50 µm² - these parameters are still discussed (radius could go down, pixel size could go to 25×100 µm²)

Strong French commitment to OB construction!



Hybrid pixel module

- Most of the modules are ~4×4 cm² quad hybrid modules:
  - Planar sensor
  - Read out by 4 ROC, each 384×400 channels



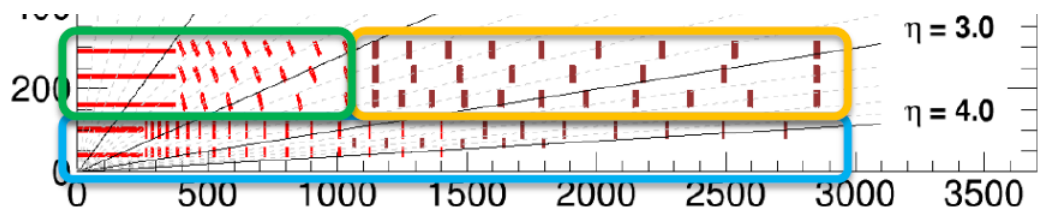
- Lots of experience from current detectors, yet needs a factor 10 scale up wrt current detector in total production capability!

Sensors / ROC

- Various sensors options depending on location

Inner system:

- L0 and R0: 3D sensors
- L1 and R1: 100 μm thin planar



Outer barrel and endcaps:

- L2-4 and R2-4: 150 μm thick planar
- In L4: Option of using monolithic CMOS sensor recently dropped out

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  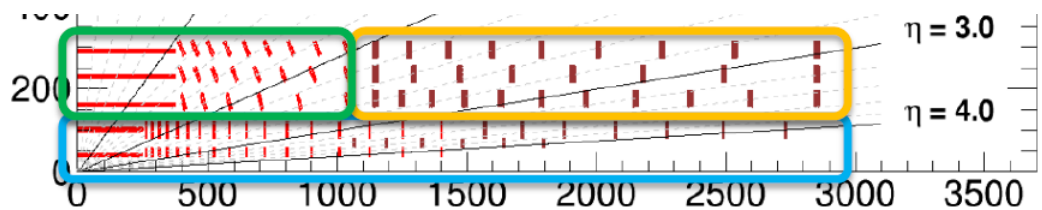

  <u>Outer barrel and endcaps</u>:
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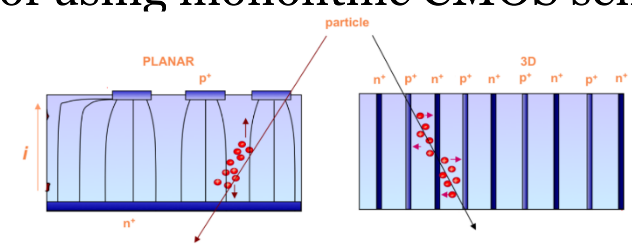
Planar vs. 3D Si sensor



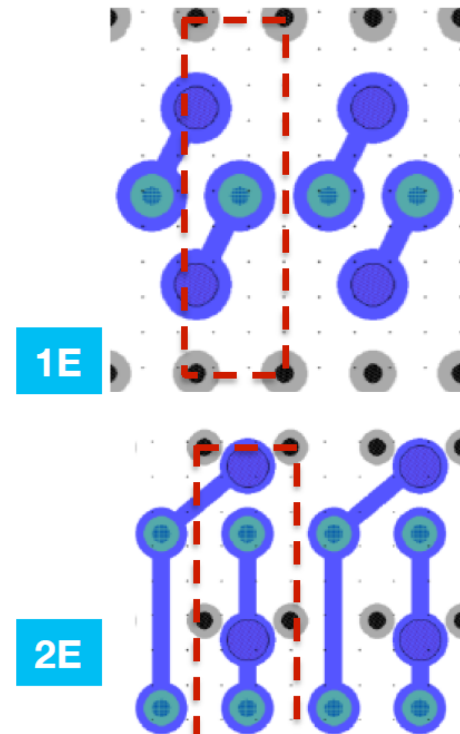
- The sensor technology is chosen wrt several criteria:
  - Radiation hardness
  - Cost
  - Production capability

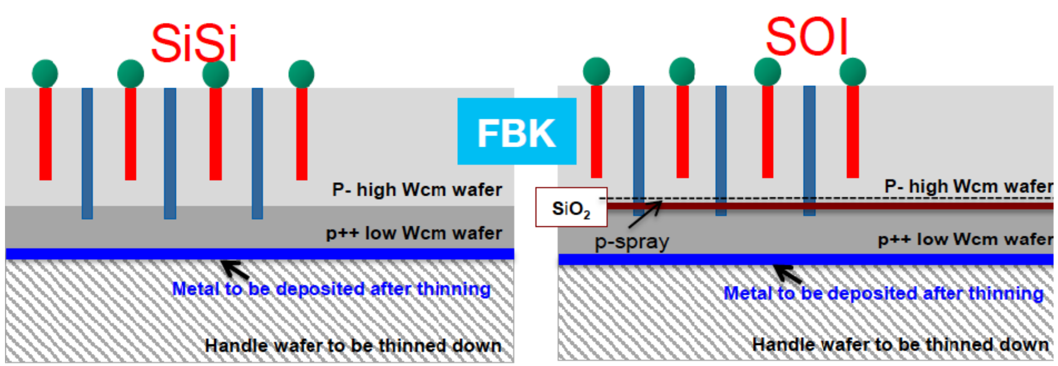
Layer/Ring	Single	Quads
Layer 0	1064	
Layer 1		920
Layer 2-4		4472
Ring 0	336	
Ring 1		280
Ring 2-4		2344

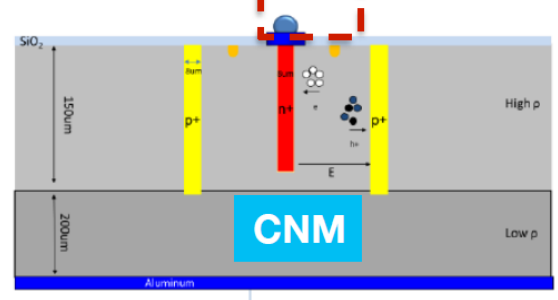
3D sensors

- Need to cope with approx. 1.3 10^{16} $n_{eq}.cm^{-2}$ (for 2000 fb^{-1} at half life).
  - Single-ROC module (~2×2cm²)
  - Active 150 µm (on top of 100 µm support wafer)
  - Sensors produced at FBK, CNM and Sintef
  - 50×50 µm² demonstrated
  - (If needed) 25×100 µm² TBD in assembly: rad hard 1 Electrode design vs. yield 2 Electrode design ?

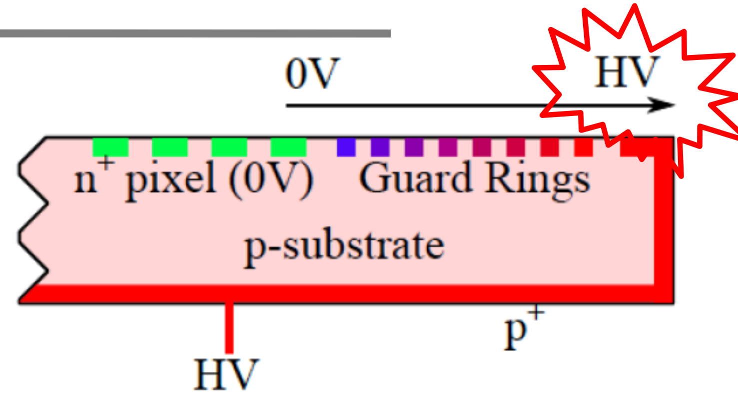
    (In all cases hybridisation at 50 µm pitch)







Planar sensors



- All quad modules.

- n implants in p substrate type:
  - One side processing: cost down.
  - Requires HV protection for the facing ROC at the sensor edge
    (BCB or parylene under evaluation)

- Thin sensors in L1:
  - Suited for radiation environment (4.5 10^{15} $n_{eq}.cm^{-2}$ for 2000 fb^{-1}) in L1-R1:
    Hit efficiency saturates at lower bias voltage: Ileak & power consumption down!
  - Many vendors on market

Hybrid FE / RD53 collaboration

- RD53 project : Design and develop pixel chips for ATLAS/CMS phase 2 upgrades, started in 2013
- Extremely challenging requirements for HL-LHC
  - Hit rates: 3 GHz/cm² (200 MHz/cm² in the current system) / ~220 hits/IC/bx
  - Small pixels: 50 x 50 μm² - Low power - Low mass
  - Radiation : 500 Mrad - 10^{16} n_{eq}/cm² over 5 years
    - Inner layer to be changed after 5 years
  - Local memory for 500 bx
- Baseline technology : 65nm CMOS

~100 people from 20 institutes :

- Bonn University
- CERN
- Fermilab
- INFN : Bari - Bergamo-Pavia – Milano - Padova – Perugia – Pisa - Torino
- IN2P3 : CPPM – LAPP – LAL - LPNHE
- LBNL
- New Mexico
- NIKHEF
- Prague IP/FNSPE-CTU
- RAL
- Sevilla University

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- Baseline technology : 65nm CMOS
- RD53A chip half size prototype
  - Sensitive area : 2 cm x 1.18 cm → 400 x 192 pixels of 50 x 50 µm²
  - 3 different Analog Front End flavors : Synchronous, Linear, Differential
  - Submission August 2017
  - First chip tested December 2017
  - First bump-bonded chip tested April 2018

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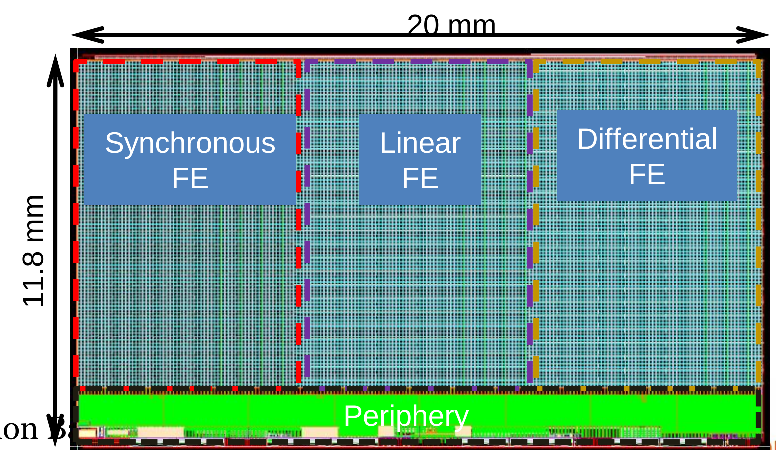
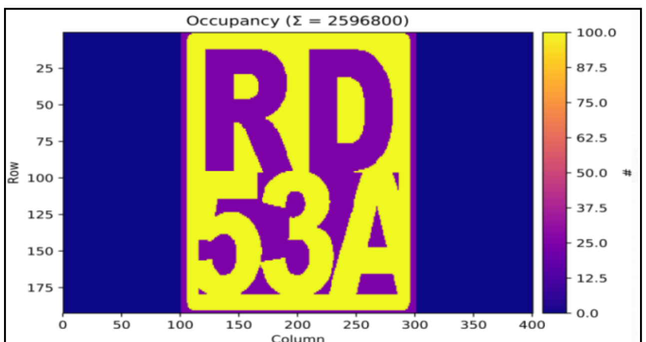
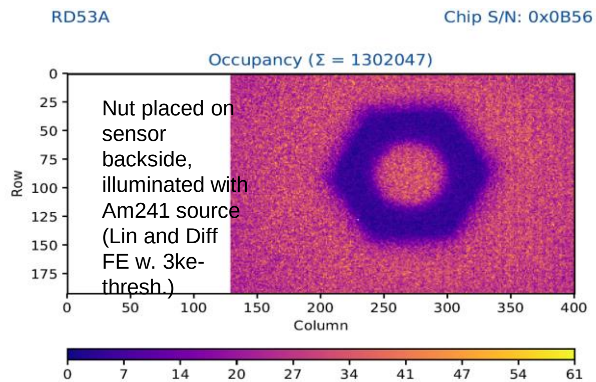


Final production IC development

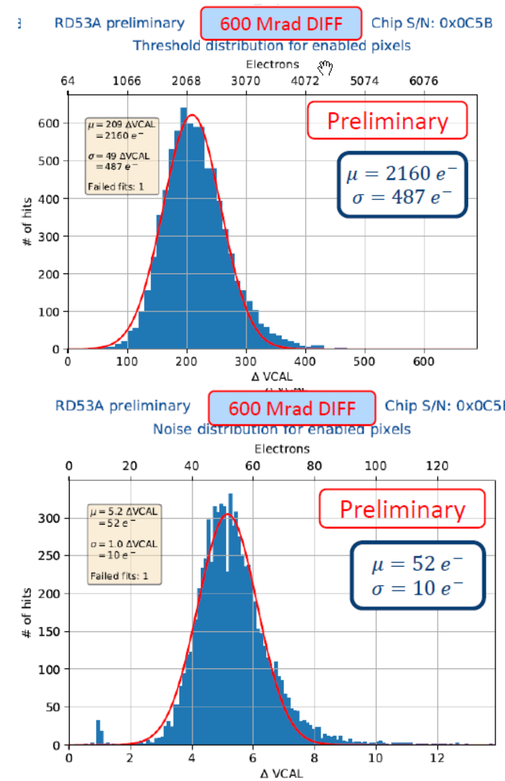
- Test results show that RD53A is a solid baseline for final chip development
  - The Analog FE for ATLAS fulfills specifications but needs additional minor modifications for final chip
  - RD53A bug fixes and improvements (SEU, Data compression, 80MHz ToT, 6-to-4 ToT, clock gating…)
  - Small prototypes have been submitted for some blocks requiring major changes



Complex digital scan



Am241 illumination of nut



Threshold and Noise @ 600 MRad

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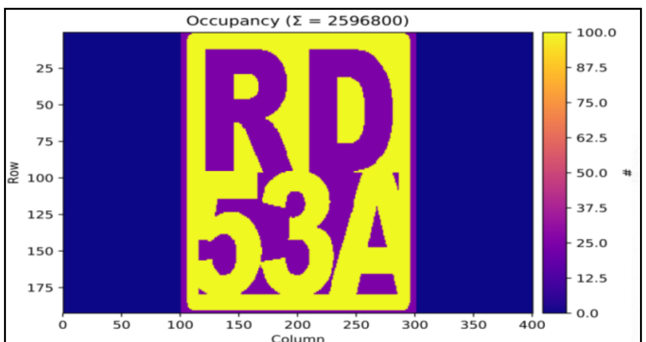
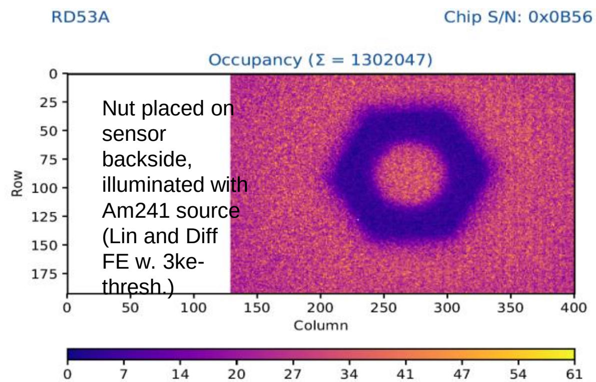
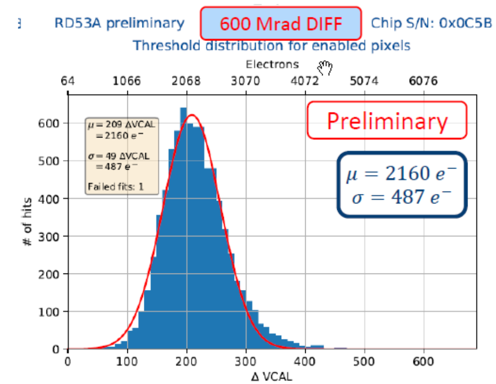
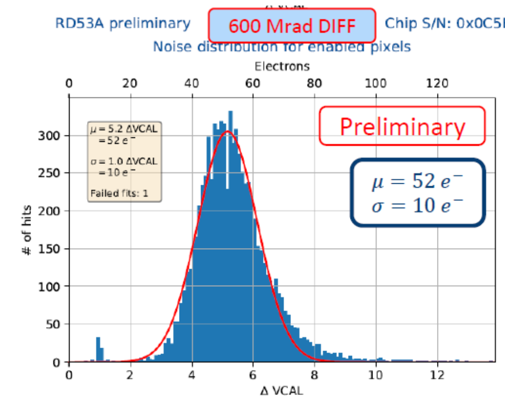


Complex digital scan



Am241 illumination of nut



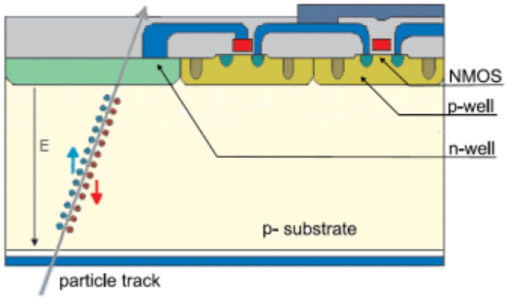


Threshold and Noise @ 600 MRad

- Development of the final production chips is ongoing
  - ATLAS chip submission target July 2019 (20 mm × 21 mm)
  - CMS chip submission December 2019 (21.7 mm × 18 mm)
  - Both chips are synthesized from a common design framework

Monolithic depleted CMOS

- Could provide an advantageous alternative to hybrid pixels.



Depleted active monolithic CMOS Pixels

- Key ingredients:
  - Depletion → Charges collected by drift.
  - Consequence → Fast signal response & radiation hardness.
  - Technology requirements → High Voltage process (apply 50-200 V), High Resistive wafers (>100Ωcm) and multiple nested wells (for full CMOS & shield)

(depleted layer $d \sim \sqrt{\rho . V}$)

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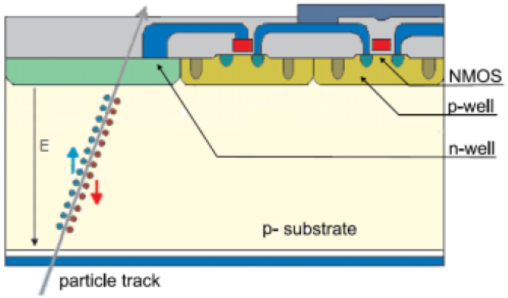

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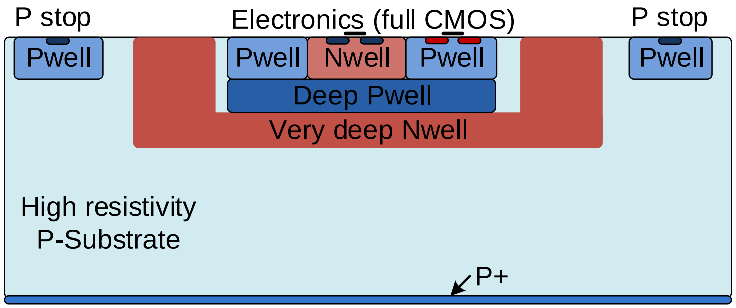
(depleted layer $d \sim \sqrt{\rho . V}$)

- Advantages:
  - Usage of commercial process: production capability, reliability, low cost…
  - Simple less expensive module (wrt hybrid): no hybridization and much easier production! Can be used for larger area applications
  - Small pixel size possible (in some process)
  - Less power, less material…

CMOS sensor development lines

Monolithic depleted sensors with electronics all in one!

2 lines of development followed : (a) large electrode design / (b) small electrode design



- LFoundry 150 process (or AMS/TSI)
- Pros:
  - Full CMOS
  - Uniform field, short drift distance → radiation hardness (TID & NIEL), 2.10^{15} $n_{eq}.cm^{-2}$ proven
  - HV rev. bias > 300V possible
  - BS thinning and processing possible
- Cons:
  - Deep nwell Q collection → big Capacitance (>200 fF) → noise, power & crosstalk

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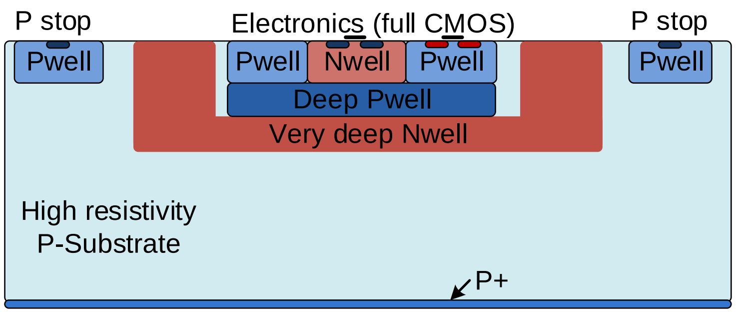

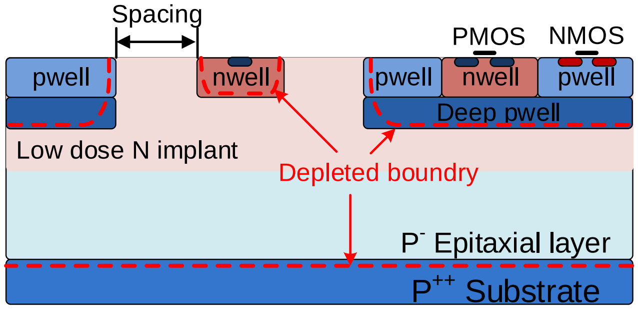

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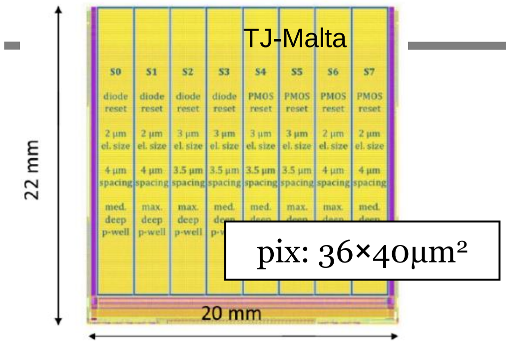
  - HV rev. bias > 300V possible
  - BS thinning and processing possible
- Cons:
  - Deep nwell Q collection → big Capacitance (>200 fF) → noise, power & crosstalk

- Modified TowerJazz 180 process

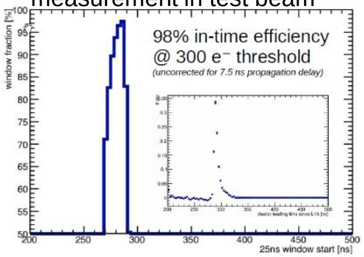
(W. Snoeys et al., NIM A871 (2017) 90–96)

- Pros:
  - Full CMOS
  - Small capacitance (<10fF) → low noise & low power.
  - Vendor established at CERN
  - Thin detector possible.
- Cons:
  - Limited depletion, long drift distance → radiation hardness TBD

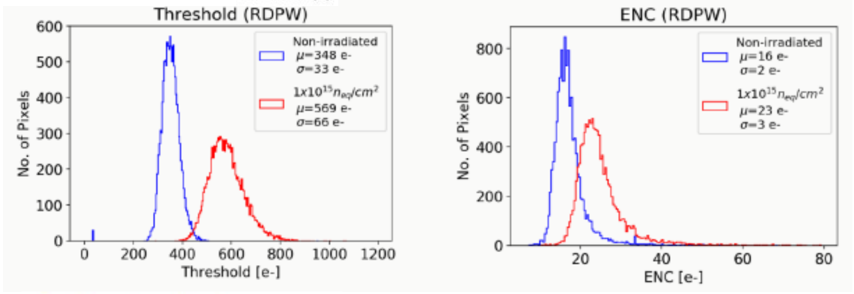
State of the art TJ and plans



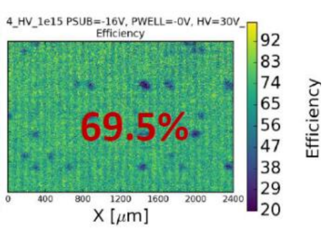
E.J. Schioppa, digital measurement in test beam

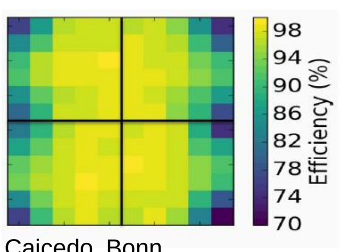


10^{15} $n_{eq}cm^{-2}$,th=570e, ENC=23e



Neutron irradiated





I. Caicedo, Bonn, summer 2018

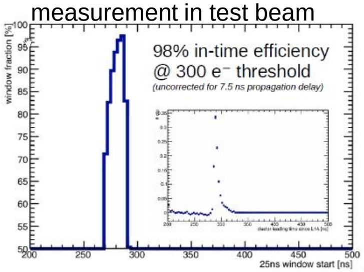
TJ in-time efficient.

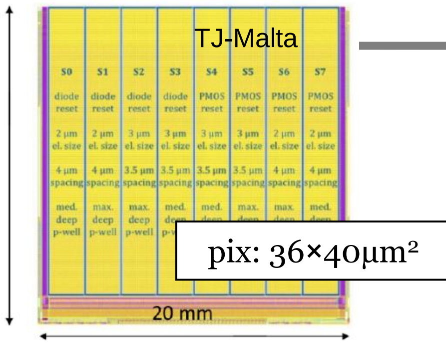
TJ has small noise / small threshold.

BUT: Despite modified process, charge collection on pixel corners still a problem!

State of the art TJ and plans

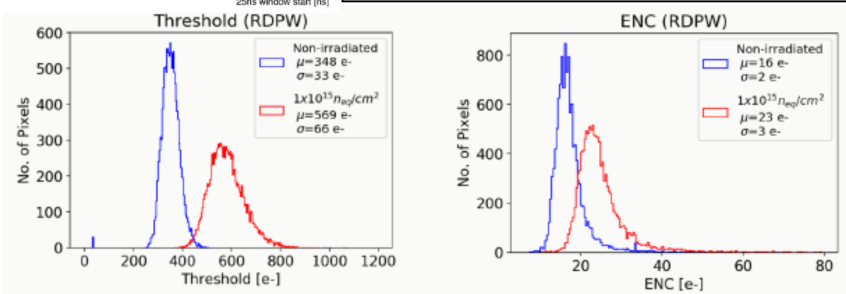
E.J. Schioppa, digital measurement in test beam





pix: 36×40μm²

10^{15} $n_{eq}cm^{-2}$,th=570e, ENC=23e



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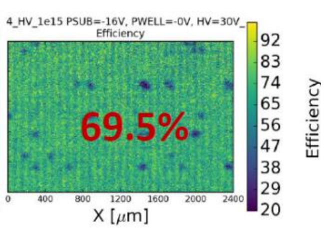
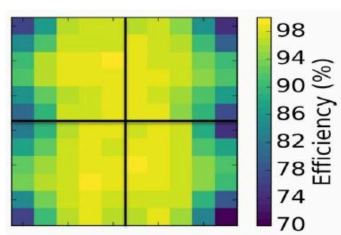




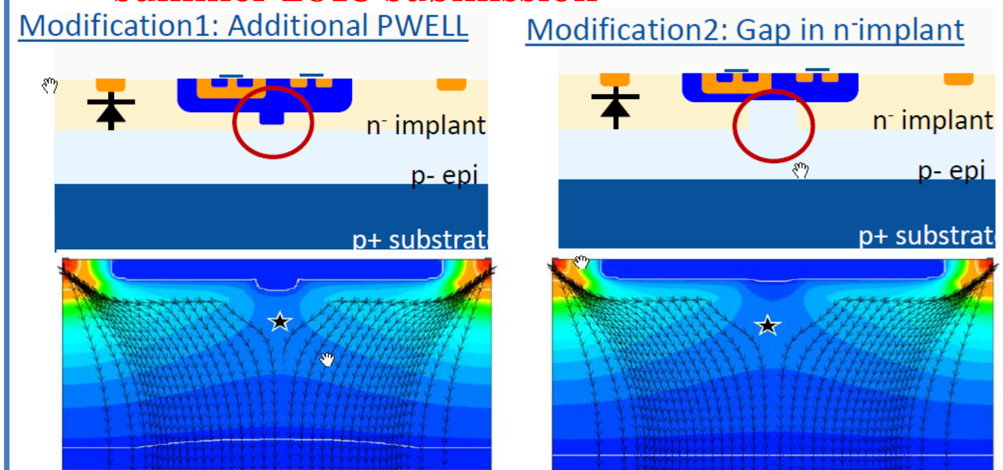
I. Caicedo, Bonn, summer 2018

TJ in-time efficient.

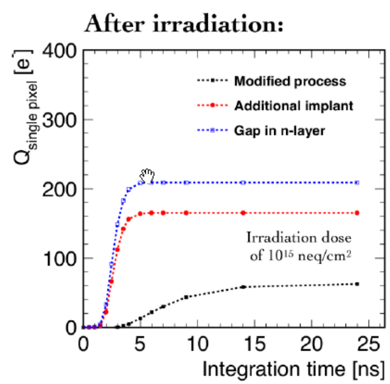
TJ has small noise / small threshold.

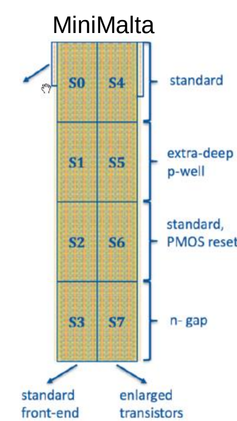
BUT: Despite modified process, charge collection on pixel corners still a problem!

- Weakness understood: weak E field under electronics.
- Modification with (reactive!) founder → summer 2018 submission



3D TCAD by M. Munker, CERN



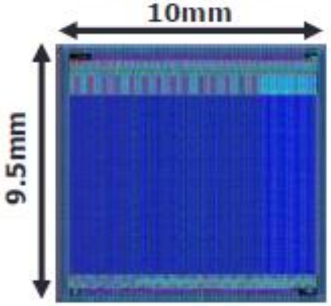


MiniMalta beam test ongoing, first indication very encouraging, more results soon

Large TJ submission in 2019

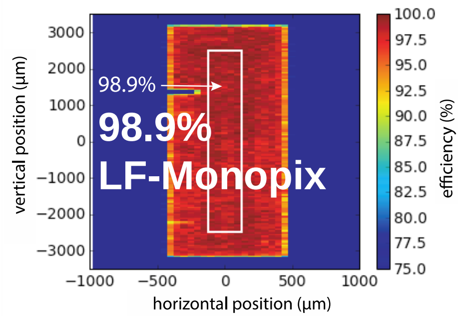
State of the art LF and plans

LF-Monopix1 (Monolithic)

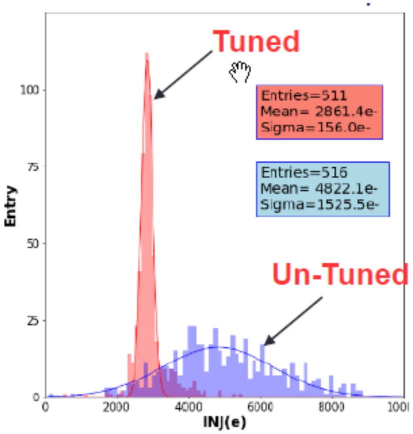


LF-Monopix1

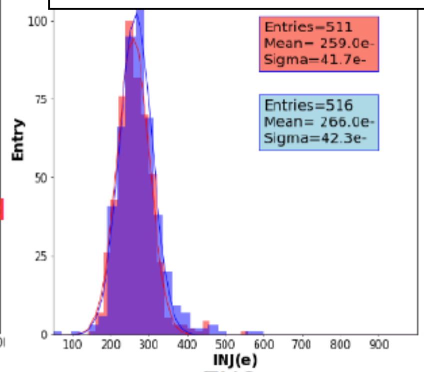
Efficiency @ 10^{15} $n_{eq}cm^{-2}$



Threshold and ENC 160 Mrad proton irrad (80d anneal)



Threshold



ENC

LF efficient after radiation.

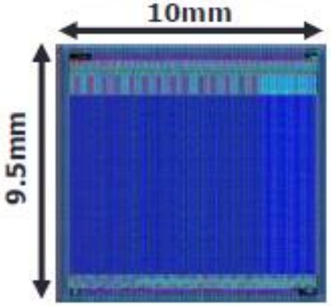
LF is easy to access and relatively low cost → large area OK!

But pixel size rather large.

pix: 50×250μm²

State of the art LF and plans

LF-Monopix1 (Monolithic)



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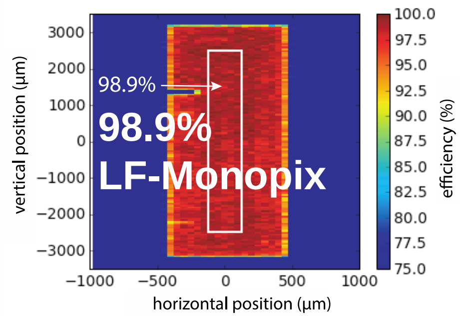

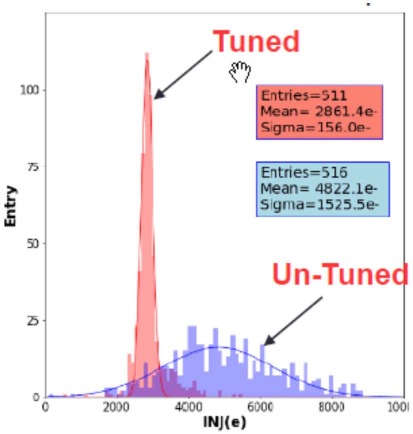

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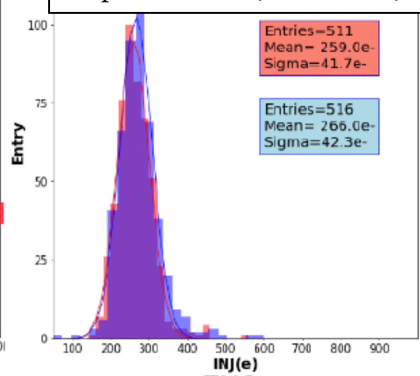

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LF is easy to access and relatively low cost → large area OK!

But pixel size rather large.

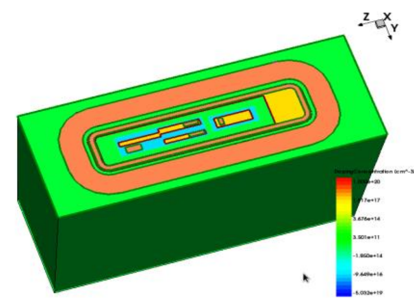
pix: 50×250μm²

Limitations in Monopix1:

Timing marginal (discriminator needs improvement).

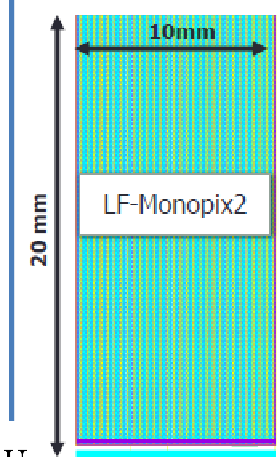
Crosstalk seen from some digital signal. Better isolation needed.

Pixel size should be reduced.



Breakdown Voltage and Pixel Size reduction studies

Mei Zhao IHEP / CPPM



LF-Monopix2

Monopix2:

target: 50×150μm²

Plan for a large matrix of 2cm height in 2019 → timing addressed / smaller pixel

Collab Bonn/CERN/CPPM/IRFU +ACC

DepCMOS future plans

- Option to use depCMOS in ATLAS ITk L4 recently dropped out.
  - The high level of development and the closeness to specifications was recognized, but concern is that depCMOS diverts attention from main hybrid-like solution at a time when schedule is tight and several challenges still lay ahead for the standard solution.

DepCMOS future plans

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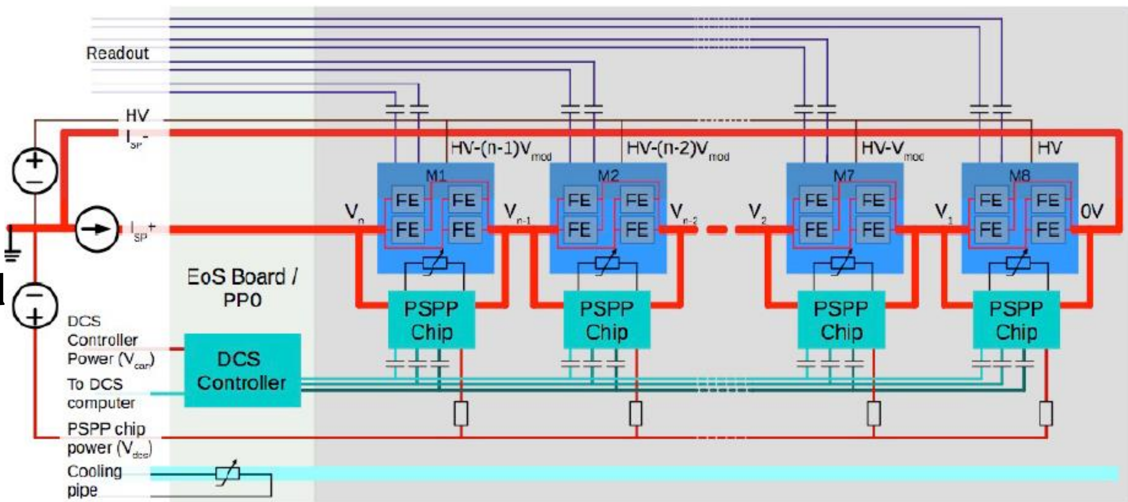
  - The high level of development and the closeness to specifications was recognized, but concern is that depCMOS diverts attention from main hybrid-like solution at a time when schedule is tight and several challenges still lay ahead for the standard solution.

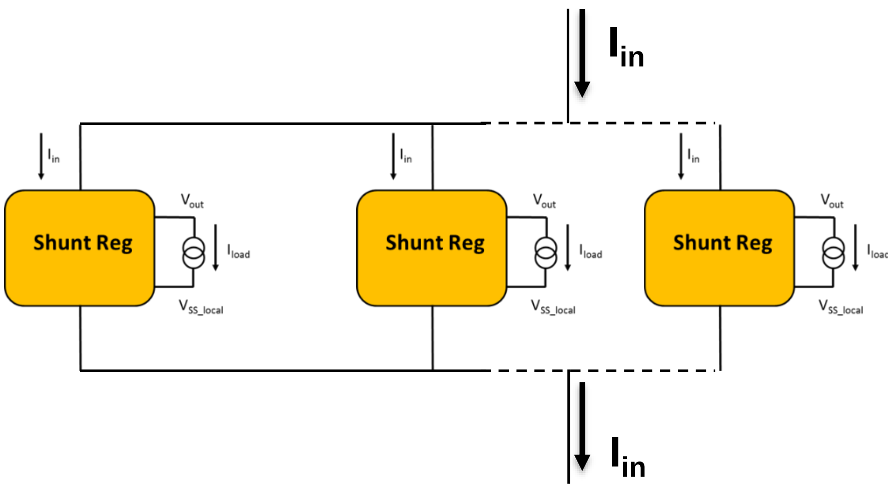
- The value of this technology for future applications makes no doubt:
  - Work continues with other targets:
    - Future application in ATLAS…
    - CepC, FCC-ee, Belle experiment, future hadron circular collider…
    - Timing layers, imaging applications…
  - Applications in which radiation hardness, high hit rate, speed is required.

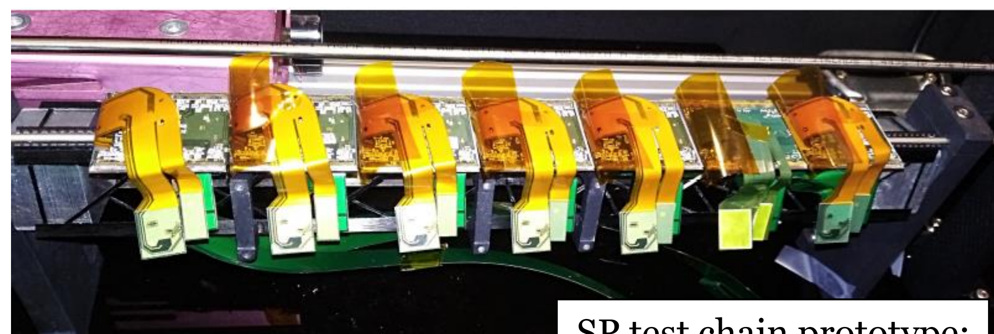
- Strong collaboration (start ~2014) with our partners in various framework (ACC, Bonn/CPPM/CERN/CEA-IRFU collaboration, CERN RD50…)

ITk / challenge ahead: SP

- Serial Powering:
  - Never used in real experiment
  - Up to 7A / module
  - Up to 14 modules in a chain
  - All data transmitted AC coupled
  - Reliability primordial





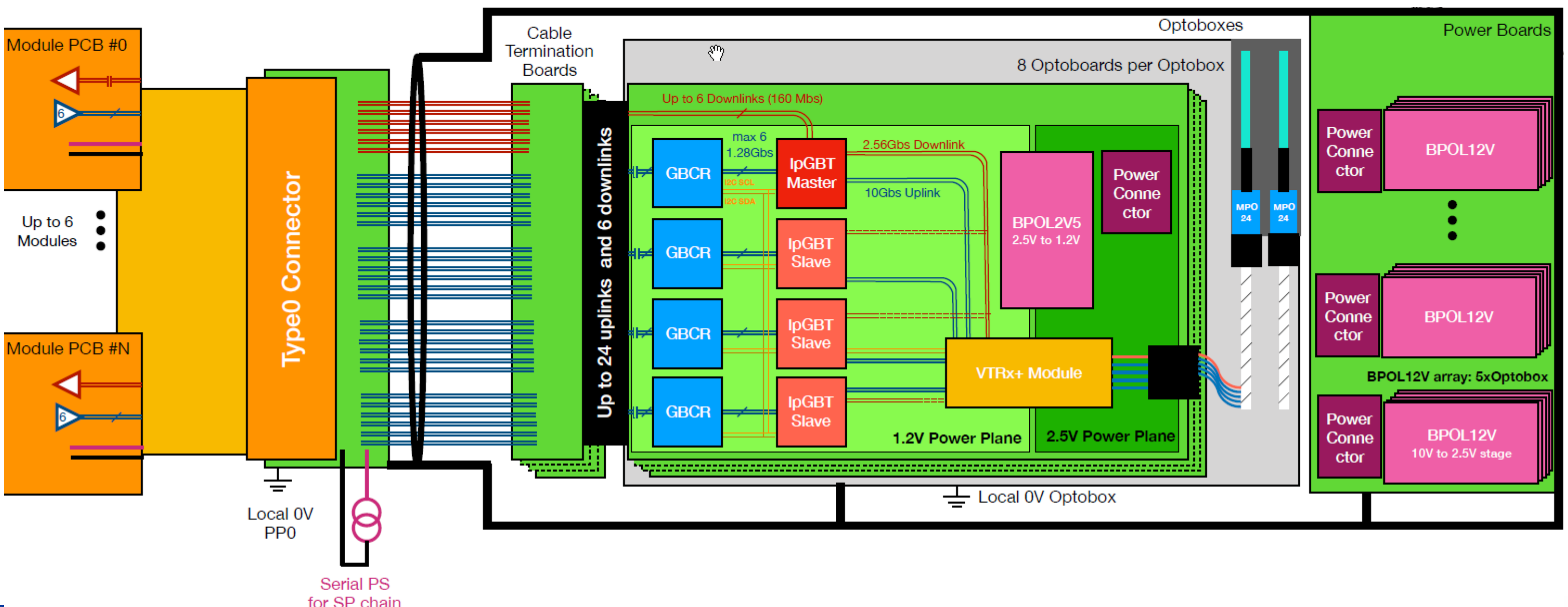


demonstrator program

SP test chain prototype: 7 FE-I4 quads in series

ITk /challenge ahead: Data transmission

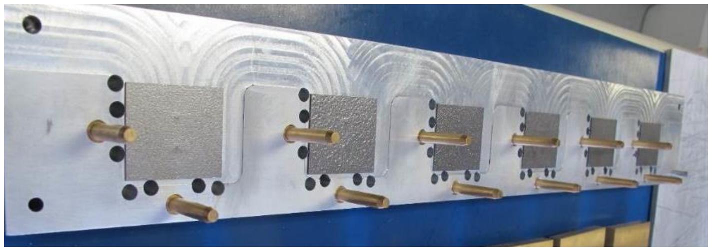
- Data transmission:
  - Baseline recently established:
    - Direct transmission from RD53B to Optoboard
    - 1.28 Gbps uplink and 160 Mbps downlink over low volume electric cable (max 6m!)
  - To be assessed:
    - Signal integrity over full chain & extra material introduced by the scheme

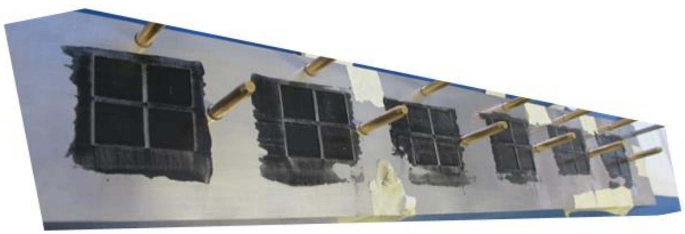


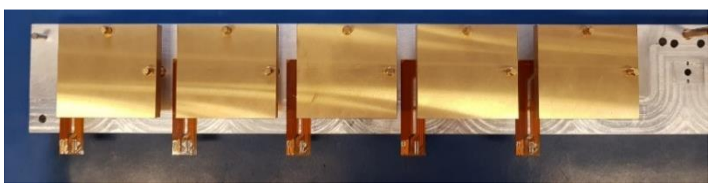
ITk / challenge ahead: Gearing up for production

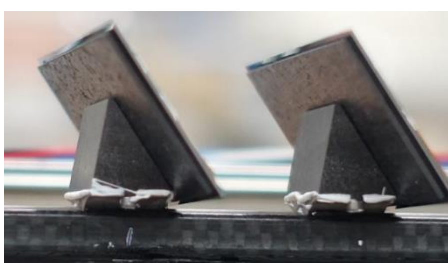
One example: Cell loading + integration

Outer barrel: > 4000 quads!





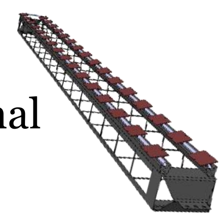




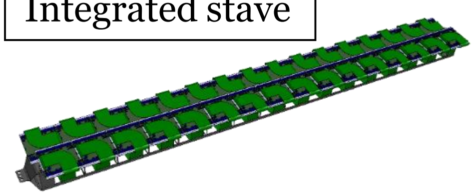
- **Current activities**
  - Development of loading methodology
    - Tooling design
    - Glue pattern and deposition method
    - Loading procedure
    - Survey procedure of loaded cells
  - Material Qualification
    - Thermal & electrical properties
    - Mechanical properties
    - Filler particle size
    - Radiation hardness
    - Handling and storage
  - Thermal QC of loaded cells
  - Electrical QC of loaded cells

6 Cell Loading sites in production:
- **CERN**
- **CPPM**
- **KEK/QU**
- **LPSC**
- **UniGE**
- **Wuppertal**

With a functional stave



Integrated stave

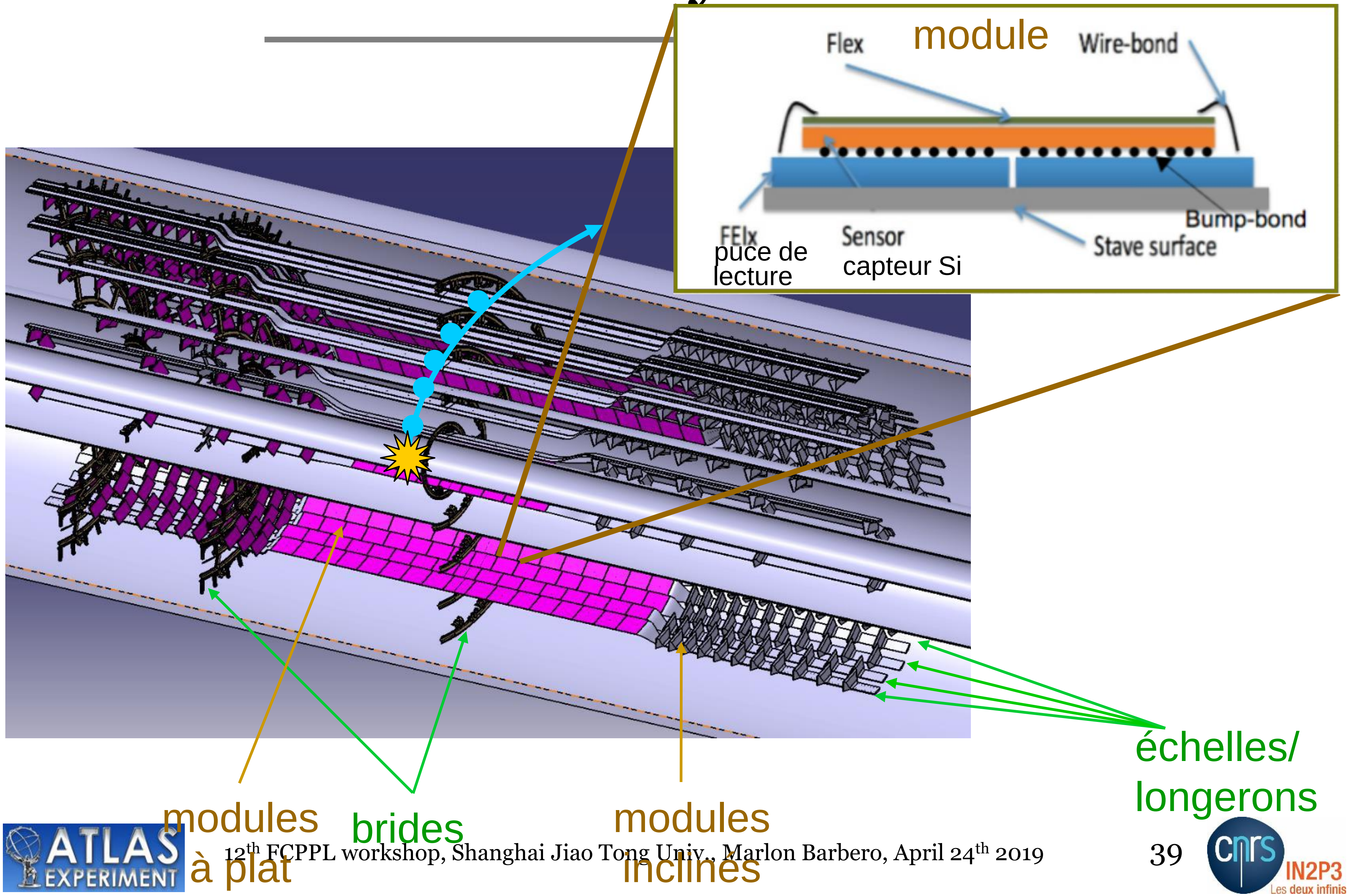


TBD in ~2 years! (2022-23)

Conclusion

- ATLAS Upgraded ITk will cope with 5-7 times more pile-up than at present, yet it should have close to identical performances wrt present with higher η coverage.
- The ITk pixel detector is an ambitious detector to fulfill this goal, in which innovation is required on the detector Front-End, but also on the services!
- All the baseline components of the detector have been defined.
- Schedule is tight, but production phase is now getting in sight.

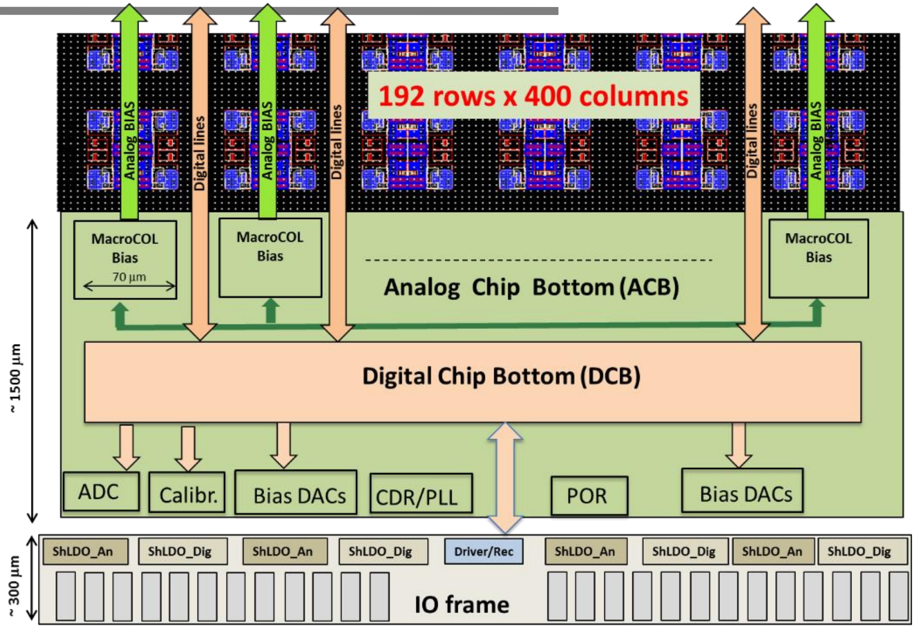
Itk layout

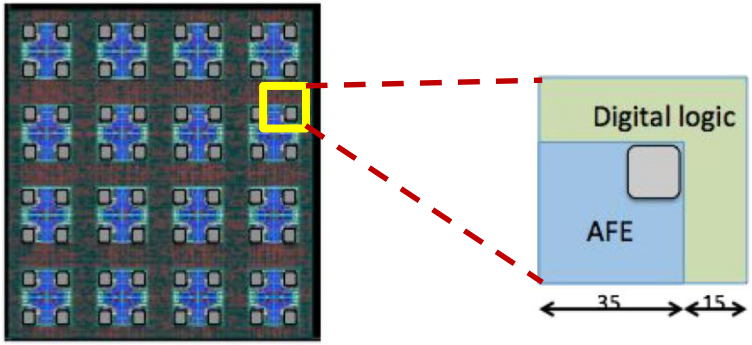

module
Flex
Wire-bond
FEIx
puce de lecture
Sensor
capteur Si
Bump-bond
Stave surface
modules à plat
brides
modules inclinés
échelles/ longerons

RD53A floorplan

- Array of 400 x 192 pixels
- Peripheral circuitry in the bottom of the chip
  - Bias, configuration, monitoring and readout
- I/O PADs is a single row in the bottom
- The pixel matrix : 8 x 8 pixel cores
  - 1 core → 16 analog islands with 4 fronts ends each
  - Analog FE embedded in a flat digital synthesized "sea"
- The digital core is synthesized as one digital circuit
  - Provides configuration bits to the analog islands receives four binary outputs from each island
  - Handles all processing of the binary outputs
  - Receives all input signal from the previous core closer to the chip bottom
  - Regenerates the signals for the next core
- Calibration pulses generated via commands starting from 2 DC voltages
  - Common calibration circuitry for the 3 FE flavours
  - Pulses can be phase shifted with a global fine delay (640 MHz clk).
- The clock and injection edge signals are internally delayed in the core to ensure a uniform timing (within 2 ns)

RD53A functional floorplan



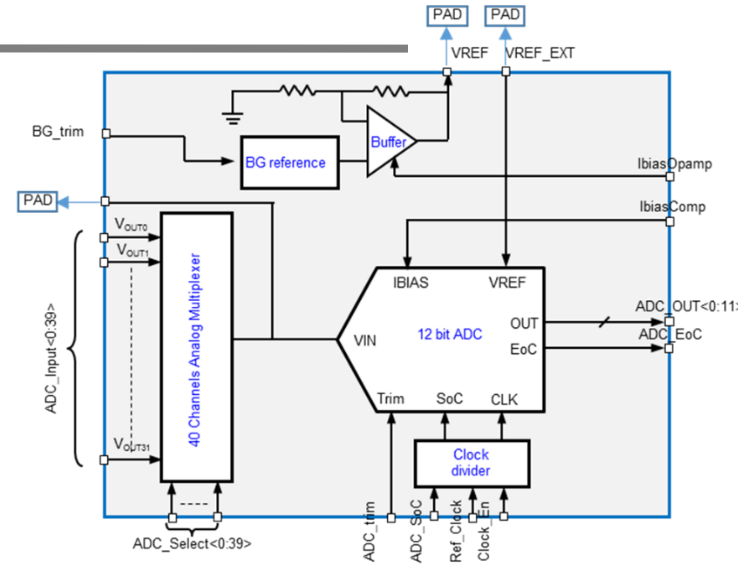


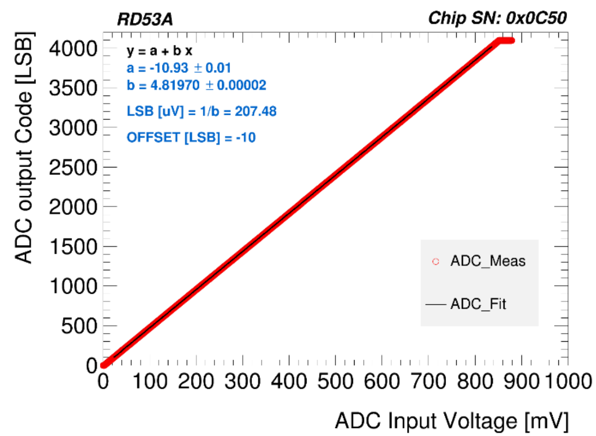
8 X 8 pixel core

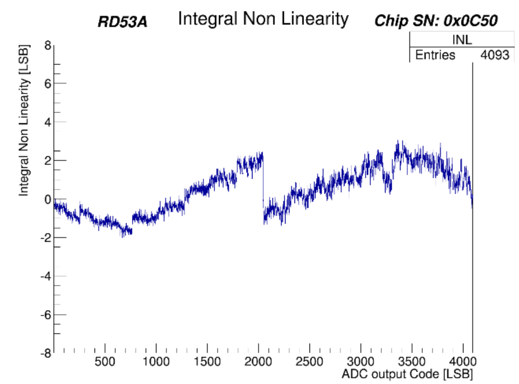
pixel

CPPM activities

- Test and qualification of 65 nm process for a dose level of 1 Grad
- CPPM leader of the irradiation RD53-WG
- Development of Irradiation corner model distributed to the collaboration
- Analog IP blocks
  - 12-bit ADC for monitoring
  - Bandgap voltage reference
  - Temperature sensor
  - Radiation monitor
- Analog pixel and Chip Bottom
  - SEU tolerant configuration memories
- Participation to the RD53A integration and verification
  - Monitoring block design
  - Verification and simulation
- Test of the RD53A chip : Irradiation, SEU ....

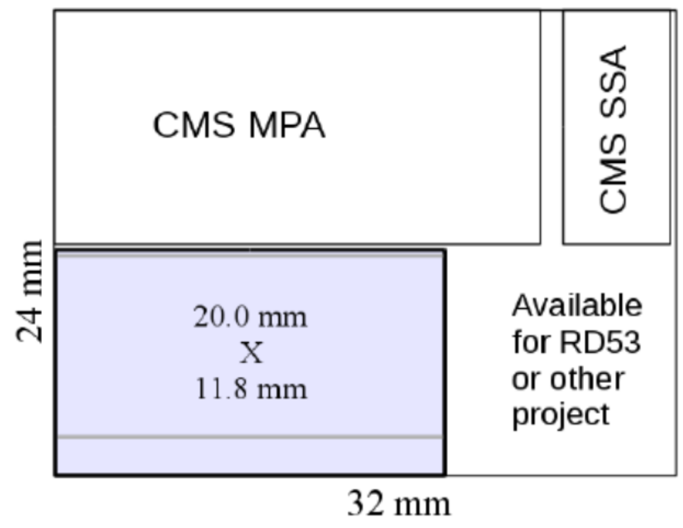






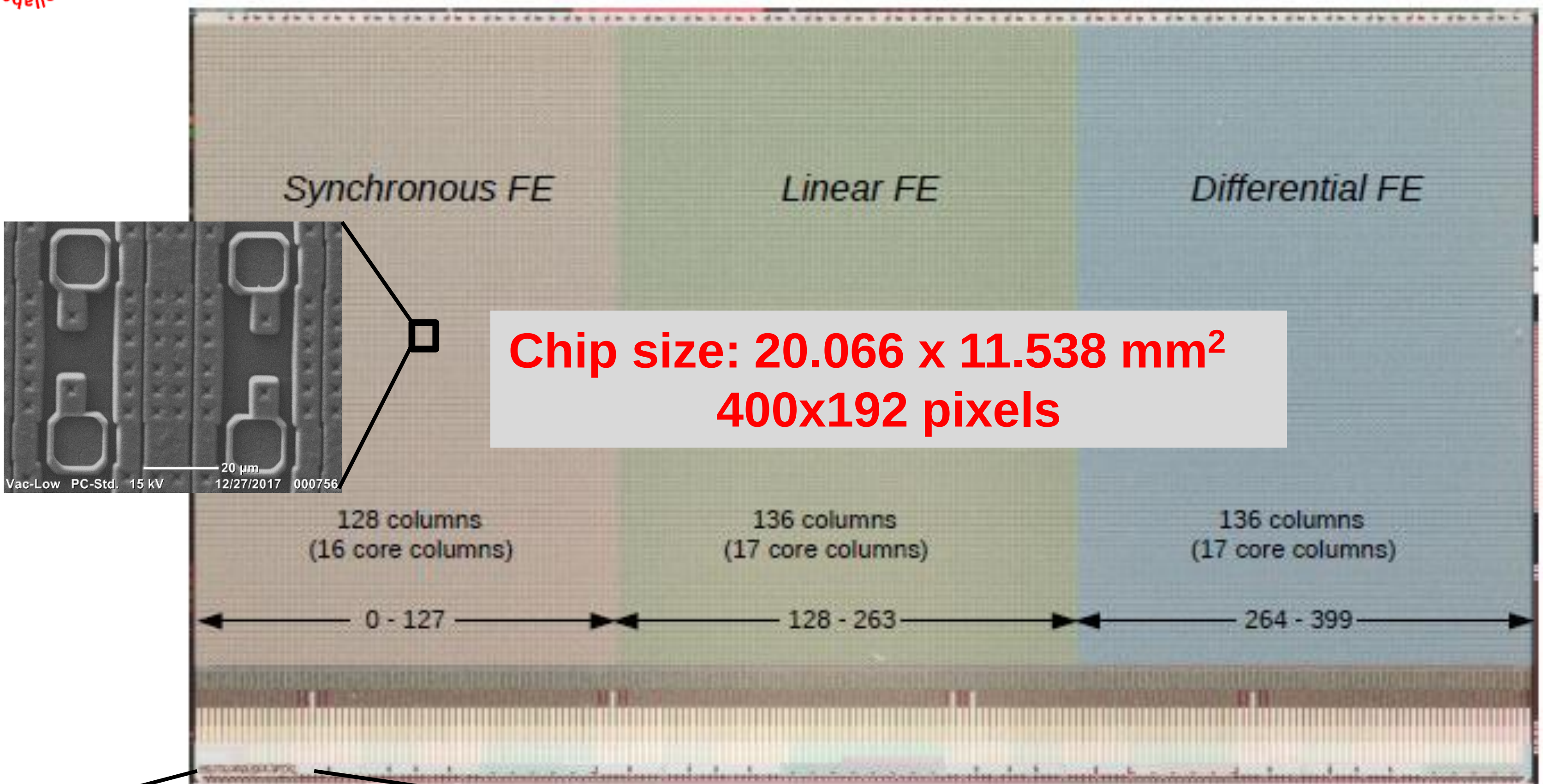
RD53A Specifications

Process	65 nm CMOS
Pixel size	50 x 50 µm^2
Pixels	192 x 400 = 76800 (50% of production chip)
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	< 600 e-
In-time threshold	< 1200 e-
Noise hits	< 10^{-6}
Hit rate	< 3 GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	Max 1 MHz
Digital buffer	12.5 µs
Hit loss at max hit rate (in-pixel pile-up)	≤1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	1-4 links @ 1.28 Gbit/s = max 5.12 Gbit/s
Radiation tolerance	500 Mrad, 1 10^{16} 1Mev eq. n/cm^2 at -15^{o}C
SEU for the whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1W/cm^2 including SLDO losses
Pixel analog / digital current	4 µA / 4 µA
Temperature range	-40 ^{o}C to +40 ^{o}C



- RD53A : Large scale demonstrator
- Common engineering run with CMS MPA to share a full reticle

RD53A: 3 analog flavors



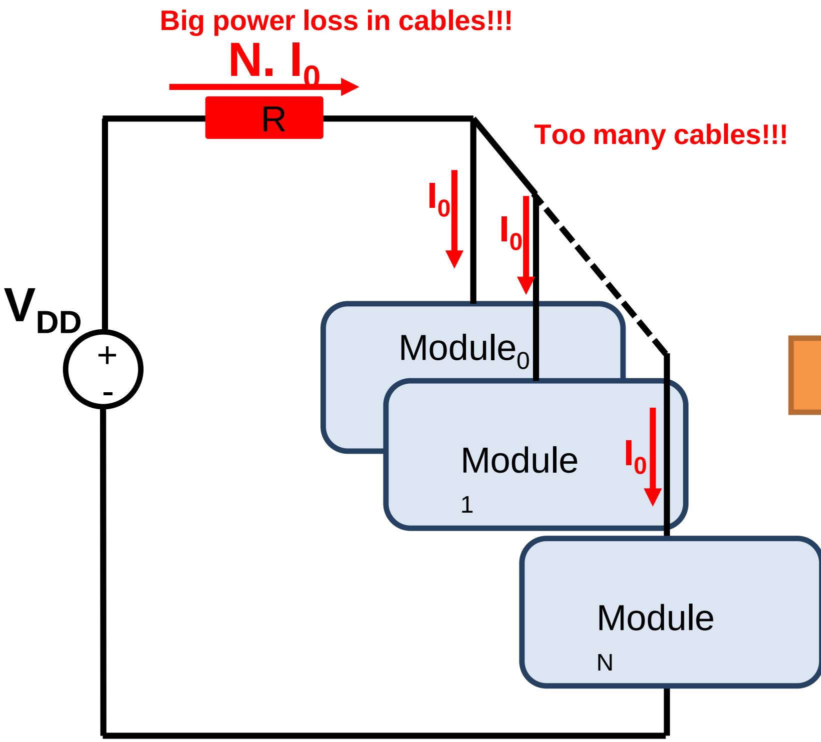
- **Aug. 31, 2017: Submission**
- **Dec. 6, 2017: First chip test**
- **Mar. 15, 2018: 25 wafers ordered**
- **Apr. 13, 2018: First bump-bonded chip test**

SEU protection of critical blocks

- Global strategy:
  - All digital global signals that could cause SEU problems at the chip level are deglitched before being routed.
  - No signal triplication has been performed.
- PixelRegion:
  - Triple Modular Redundancy (TMR) cannot be used due to area constraints.
  - RD53A relies on fast and continuous configuration refresh in order to mitigate SEU effects.
- Digital Chip Bottom:
  - All critical signals are deglitched.
  - TMR is used for Global Configuration. Automatically added to the design via script.
  - New Virtuoso version allows to spread triplicated FF's by a user defined distance (15 um were chosen).
- The new input protocol allows for fast and continuous writing of all configuration bits.
- The whole chip (including Pixel configuration bits) can be reconfigured in ~30 ms.

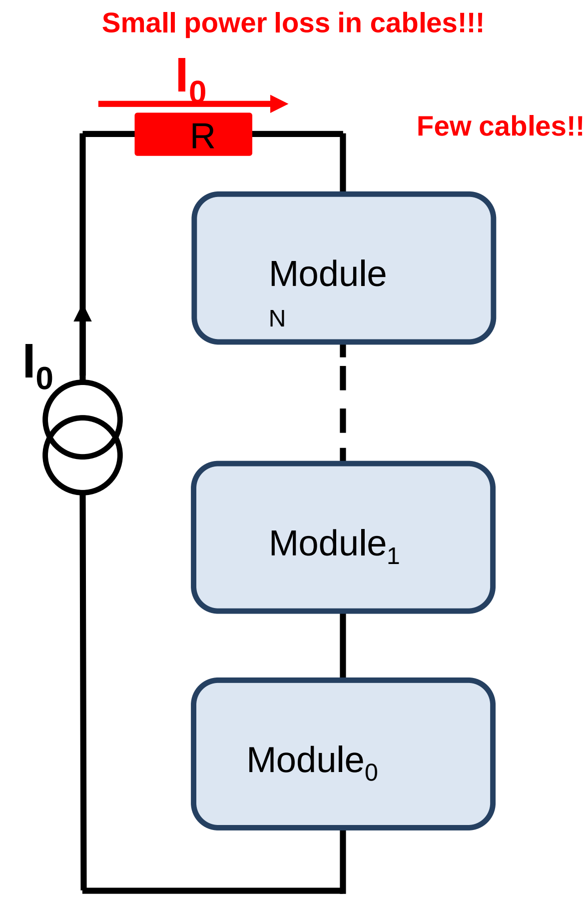
e.g. dvp new blocks: for Serial Powering

Traditional: Parallel Powering



Cannot be done in ITk

In ITk: Serial Powering

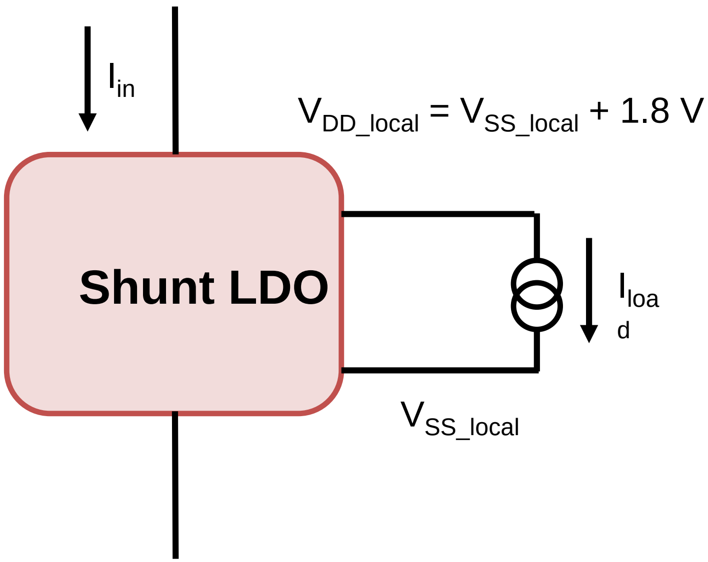


Solution for ITk

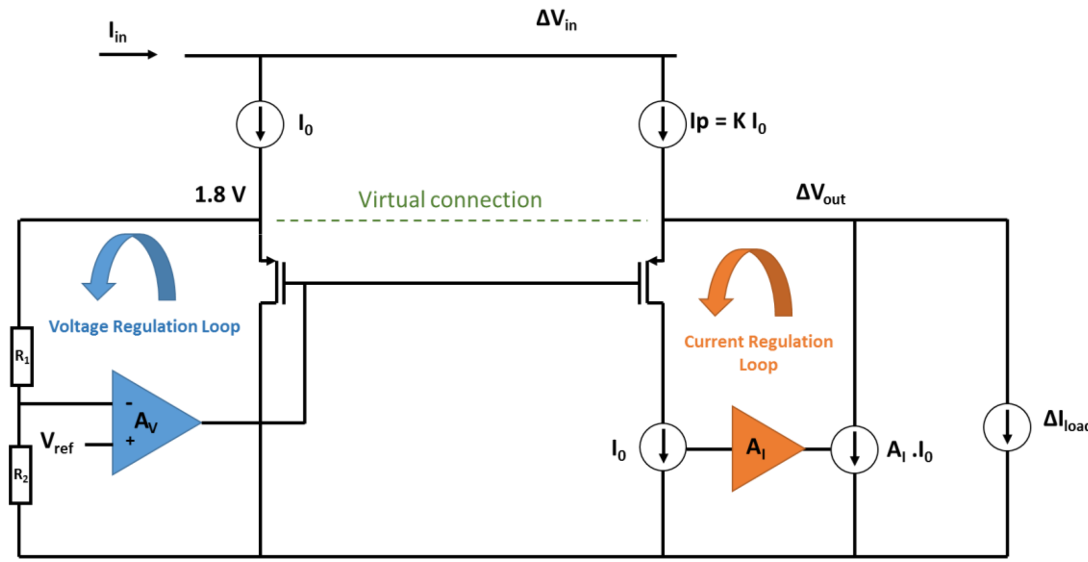
Shunt-LDO en TJ: to power electronics

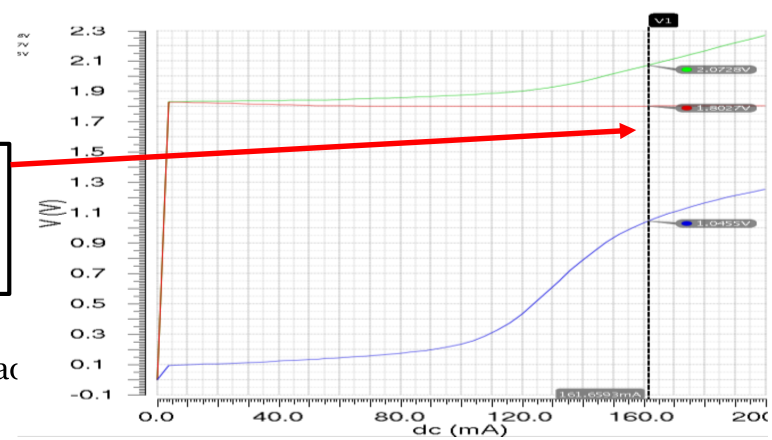
Shunt Low Drop Out Regulator

Main idea



Possible solution

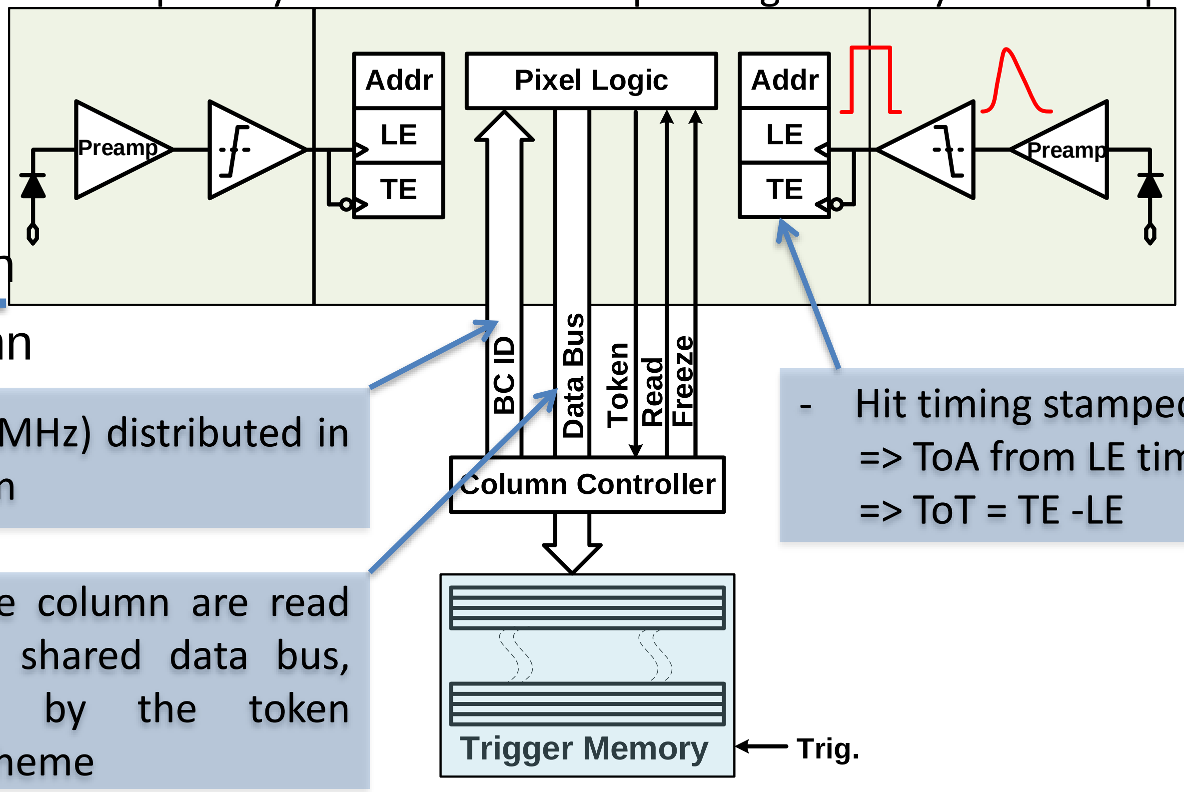




For a nominal current (160 lmA), V_{out} is regulated at 1.8V, with a drop out of 200 mV

LF-MONOPIX1
Column drain readout architecture

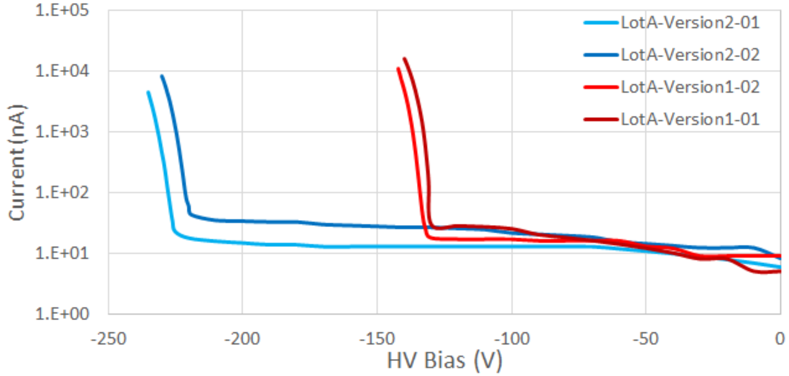
- Similar to the current ATLAS pixel readout chip **“FE-I3”**
  - Sufficient rate capability with affordable in-pixel logic density for CMOS pixels



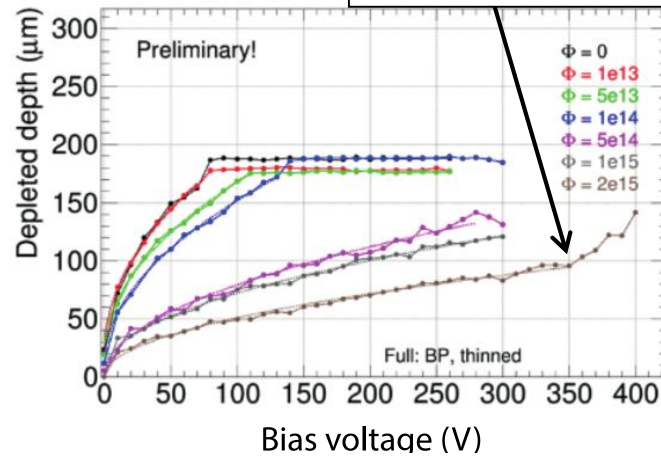
- BC ID (40 MHz) distributed in the column
- Hits in the column are read out on a shared data bus, arbitrated by the token passing scheme
- Hit timing stamped in pixel
  => ToA from LE time stamp
  => ToT = TE -LE

Results for LF

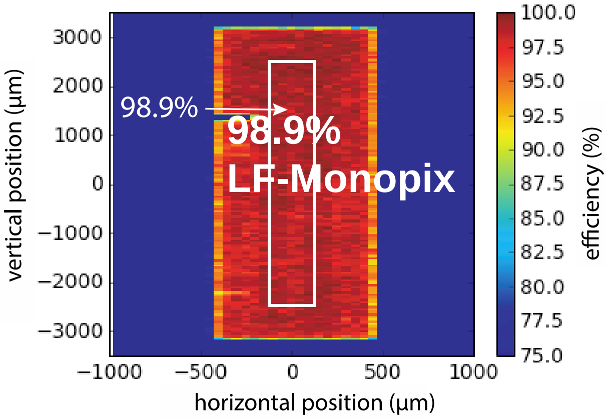
Thesis Jian Liu -Shandong-

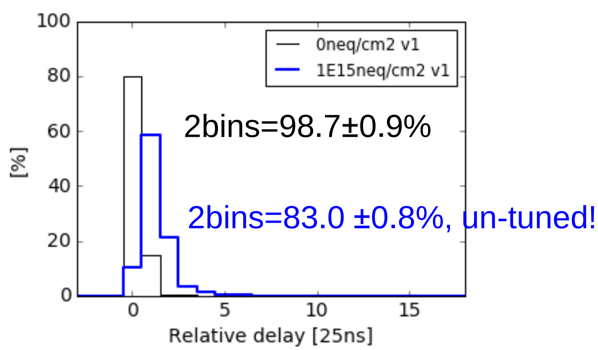


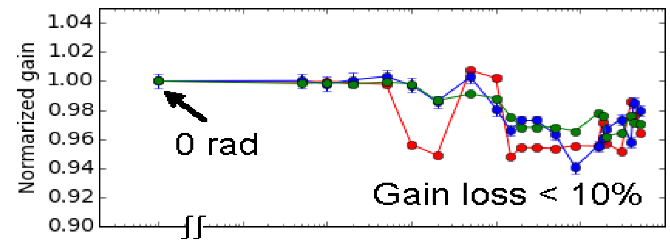
NIEL: 100µm @ 2×10^{15}

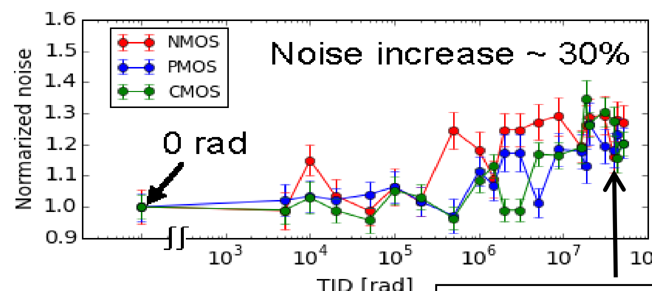


Efficiency @ 10^{15} $n_{eq}cm^{-2}$







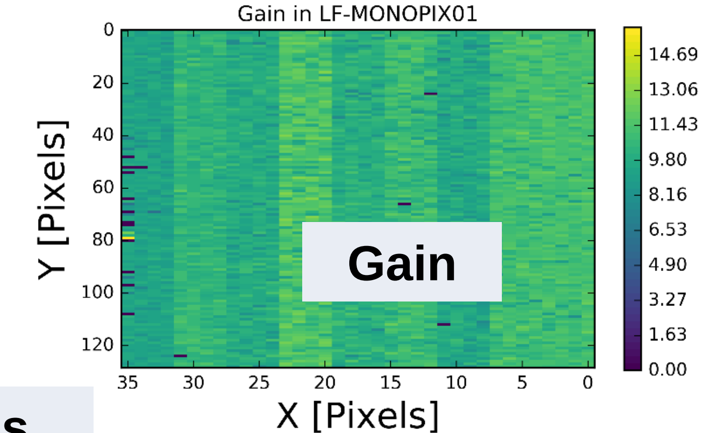


TID 100 MRad

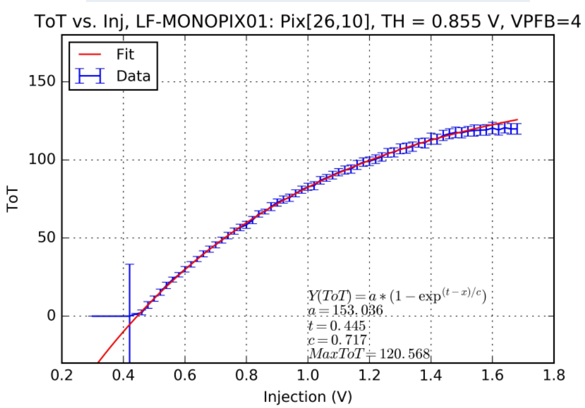
LF-MONOPIX1 : Laboratory results

- Breakdown @ **-280 V** => up to ~ 300 µm depletion
- ToT calibrated with sources: ^{241}Am, terbium
- Gain **10 -12 µV/e$^-$**
- Typical ENC ~ **200 e$^-$**
- Tunable threshold down to **1400 e$^-$**
  - dispersion ~ **100e$^-$** after tuning

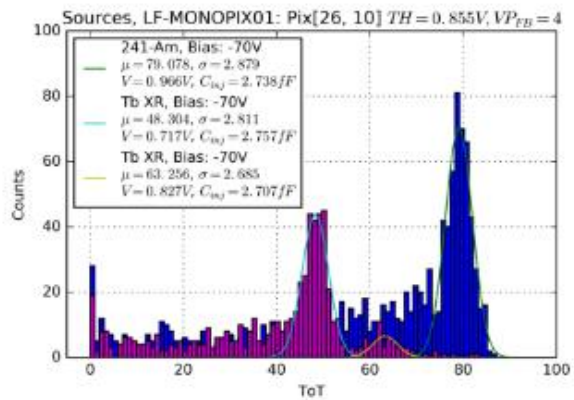
I. Caicedo @Bonn

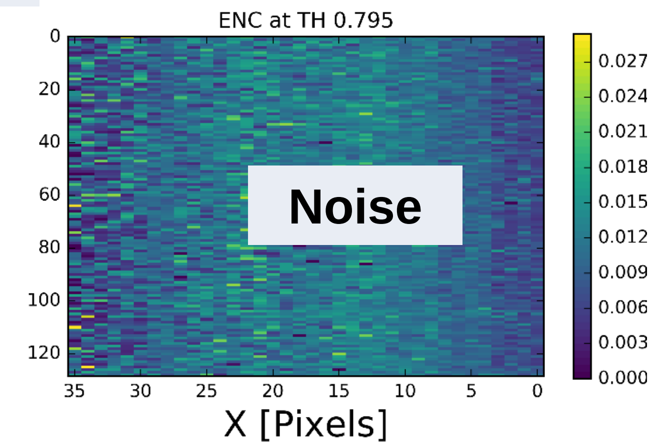


ToT vs. Injection

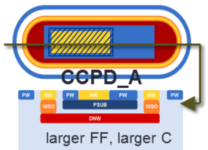


Response to sources

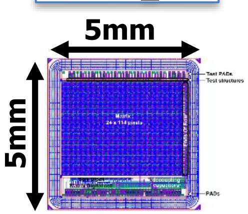




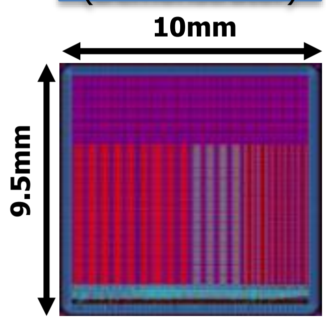
LFoundry DMAPS prototyping line



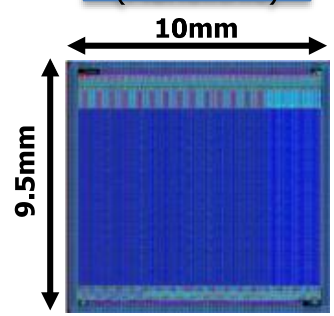
CCPD_LF

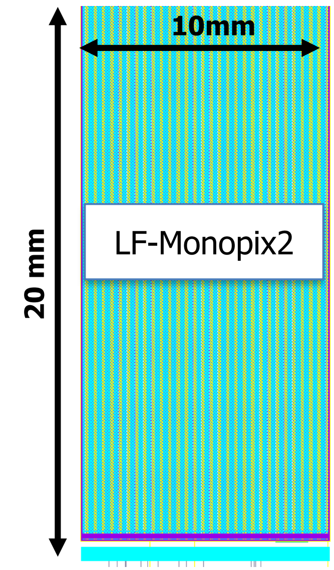


LF-CPIX (Demonstrator)



LF-Monopix1 (Monolithic)



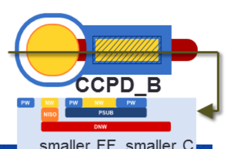


CCPD_LF
- *Subm. in **Sep. 2014***
- *33 x 125 μm² pixels*
- *Fast R/O coupled to FE-I4*
- *Standalone R/O for test*
- *Bonn/CPPM/KIT*

LF-CPIX (DEMO)
- *Subm. in **Mar. 2016***
- *50 x 250 μm² pixels*
- *Fast R/O coupled to FE-I4*
- *New Sensor Guard-Ring*
- *Standalone R/O for test*
- *Bonn/CPPM/IRFU*

LF-Monopix1
- *Subm. in **Aug. 2016***
- *50 x 250 μm² pixels*
- *Fast column drain R/O*
- *Bonn/CPPM/IRFU*

LF-Monopix2
- *Being designed*
- *50 x 150 μm² pixels*
- *Full height matrix*
- *Fast column drain R/O*
- *Bonn/CERN/CPPM/IRFU*



DMAPS collaboration

Developing detectors for HL-LHC environment is actually **paving the road** for a general use of this technology

- Generating a collaborative effort of **~25 ATLAS ITK institutes**
- Capable of attracting also non-ATLAS institutes and resources

Exploring **different solutions is paramount**:

- Every solution has pros and cons
  → avoid missing opportunities or delays by technical difficulties of one specific solution

- **Close collaboration** with foundries is critical
  → risk mitigation against industrial policies

WP6: Novel high voltage and resistive CMOS sensors

STREAM, Smart Sensor Technologies and Training for Radiation Enhanced Applications and Measurement
Innovative Training Network (ITN)
under the Marie Skłodowska-Curie Actions
https://stream.web.cern.ch/