



LLRF Activities at IMP

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Contents



- IMP Facilities Introduction
- LLRF Systems in IMP
 - Cyclotrons LLRF
 - Synchrotrons LLRF
 - ADS Linac LLRF
 - Prototype LLRF
- Future Porjects
 - HIAF
 - CiADS

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Overview of HIRFL



- Heavy Ion Research Facility in Lanzhou (HIRFL)
 - The largest ion-accelerator complex in China



The Injector SFC



- Built in 1961 with the assistance of the Soviet Union
- H&He 1970s, upgraded, Carbon~Uranium
 - K~ 69
 - R ~ 0.75 m
 - E ~ 10 MeV(C)
 - 1 MeV/u(U)



The Main Cyclotron SSC



- 1988
 - K~450
 - R ~3.203 m
 - α~U
 - E:100 MeV/u(C)
 - 10 MeV/u (U)





CSR

- Synchrotron and Storage Rings (CSR)
 - CSRm 161.0m
 - $G_{max} = 11.3Tm$



- CSRe 122.8m
- $G_{max} = 9.0 \text{ Tm}$



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- Analog system
 - ALC



- AFC





Details





- One master oscillator for all cavities
- Analogue feed back
- Temperature controled oven



Monitoring system of rf and beam stability based on Lock-in Amp.





Time (s)

Requirements of the LLRF System

- Regulate the amplitude and phase
- Beam Loading Compensation
- Adjust phase between different cavities
- Synchronous phase control
- Adjust the working frequency according to BPM signal
- All digital system
- Base cPCI Bus





BRing-gap voltage waveform





LLRF System of Sring and Bring

Multi-control loops of the LLRF



Principle Diagram of the Multi-Control Loops



• LLRF System of Sring and Bring



Principle Diagram of Phase/Amplitude stabilization Loop



• LLRF System of Sring and Bring



Principle Diagram of Demodulation and Digital Down Convert



• LLRF System of Sring and Bring

Hardware

- 6U 8-slot CompactPCI
- PICMG2.5 H.110 CT Bus
- PICMG2.1 Hot Swap compliant 64-bit
- backplane with P3 & P5 rear I/O
- Dual AC power inlets





cPCI-6520

- The 3rd generation Intel Core i7
- Dual channel DDR3 ECC memory
- Three independent displays
- USB 3.0 and PCI Express Gen3 support
- Remote management and optional TPM support

cPCIS-6418U



Hardware

- Xilinx XC5VSX95T-1FF1136
- Configurable Logic Blocks 160 x 46
- Max Distributed RAM 1,520Kb
- DSP48E 640, CMT 6, IObank 20





Main Board Block Diagram

Main Board





LLRF System of Sring and Bring

Hardware

- FMC interface
- 2CH, 14bit, 125MSPS, AD62P45, ADC
- 2CH, 16bit, 160MSPS, AD9777, DAC
- AD9516 clock chip





ADC/DAC Block Diagram

ADC/DAC Board

• LLRF System of Sring and Bring

Challenge

- Beam loading compensation

 $V_{cav}(t) = V_{cav,dr}(t) + V_{cav,wake}(t) + V_{cav,FF}(t)$ $= H_{dr}^{cav}(t) \cdot V_{dr}(t) + Z'_{cav}(t) \cdot I_{beam}(t) + Z_{FF}(t) \cdot I_{beam}(t)$













Required functions:

- Cavity field control
- Cavity resonance control
- RF reference generation and distribution
- HPRF protection

Table 1 : LLRF specifications

Frequency	162.5 MHz			
Operation mode	CW/Pulse			
Amplitude stability	0.3%			
Phase stability	0.3°			
Tunning	±1°			



• work mode:

normal mode: On the startup, work in Pulse mode to train the cavity, then switch to CW mode

commissioning mode: To avoid high radiation levels, during the commissioning of the machine, work in pulse mode

Self-Exited Loop

• special for RFQ:

Due to poor cooling system, heat detunes the cavity, On the startup LLRF takes self-exited loop to follow the resonance frequency of the cavity Once the RFQ has achieved steady operation, frequency change to MO (GDR)







10MeV with beam test result:



Test Results : Amplitude stability 3.5%, Phase stabiliy: $\pm 0.4^{\circ}$, ADS LLRF operating over 5000 Hs







9:58:05.359	2019/06/21 1					面	系统运行监测界	时频超导 系	9						
cher1	Bun	腔体相位误差	腔体幅度误差	相位。	Epk(MV/m)	联续准加	闭环状态&RF开关	CM1	腔体相位误差	腔体幅度误差	相位*	Epk(MV/m)	N.IKABXI	闭环状态&RF开关	CM1
	READY	0	-1	138.0	20.5	0	0	CM1-4	2	0	20.1	7.8	0	0	CM1-1
22480.00	AMP	0	-1	-41.2	16.9		0	CM1-5	24	0	-3.3	17.4		0	CM1-2
44.17	PHASE	-3	0	105.7	19.5		0	CM1-6	0	0	-107.2	9.6			CM1-3
104.54	VACC		_												
204.54	VACC	腔体相位误差	腔体幅度误差	相位。	Epk(MV/m)	UKSEXI	闭环状态&RF开关	CM2	腔体相位误差	腔体幅度误差	相位。	Epk(MV/m)	联统准加	团环状态&RF开关	CM2
3.69	PW_IN	2	-1	81.3	27.9	۲	0	CM2-4	22	0	70.3	25.0	0	0	CM2-1
0.67	PW_RE	42	-13	-59.0	22.9	0	0	CM2-5	0	-1	-86.7	27.5		0	CM2-2
23900 +	AMP_SET	-79	8	21.8	34.0	0	0	CM2-6	-1	2	105.6	32.5		0	CM2-3
51.3 ×	PHASE_SET														
cher2	Bun	腔体相位误差	腔体幅度误差	相位。	Epk(MV/m)	联顿准加	团环状态&RF开关	СМЗ	腔体相位误差	腔体幅度误差	相位。	Epk(MV/m)	联续准加	团环状态&RF开关	CM3
	READY	6	0	-176.7	28.2	0	0	CM3-4	2	0	-53.0	13.0	۲	0	CM3-1
12806.00	AMP	6	2	13.2	25.4	۲	0	CM3-5	6	-1	-2.6	25.9	۲	0	CM3-2
131.37	PHASE								8	2	-130.1	28.5	0	0	CM3-3
114.54	VACC														
4 79	DW/ IN	腔体相位误差	腔体幅度误差	相位。	Epk(MV/m)	联锁准加	闭环状态&RF开关	CM4	腔体相位误差。	腔体幅度误差%	相位。	Epk(MV/m)	联锁机加	闭环状态&RF开关	CM4
4.70	PW_IN	-48.9	100.0	119.6	0.0	۲	0	СМ4-4	-17.1	100.0	90.0	0.0	۲	0	CM4-1
0.21	PW_RE	-40.6	100.0	-180.0	0.0	۲	0	CM4-5	-139.4	100.0	-105.9	0.0		0	CM4-2
12738 🚖	AMP_SET	-159.4	99.8	-153.8	0.0	0	0	CM4-6	-137.7	100.0	-90.0	0.0	۲	0	CM4-3
131.4 🚖	PHASE_SET					_				_					

Prototype LLRF System







clocks distribution



Frequency Conversion



Mixer: ZMY-2+ Mini-Circuit





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Future Projects



Recent and future projects based on HIRFL



Future Projects

- Universal Hardware
 - LLRF
 - Timing system
 - Beam diagnostic system
 - Data acquisition system

- ...

- Backplane bus standard
 - mTCA
 - PCle
 - ...

Summary



- LLRF Activities in IMP:
- Cyclotrons LLRF (SFC, SSC)
 - Adopted analog circuit
 - consists of Phase stabilizer, amplitude controller and tuning controller.
- Synchrotrons LLRF (CSRm, CSRe)
 - The low level control system aims to realize the adjustment and stability of rf acceleration voltage, synchronization of acceleration voltage and beam phase, rf frequency correction, beam load feedforward and feedback and other control functions to ensure the stable operation of rf system in accordance with physical requirements.
- ADS linac LLRF
 - To control the cavity to work in the resonance state under the condition of large beam load and strong Lorentz force detuning to reducing the rolling fluctuation. The effects of temperature, cavity deformation and noise on the tuning process.



Thanks for your attention!