MTCA GS ADCs & user firmware integration

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The MTCA/ATCA Workshop for Research and Industry
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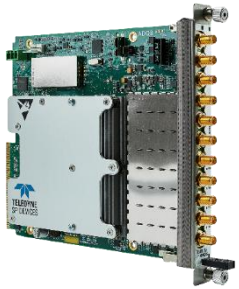
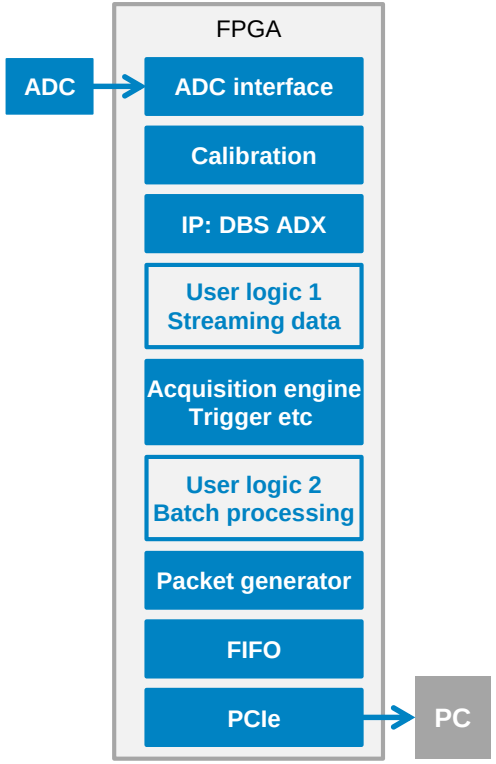
Agenda

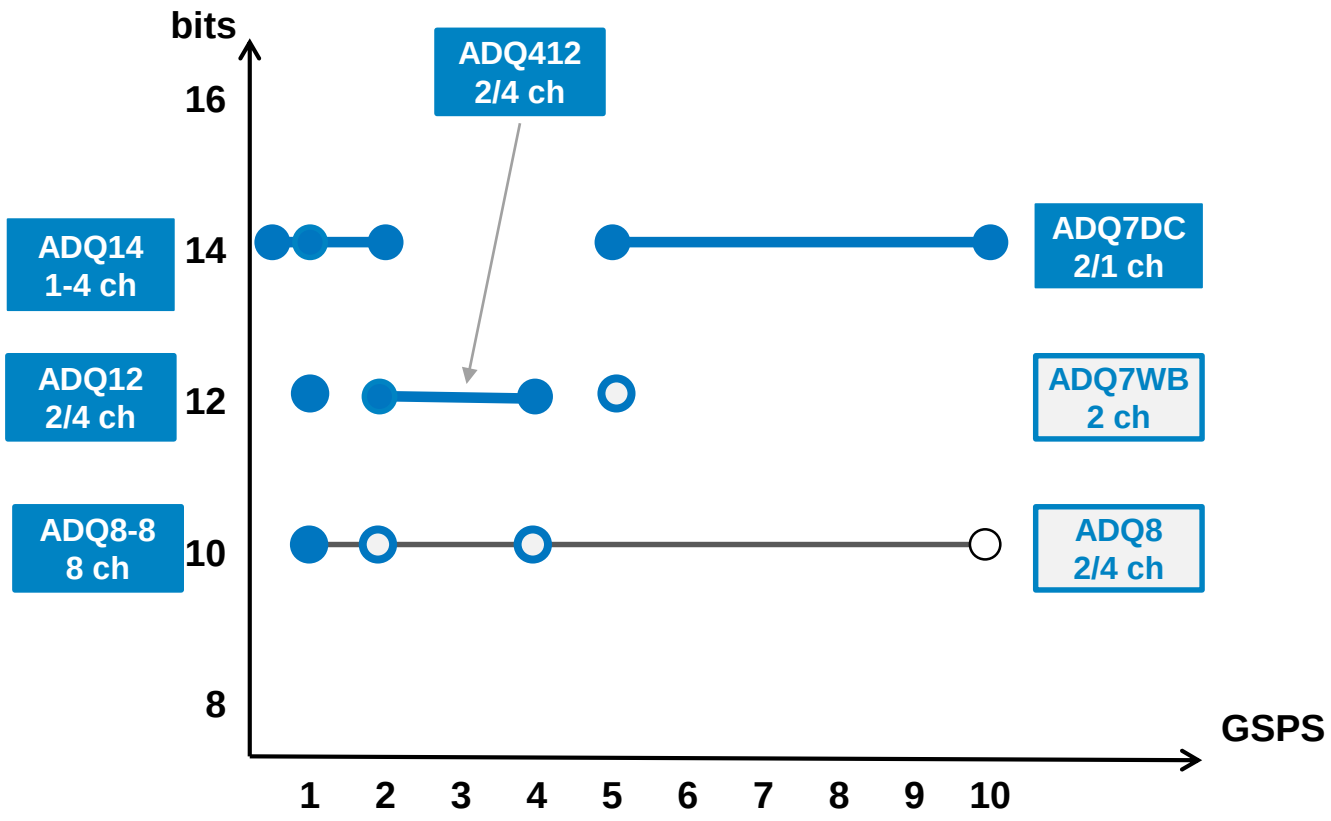
- Latest GS ADCs for MTCA.4
- Upcoming GS ADCs for MTCA.4
- Open FPGA Digitizer firmware framework
- Trigger time interpolation use case





Roadmap hardware (3rd gen)

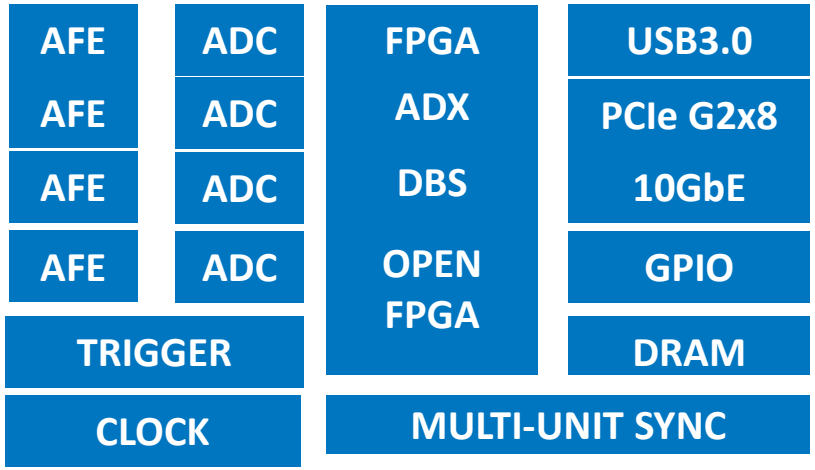
Available | In development



ADQ14 Series Digitizer

(working horse)

- **14 bits** vertical resolution
- ADQ14 supports 1, 2, or 4 channels
- Sampling rates of 500, 1000, or **2000 MSPS**
- AC- or DC-coupled analog front-ends
- Optional variable gain
- **Open** Xilinx Kintex 7 K325T **FPGA**
- **Proprietary performance enhancement IP**
- 2 Gbyte on-board DDR3 DRAM
- General-purpose I/O (GPIO)
- High-precision trigger (resolution:125ps; jitter:25ps)
- Flexible clocking capabilities
- Multi-channel synchronization support
- Multiple form factors
- 3.2Gbytes/s sustained data transfer (PCIe gen2x8)



- SDK supporting multiple environments
- Windows and Linux support
- Firmware options for pulse detection, averaging and software defined radio
- FPGA firmware development kit
- **EPICS** support

ADQ14 - Success Story – W7-X

- Wendelstein 7-X stellarator at Max-Planck IPP
- Thomson scattering for plasma temperature measurement
- ADQ14DC-4C-MTCA
  - 14 bits vertical resolution, 4 channels @ 1 GSPS
  - 70 Boards, 280 channels, synchronized sampling
- Comment from the customer[1]:

“The combination of 14 bits dynamic range and 1 GS/s sampling rate is taking the performance of digitizer for TS system to an unprecedented performance level. The ADC boards are also equipped with Kintex-7 FPGAs for real-time signal processing.”

[1] “The Thomson scattering System at Wendelstein 7-X”

ADQ7- Series Digitizers

(highest performance)

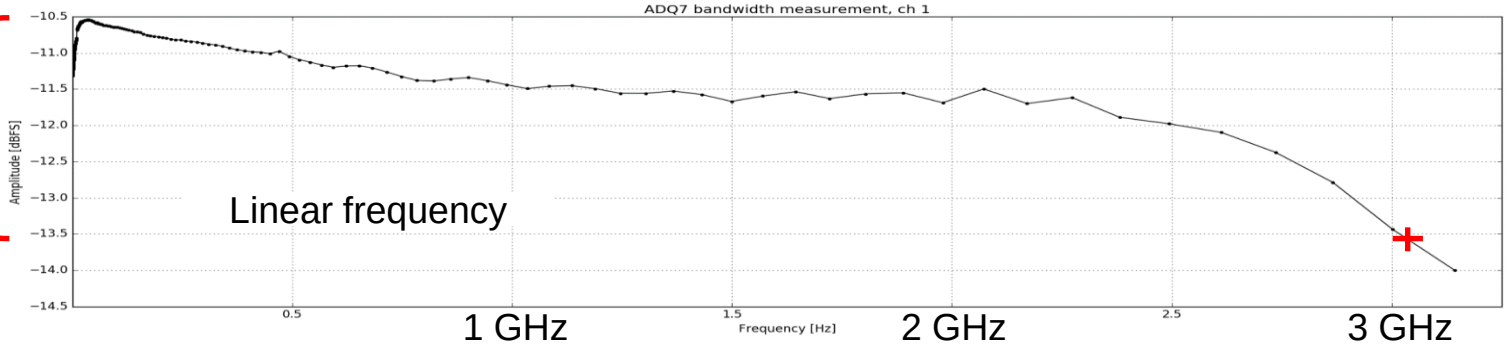
ADQ7DC

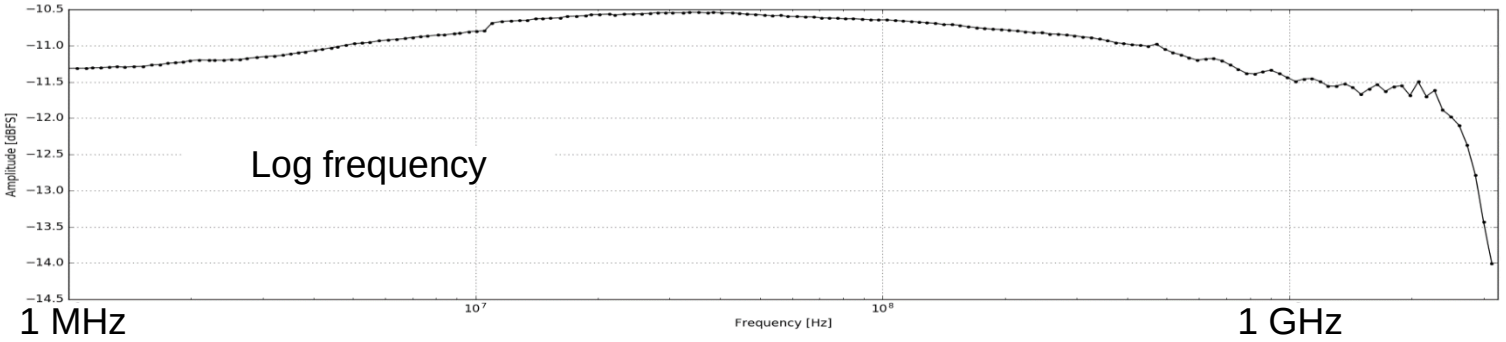
- **14 bits** vertical resolution
- DC-coupled version for pulse data
  - 1 / 2 channel @ **10 / 5 GSPS**
  - **3 GHz analog bandwidth**
- **Proprietary performance enhancement IP**
- 4 Gbyte onboard DRAM
- **Open** Xilinx Ultrascale **FPGA** XCKU085
- High-precision trigger (50 ps)
- Flexible clocking capabilities
- Multi-channel synchronization support
- Multiple form factors incl. MTCA.4
- 6.8 Gbyte/s peak data transfer (PCIe gen3x8)

- SDK supporting multiple environments
- Windows and Linux support
- Firmware options for pulse detection, advanced time-domain and software defined radio
- FPGA firmware development kit option
- **EPICS** support

ADQ7DC - Bandwidth (1 channel 10 GSPS)

-3 dB

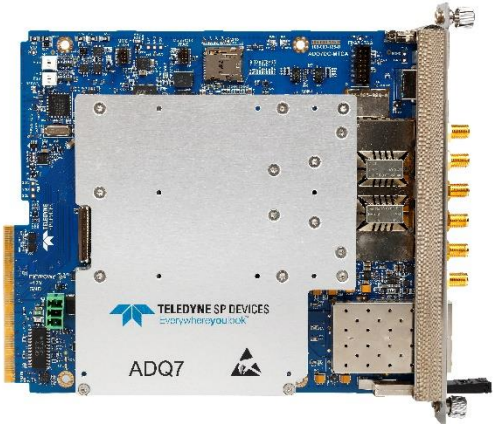




Preview: ADQ7WB- Series Digitizers (largest analog bandwidth)

Wideband digitizer key specifications

- **12 bits** vertical resolution
- **AC-coupled** version for RF capture
  - **2 channels @ 5 GSPS**
  - **Target 4-6 GHz analog bandwidth**
- **Proprietary performance enhancement IP**
- 4 Gbyte onboard DRAM
- **Open** Xilinx Ultrascale **FPGA** XCKU085
- High-precision trigger (50 ps)
- Flexible clocking capabilities
- Multi-channel synchronization support
- PCIe and PXIe form factors (MTCA tbd)
- 6.8 Gbyte/s peak data transfer (PCIe gen3x8)

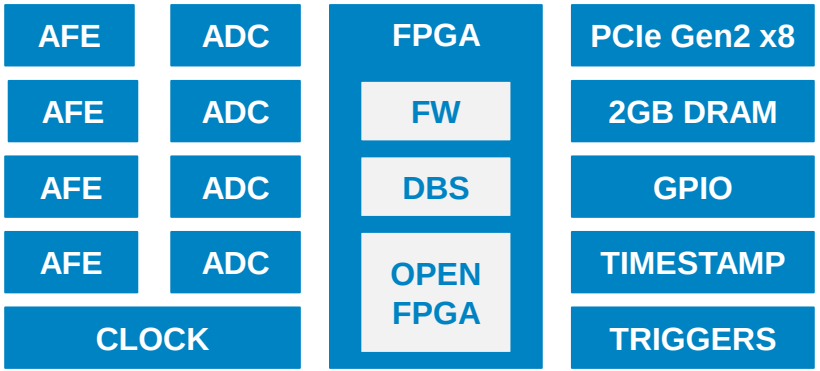


- SDK supporting multiple environments
- Windows and Linux support
- Digital downconverter firmware option
- FPGA firmware development kit option

ADQ12 Series Digitizer

(no export license required)

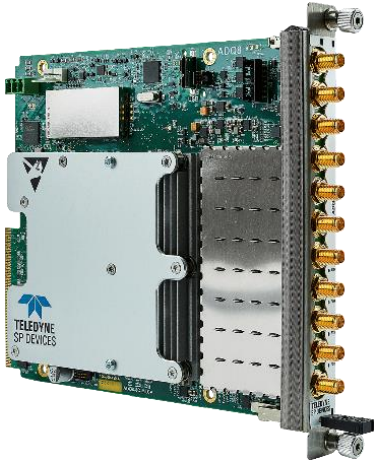
- **12 bits** vertical resolution
- **2 or 4 channels**
- Sampling rate **1000 MSPS**
- AC- or DC-coupled analog front-ends
- Variable gain option
- **Open** Xilinx Kintex 7 K325T **FPGA**
- **Proprietary performance enhancement IP**
- 2 Gbyte on-board DDR3 DRAM
- General-purpose I/O (GPIO)
- High-precision trigger (resolution:125ps; jitter:25ps)
- Flexible clocking capabilities
- Multi-channel synchronization support
- Multiple form factors
- 3.2Gbytes/s sustained data transfer (PCIe gen2x8)



- Data acquisition firmware
- Application firmware option for pulse detection
- Application firmware option for averaging

ADQ8-8 Series Digitizer (highest channel count & no export license required)

- **10-bit** vertical resolution
- **8 channels** with **1 GSPS** / channel
- DC - 500 MHz
- Variable gain from 0.25Vpp to 5Vpp
- DRAM: 1 Gbyte
- 1-slot, MTCA.4
- **Proprietary performance enhancement IP**
- **Open** Xilinx Kintex 7 K325T **FPGA**
- Superior timing engine
  - **4µs re-arm time**
  - 25ps Trigger time-resolution
  - Internal clock reference: 10 MHz +/- 3 ppm
  - Time-stamp information
- **EPICS** tbd



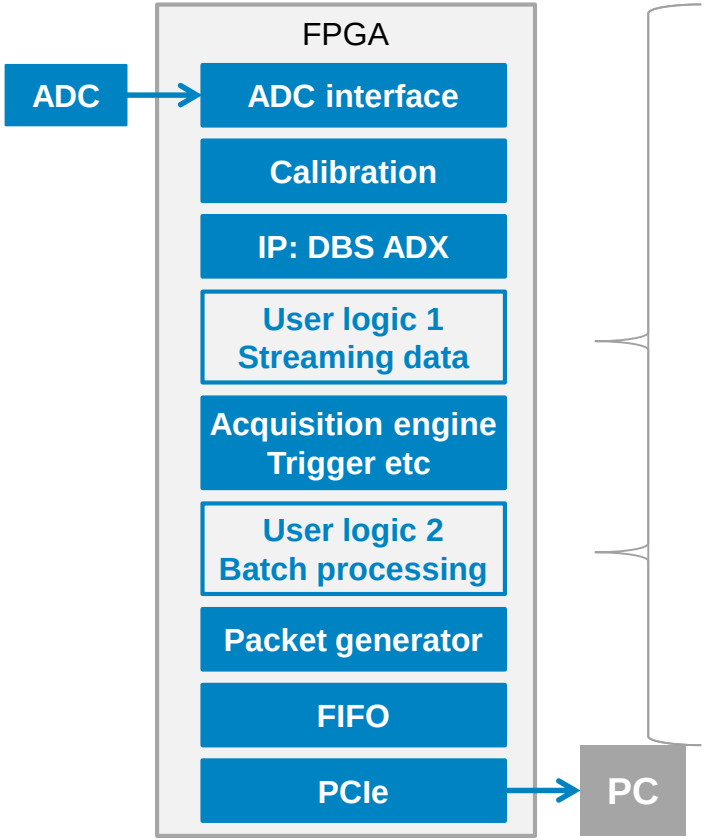
- Options
  - FPGA development kit
- *Possible*
  - *52ns re-arm time*
  - *Pulse detection firmware*

Preview: ADQ8-4X Series Digitizer

- **10-bit** vertical resolution
- **4 channels** @ **2 GSPS** or **2channels** @ **4GSPS**
- DC - 1000 MHz
- Fixed gain 0.25Vpp?
- DRAM: 1 Gbyte
- 1-slot, MTCA.4
- **Proprietary performance enhancement IP**
- **Open** Xilinx Kintex 7 K325T **FPGA**
- Superior timing engine
  - **4µs re-arm time**
  - 25ps Trigger time-resolution
  - Internal clock reference: 10 MHz +/- 3 ppm
  - Time-stamp information
- **EPICS** tbd

- Options
  - FPGA development kit
- *Possible*
  - *52ns re-arm time*
  - *Pulse detection firmware*

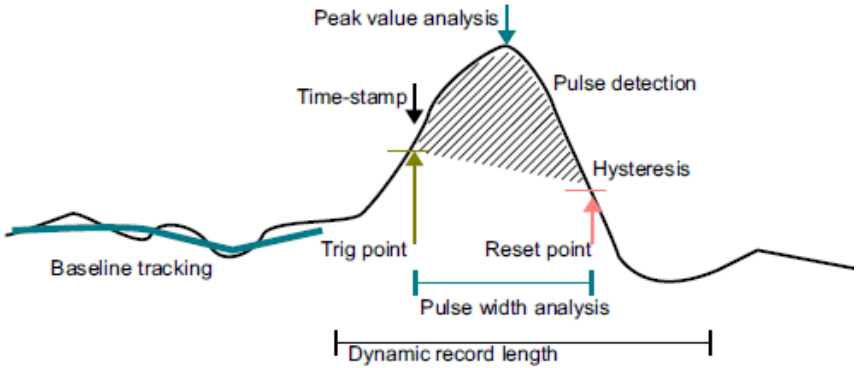
Digitizer Firmware framework

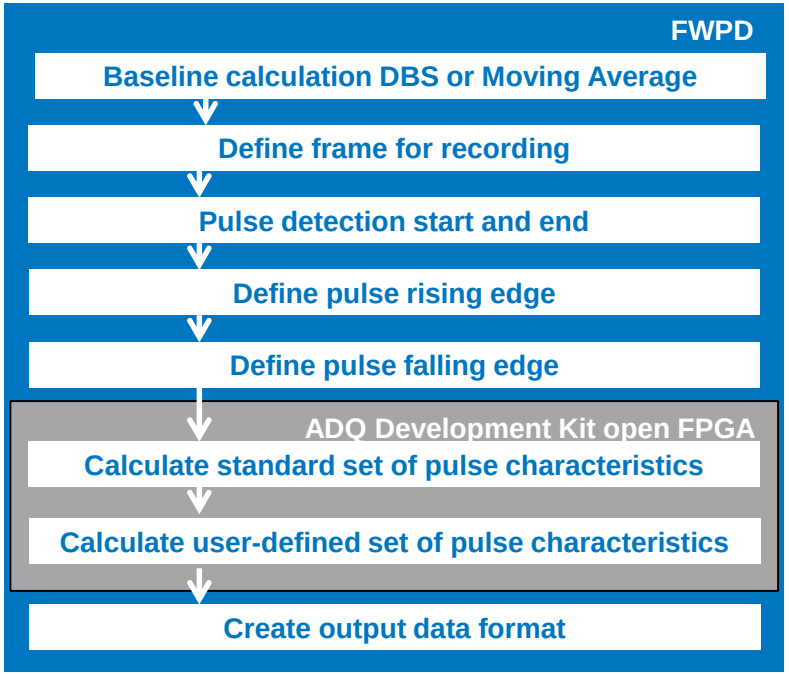


- Framework
  - Base digitizer functions
  - Unique signal processing IP
- Application specific firmware options
  - FWPD
  - FWATD
  - FW4DDC
- 2 user logic firmware blocks
  - Streaming data
  - Batch data

Pulse detection firmware “FWPD” & user logic

- Key specifications
  - Baseline stabilization with moving averaging filter or DBS IP
  - Adaptive record length for zero suppression
  - Individual trigger and data recording
  - Coincidence trigger for channels interaction
  - Histogram calculation of pulse width and peak value
  - Time-stamp with 25ps precision

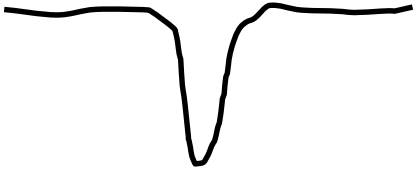




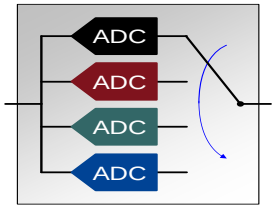
Digital Baseline Stabilizer IP “DBS”

(most appreciated IP)

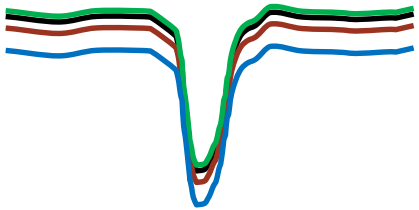
Interleaving correction



High frequency
input signal

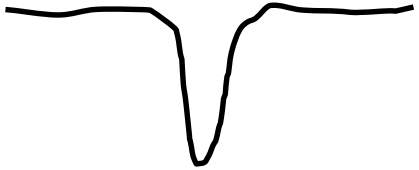


Interleaved ADCs for
high sample rate



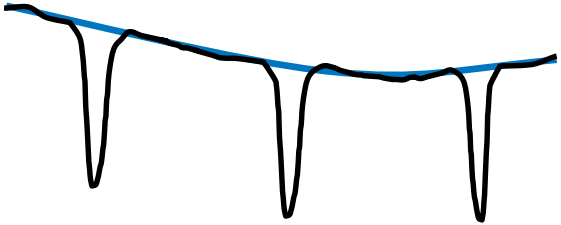
Typical distorted
time-interleaved signal

DBS corrects for
base-line differences



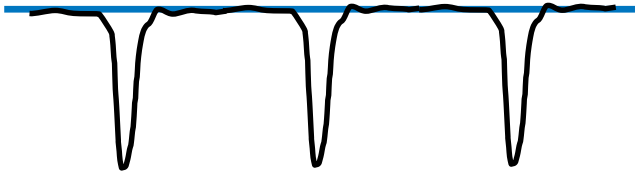
Signal restored by DBS

Baseline stabilizer



Baseline fluctuation
(for example due to temperature)

DBS corrects for base-
line variations

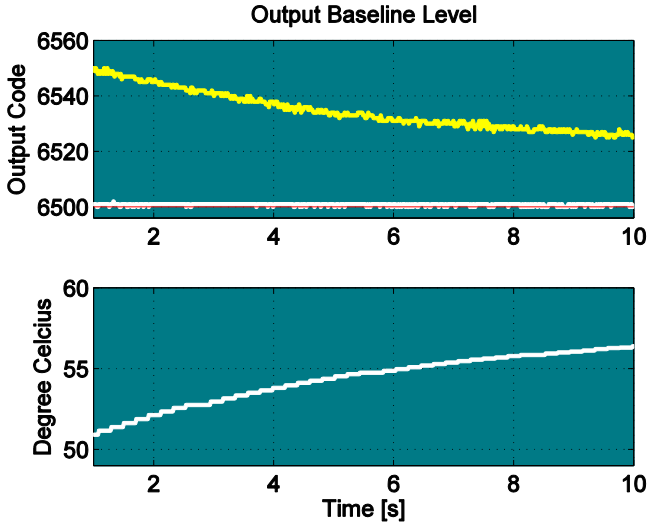


Signal restored by DBS

DBS – Digital Baseline Stabilization

Digital Baseline Stabilizer tracks slow and periodic baseline variation

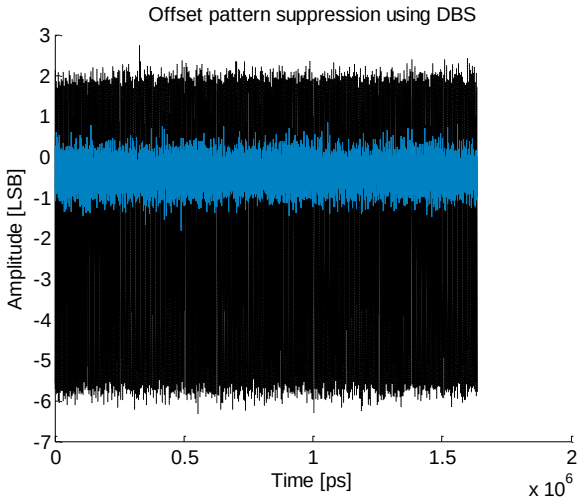
- Temperature variation
- Component aging
- Pattern noise from ADC due to interleaving



DBS benefit versus temperature variation

DBS disabled

DBS enabled

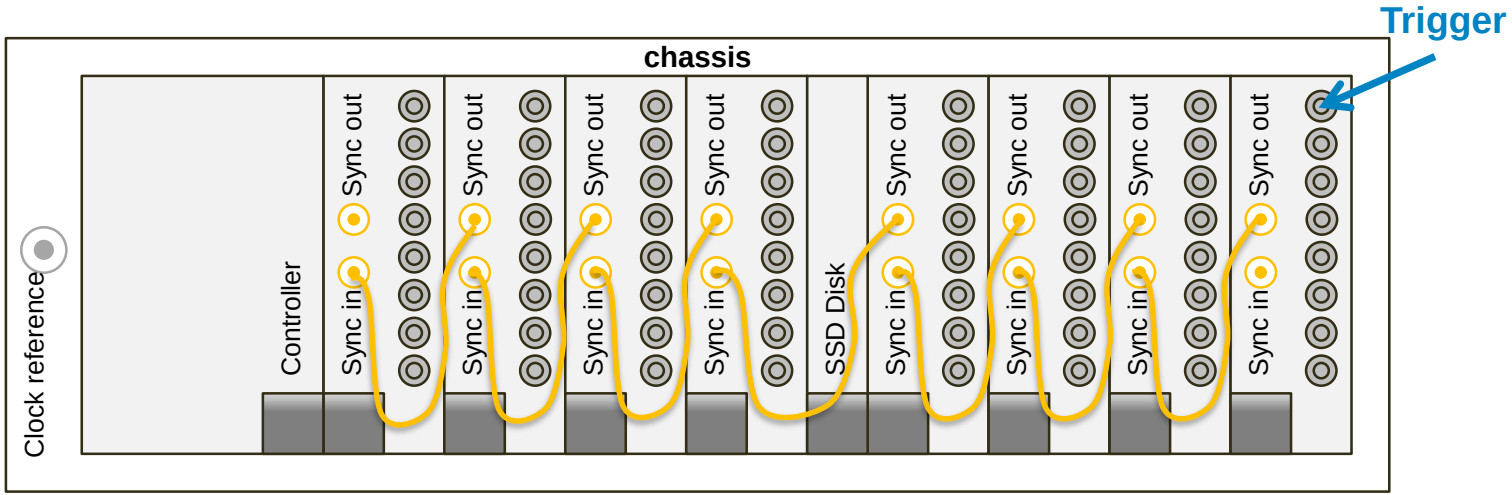


DBS benefit versus pattern noise

Trigger method for large scale systems (196 channels + 196 channels + …)

We developed an automated calibration routine

- Use one channel as trigger for interpolation of trigger timing <25ps
- Chassis clock reference for timing alignment
- Factory calibration timing between ADQ modules
- Daisy chain trigger distribution
- Calculate trigger position for each channel



Summary

- GigaSample Digitizers ranging from
  - 1GSPS – **10GSPS** sampling rate
  - 10-bit – **14-bit** vertical resolution
  - 500MHz – 6GHz analog bandwidth
  - **Proprietary performance enhancement IP**

- Open Digitizer framework enabling combination of
  - Out of the box base digitizer functionality
  - Access to **Proprietary performance enhancement IP**
  - **Open FPGA** for adding user-defined real-time algorithms

- Trigger method for large scale systems
  - We have the know-how to help you with timing challenges

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