ADS Timing System

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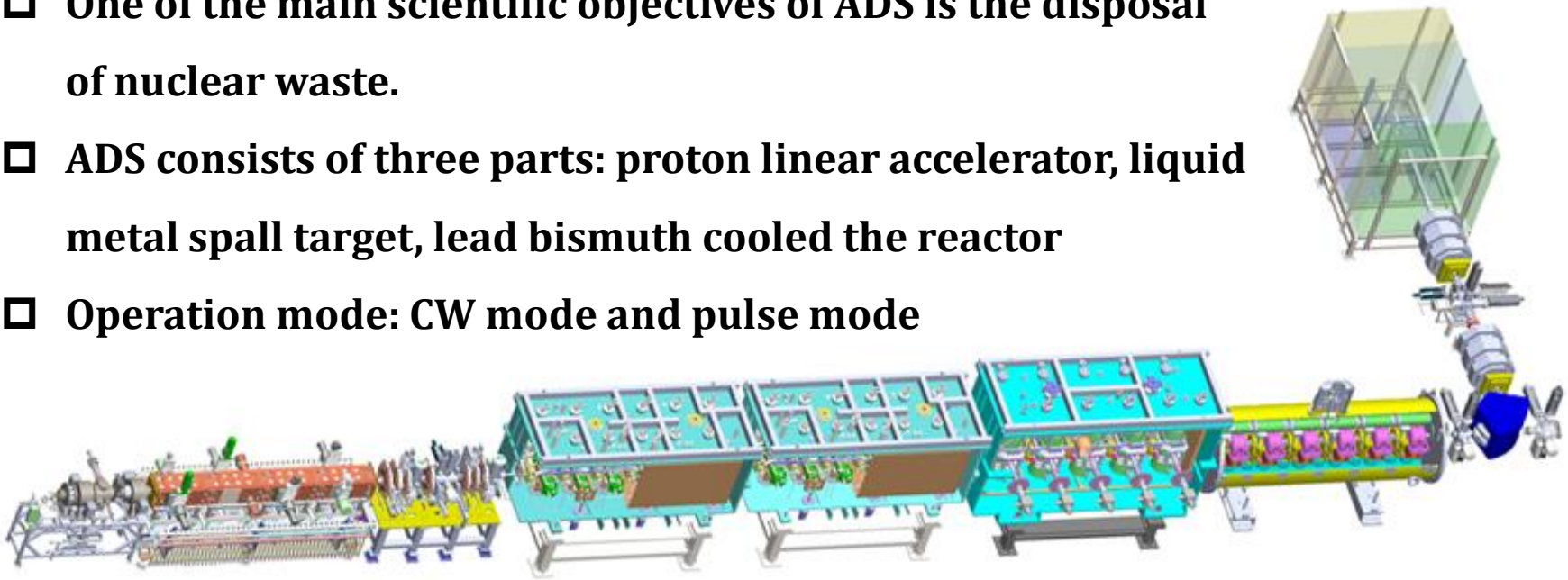
Outline

- Introduction of ADS project
- Objectives of the timing system
- Scheme and operation status
- Improvement based on WR
- WR testing and progress
- The next work plan

ADS Front-end Demo Linac (2011-2017)

- One of the main scientific objectives of ADS is the disposal of nuclear waste.
- ADS consists of three parts: proton linear accelerator, liquid metal spall target, lead bismuth cooled the reactor
- Operation mode: CW mode and pulse mode



Prototype of the front part of the 25MeV proton linear accelerator

- Completed in 2016, with 25MeV pulse beam test
- Verify the technical scheme of CiADS low energy section
- do technical research for CiADS accelerator

ECR + LEBT + RFQ + MEBT + CM1 + CM2 + CM3 + CM4 + HEBT

One of mission objective of timing system

- In the pulse operation mode, synchronization and trigger signals are provided for related devices

EVG/EVR 1 chassis
(input signal 162.5MHz)
provided by IMP

EVG/EVR 2 chassis
(input signal 325MHz)
provided by IHEP

These devices include: microwave machines for ion sources 、 LEBT chopper、 LLRF、 BPM、 Beam detection equipment

Task objective 2 of timing system

- **Realize chain protection function**

Normal operation (high pulse width)

When fault signal coming and the pulse width automatically changes to low pulse width

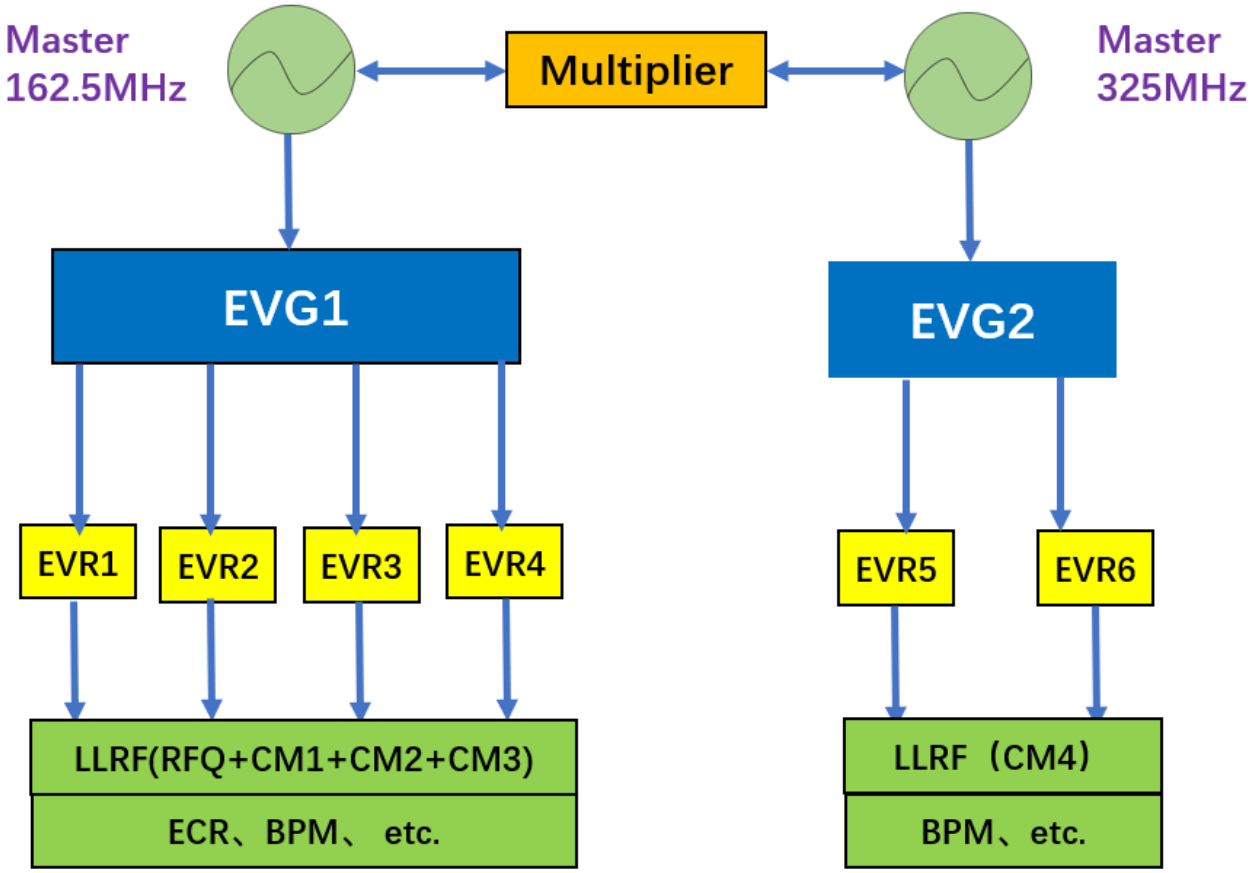
Combined with the MPS system, the low duty ratio pulse beam in the accelerators can avoid the damage caused by beam bombardment to the key equipment distributed on the beam line due to the low energy

Technical indicators of ADS Timing System

Demand target:

project	parameter
Trigger period	1μs~10s
Delay range	0~10ms
Delay accuracy (step)	≤0.25ns
The pulse width	0~10ms
Pulse width precision	≤6ns
Level standard	3.3V LVTTL、5V TTL
Total number of triggers	≥33
jitter	≤50ps（RMS）
Rising edge of delay signal	≤3ns

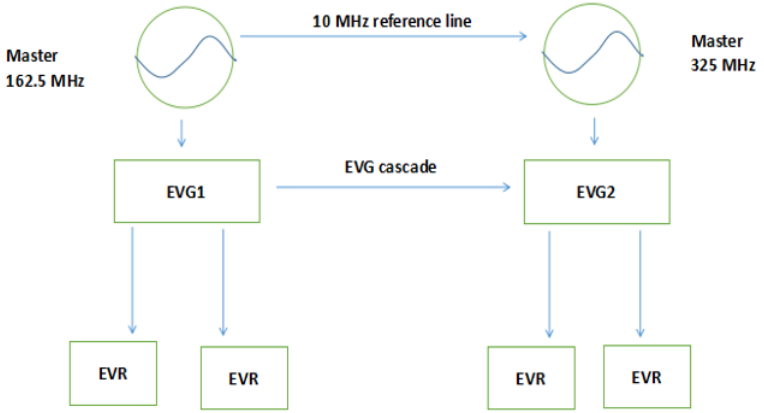
ADS Timing system architecture diagram

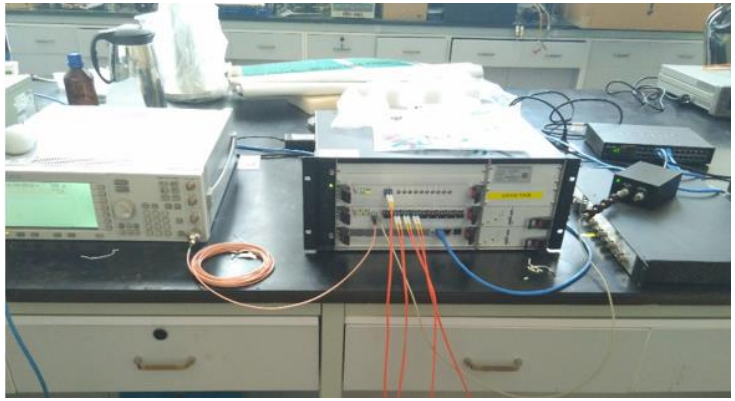


Function structure diagram of 25MeV timing system

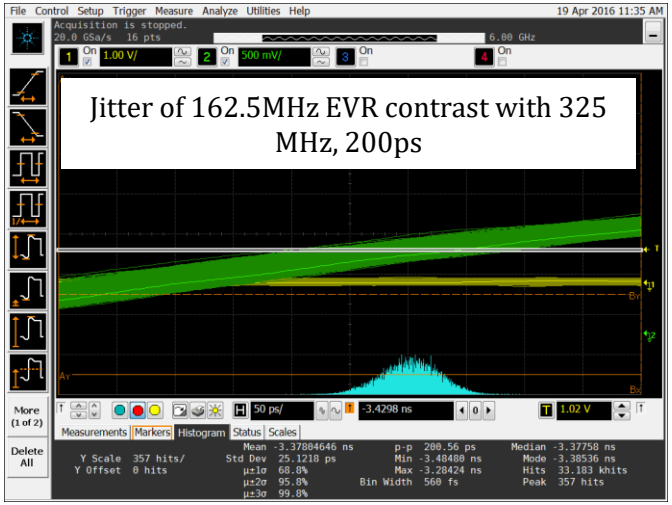
The alignment of injector I - II timing system

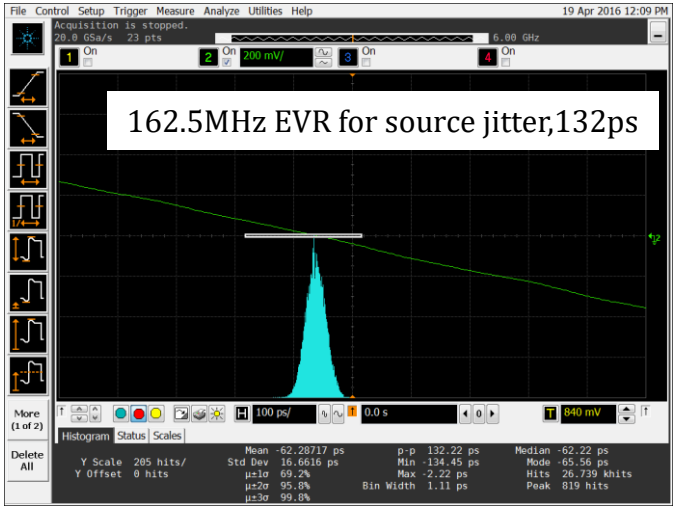
Alignment scheme



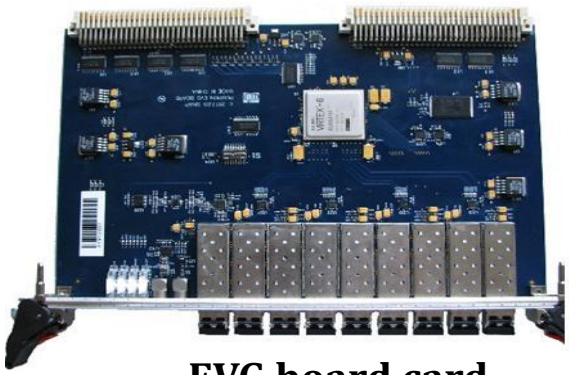


picture of real products



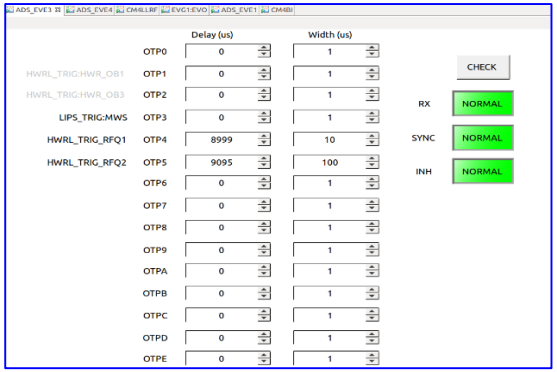


The interface and object of ADS Timing System

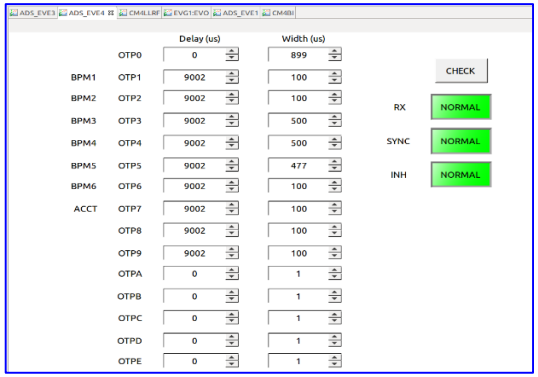


EVG board card

EVR board card



Working interface (part 1)



Working interface (part 2)

Problems

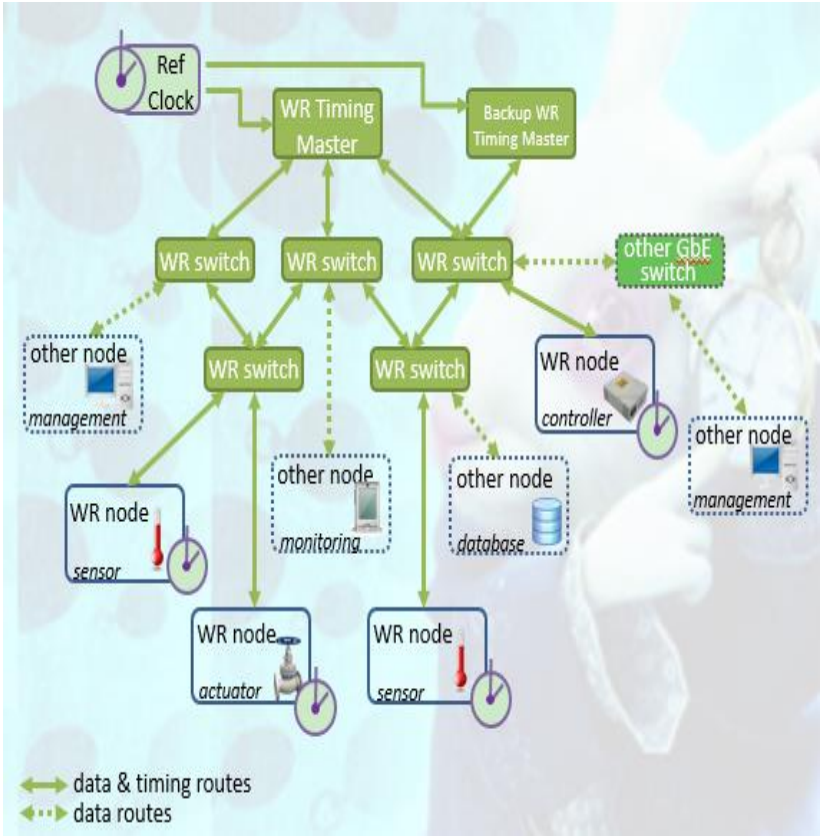
- The historical data associated with MPS requires a high precision us-ns timestamp, but the timing system has not yet implemented this function
- Field applications do not implement the event pattern
- ADS Timing system only has SMA connectors, no 10M low-speed optical fiber interface, temporarily implemented by external conversion board card

- Etc…

Improvement and next plan

- **Objective: WR is used to realize integration of three networks, including timing network for synchronization and triggering, MPS fast protection control network and unified timing network with high precision timestamp.**
- **Method: now we want to replace EVG/EVR with WR for pulse distribution, and combine WR with MPS based on the MicroTCA platform for CiADS timing system . When the fault signal arrives, WR can mark the time of the fault signal accurately and inform the upper interface to facilitate online and offline fault query.**

WR technology introduction



Distribution architecture diagram of WR

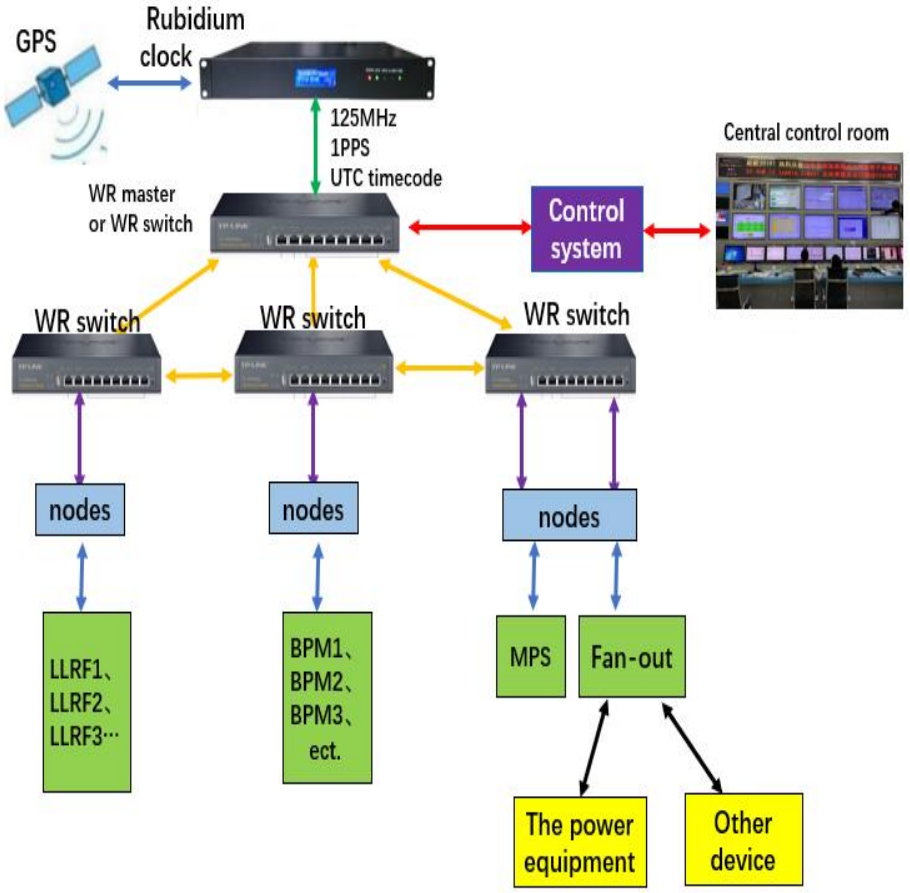
For more information,
please visit: https://ohwr.org

- **WR network uses IEEE 802.3 standard gigabit Ethernet protocol, WR synchronization network consists of three main parts: clock reference source, WR switch and WR nodes.**
- **In WR network, clock synchronization includes two parts: one is clock frequency synchronization ; The second is absolute timestamp synchronization.**

Design of timing system based on WR

Planned technical indicators and parameters:

distance	<10 km
nodes	<2000
jitter	<100ps
synchronization precision	<1ns
Data bandwidth	1Gbps
Ease of deployment	easy
Price (deployment distance and quantity)	low



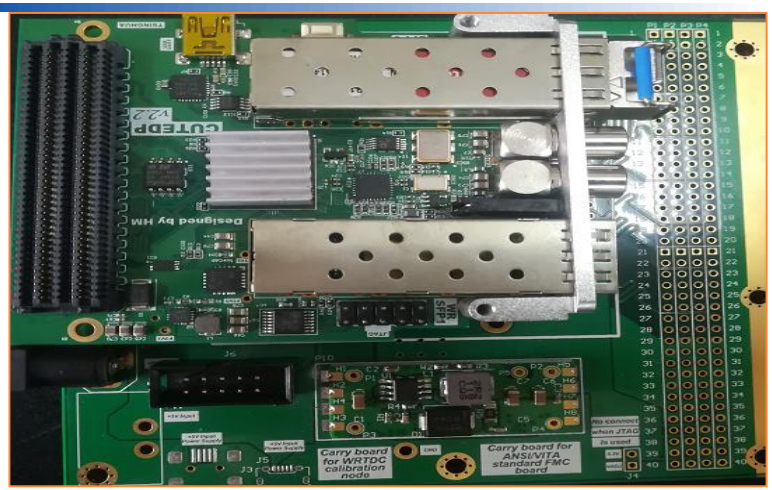
The structure diagram of timing system based on WR

Hardware and software requirements

hardware	WR switch WR nodes based on MicroTCA
FPGA	FPGA Xilinx XC6SLX45T….(sparten-6) Kintex-5 Zynq 7000 Etc.
software	Verilog、C EPICS framework
EPICS	EPICS IOC server provided by default

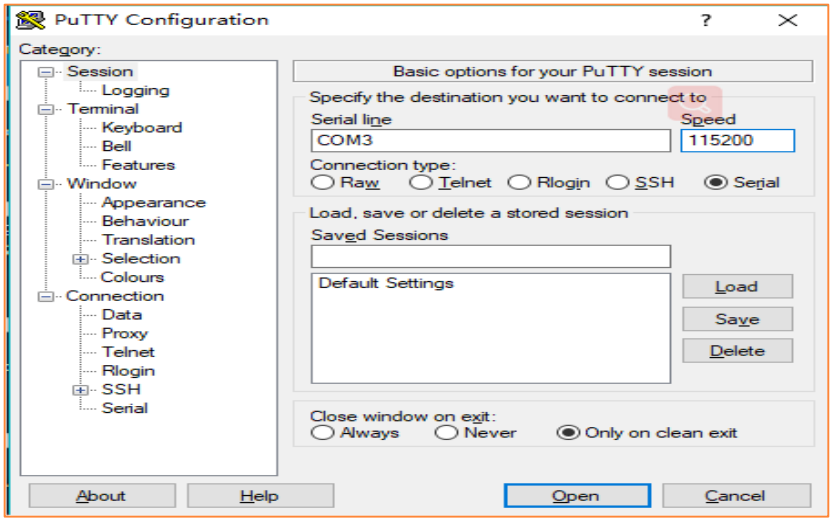
Completed test work

Physical object of WR switch



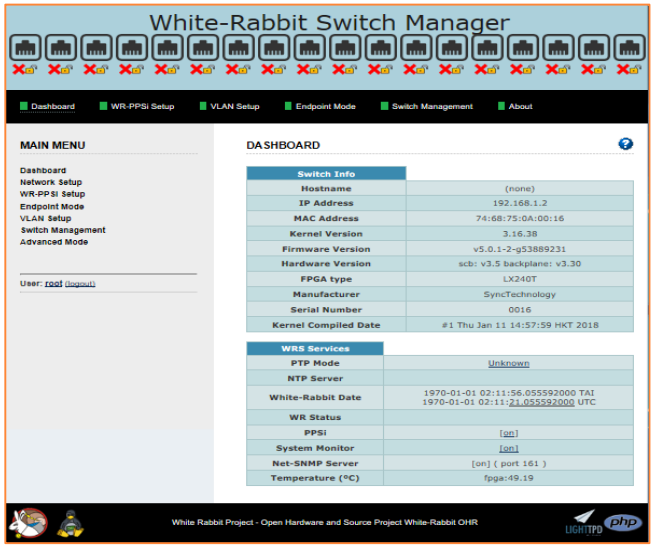
Physical object of WR node

WR test preparation

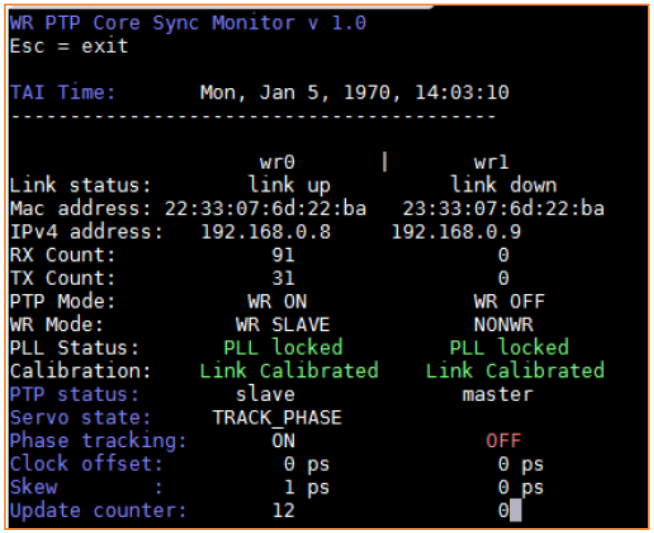


WR login on Windows

Simple tests that have been completed

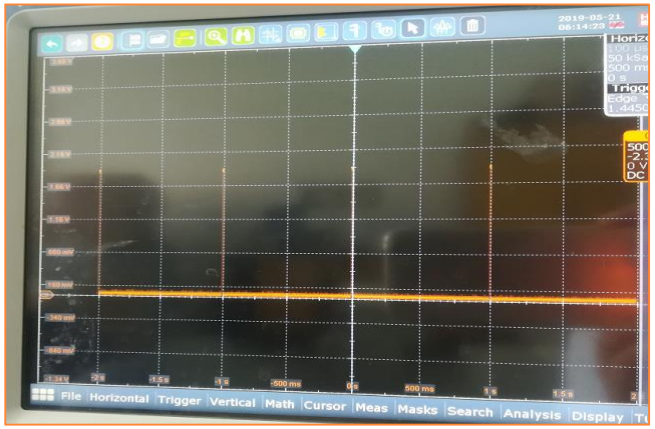


WR switch login interface



WR node synchronize with WRS

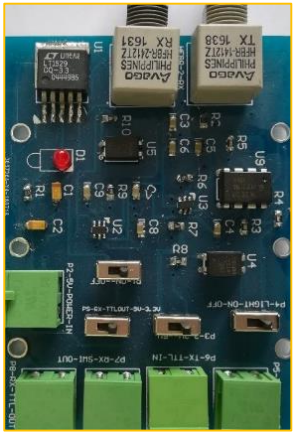
Synchronous clock signal test



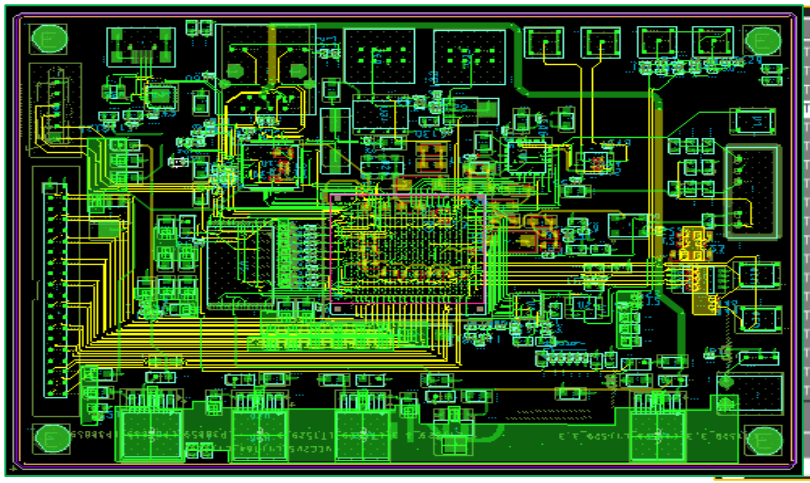
PPS signal test

Other related work

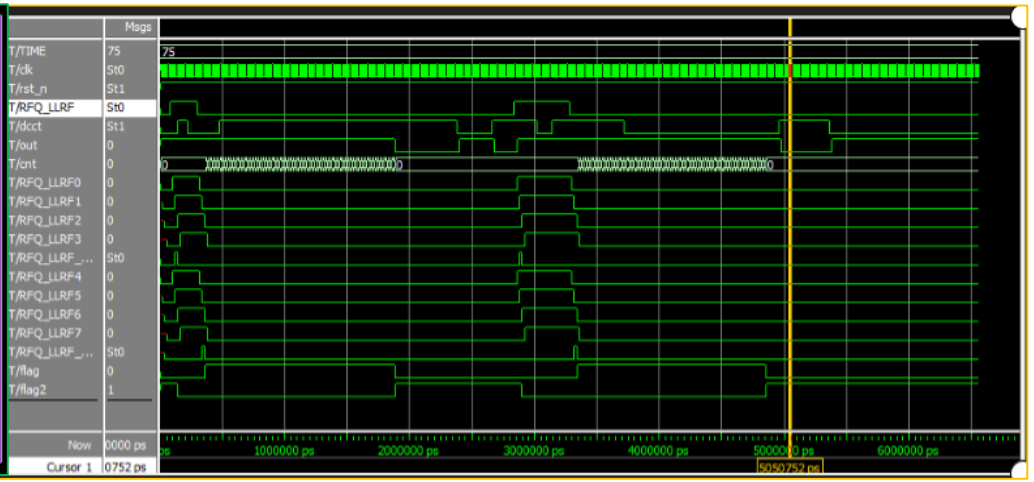
Switch board card for electrical signal and switch signal



Photoelectric signal conversion card



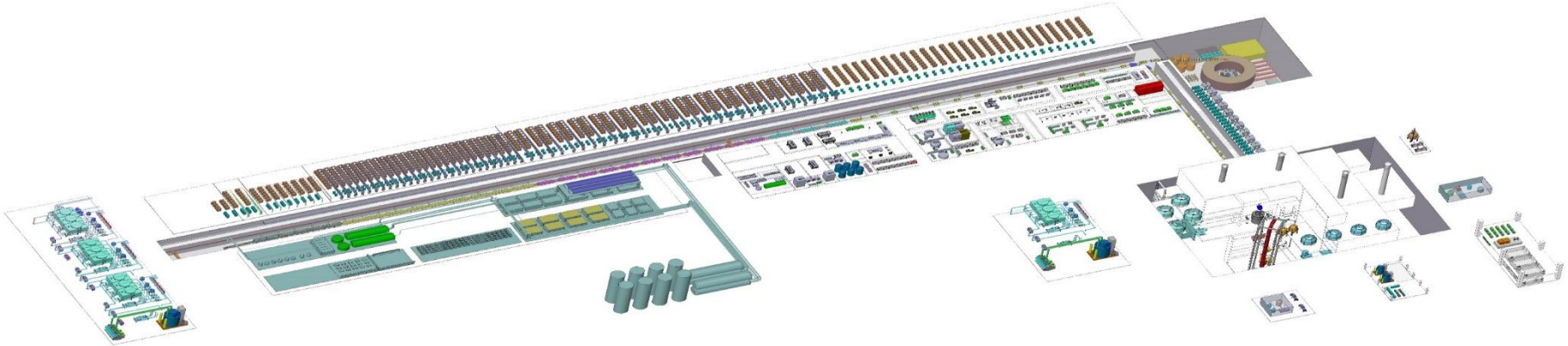
FPGA PCB layout



the related Verilog simulation , according to the field work requirements

Next work plan and outlook

- **The implementation methods of PTP precise time protocol, phase tracking, dual digital mixing phase discrimination and clock data recovery**
- **Based on Micro TCA bus standard, WR node hardware that meets the requirements of CiADS field equipment will be designed and completed**
- **Summarize the technical experience and prepare for the pre-research of CiADS timing system design.**



CiADS large scientific engineering installation diagram

Thank you for listening!