







Yi Cheng Institute of Modern Physics









- Introduction of ADS project
- Objectives of the timing system
- Scheme and operation status
- Improvement based on WR
- WR testing and progress
- The next work plan







- One of the main scientific objectives of ADS is the disposal of nuclear waste.
- ADS consists of three parts: proton linear accelerator, liquid metal spall target, lead bismuth cooled the reactor
- **Operation mode: CW mode and pulse mode**

Prototype of the front part of the 25MeV proton linear accelerator

- Completed in 2016, with 25MeV pulse beam test
- Verify the technical scheme of CiADS low energy section
- do technical research for CiADS accelerator

ECR + LEBT + RFQ + MEBT + CM1 + CM2 + CM3 + CM4 + HEBT





In the pulse operation mode, synchronization and trigger signals are provided for related devices



EVG/EVR 1 chassis (input signal 162.5MHz) provided by IMP



EVG/EVR 2 chassis (input signal 325MHz) provided by IHEP

These devices include: microwave machines for ion sources ,

LEBT chopper、 LLRF、 BPM、 Beam detection equipment



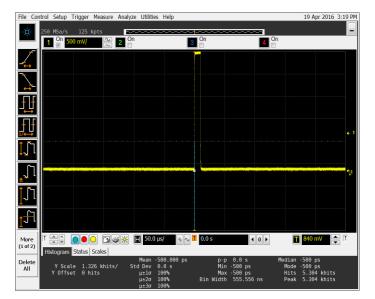




Realize chain protection function



Normal operation (high pulse width)



When fault signal coming and the pulse width automatically changes to low pulse width

Combined with the MPS system, the low duty ratio pulse beam in the accelerators can avoid the damage caused by beam bombardment to the key equipment distributed on the beam line due to the low energy







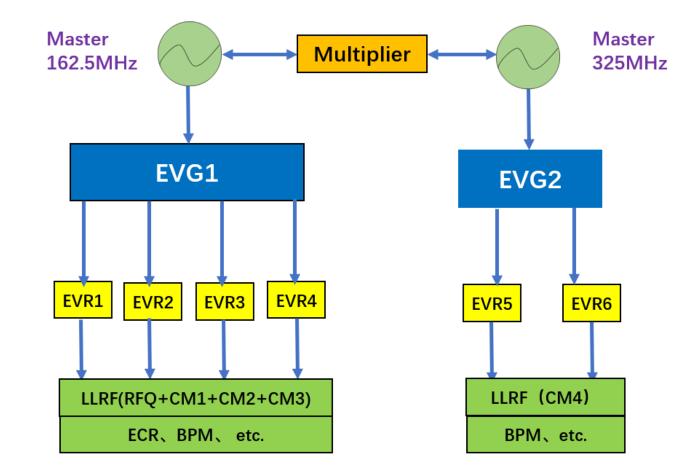
Demand target:

project	parameter
Trigger period	1μs~10s
Delay range	0~10ms
Delay accuracy (step)	≤0.25ns
The pulse width	0~10ms
Pulse width precision	≤6ns
Level standard	3. 3V LVTTL, 5V TTL
Total number of triggers	≥33
jitter	≤50ps (RMS)
Rising edge of delay signal	≤3ns



ADS Timing system architecture diagram



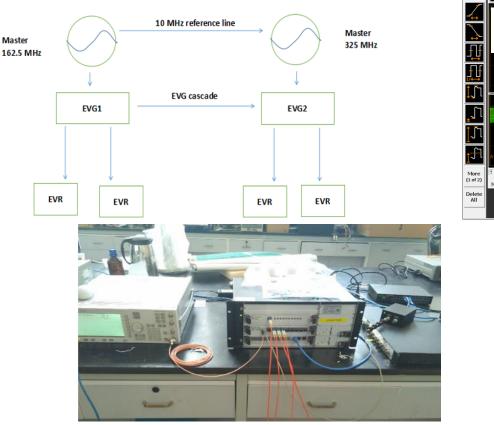


Function structure diagram of 25MeV timing system



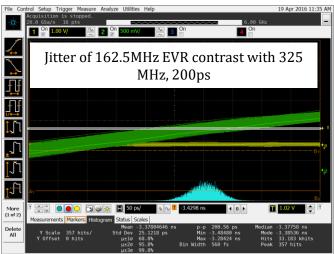
The alignment of injector I - II timing system

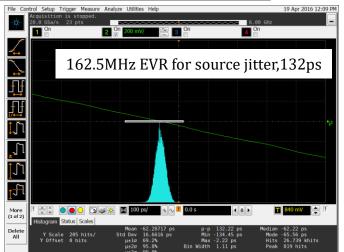




Alignment scheme

picture of real products



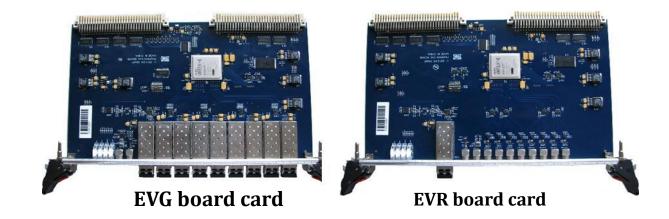




IMP







ADS_EVEN TO ADS_EVEN	AALLRF 🔛 E	VG1:EVO 🚰 ADS_E	VE1 🔛 CM	MBI		
		Delay (us)		Width (us)		
	OTP0	0	-	1 🌻		
HWRL_TRIG:HWR_OB1	OTP1	0	-	1 🌩		CHECK
HWRL_TRIG:HWR_OB3	OTP2	0	÷	1 🌻	RX	NORMAL
LIPS_TRIG:MWS	ОТРЗ	0	* *	1 🌻		TOURSE
HWRL_TRIG_RFQ1	OTP4	8999	÷	10 🌻	SYNC	NORMAL
HWRL_TRIG_RFQ2	OTP5	9095	*	100 🌻	INH	NORMAL
	OTP6	0	*	1 🌻		NORMAL
	OTP7	0	÷	1 🌻		
	OTP8	0	-	1 🌲		
	OTP9	0	\$	1 🗘		
	OTPA	0	÷	1 🗘		
	OTPB	0	\$	1 🌲		
	OTPC	0	÷	1 🌲		
	OTPD	0	÷	1 🗘		
	OTPE	0	*	1 ≑		

Working interface (part 1)

프 ADS_EVE1 프 ADS_EVE4 월 프 CHALLEF 프 EVG1EVO 프 ADS_EVE1 프 CHABI							
		Delay (u:	5)	Width	(us)		
	OTP0	0	+	899	*		
BPM1	OTP1	9002	-	100	+		CHECK
BPM2	OTP2	9002	*	100	*	RX	NORMAL
BPM3	OTP3	9002	*	500	*	100	HOIMAL
BPM4	OTP4	9002	÷	500	÷	SYNC	NORMAL
BPM5	OTP5	9002	+	477	÷	INH	NORMAL
BPM6	OTP6	9002		100	-	INT	NORMAL
ACCT	OTP7	9002	*	100	÷		
	OTP8	9002	*	100	\$		
	OTP9	9002	*	100	-		
	OTPA	0	*	1	*		
	OTPB	0	+	1	-		
	OTPC	0	*	1	÷		
	OTPD	0	*	1	-		
	OTPE	0	*	1	*		

Working interface (part 2)







- The historical data associated with MPS requires a high precision us-ns timestamp, but the timing system has not yet implemented this function
- Field applications do not implement the event pattern
- ADS Timing system only has SMA connectors, no 10M lowspeed optical fiber interface, temporarily implemented by external conversion board card
- •Etc...





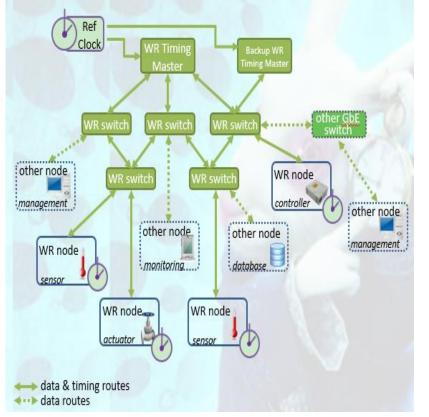


- •Objective: WR is used to realize integration of three networks, including timing network for synchronization and triggering, MPS fast protection control network and unified timing network with high precision timestamp.
- Method: now we want to replace EVG/EVR with WR for pulse distribution, and combine WR with MPS based on the MicroTCA platform for CiADS timing system. When the fault signal arrives, WR can mark the time of the fault signal accurately and inform the upper interface to facilitate online and offline fault query.









Distribution architecture diagram of WR

For more information, please visit: https://ohwr.org

- WR network uses IEEE 802.3 standard gigabit Ethernet protocol, WR synchronization network consists of three main parts: clock reference source, WR switch and WR nodes.
- In WR network, clock synchronization includes two parts: one is clock frequency synchronization ; The second is absolute timestamp synchronization.

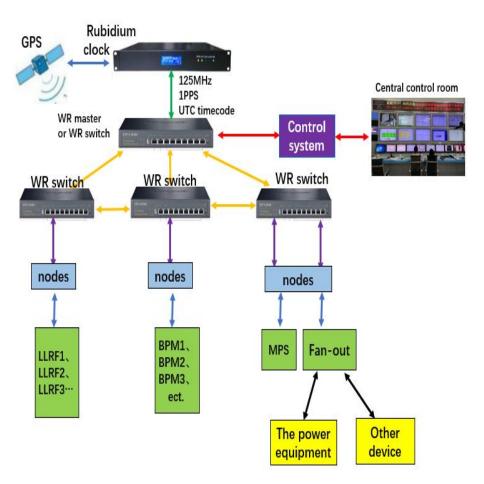






Planned technical indicators and parameters:

distance	<10 km
nodes	<2000
jitter	<100ps
synchronization precision	<1ns
Data bandwidth	1Gbps
Ease of deployment	easy
Price (deployment distance and quantity)	low



The structure diagram of timing system based on WR







hardware	WR switch WR nodes based on MicroTCA
FPGA	FPGA Xilinx XC6SLX45T(sparten-6) Kintex-5 Zynq 7000 Etc.
software	Verilog、C EPICS framework
EPICS	EPICS IOC server provided by default







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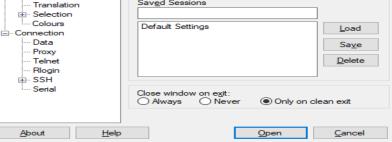


Physical object of WR switch





Physical object of WR node Reputition Putty Configuration ? Category: Session Basic options for your PuTTY session Logging Specify the destination you want to connect to 🛓 - Terminal Speed Serial line Keyboard COM3 115200 Bell Features Connection type: ○ Raw ○ Telnet ○ Rlogin ○ SSH ● Serial . ⊡ · Window Appearance Load, save or delete a stored session Behaviour Saved Sessions Translation



WR test preparation

WR login on Windows

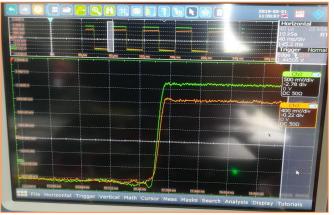






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Dashboard WR-PPSi Setup	VLAN Setup Endpoint Mode Sy	witch Management About	
		About	
MAIN MENU	DASHBOARD	0	
Dashboard	Switch Info		
Network Setup WR-PPSI Setup	Hostname	(none)	
Endpoint Mode	IP Address	192.168.1.2	
VLAN Setup	MAC Address	74:68:75:0A:00:16	
Switch Management	Kernel Version	3.16.38	
Advanced Mode	Firmware Version	v5.0.1-2-g53889231	
	Hardware Version	scb: v3.5 backplane: v3.30	
User: root (logout)	FPGA type	LX240T	
	Manufacturer	SyncTechnology	
	Serial Number	0016	
	Kernel Compiled Date	#1 Thu Jan 11 14:57:59 HKT 2018	
	WRS Services		
	PTP Mode	Unknown	
	NTP Server		
	White-Rabbit Date	1970-01-01 02:11:56.055592000 TAI 1970-01-01 02:11: <u>21.055592000</u> UTC	
	WR Status		
	PPSi	[<u>on</u>]	
	System Monitor	[on]	
	Net-SNMP Server	[on] (port 161)	
	Temperature (°C)	fpga:49,19	

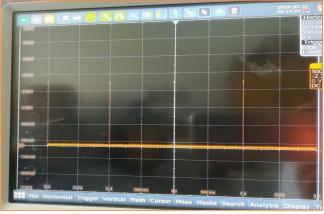
WR switch login interface



Synchronous clock signal test

WR PTP Core Sync Monitor v 1.0 Esc = exit				
ESC = eXIL				
TAI Time:	Mon, Jan 5, 1970	9, 14:03:10		
	wrΘ	wrl		
Link status:	link up	link down		
Mac address: 22	:33:07:6d:22:ba	23:33:07:6d:22:ba		
IPv4 address:	192.168.0.8	192.168.0.9		
RX Count:	91	Θ		
TX Count:	31	Θ		
PTP Mode:	WR ON	WR OFF		
WR Mode:	WR SLAVE	NONWR		
PLL Status:	PLL locked	PLL locked		
Calibration:	Link Calibrated	Link Calibrated		
PTP status:	slave	master		
Servo state:				
Phase tracking:	ON	OFF		
Clock offset:	Θps	θps		
Skew :	l ps	θps		
Update counter:	12	Θ		

WR node synchronize with WRS



PPS signal test

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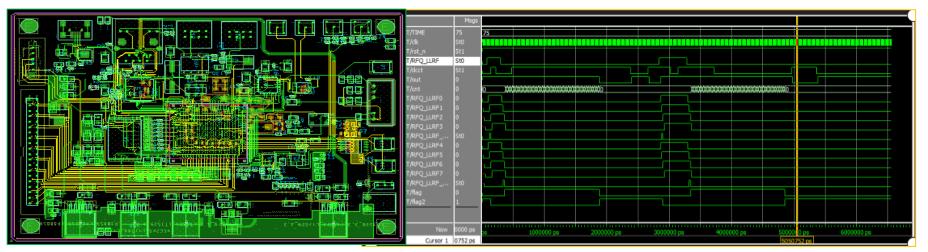




Switch board card for electrical signal and switch signal



Photoelectric signal conversion card



FPGA PCB layout

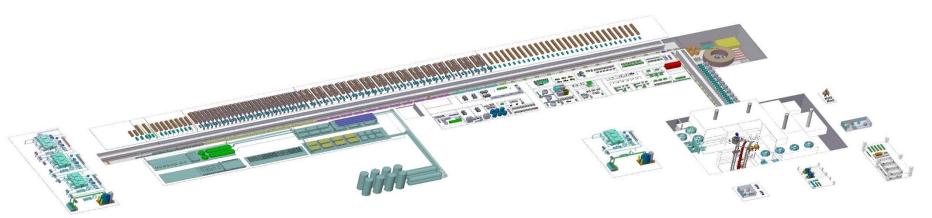
the related Verilog simulation , according to the field work requirements







- The implementation methods of PTP precise time protocol, phase tracking, dual digital mixing phase discrimination and clock data recovery
- Based on Micro TCA bus standard, WR node hardware that meets the requirements of CiADS field equipment will be designed and completed
- Summarize the technical experience and prepare for the pre-research of CiADS timing system design.



CiADS large scientific engineering installation diagram



Thank you for listening!





