MicroTCA Communication Links, Clocks, Triggers & Interlocks

Kay Rehlich, DESY MicroTCA Technology Lab

HELMHOLTZ GEMEINSCHAFT

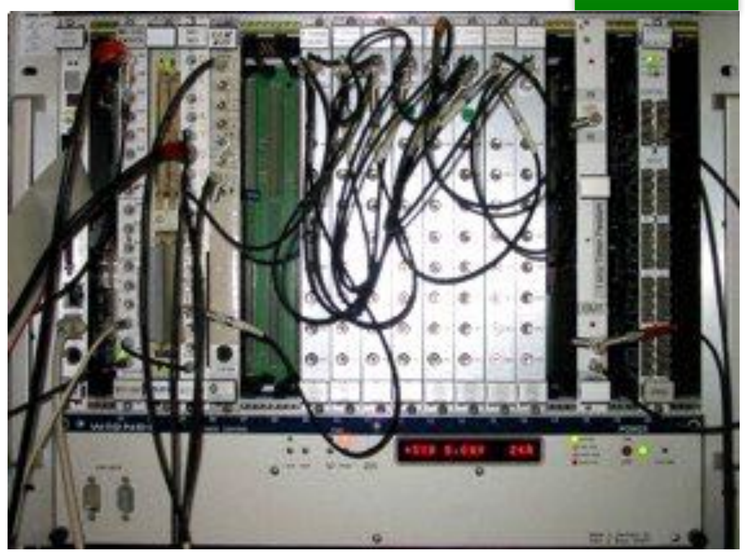
MICROTCA TECHNOLOGY LAB
A HELMHOLTZ INNOVATION LAB

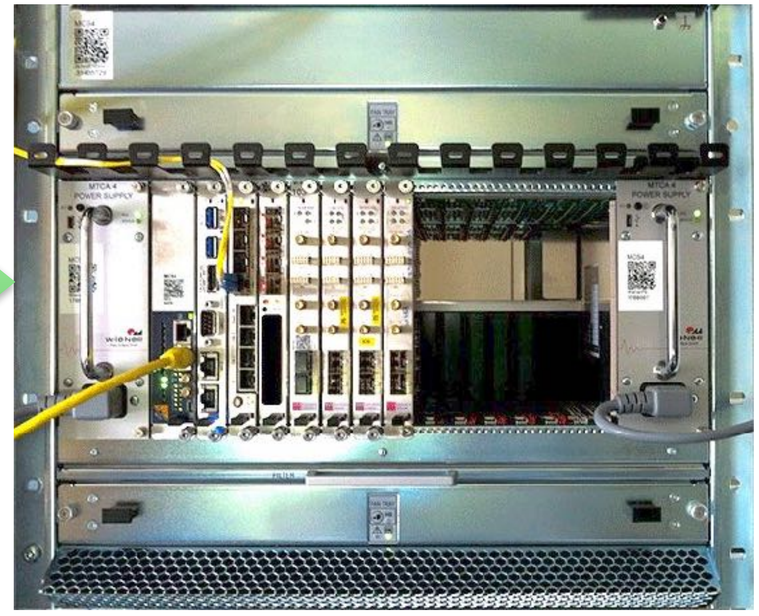
DESY

Motivation

VME is 38 years old!!!

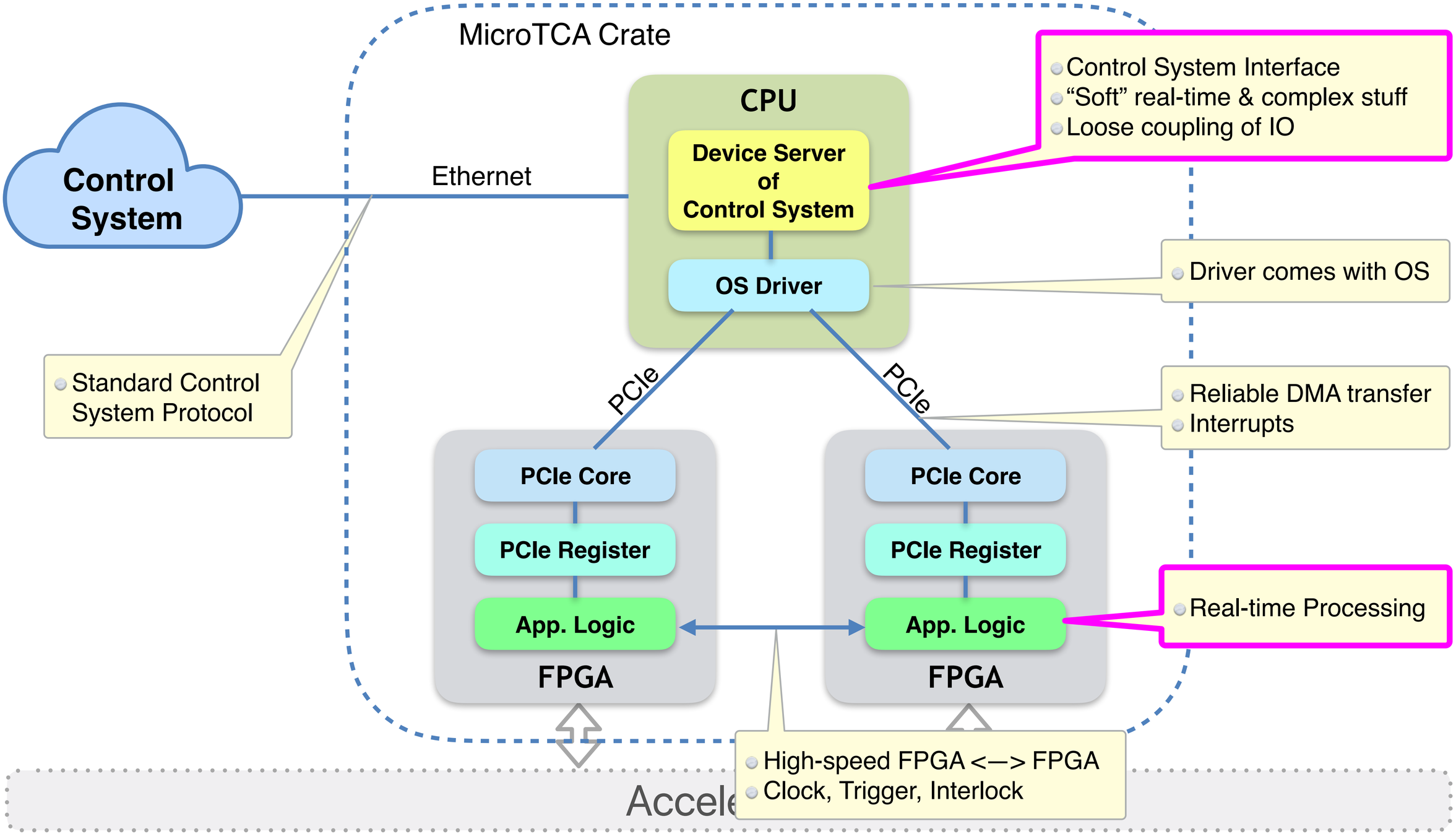
FLASH
first FEL



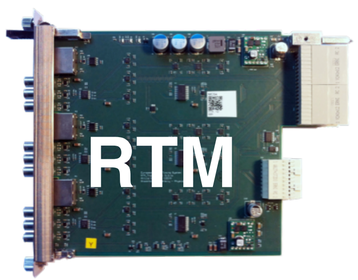


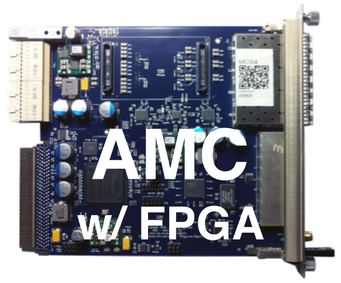
- Redundant fans & power supplies
- Internal clock & trigger distribution
- Modular: reusable components
- Complete remote management
- Modern high-speed data transfer
- Highest signal quality
- I/O cables from rear side

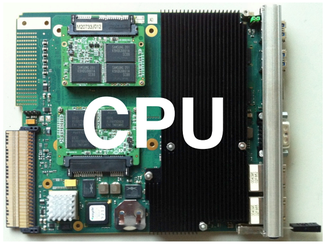
Motivation: Software Architecture



Motivation







Why did we select MicroTCA for XFEL

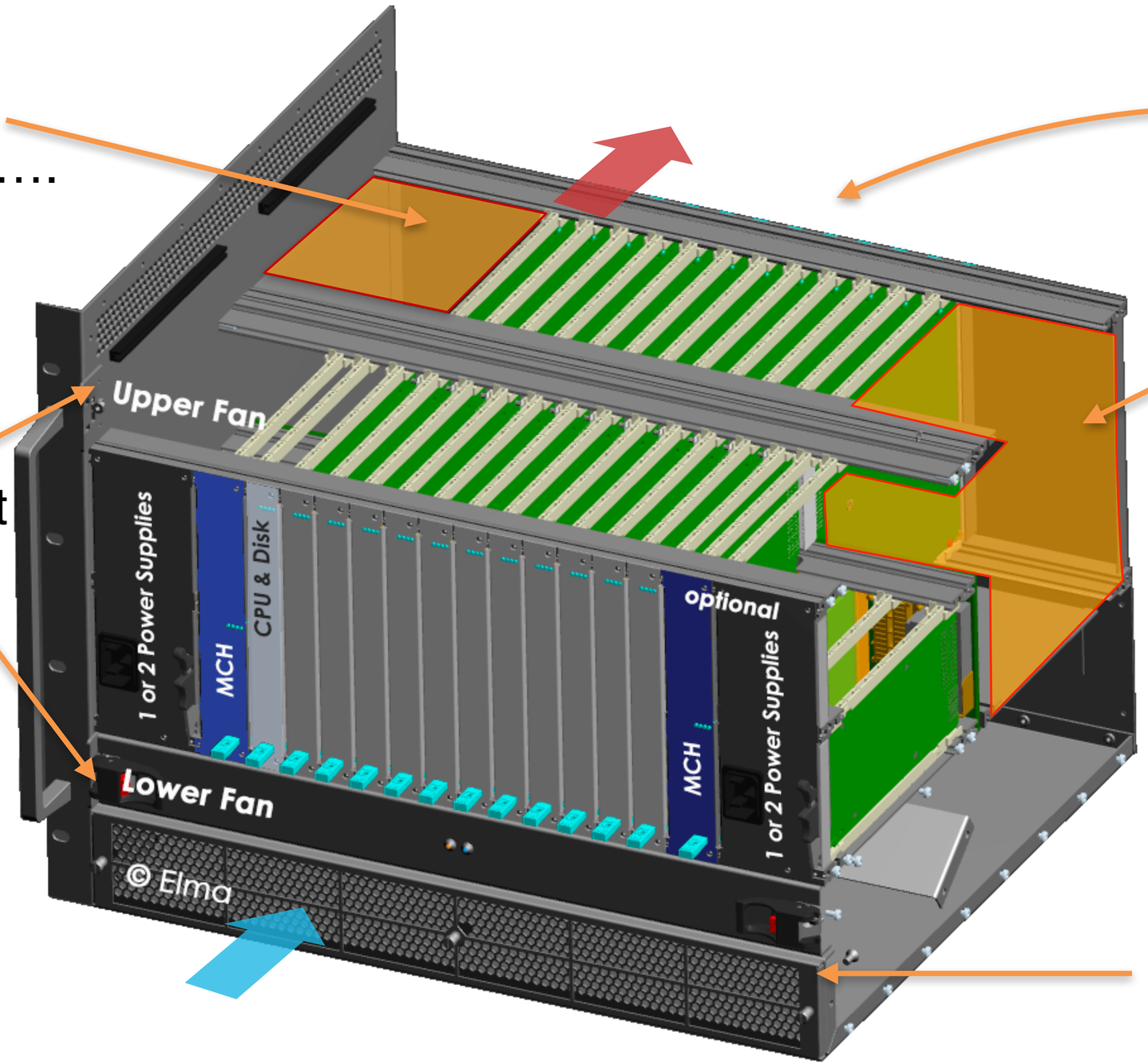
- Modularity !!!
- Standard hardware & software interfaces
- Documentation
- Loose coupling of components
- Implement functions on the right component (architecture)
  - Do complex stuff on a standard CPU: faster development
  - Allow software to crash without disturbing accelerator operation
- Simplified maintenance and good diagnostics of all components
- Remote management is a MUST for large facilities
- Redundancy of key components
- Integrated and standardised clock, trigger, interlock distribution
- Modern communication links (high-speed and low noise)

MicroTCA.4: A Modular Crate System

Space for
a CPU & ….

Most cables from rear

Space for ….



Redundant
Fans

MTCA.4.1

1 … 4 Power Supplies

Filter

MicroTCA Crate Backplane Communication

Common modules

Application modules

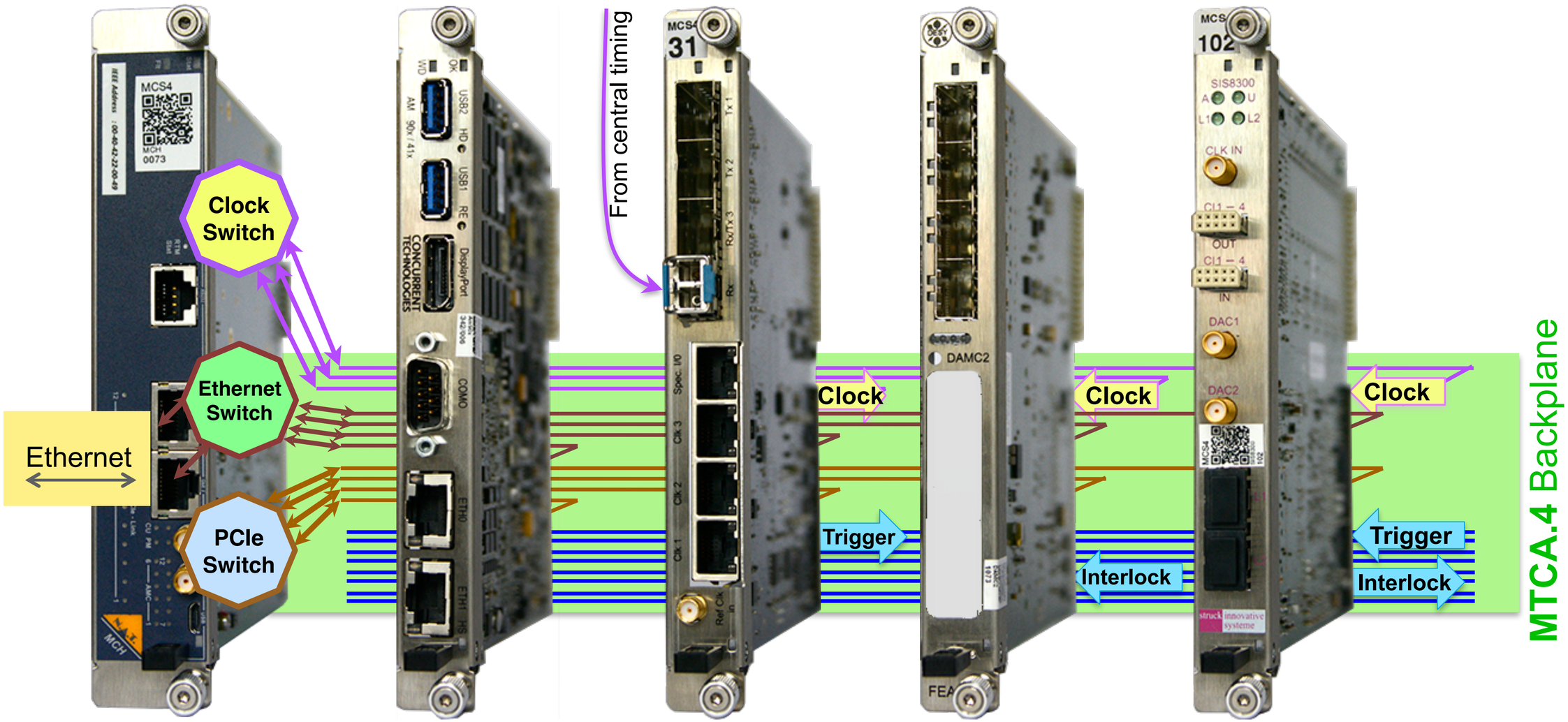
MCH

CPU

Timing

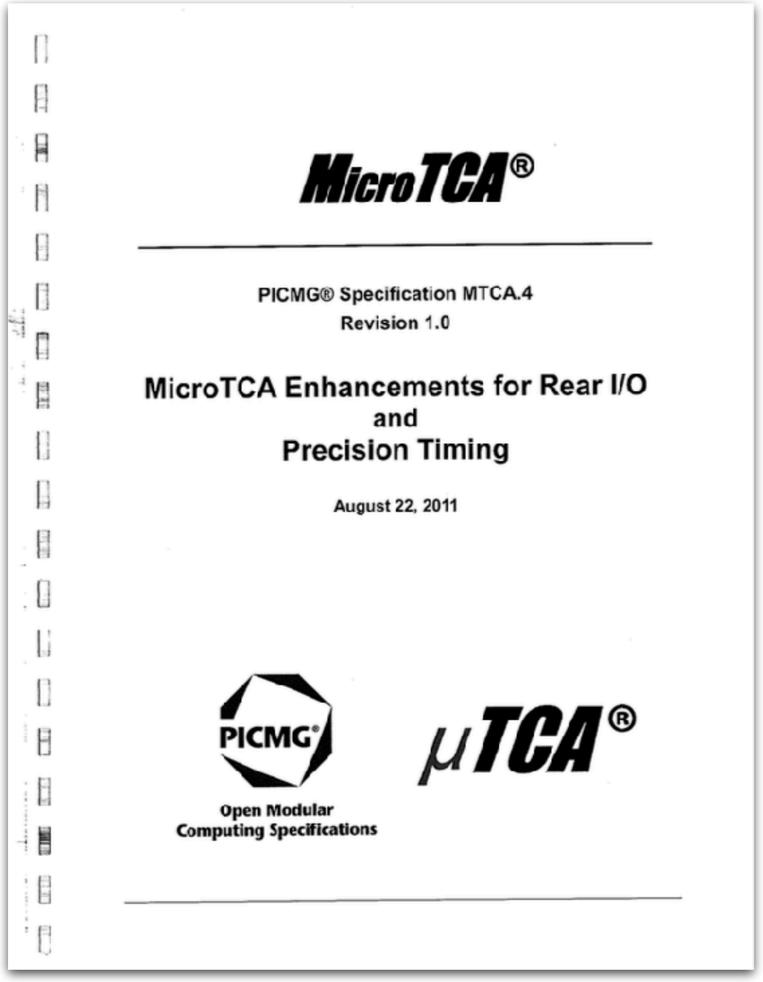
Machine Protection System

ADC
Digi. IO
Controller
….

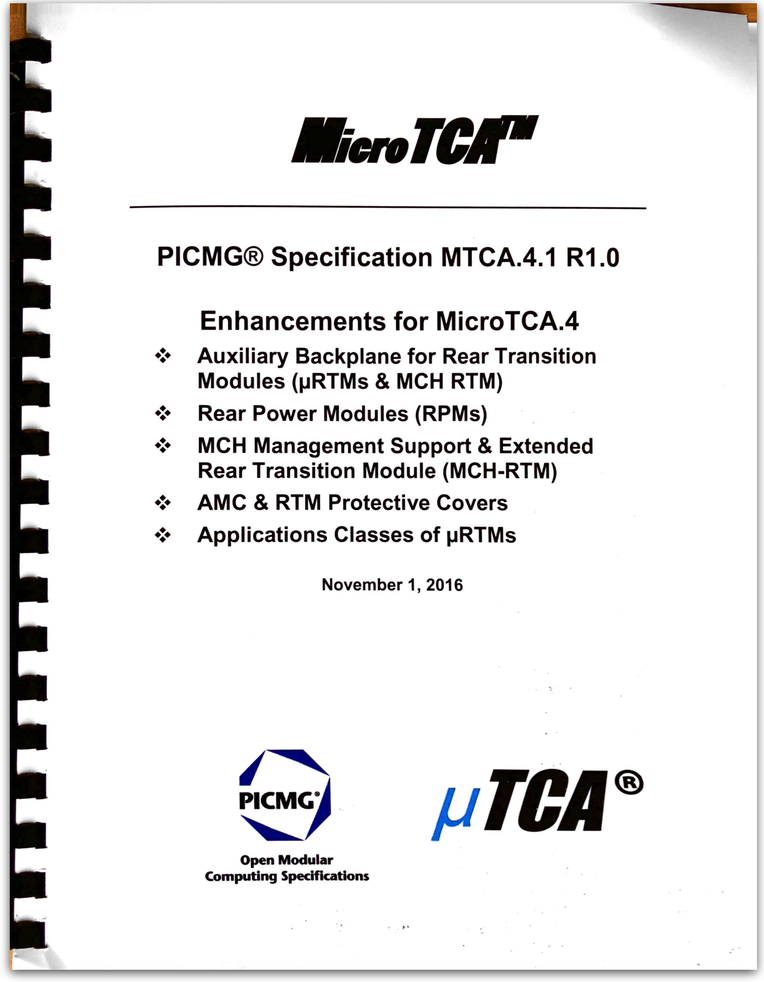


MTCA Specifications

MicroTCA.0



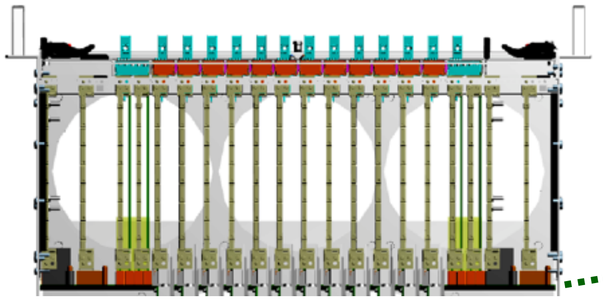
MicroTCA.4

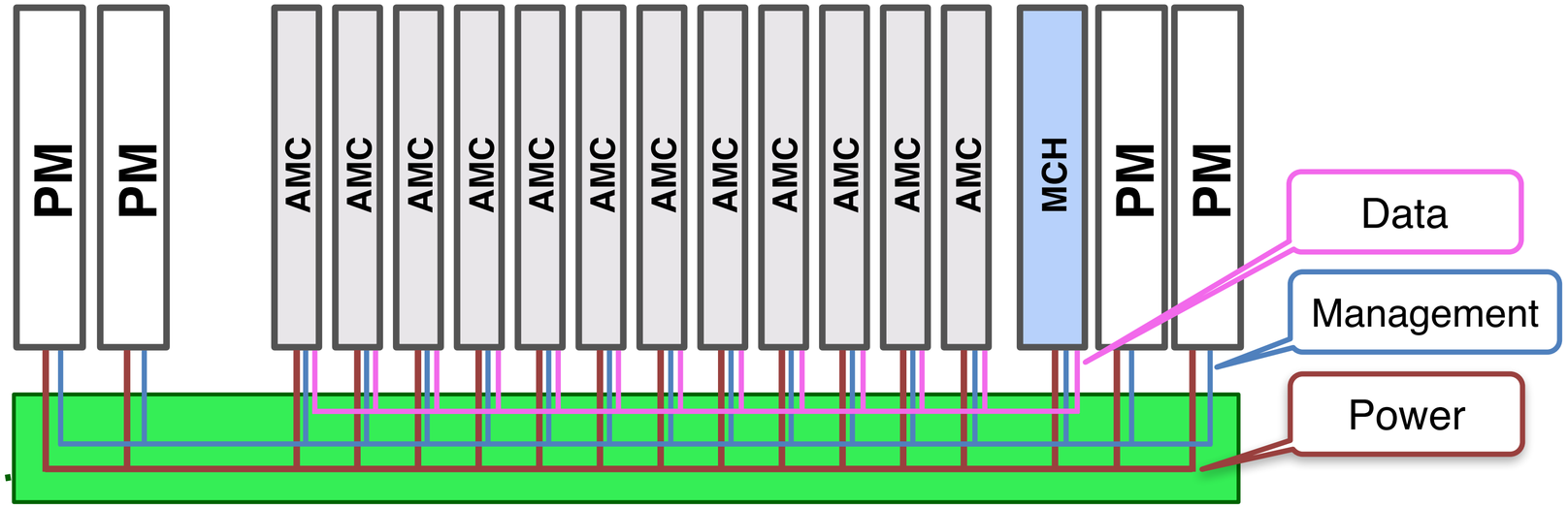


MicroTCA.4.1

MicroTCA Generations: **MTCA.0** MTCA.4 MTCA.4.1

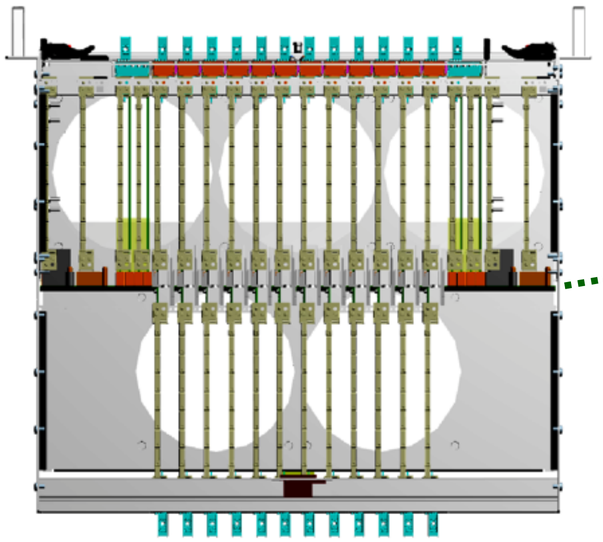
Front Side



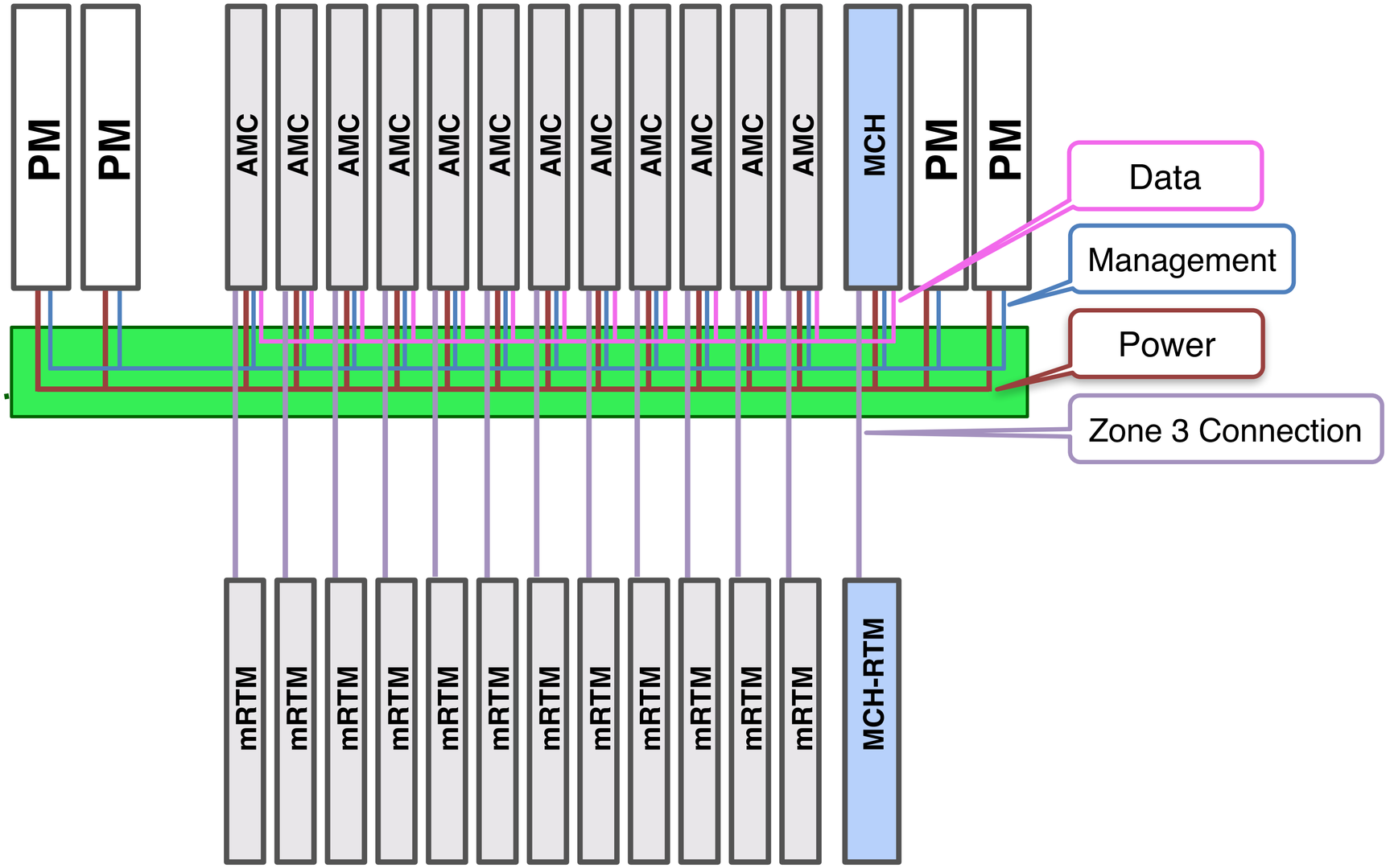


MicroTCA Generations: MTCA.0 **MTCA.4** MTCA.4.1

Front Side

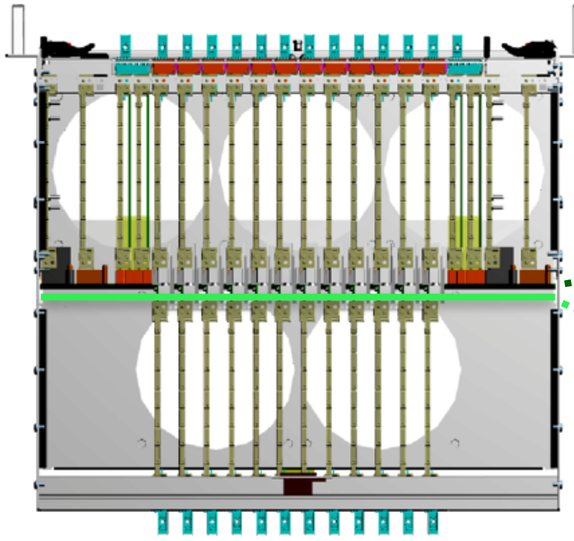


Rear Side

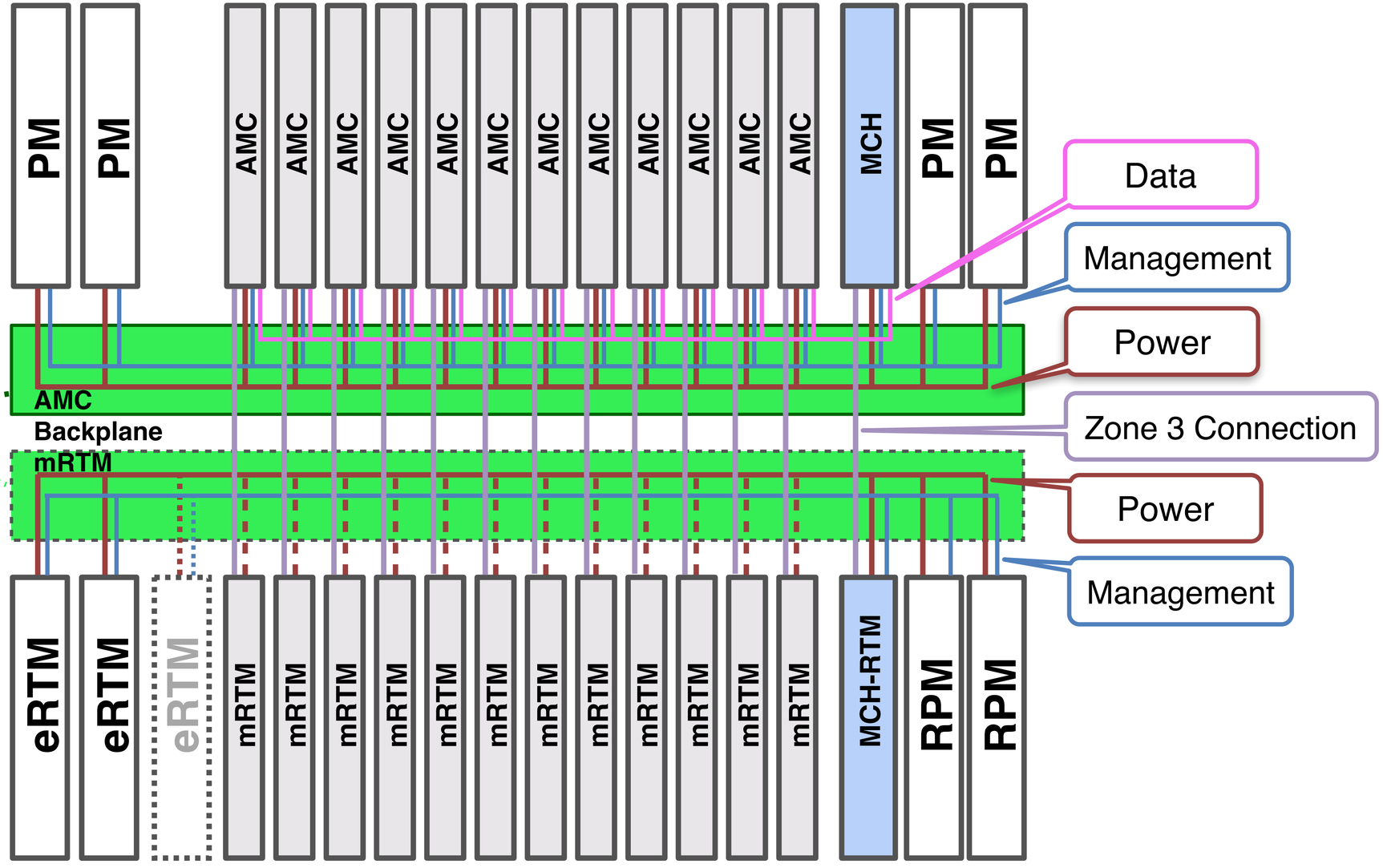


MicroTCA Generations: MTCA.0 MTCA.4 **MTCA.4.1**

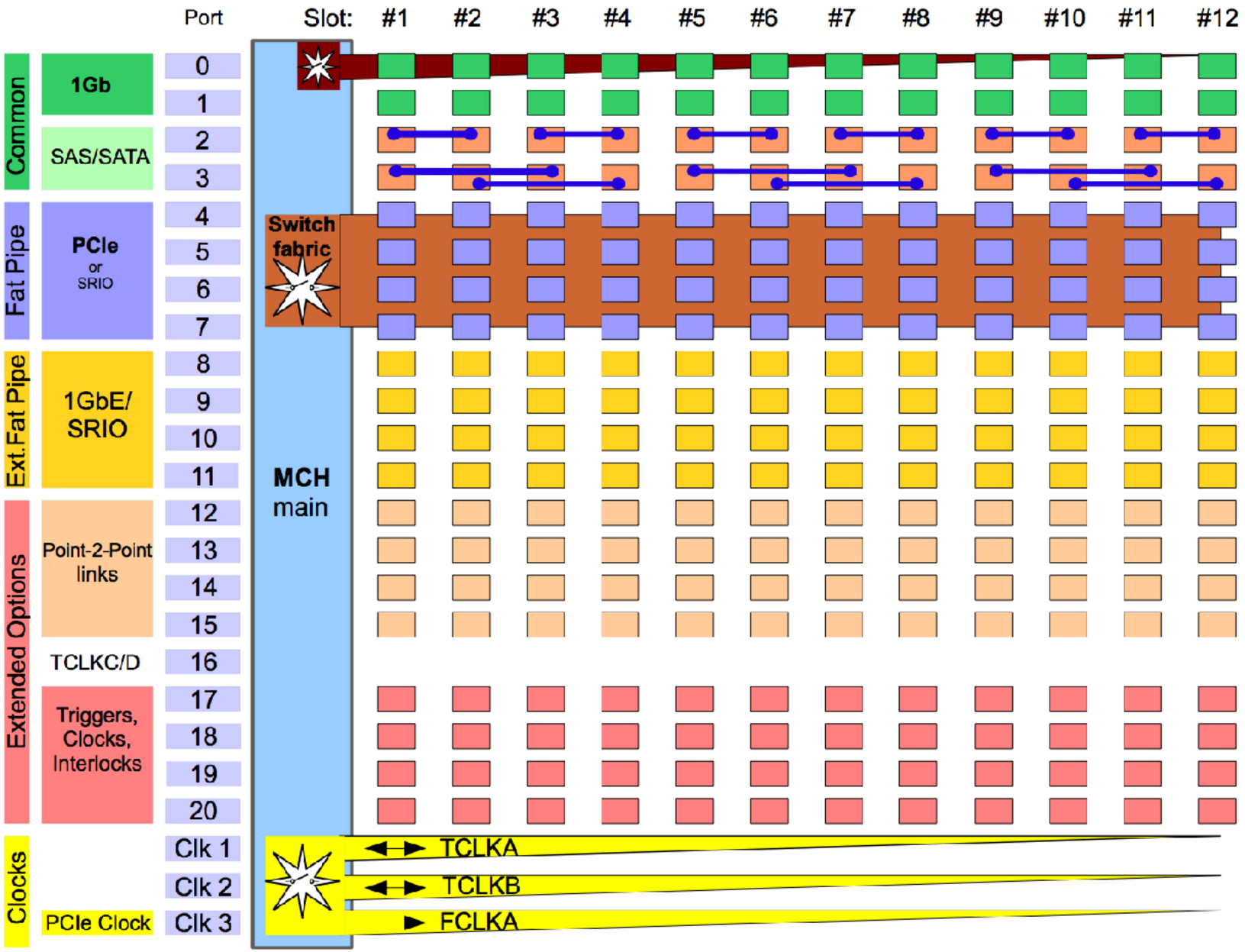
Front Side



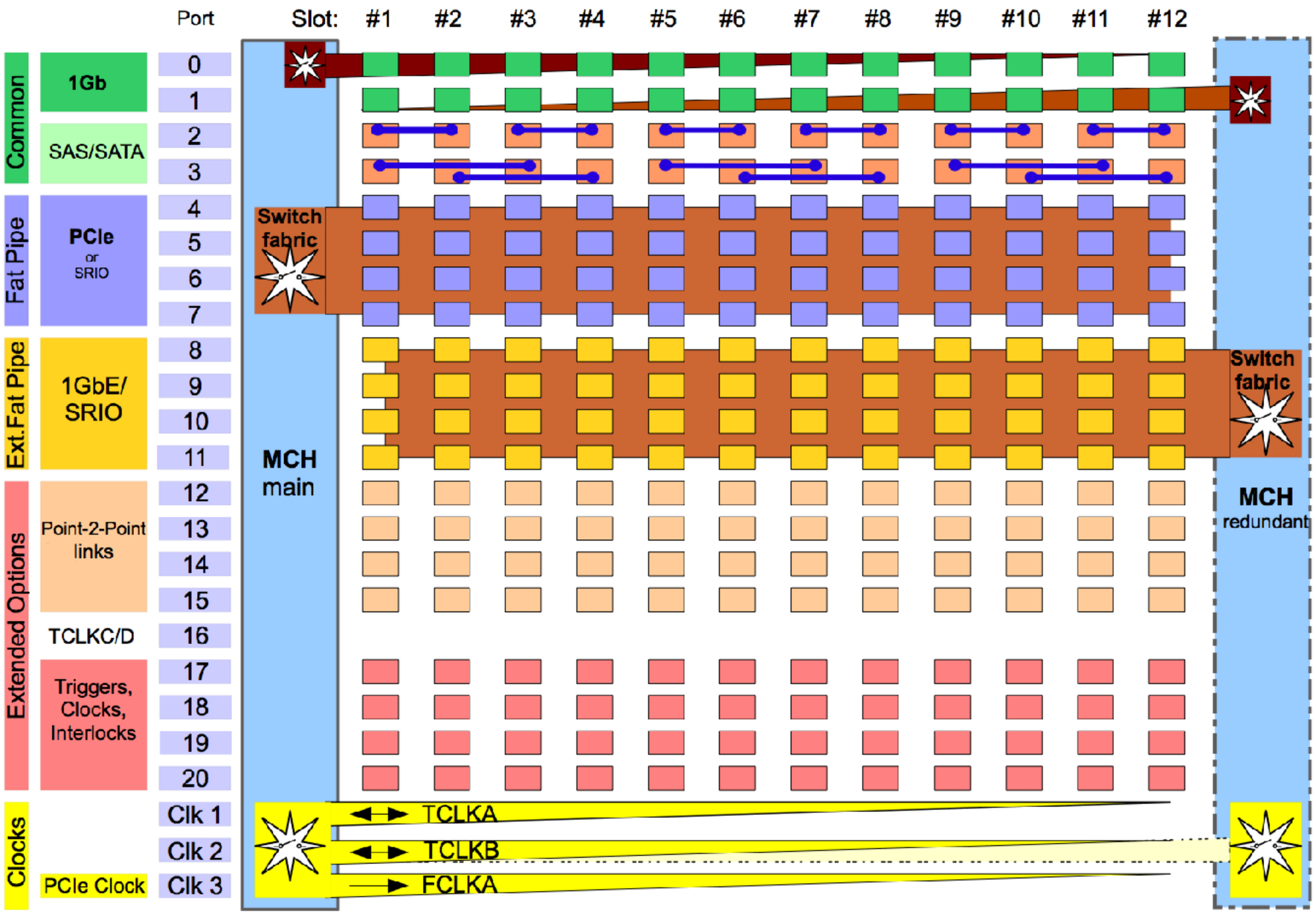
Rear Side



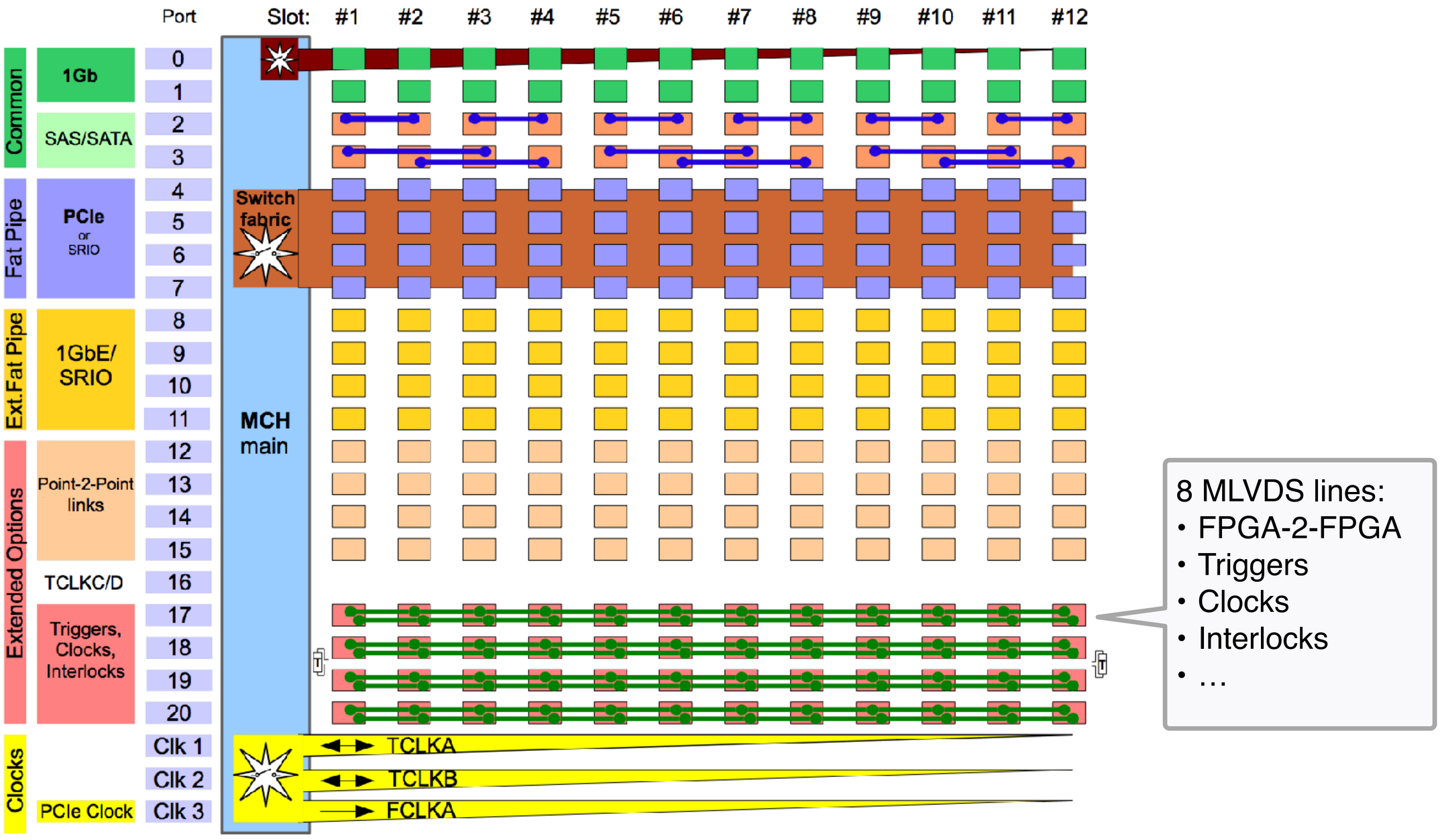
Basic MTCA.0


Port
Slot: #1 #2 #3 #4 #5 #6 #7 #8 #9 #10 #11 #12
Common
1Gb
SAS/SATA
Fat Pipe
PCIe or SRIO
Ext.Fat Pipe
1GbE/ SRIO
Extended Options
Point-2-Point links
TCLKC/D
Triggers, Clocks, Interlocks
Clocks
PCIe Clock
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
Clk 1
Clk 2
Clk 3
Switch fabric
MCH main
TCLKA
TCLKB
FCLKA

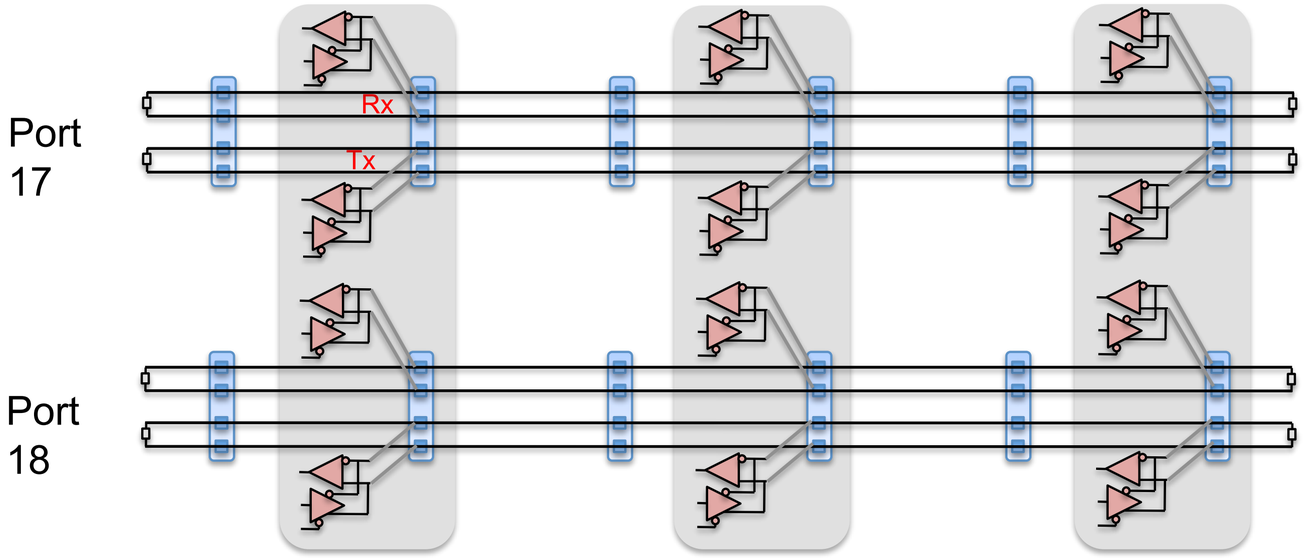
MTCA.0 with Redundancy



MTCA.4: MLVDS Bus



Port 17 … 20 Used as Wired-OR for Interlocks



M-LVDS Type-2 receivers (SN65MLVD082) implement a failsafe by using an offset threshold. In addition, the driver rise and fall times are between 1 and 2.0 ns to provide operation at 250 Mbps while also accommodating stubs on the bus.
Outputs are slew rate controlled to reduce EMI and crosstalk effects associated with large current surges.

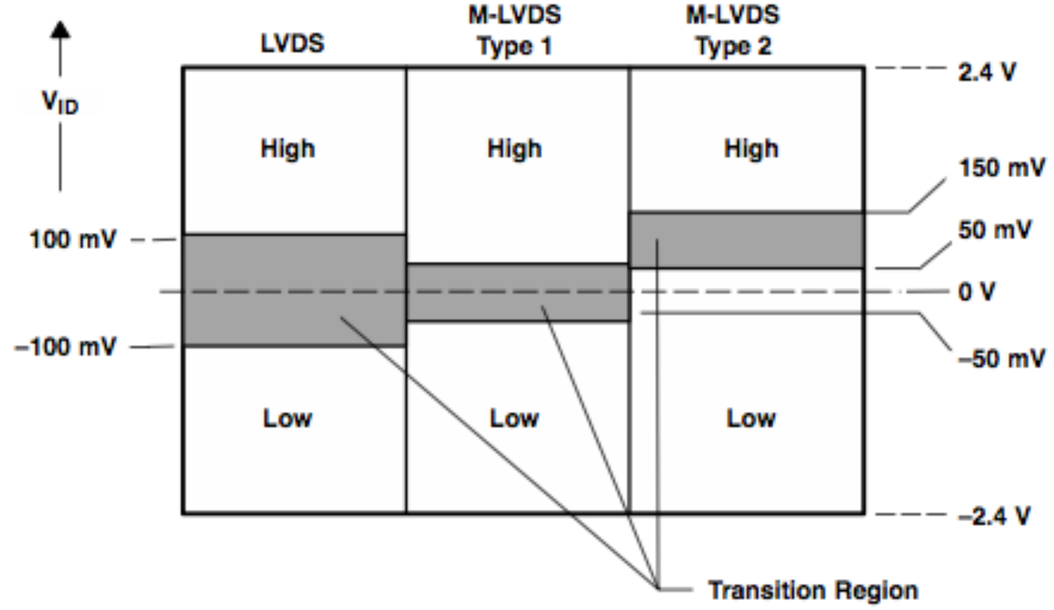
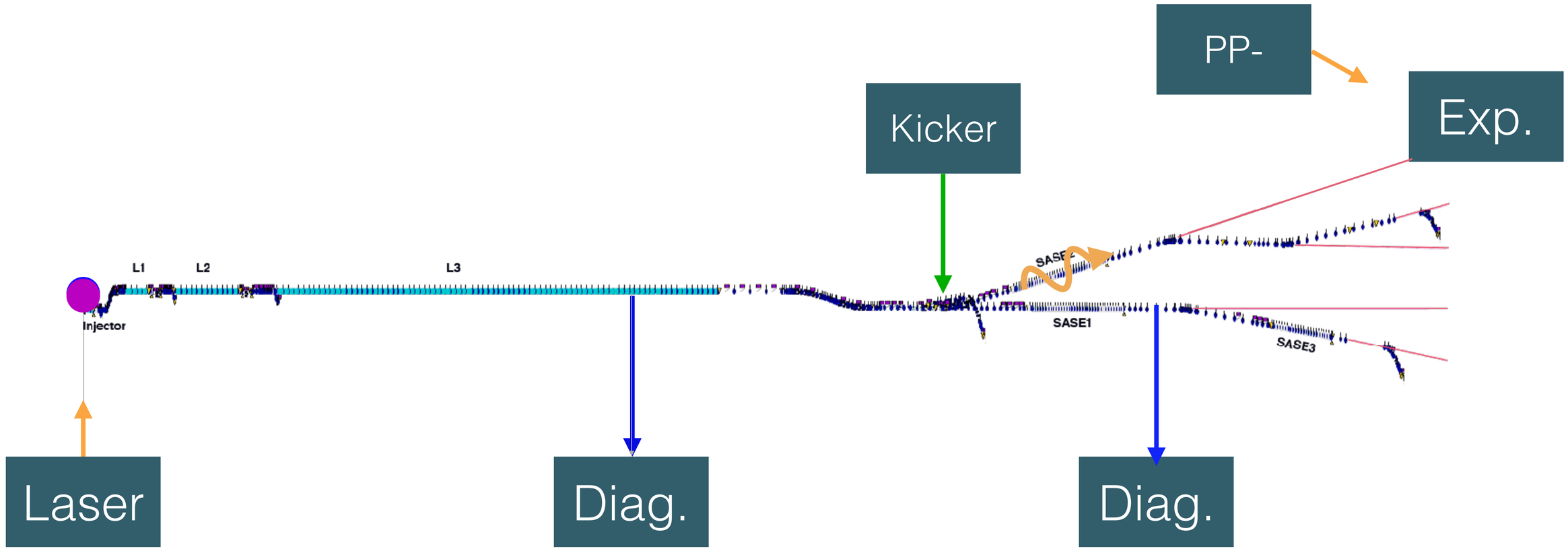


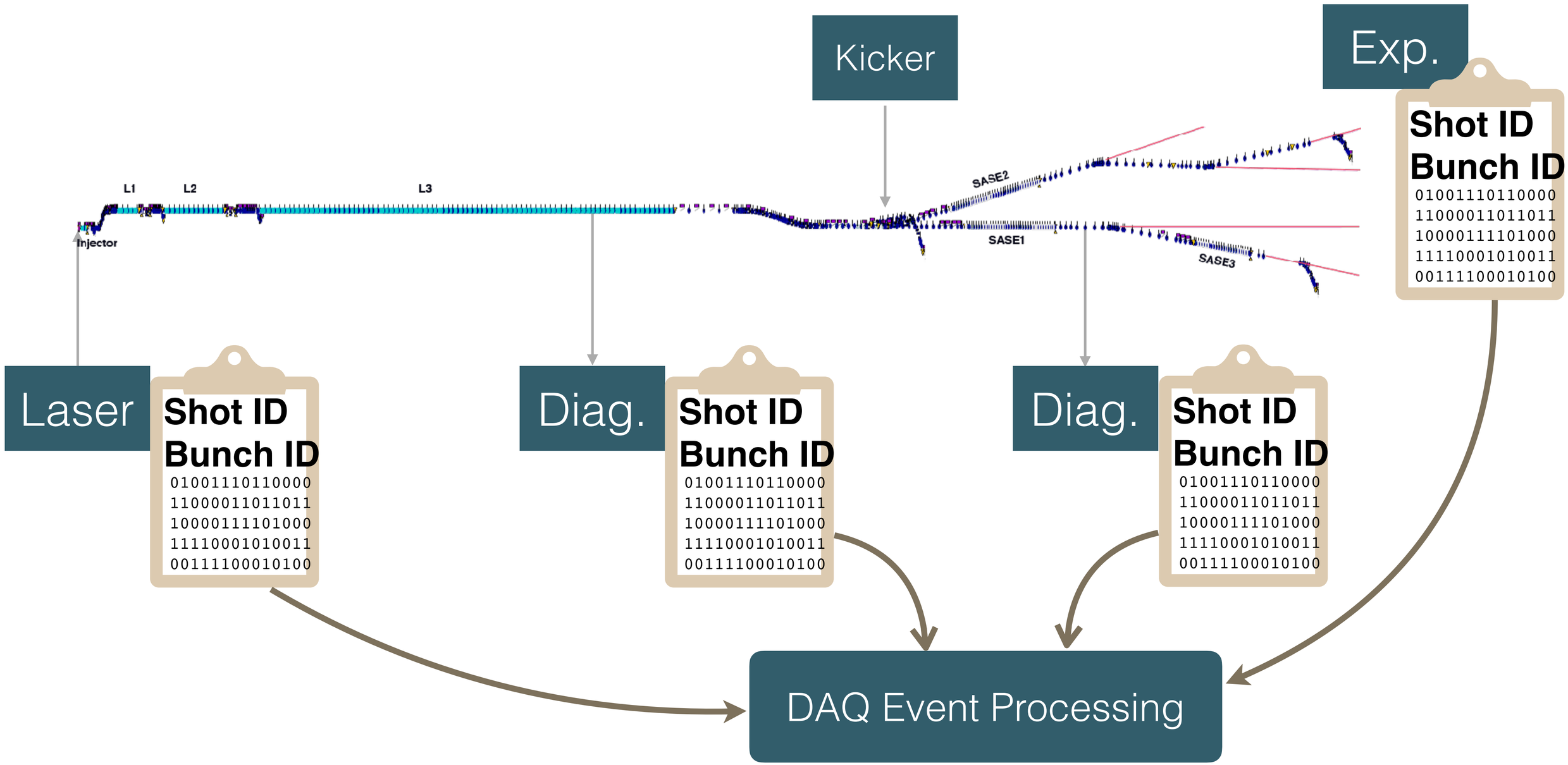
Figure 2–3. LVDS and M-LVDS Differential Input Voltage Thresholds

Introduction - Clocks & Triggers

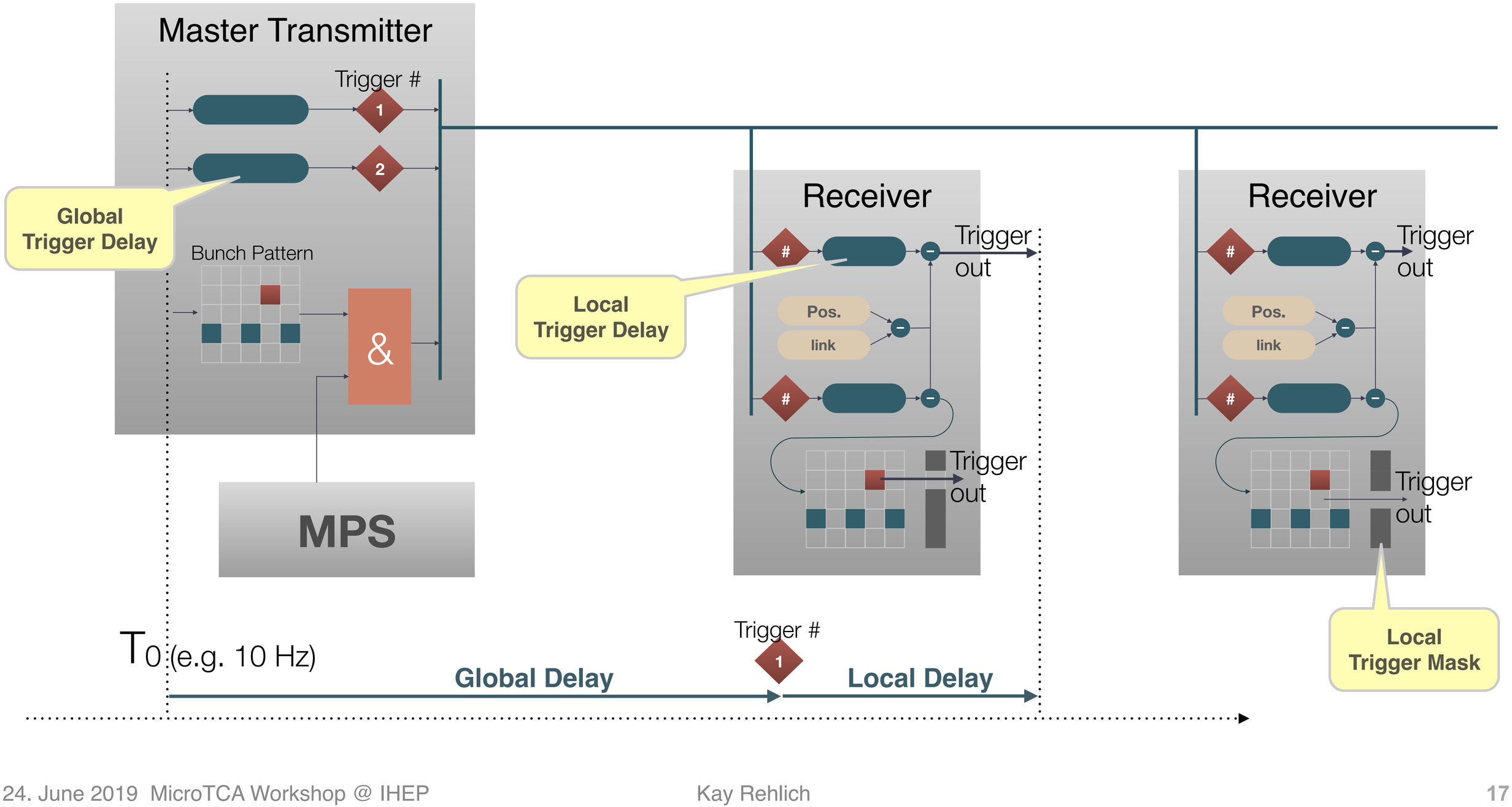


- Define the source and destination of bunches (XFEL: 27000 / sec.)
- Trigger and clocks for diagnostics and actuators depending on location

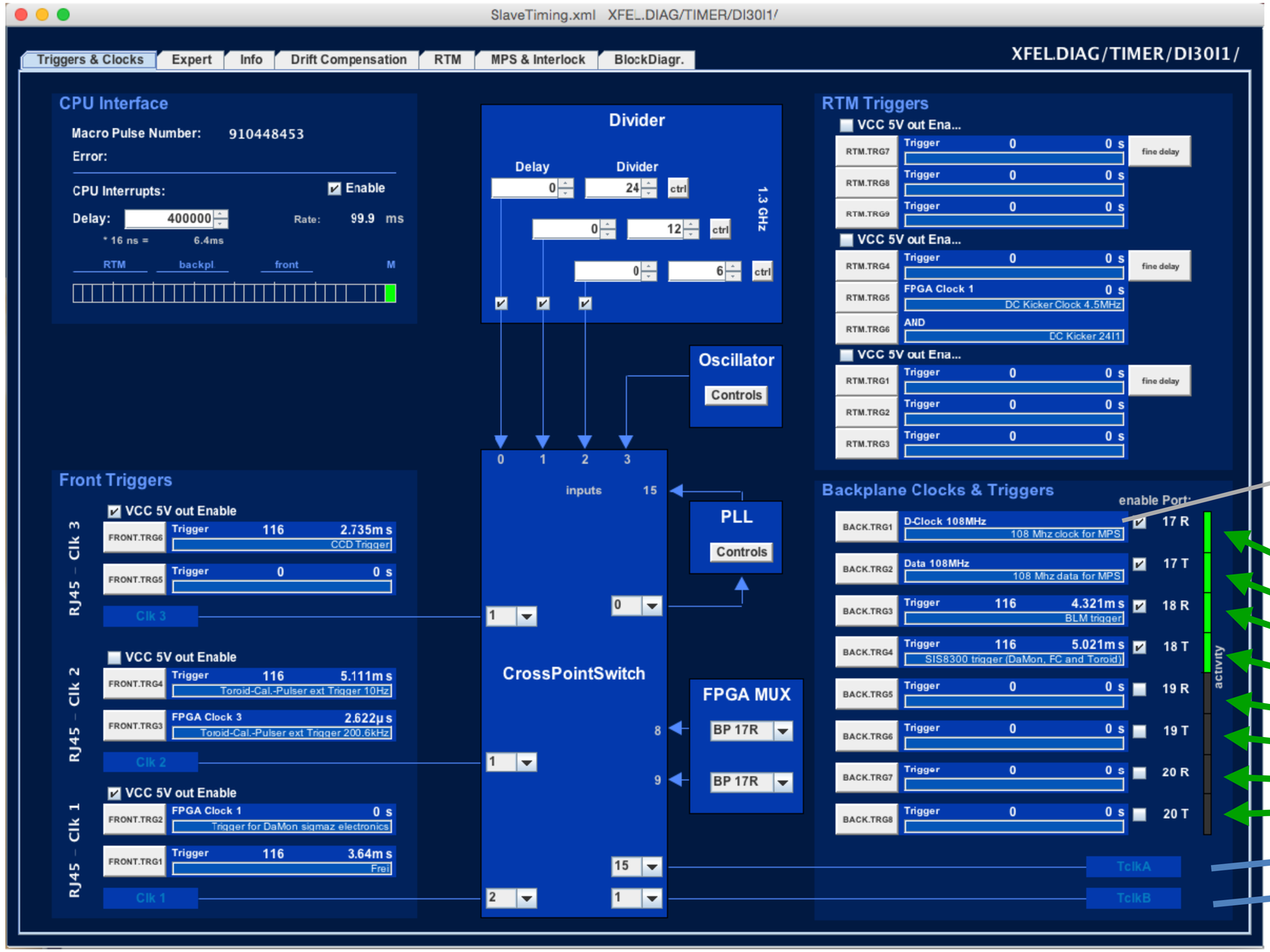
Introduction - Data Tags for Software



Trigger and Bunch Pattern Distribution



Usage of the MLVDS Lines: Timing Example



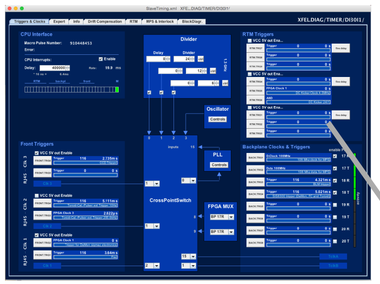
RTM Outputs

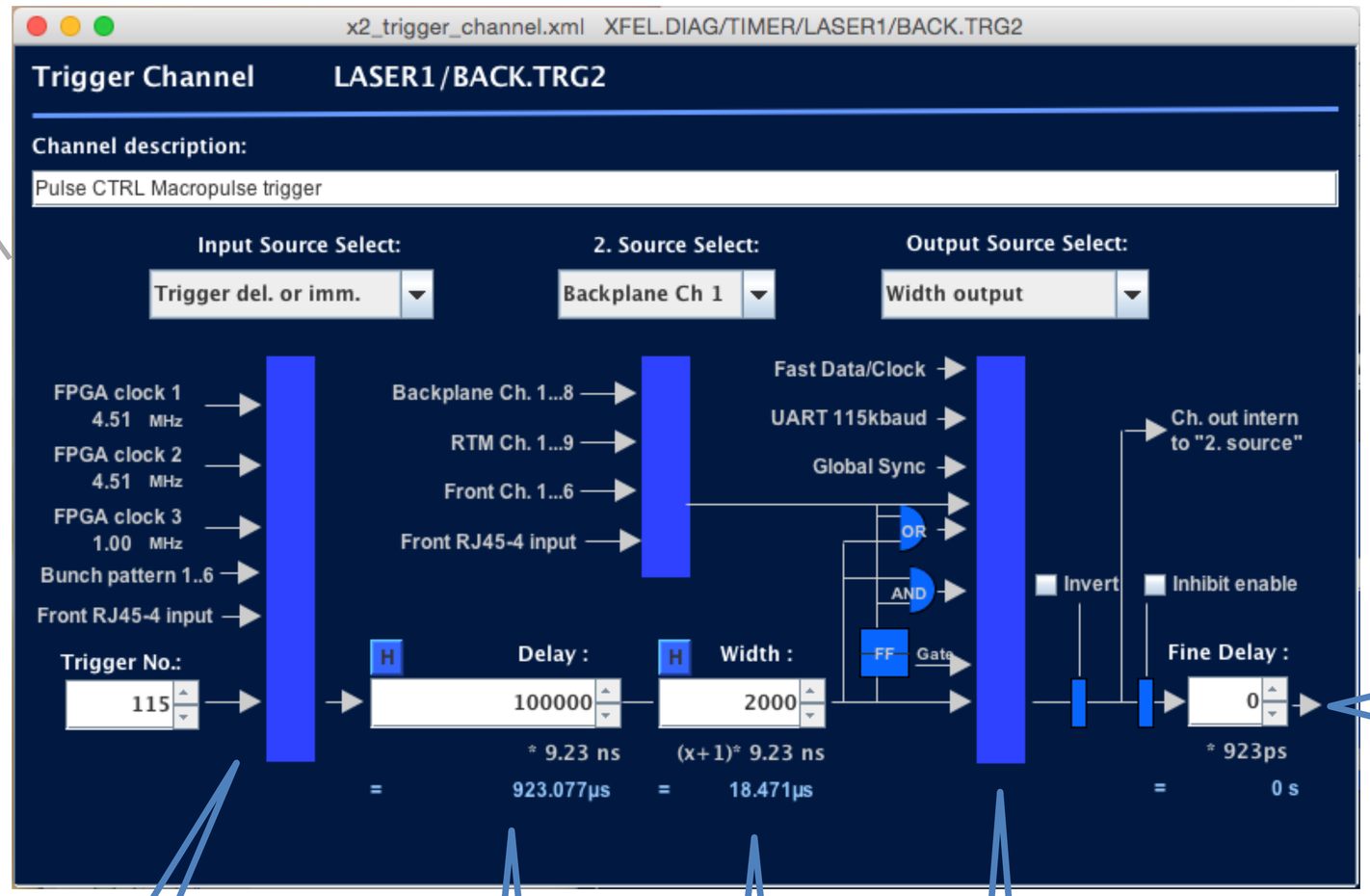
Front Outputs

Channel configuration

Backplane Outputs

One Trigger/Clock/Data Channel Configuration out of 23





Selection of:
- **Trigger # (0 … 255)**
- **Bunch Pattern**
- **Clock from FPGA**
- **Front Input**

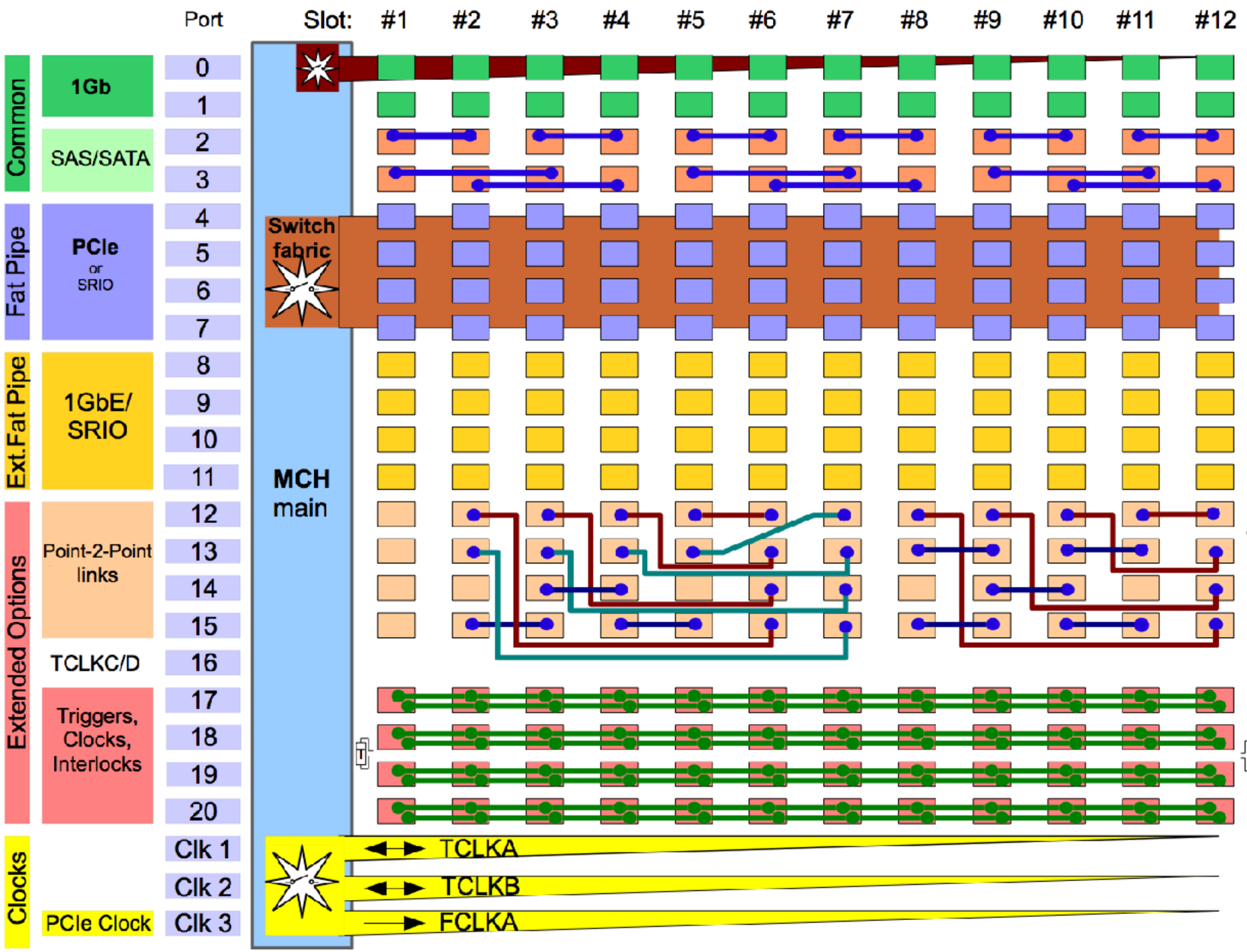
Delay and Width:
- **up to 150ms**
- **in 9.23ns steps**

Combination w/ second channel:
- **Gates (start**
- **Bursts of clocks**
- **Combine with 2nd channel**

Select source:
- **Single delayed & width**
- **Combination w/ 2nd Ch.: AND, OR, FlipFlop**
- **Serial data**

Output can be:
- **Inverted**
- **Inhibited**
- **Fine Delay: .92 ns steps**

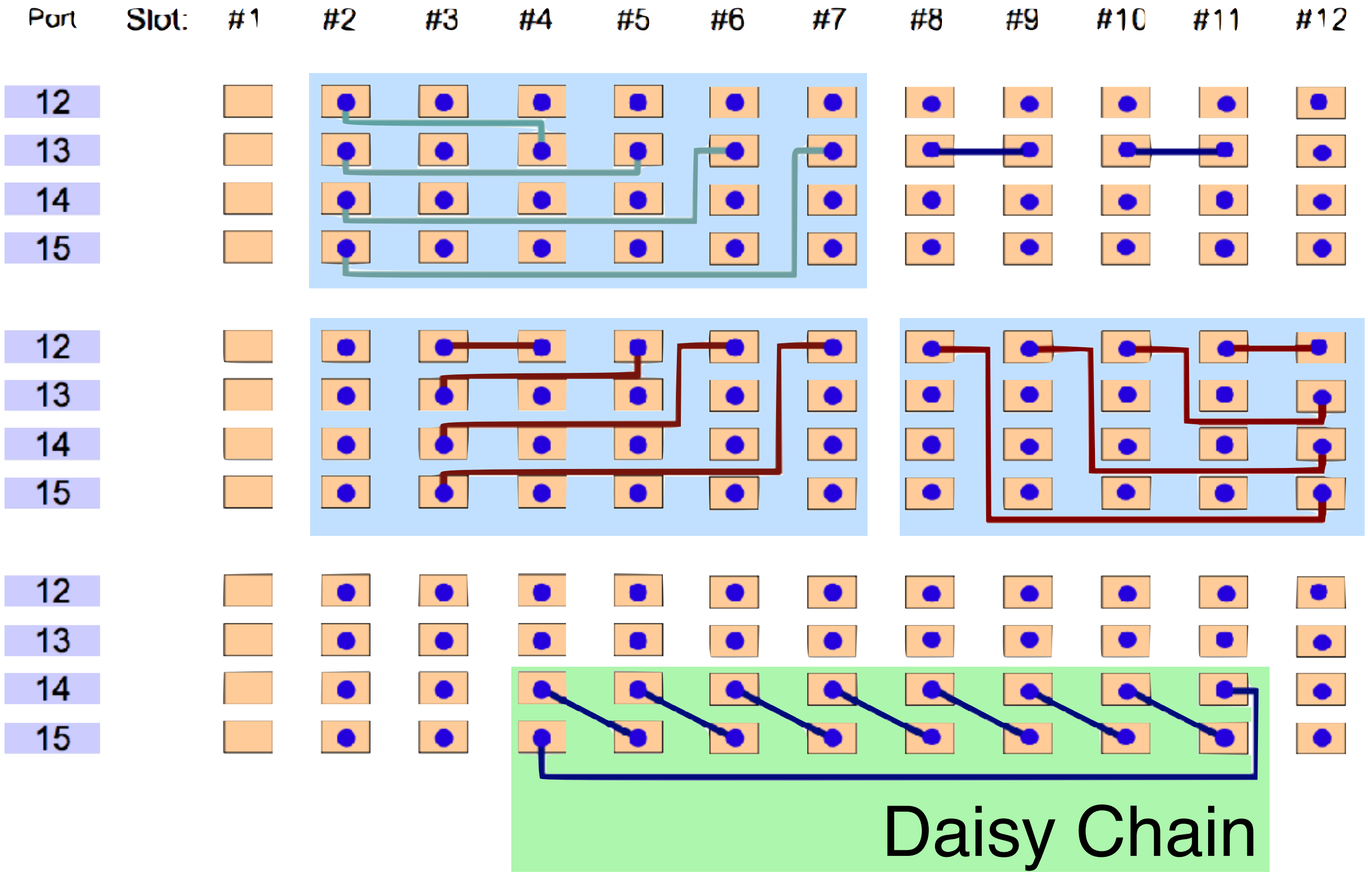
MTCA.4 with Point-2-Point Links

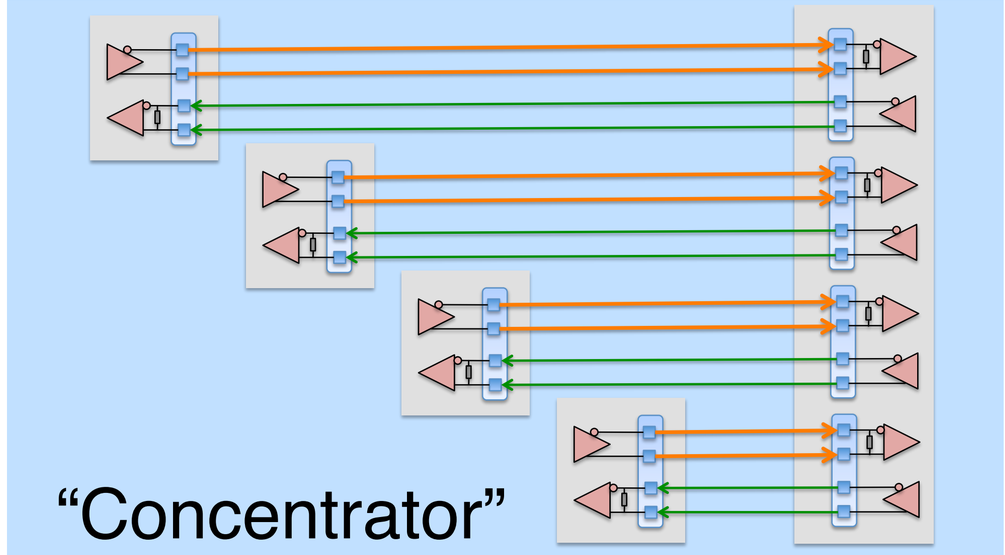


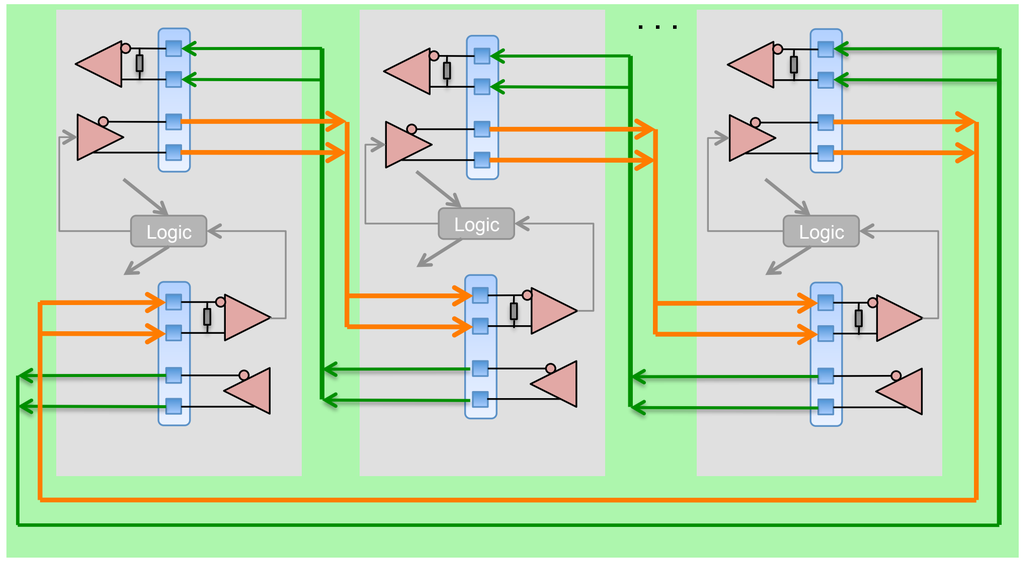
4 bi-directional LVDS lines:

FPGA-2-FPGA communication

Point-2-Point Topologies

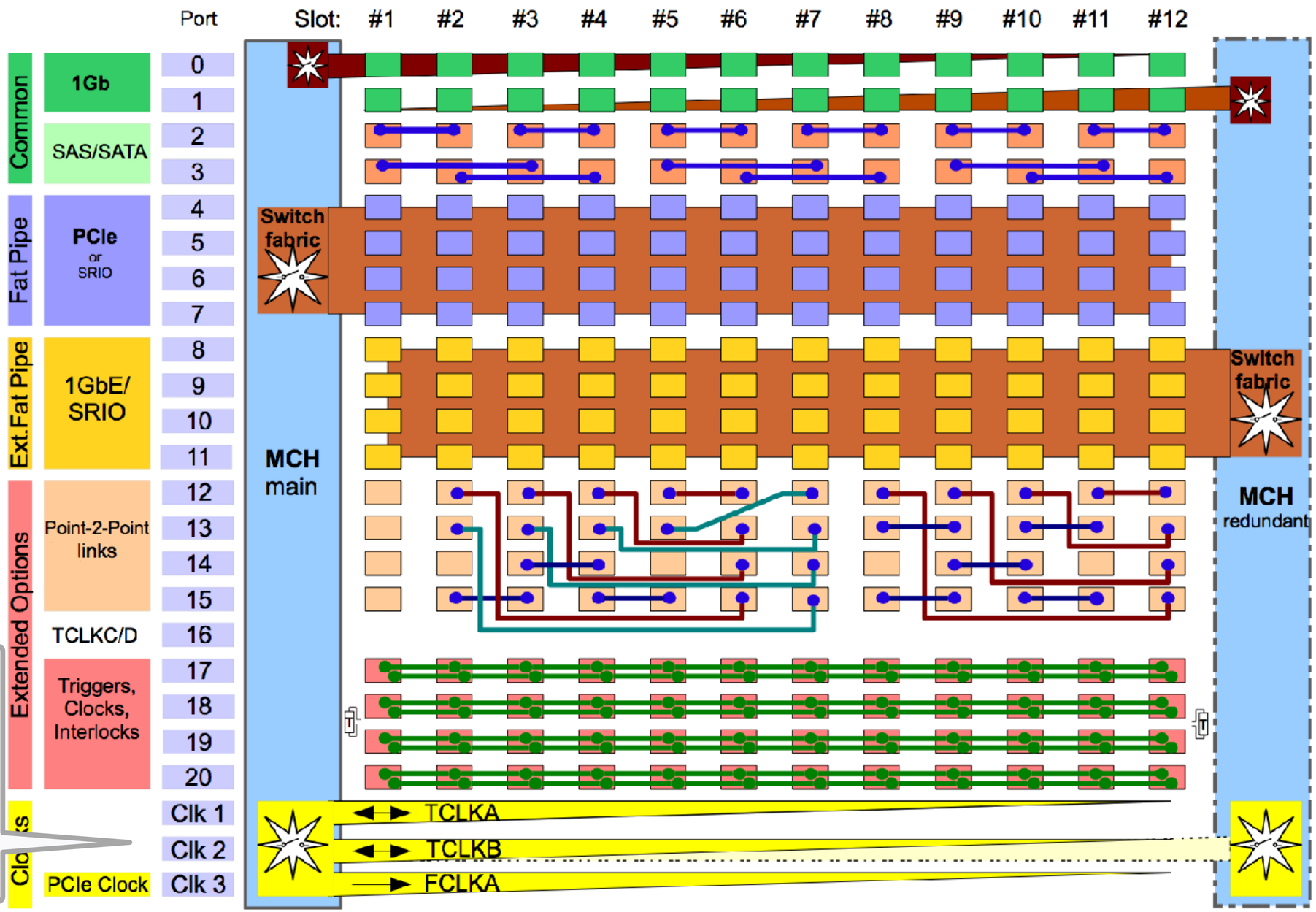






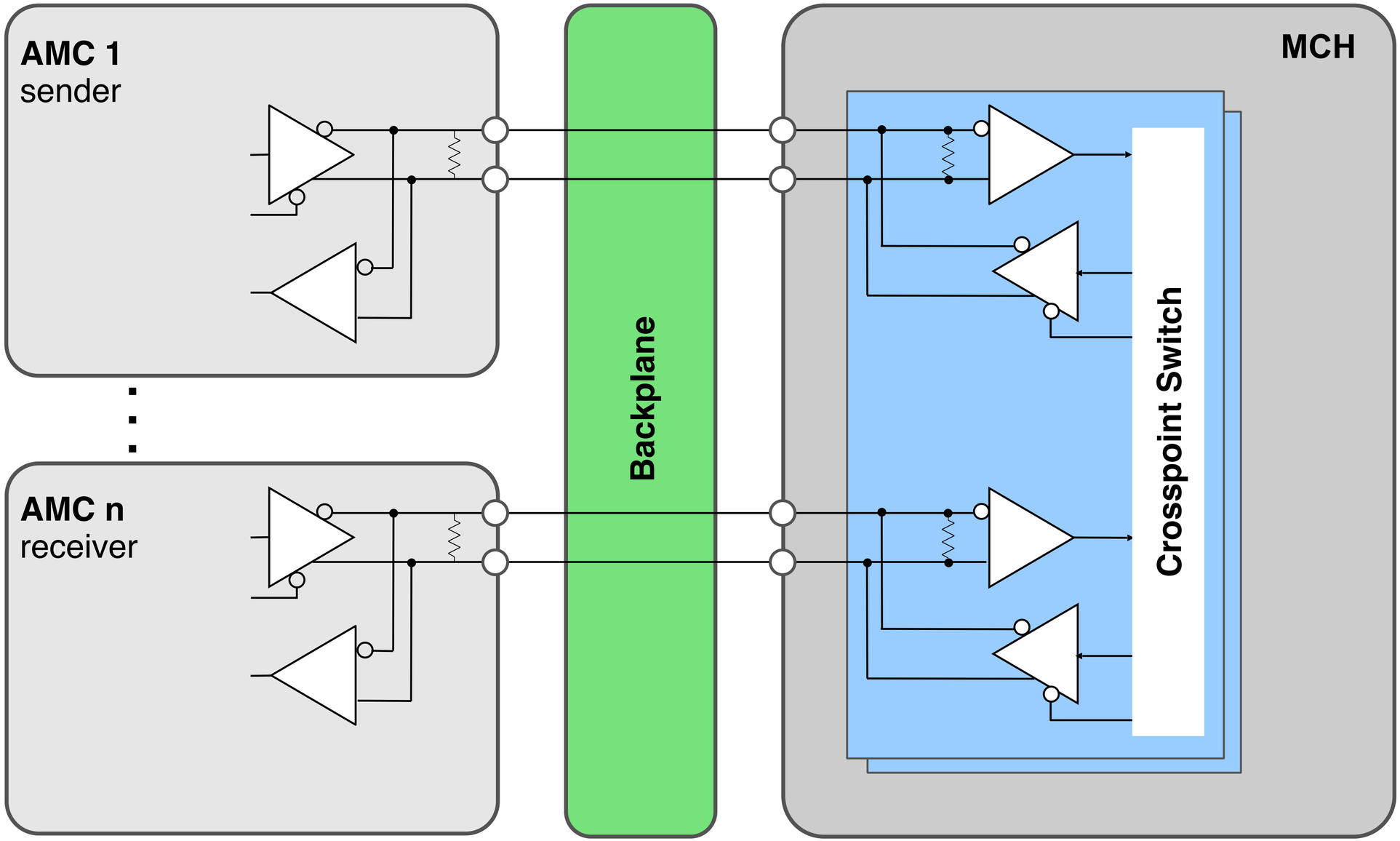
Other topologies are possible by modifying the backplane

MTCA.4 Clocks: MTCA.0 Compatible

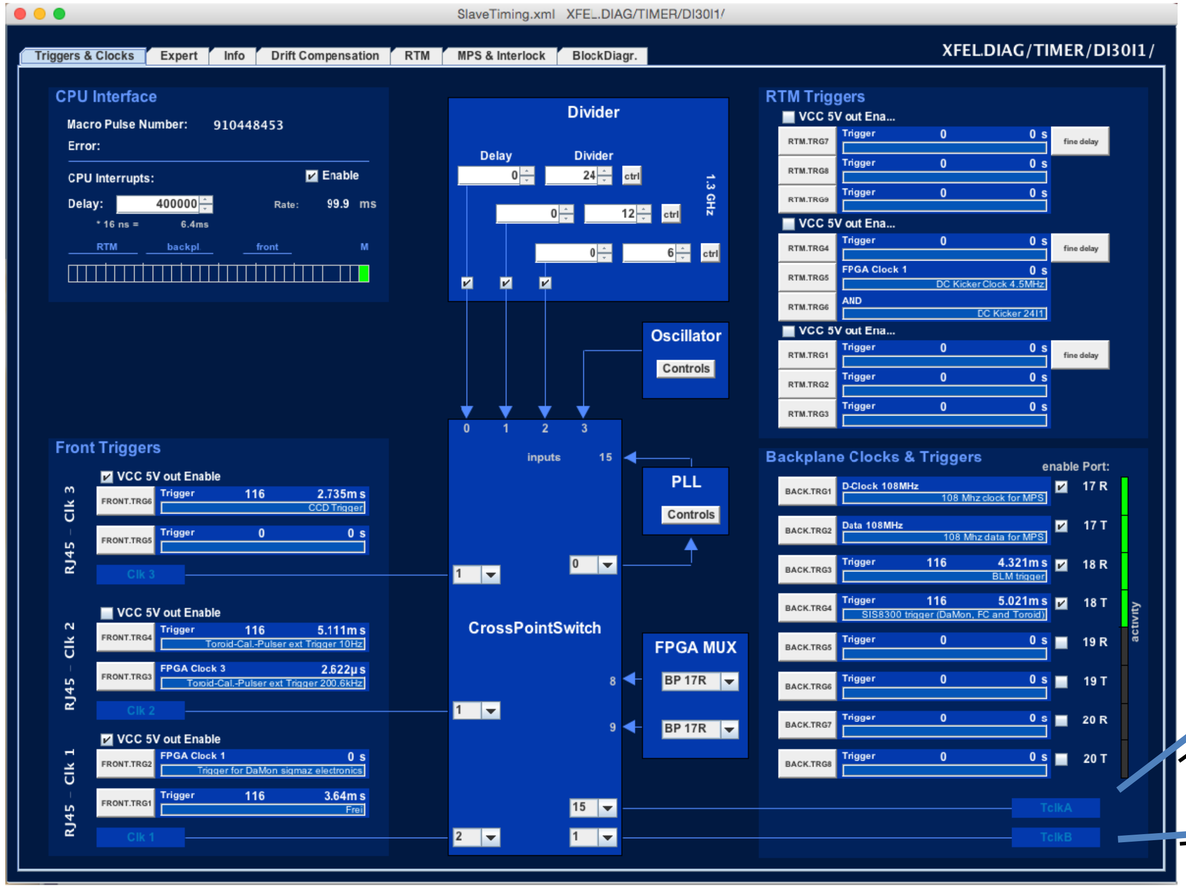


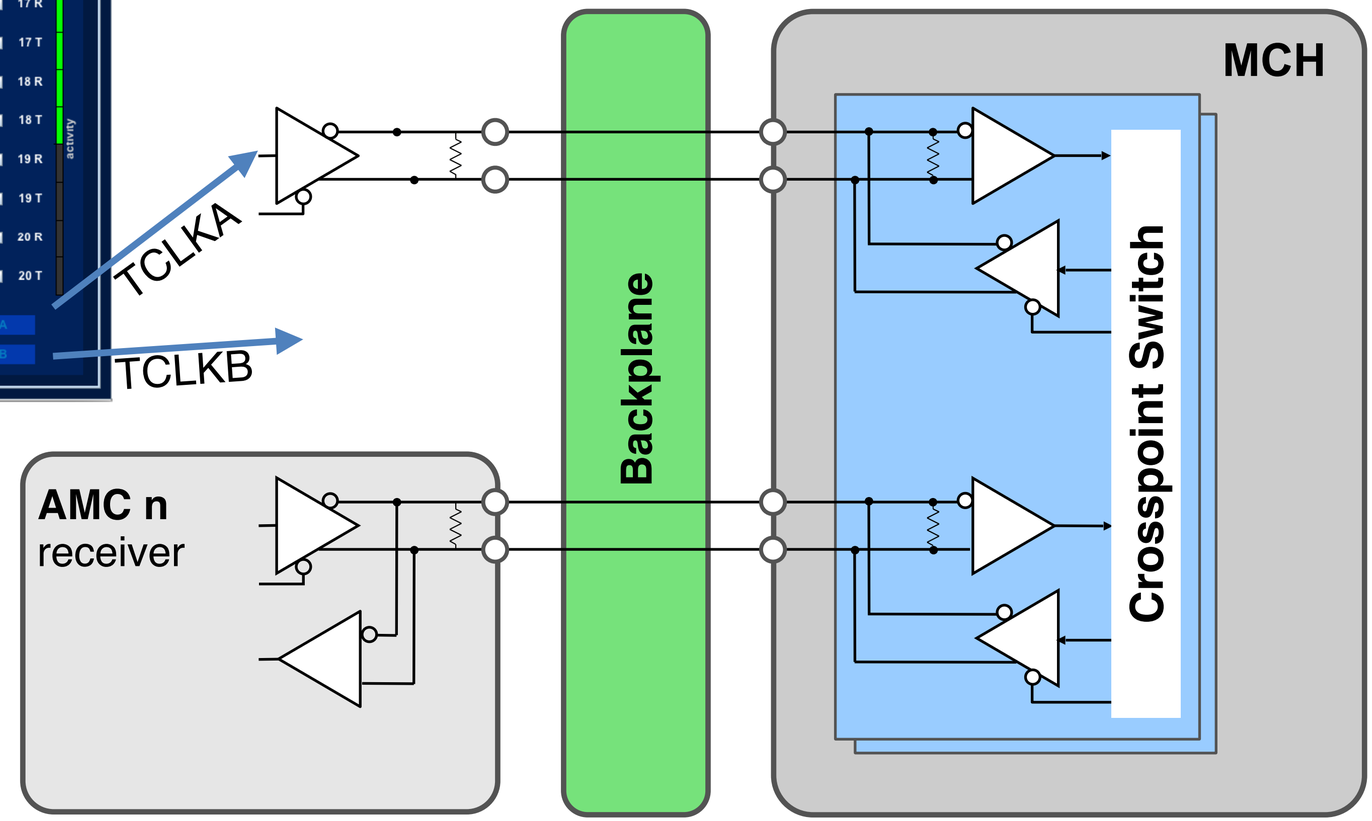
Point-2-Point Clocks:
- Low jitter
- Flexible configuration

Low Jitter Clock Distribution: Bi-directional LVDS



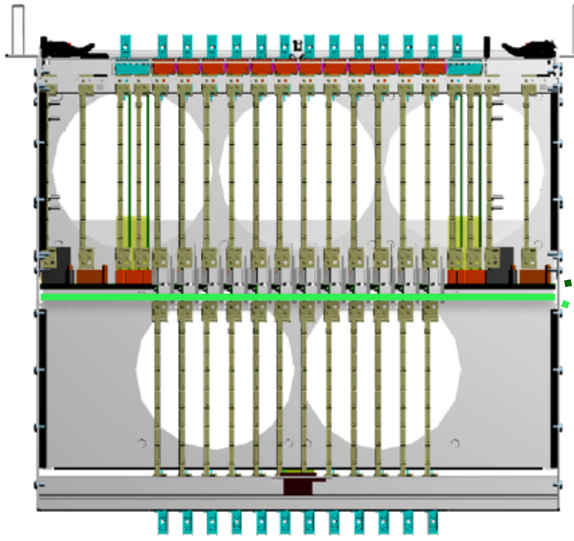
Low Jitter Clock Distribution: Bi-directional LVDS



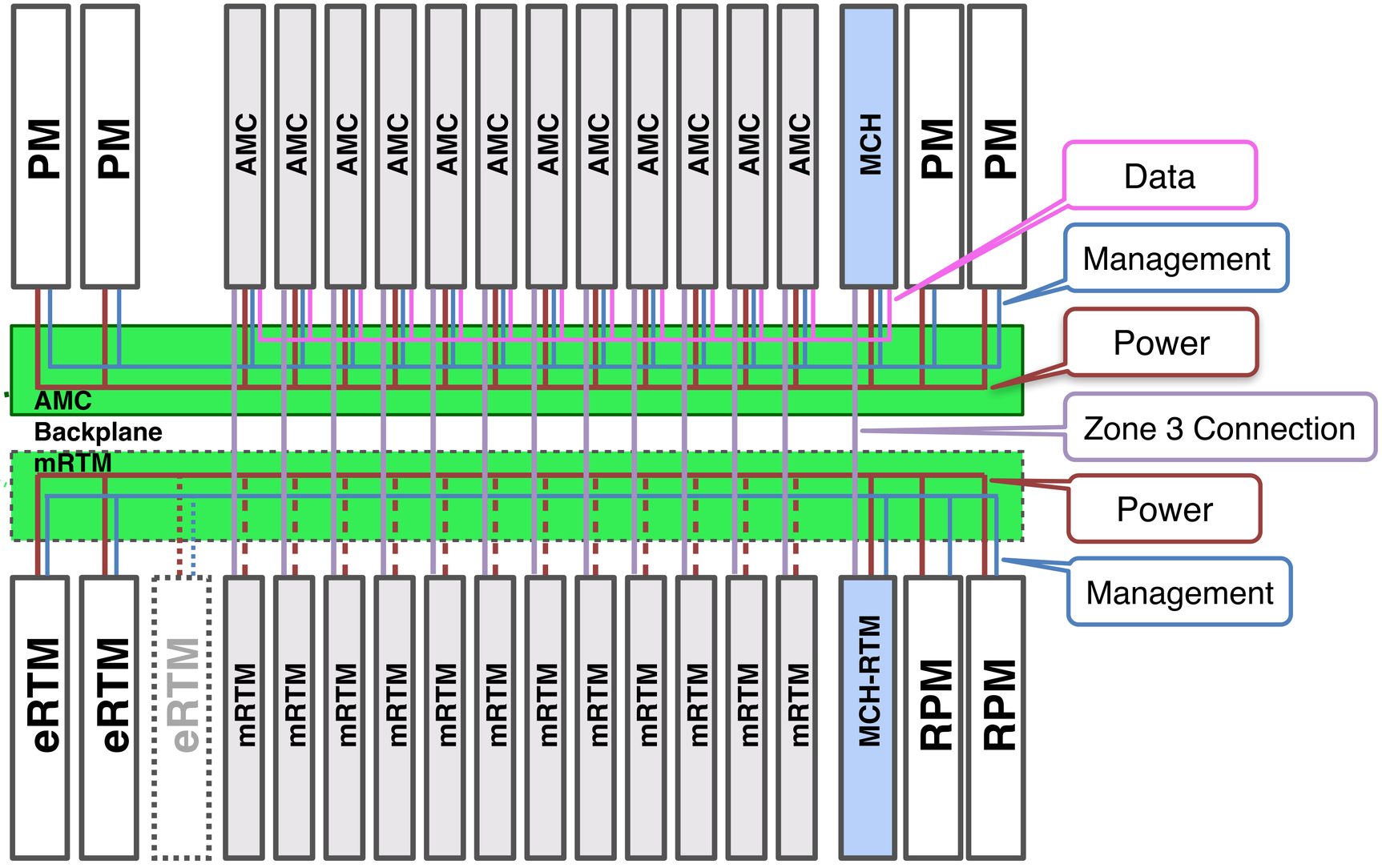


MicroTCA Generations: MTCA.0 MTCA.4 **MTCA.4.1**

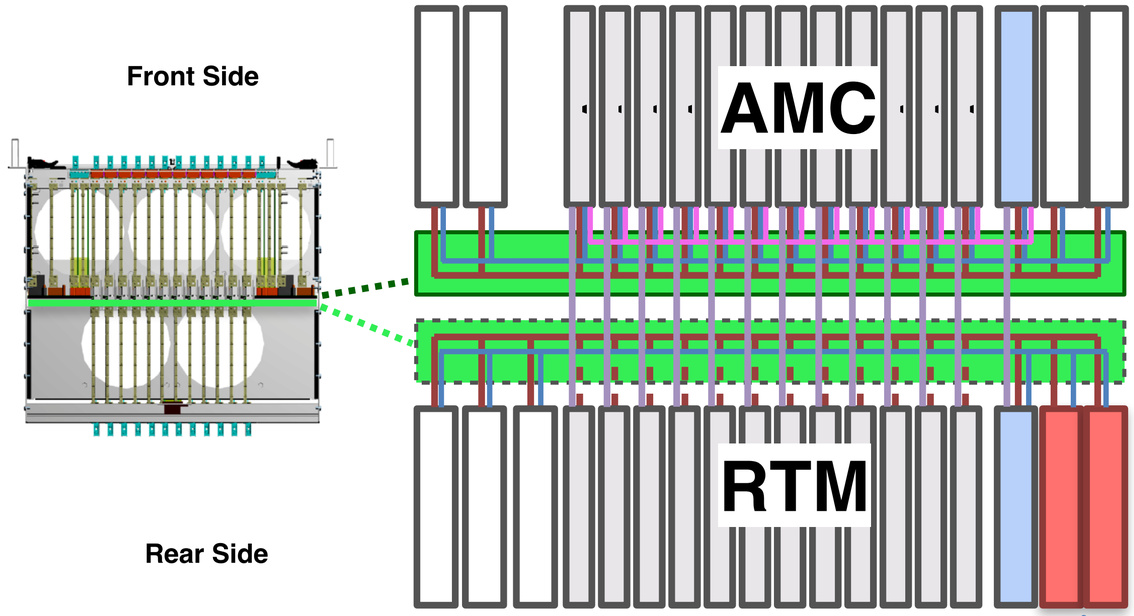
Front Side



Rear Side



MicroTCA.4.1 Rear Power Module



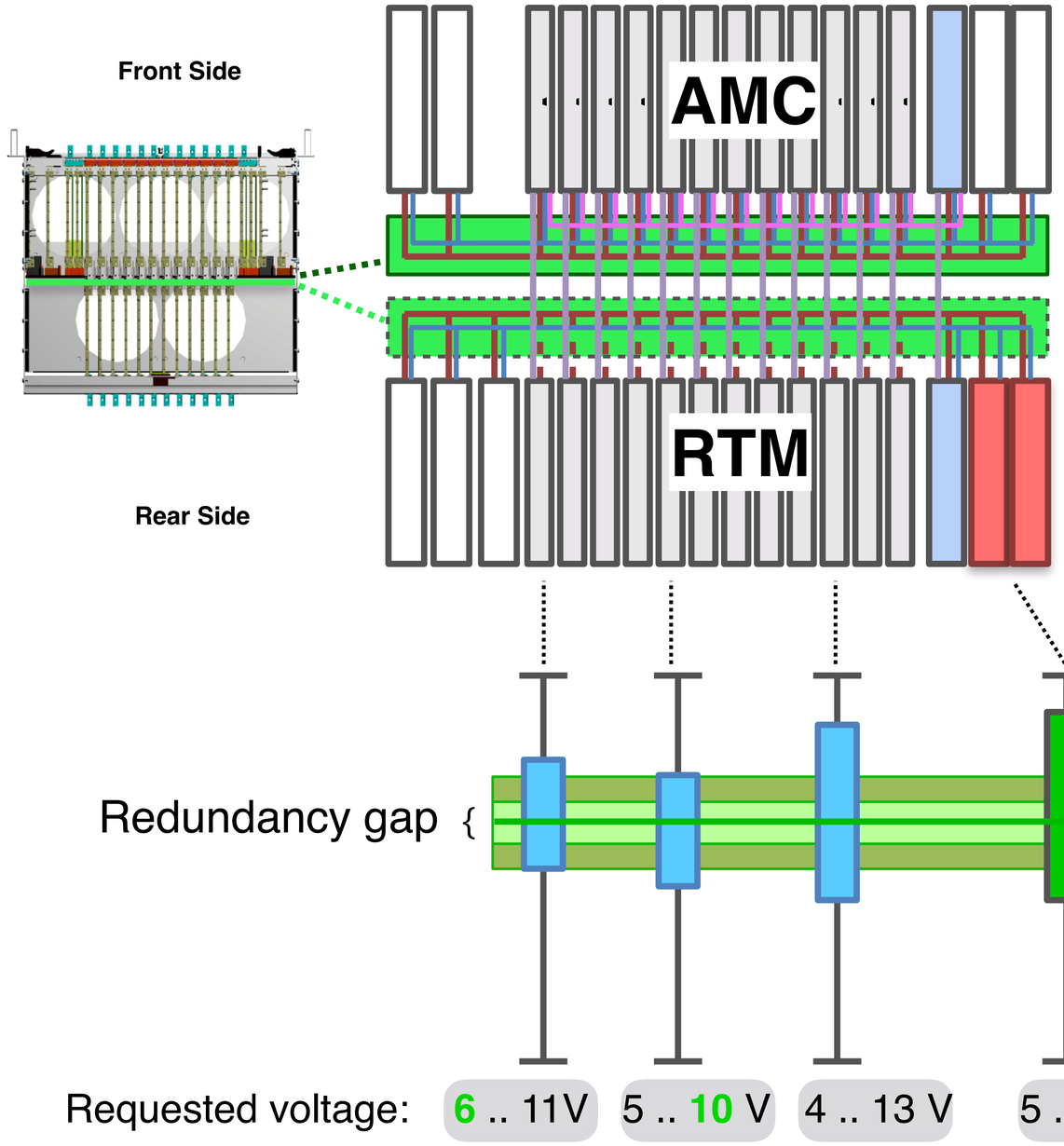
RPM: Rear Power Module

Provides:

- 3.3 V management power to eRTM
- 12 V to eRTM
- Positive variable Voltage to RTM
- Negative variable Voltage to RTM

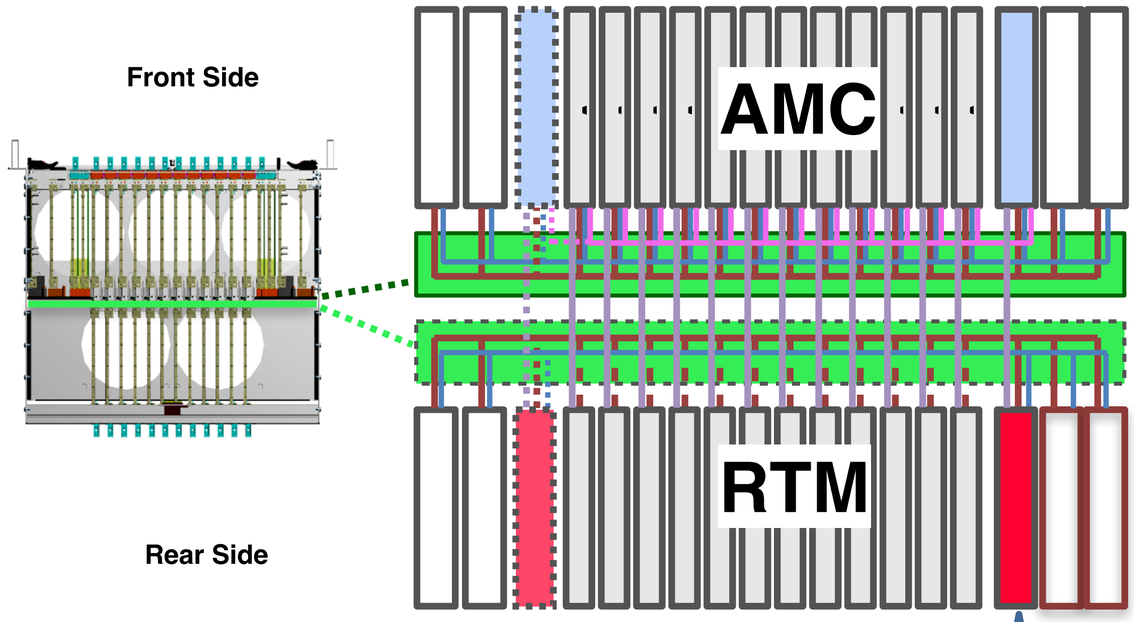
Managed by MCH via MCH-RTM

MicroTCA.4.1 Rear Power Module: Variable Voltage



Example

MicroTCA.4.1 MCH Rear Transition Module

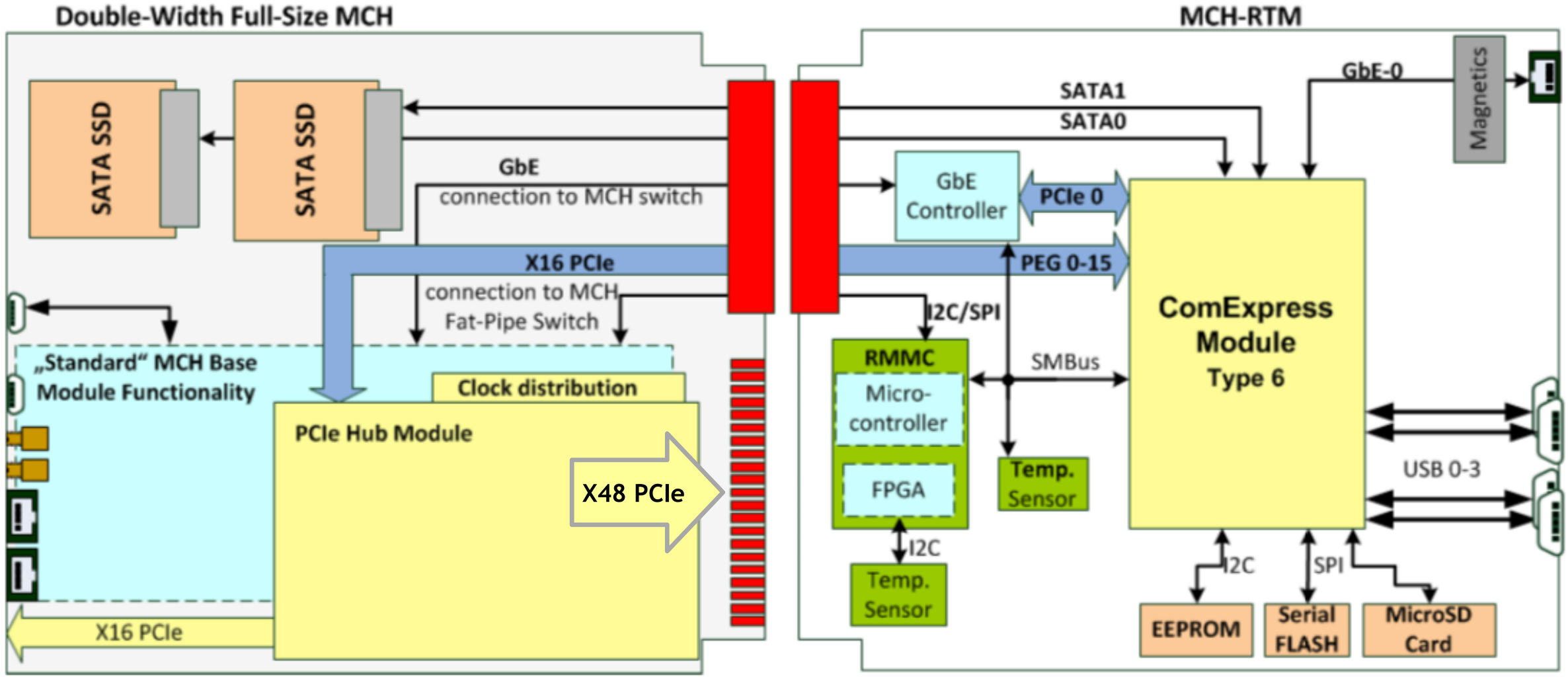


MCH-RTM: MCH Rear Transition Module

- Zone 3 plug is defined in MTCA.4.1
- The MCH is the manager, the RTM links the *μ*RTM Backplane to the MCH
- Low power eRTMs can be powered from the MCH

MicroTCA.4.1 MCH Rear Transition Module

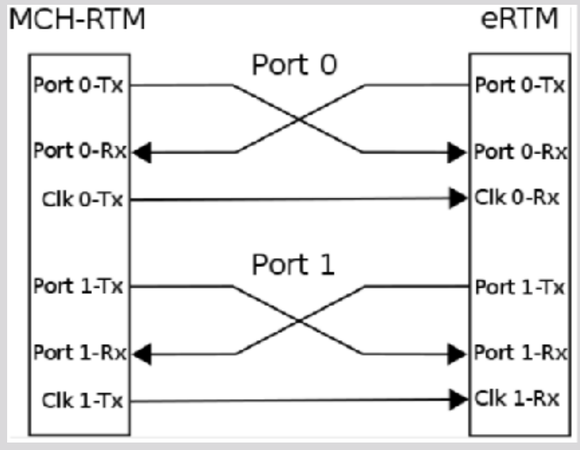
- Up to **16 additional PCIe** lanes (fat-pipes) for e.g. a CPU on MCH-RTM
- Management of a second μRTM backplane

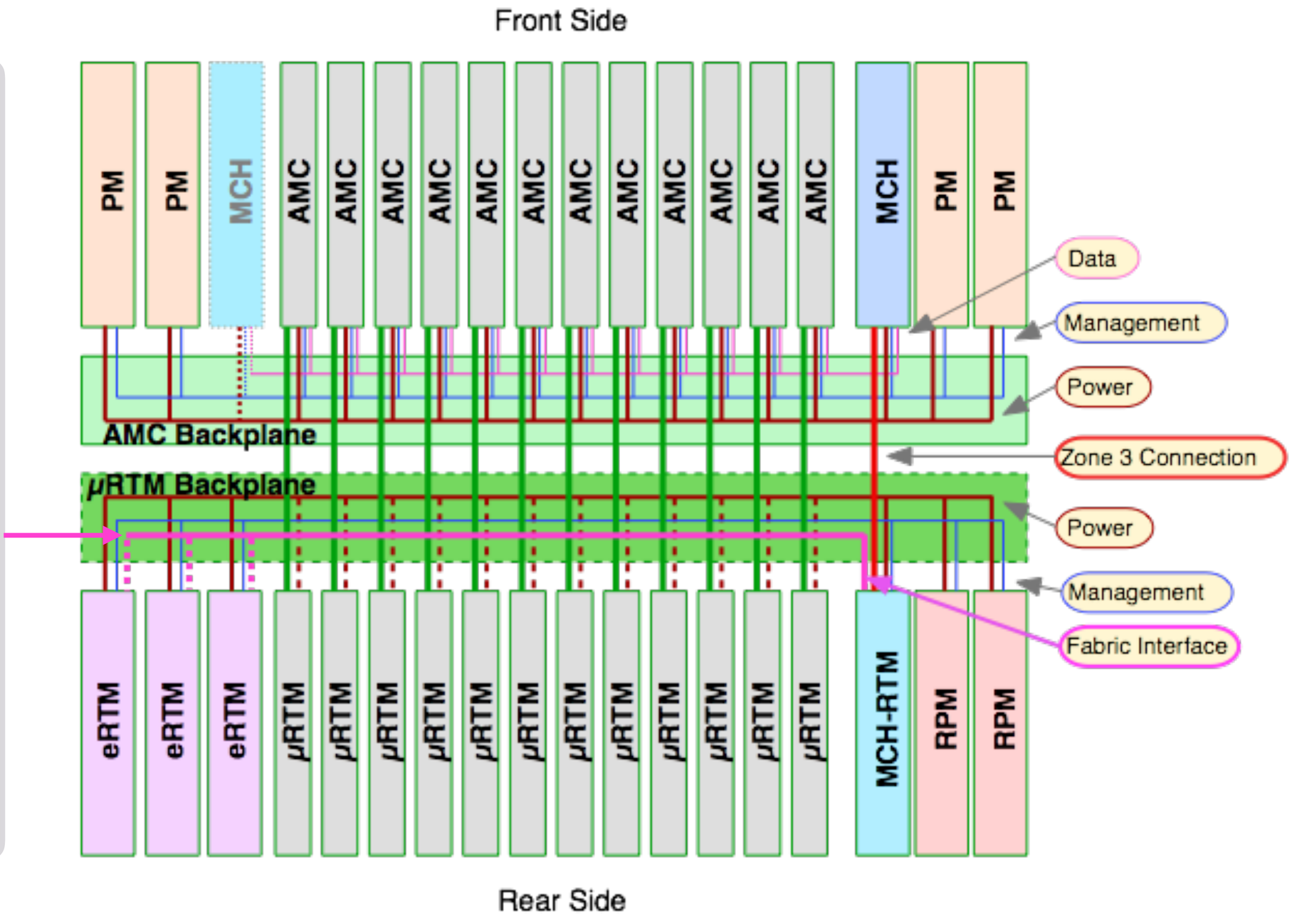


MicroTCA.4.1 MCH-RTM: 3 * 2 Fat-Pipes

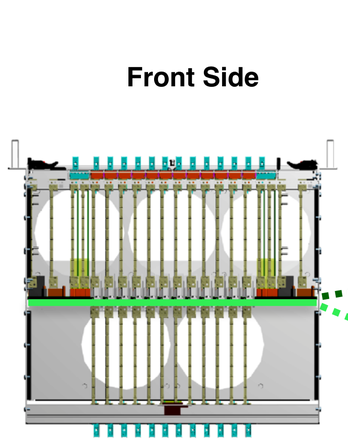
Supported Protocols:

- PCI Express
- PCI Express Advanced Switching
- Ethernet 1000Base-X
- Serial RapidIO
- Serial Peripheral Interface
- Universal Asynchronous Receiver-Transmitter
- Universal Synchronous Receiver-Transmitter
- Ethernet 100Base-T





MicroTCA.4.1 Extended Rear Transition Module



1 or 2 RPM:
Power to:
- eRTM
- μRTM
- MCH-RTM

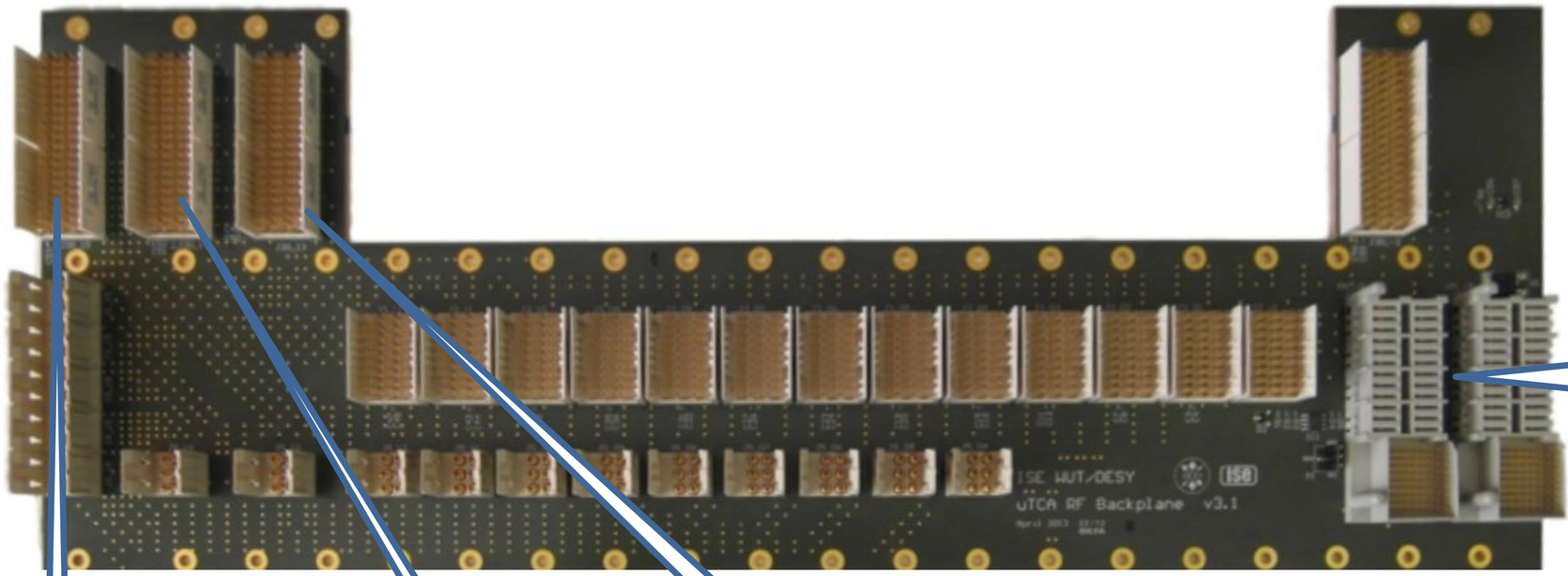
Optional

eRTM 13 or 2nd MCH-RTM:
Power from RPM

eRTM 15:
Power from MCH-RTM or RPM
Example: RF and Clock distribution

eRTM 14:
Power from RPM

Example *µ*RTM Backplane



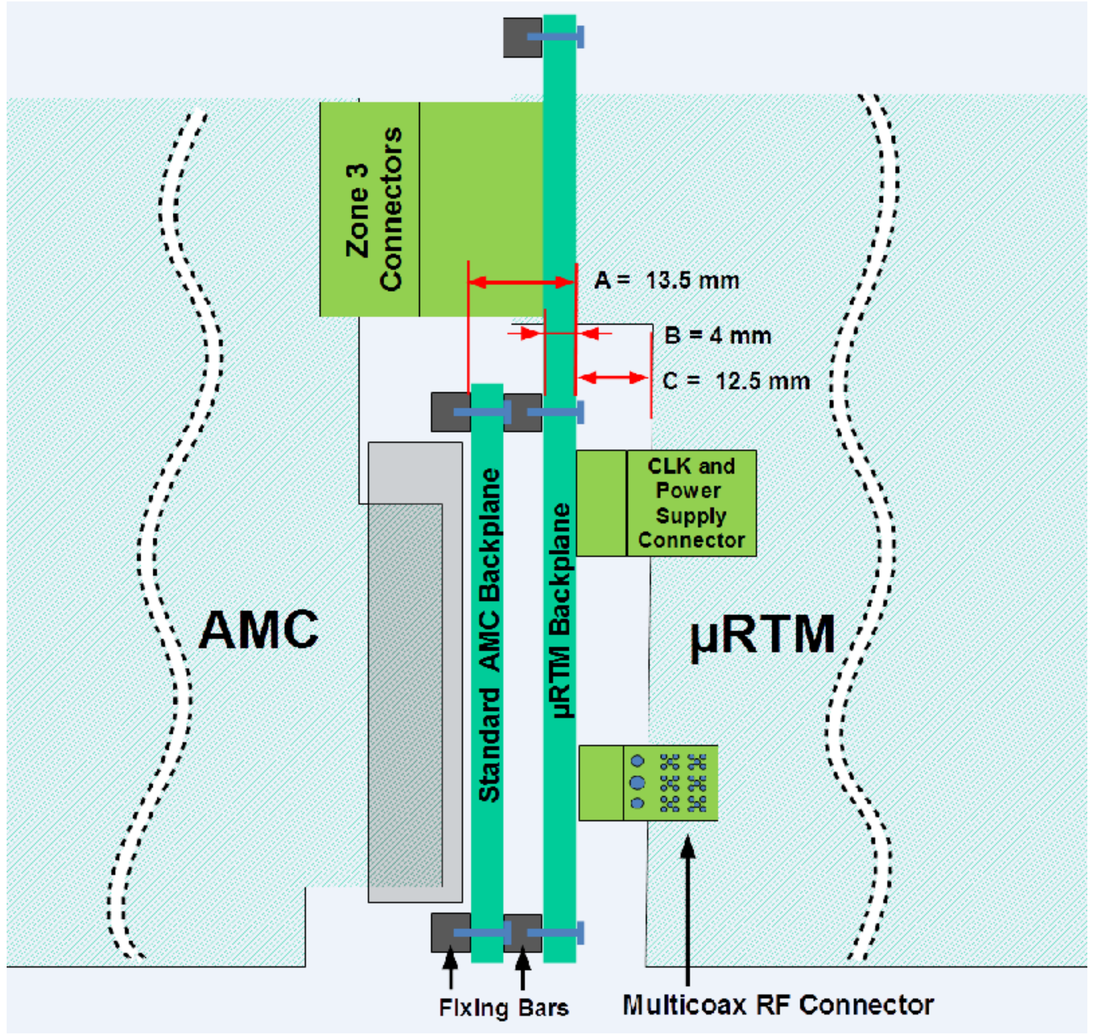
1 or 2 RPM:
Power to:
- eRTM
- *µ*RTM
- MCH-RTM

eRTM 13 or 2nd MCH-RTM:
Power from RPM

eRTM 15:
Power from MCH-RTM or RPM
Example: RF and Clock distribution

eRTM 14:
Power from RPM

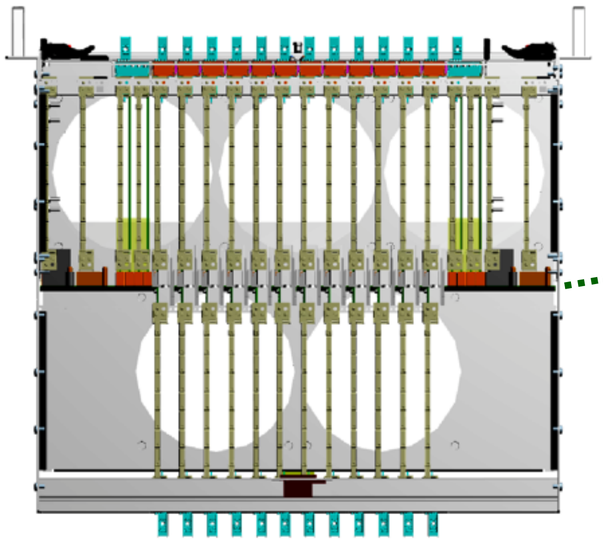
Position of the *µ*RTM Backplane



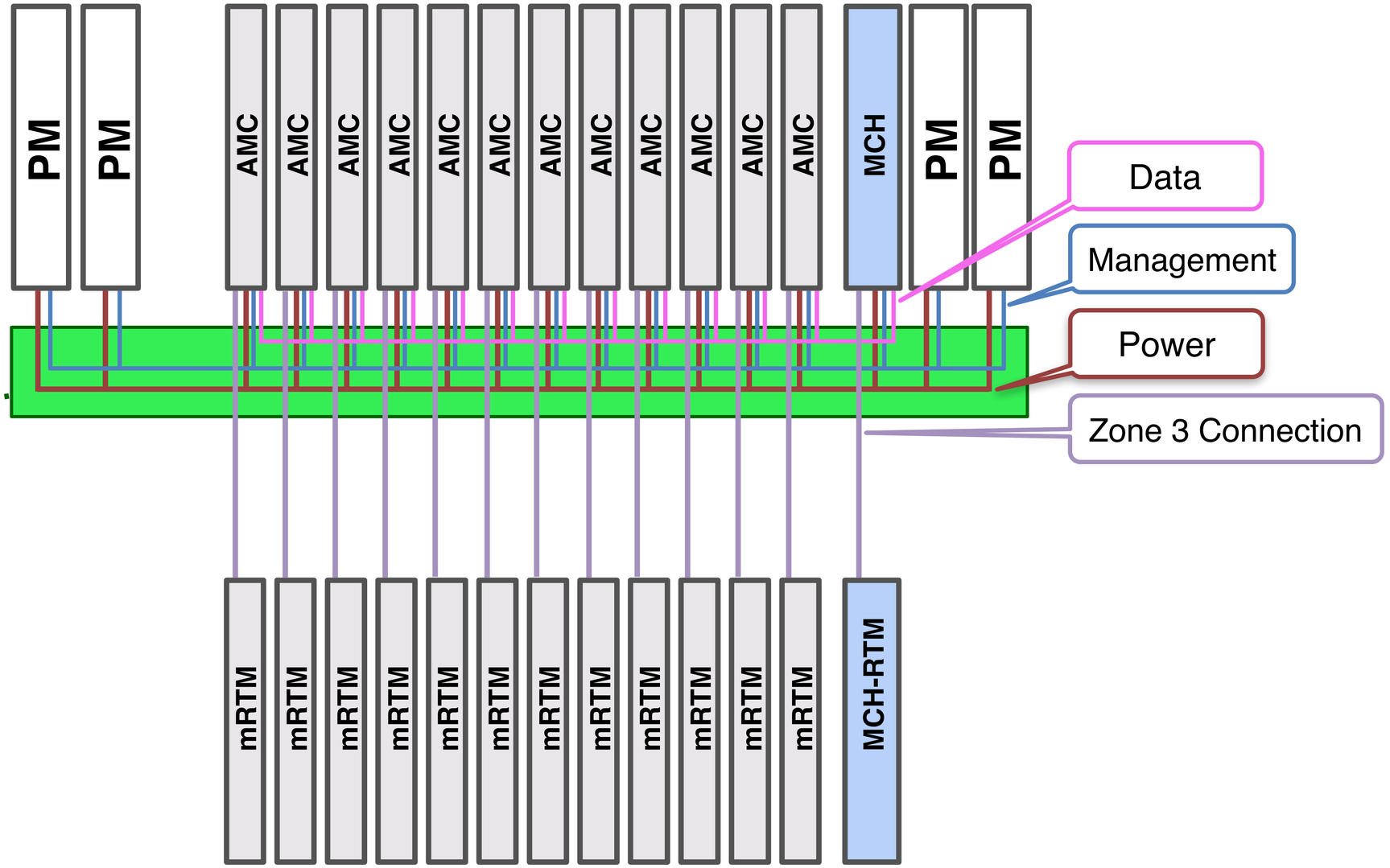
- The distance of the plugs on both backplanes are fixed
  - Independent of the backplane thickness

MTCA.4 Backplane

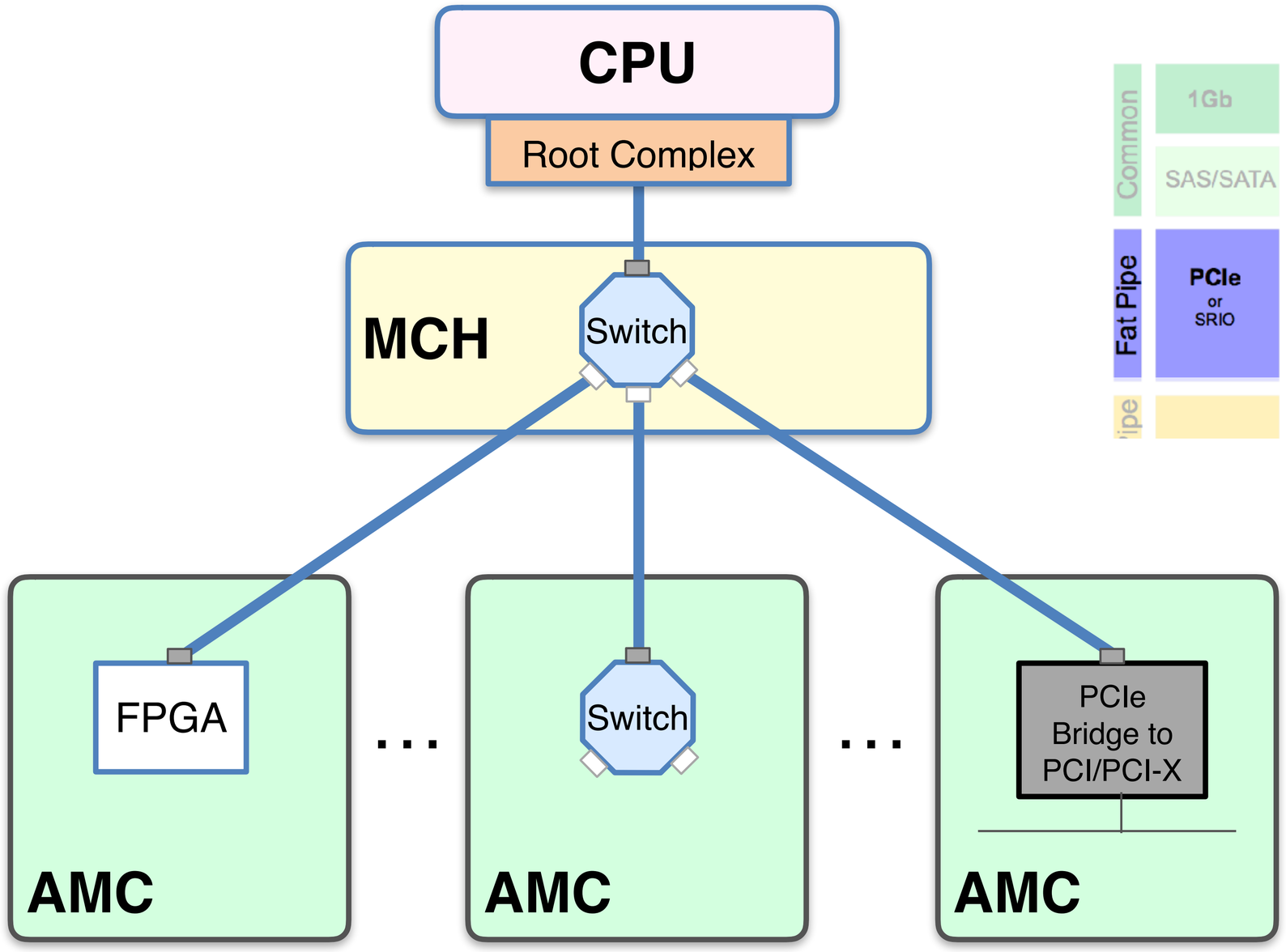
Front Side

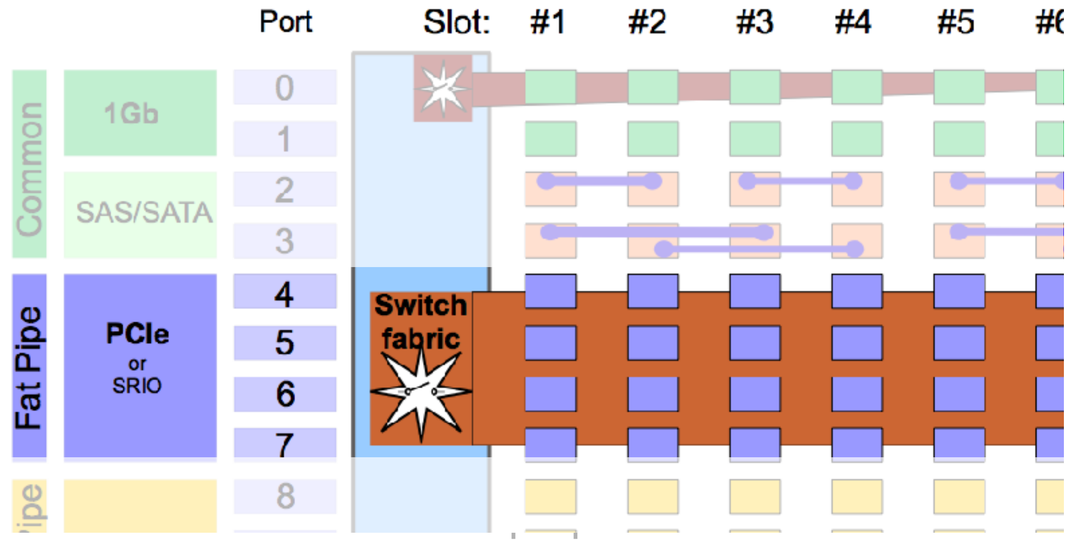


Rear Side

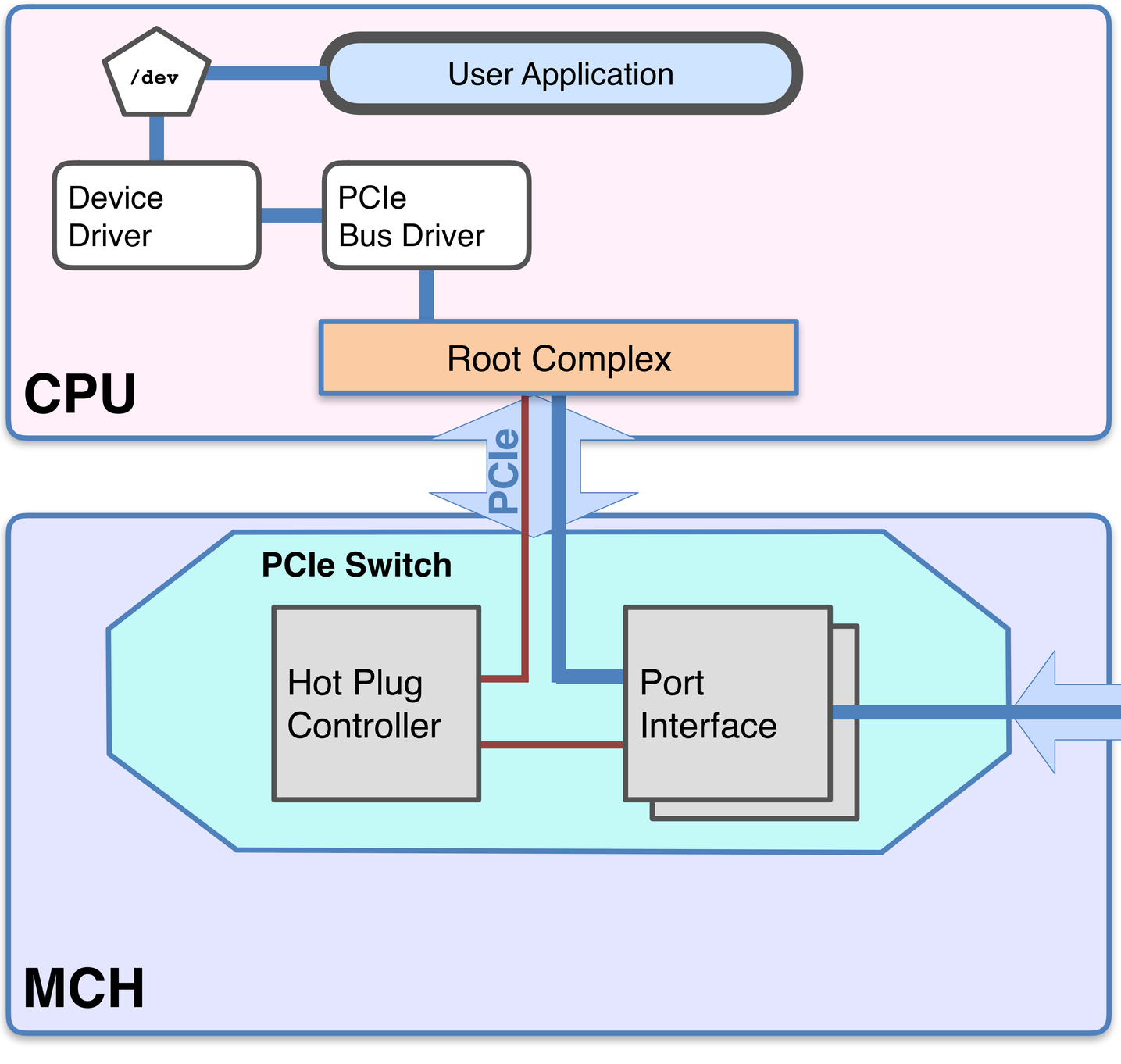


PCIe Topology





Architecture : PCIe with Hot-Swap

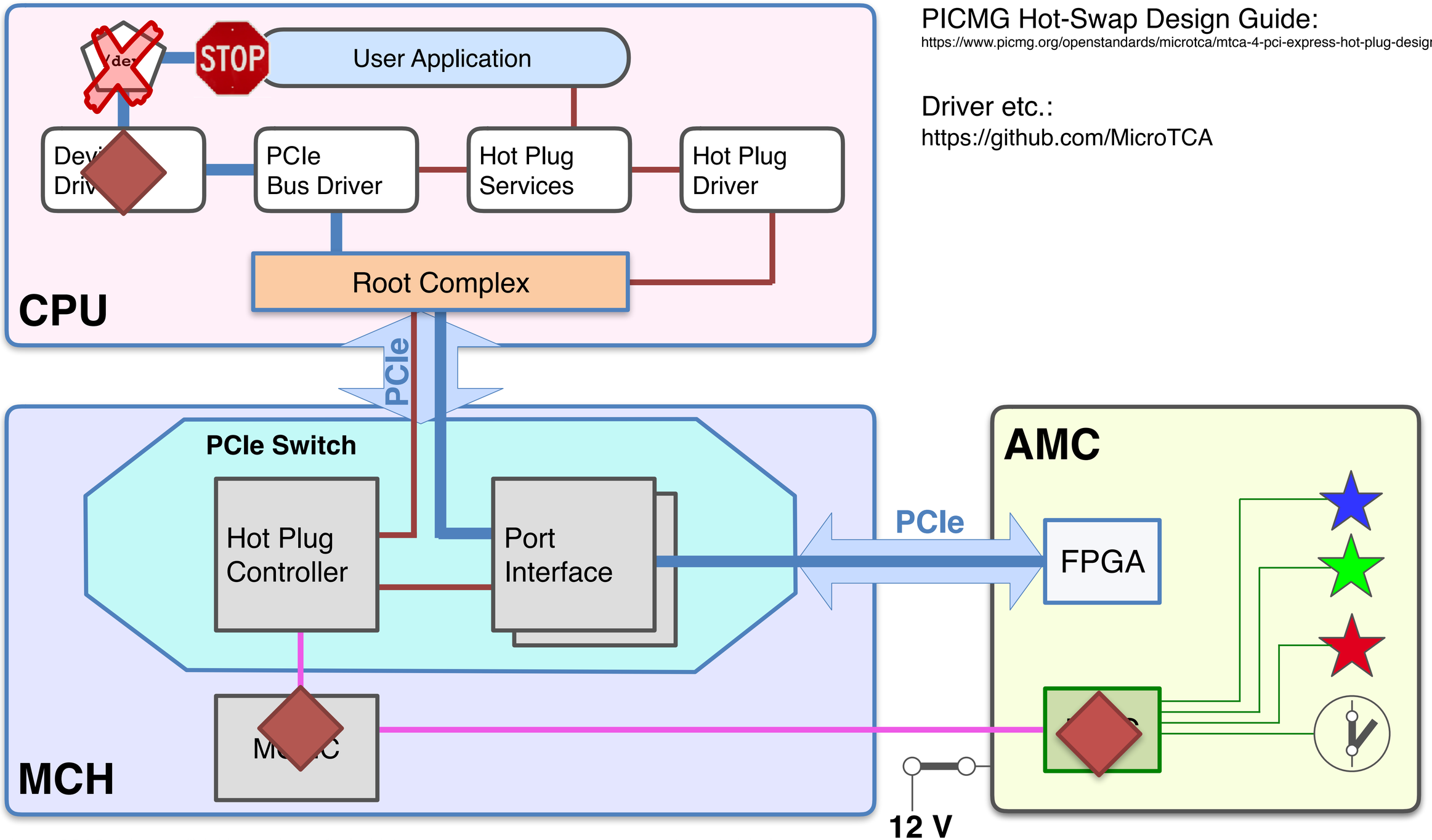


Application is running

next

Pull handle

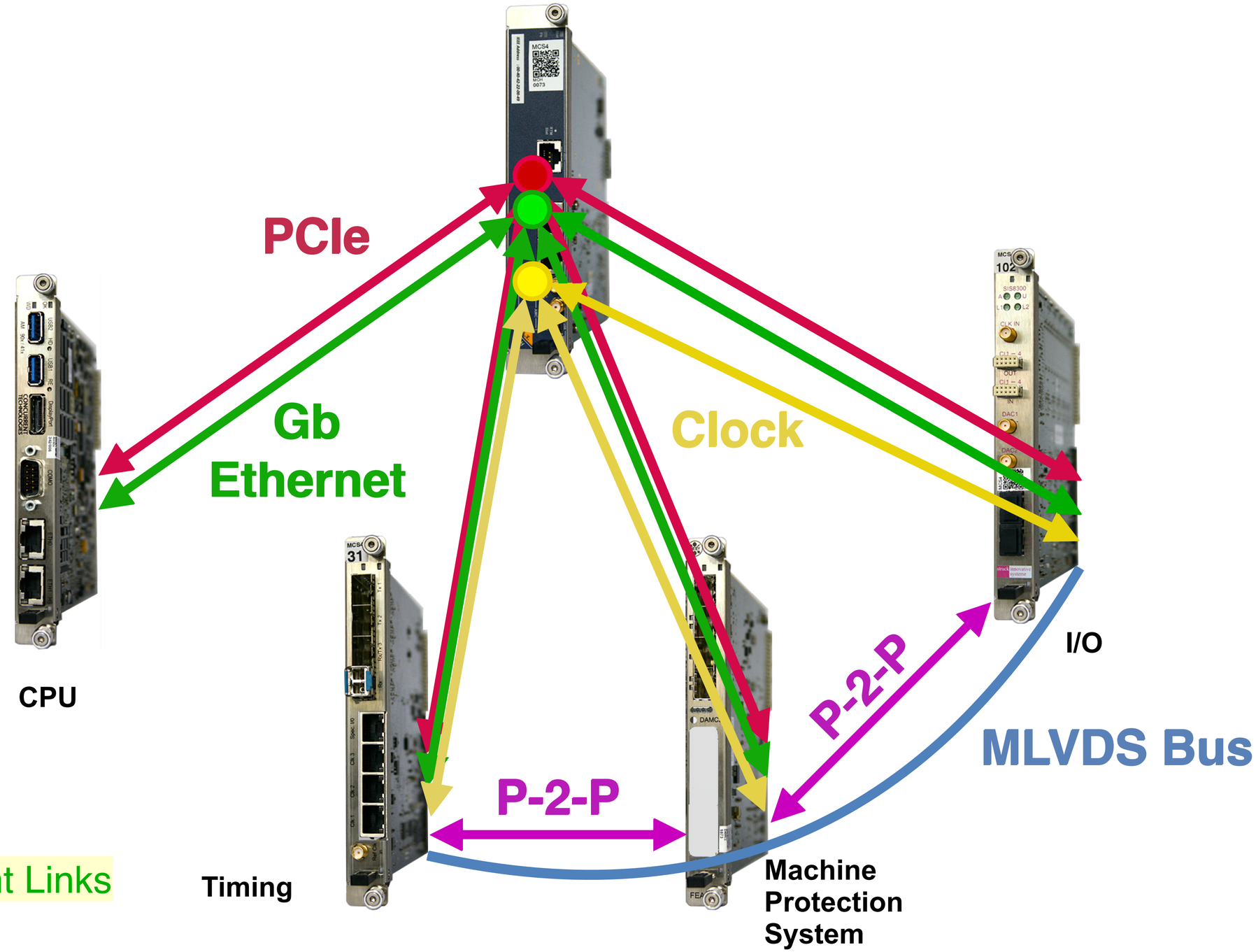
Architecture : PCIe with Hot-Swap



PICMG Hot-Swap Design Guide:
https://www.picmg.org/openstandards/microtca/mtca-4-pci-express-hot-plug-design-guide/

Driver etc.:
https://github.com/MicroTCA

MicroTCA.4 Communication Links



+ IPMI Management Links