struck innovative systeme

Fast Digitizers and Digital I/O Modules in MTCA and Applications

Dr. Matthias Kirsch

Outline

Digitizers
Mid Speed High Resolution (125/250 MSPS 16-bit)
Data Streaming
LLRF
BPM
High Speed High Resolution (2.5 GSPS 14-bit)
FCT
Picoammeter Spin off (1MSPS 20-bit)

Digital I/O
SIS8864 I/O
SIS8800 Multi Purpose Scaler

SIS8300-KU
10 channel 125 MSPS 16-bit digitizer
(250 MSPS 14-bit stuffing option)

History

Virtex 5 based

2010 SIS8300 initial development, first MTCA.4 board worldwide
2011 SIS8300 V2 > 370 units in field (in part 8 channel 250 MSPS 14-bit BPM)

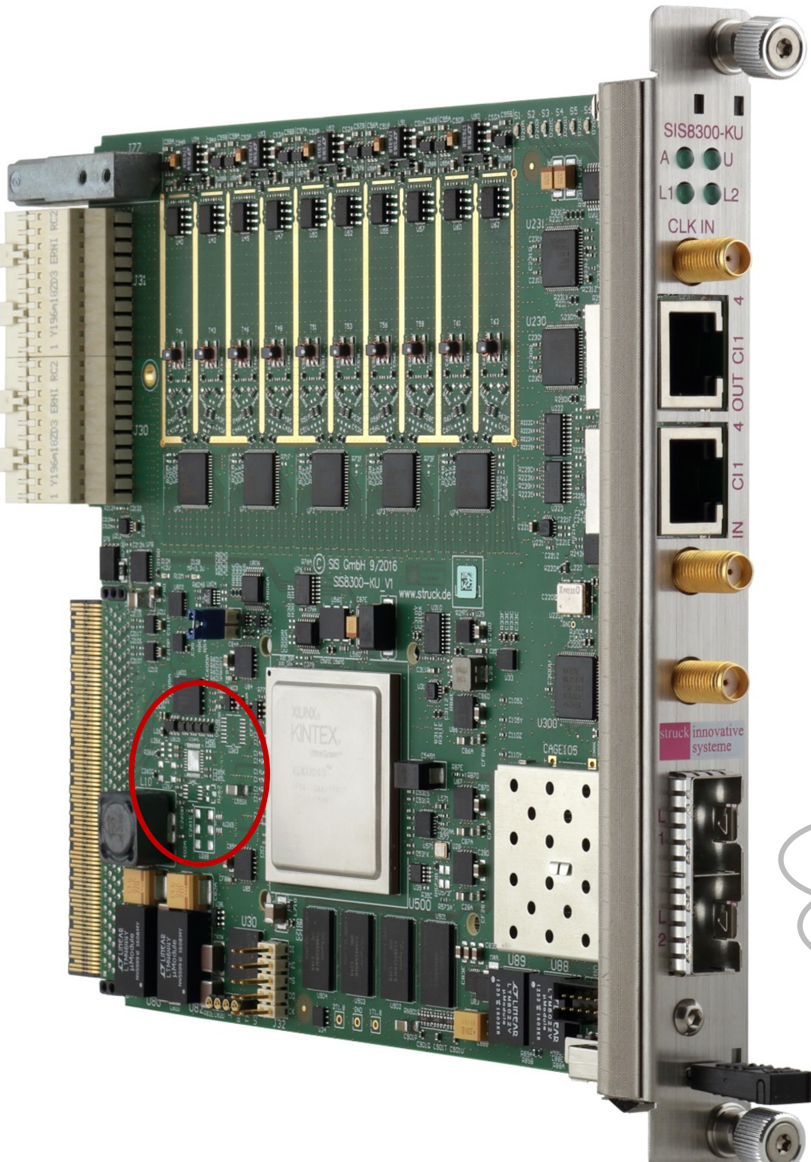
Virtex 6 based

2014 SIS8300-L > 150 units in field
2015 SIS8300-L2x > 930 units in field (L2S, L2D,…)

SIS8300-KU Properties

- 10 Channels 125 MS/s 16-bit or 250 MS/s 14-bit ADC
- 10 MS/s to 125 MS/s Per Channel Sampling Speed
- AC or DC Input Stage
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit 250 MS/s DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Multi Gigabit Link Port Implementation to Backplane
- Twin SFP+ Card Cage for High Speed System Interconnects
- White Rabbit Clock Option for SFP+ Ports
- Two RJ45 Connectors (One Clock + 3 Data or 4 Data In/Out)
- XCKU040-1FFVA1156C Kintex Ultrascale FPGA
- 2 GByte DDR4 Memory (flexible partitioning scheme)
- 4 lane PCI Express Gen3 Connectivity
- Dual boot
- MMC1.0 under DESY license LV91
- In Field Firmware Upgrade Support
- Vivado Project for Custom Firmware Development
- Zone 3 class A1.0, A1.0C or A1.1CO Compatible

SIS8300-KU White Rabbit (WR) Ready



- PLL Clock Synthesizer
- VCO, VCXO
- DACs for VCO Control
- Additional Power

CERN Kintex Ultrascale
White Rabbit PTP Core
First DESY Techlab Tests

What is WR?
Sub ns synchronisation
Synchronous Ethernet
IEEE 1588 PTP

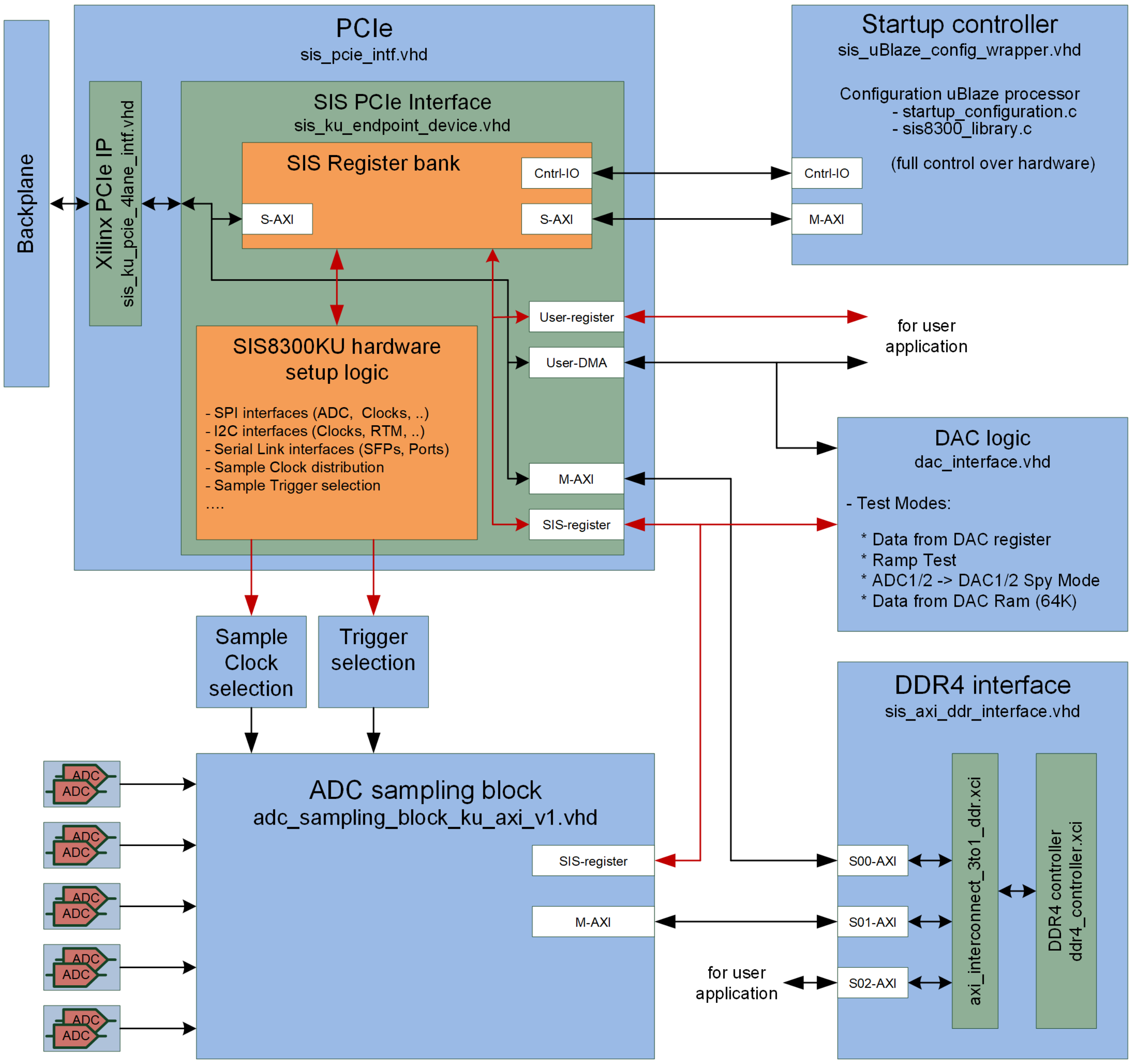
FPGA Resources/Performance

Used FPGA	XC6VLX130T-2FFG1156C (SIS8300-L2)	XCKU040-1FFVA1156C (SIS8300-KU)
System Logic Cells	128 K	500 K
CLB LUTS/Flip-Flops	80/160 K	242/484 K
Block RAM/FIFO w/ECC (36Kb each)	264	600
Block RAM/FIFO (18Kb each)	528	1200
Total Block RAM (Mb)	9.5	21.1
DSP Slices	480	1920
GTH speed	6.6 Gb/s	16.3 Gb/s
PCIe	Gen2	Gen3
Memory Controller	DDR3	DDR4

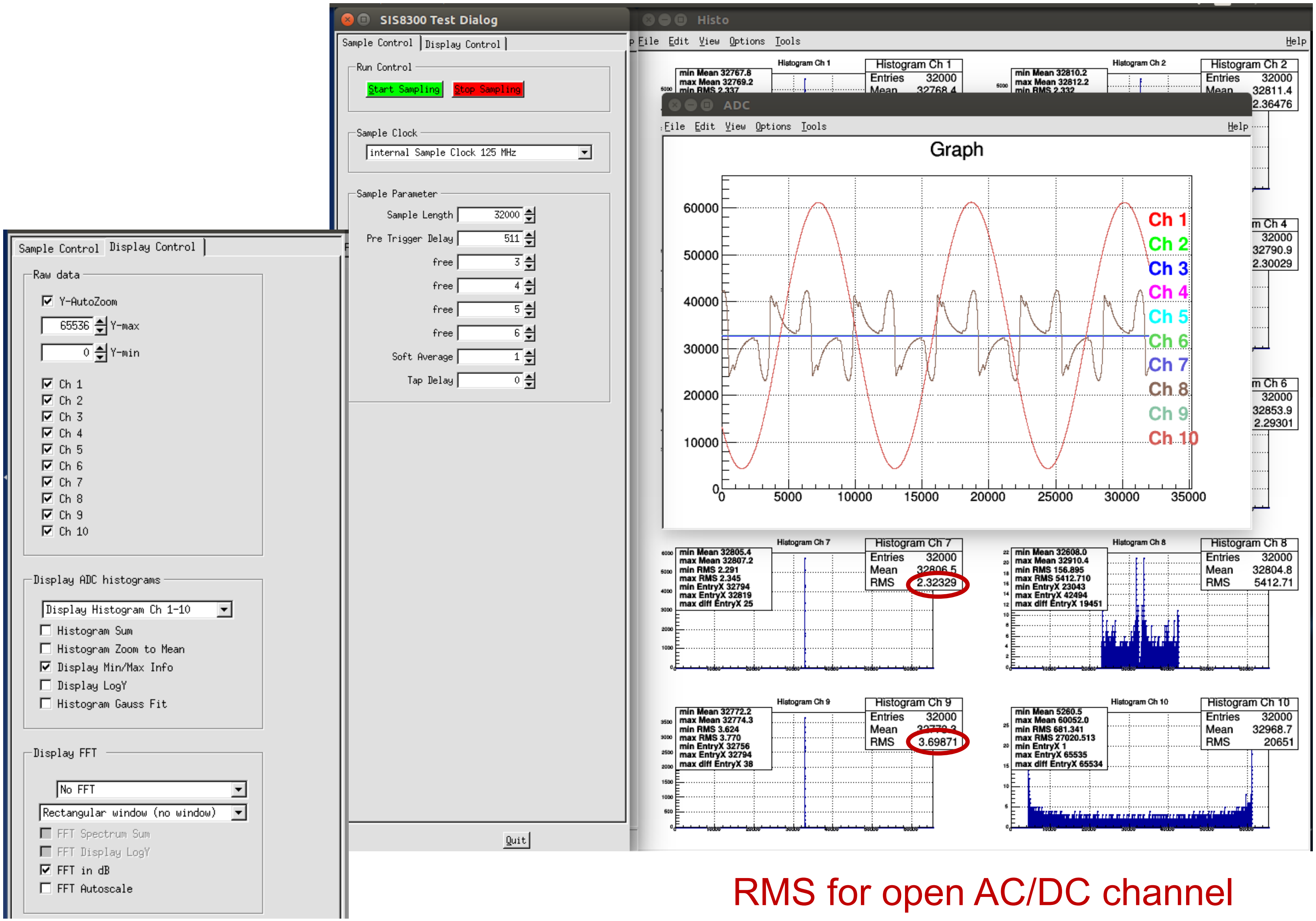
SIS8300-KU
AXI Based VIVADO Project

- Cooperation Lund University/ESS/Struck
- To Meet ESS/ERIC Firmware Specs
- ESS Version → COSYLAB EPICS
- Struck Version available to all users

Struck SIS8300-KU AXI-Based Xilinx FPGA Framework

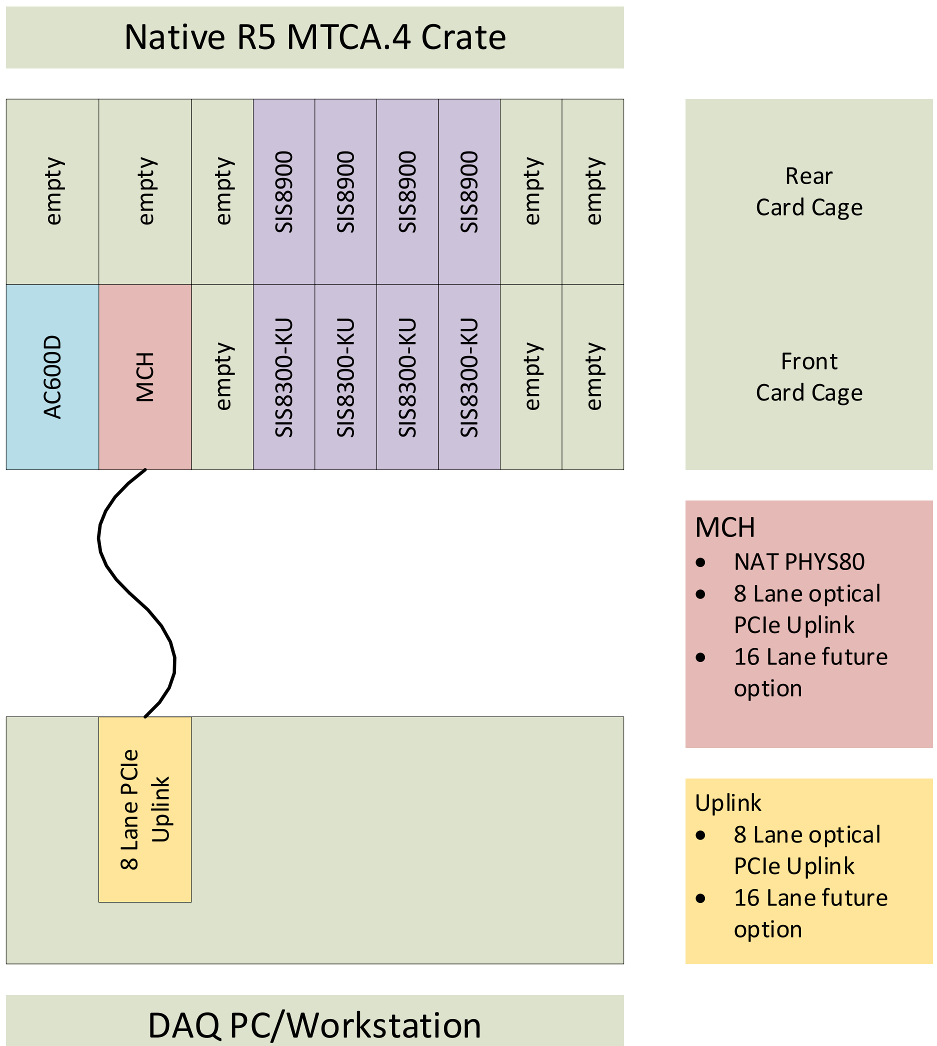


SIS8300-x ROOT GUI
SIS8300-KU 8AC2DC with SIS8900 RTM

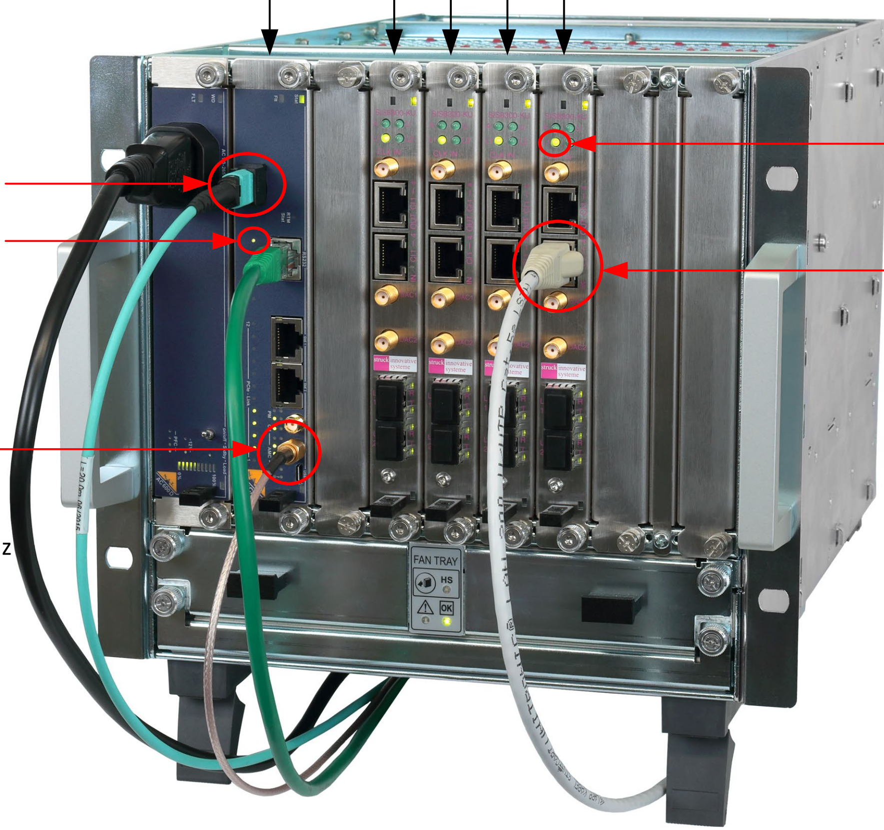


RMS for open AC/DC channel

SIS8300-KU Wendelstein X7 Application
40 Channel Streaming System



SIS8300-KU Application Example
40 Channel Streaming System (Front)

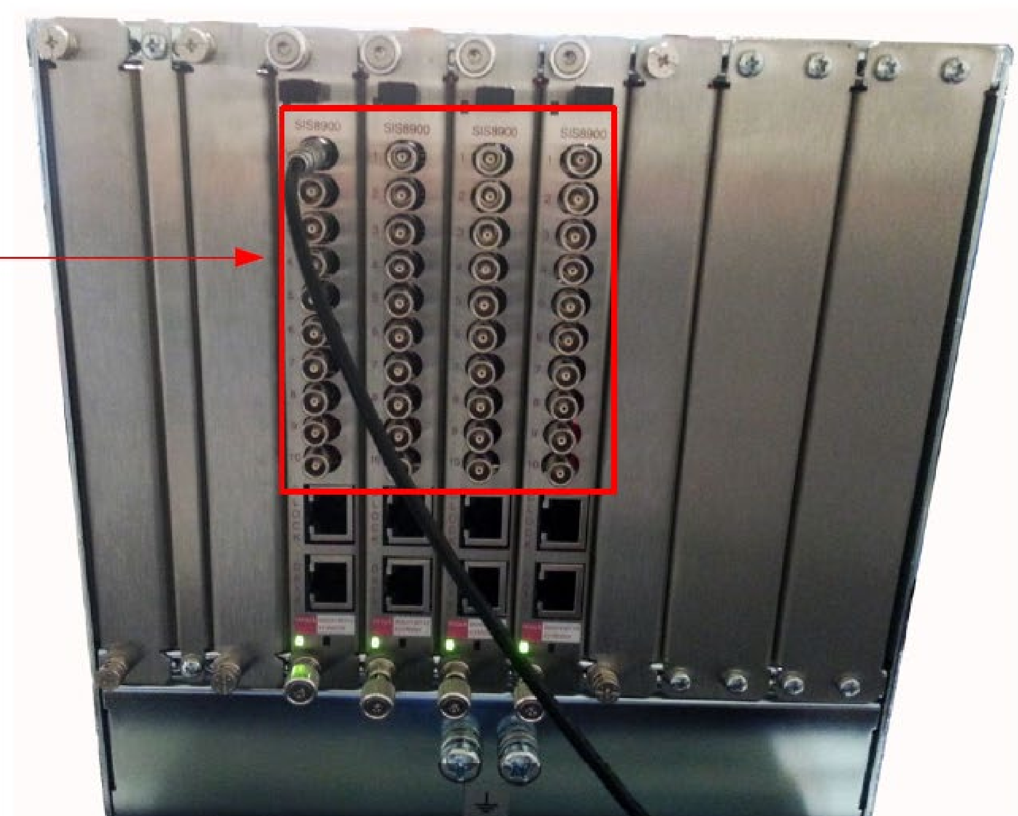


SIS8300-KU System Example
40 Channel Streaming System (Rear)

4 x SIS8900

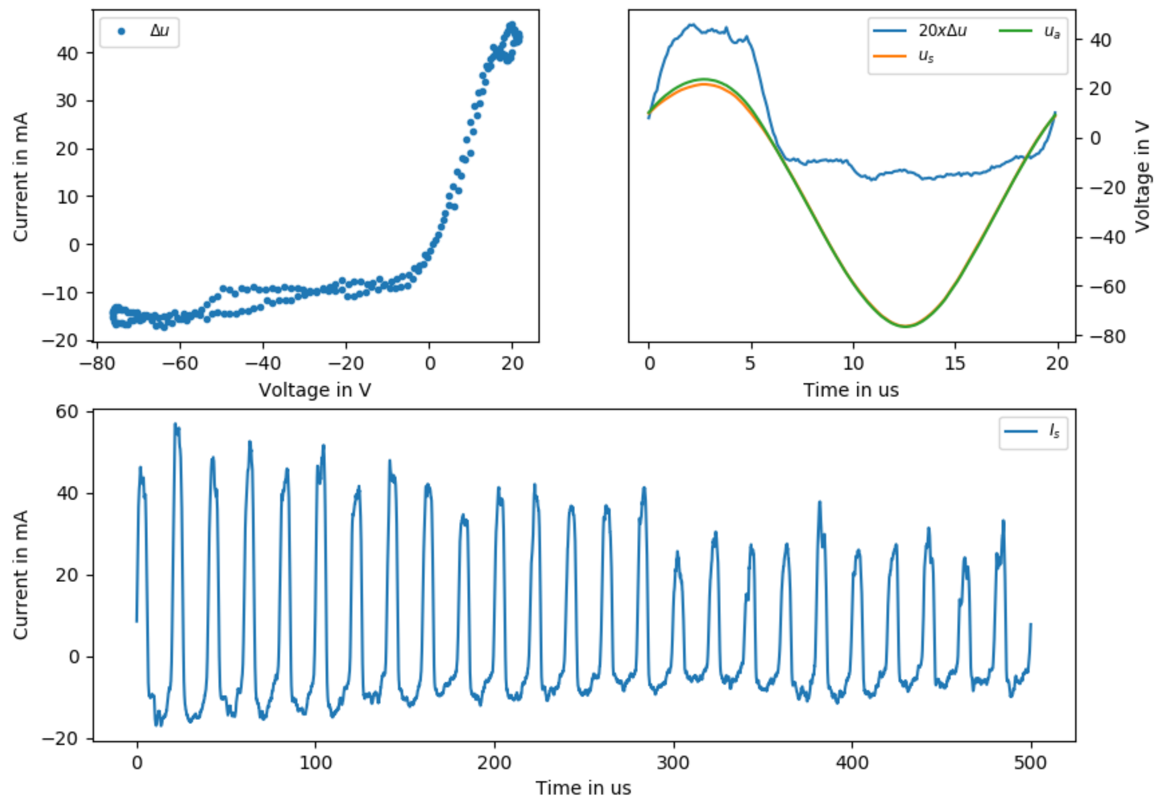
40 channel analog inputs

* DC input stage
* 50 Ohms input impedance
* -1 V to +1V input range



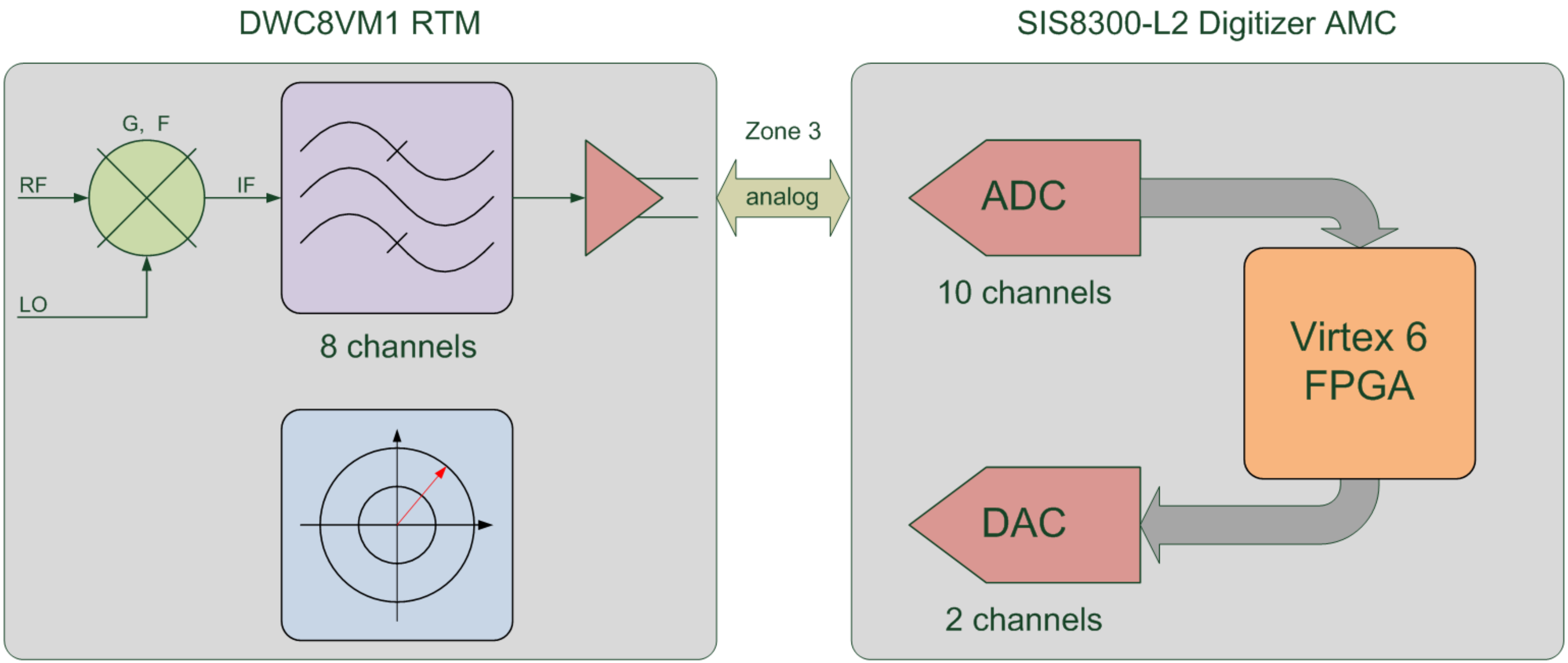
Fast Langmuir Probes on Wendelstein 7-X

- Wendelstein 7-X is a nuclear fusion experiment in Greifswald, Germany at the Max-Planck-Institute for Plasma Physics
- Langmuir probes measure plasma density and temperature
- Fast probes can resolve turbulence
- 40 ADC channels with 16b at 10 MS/s
- Synchronised with ~50 other systems
- In operation for ~500 experiments of up to 100s



Courtesy Lukas Rudischauser, IPP

SIS8300-x/DWC8VM1 as single cavity LLRF solution covering 350 MHz to 6 GHz



Current combination: SIS8300-KU Kintex Ultrascale Digitizer and DWC8VM1

DWC8VM1
8 Channel Downconverter
One Channel Vectormodulator*

Model	f_{min} in MHz	f_{max} in MHz
DWC8VM1LF	350	500
DWC8VM1	500	3500
DWC8VM1HF	3500	6000

DWC8VM1 Overview Table

*under license from DESY

(talks by Jiaoni Bai, Cagil Gümüs)

DWC8VM1 Properties

- MTCA.4 RTM Implementation
- 8 Channels Downconverter
- 350 MHz - 6 GHz (3 different types)
- 8 Channel FBM Multi Coax. Connector (CH1 to CH8)
- 2 Auxilliary Channels
- One Channel Vector Modulator
- VM Output 50 MHz to 6 GHz
- SMA Vector Modulator Output
- Various Intermediate Frequencies
- Switchable Front End Attenuators
- LO Clock From Front Panel or RF Backplane
- LO Power Level Monitor
- Interlock Scheme
- I2C Support
- Zone 3 Class A1.1 compatible

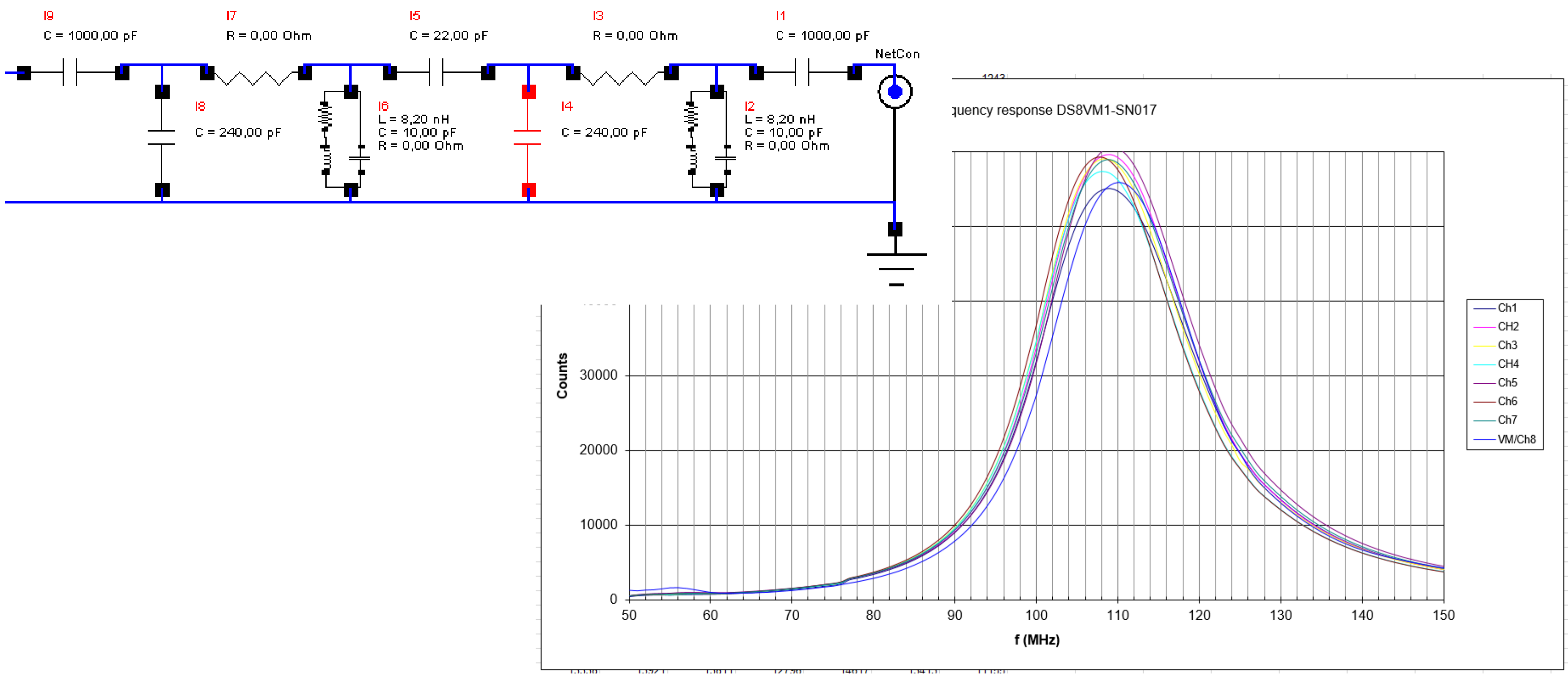
DS8VM1
8 Channel Direct Sampling
One channel vectormodulator*

SIS8300-x/DS8VM1
as single cavity LLRF solution
covering 5 MHz to 700 MHz
Undersampling in some cases

*under license from DESY

(talk by Cagil Gümüs)

DS8VM1 GSI 108 MHz Input Filter and Input Response



Jens Zappai et. al. LLRF2017 P12
A MTCA.4 BASED DIGITAL LLRF SYSTEM FOR THE GSI UNILAC

SIS8300-x BPM Application

PAL FEL

144 Stripline BPMs SIS8300 V2

in 8 channel 250 MSPS configuration

SLAC RTM

56 Cavity BPMs SIS8300-L2/SLAC RTM

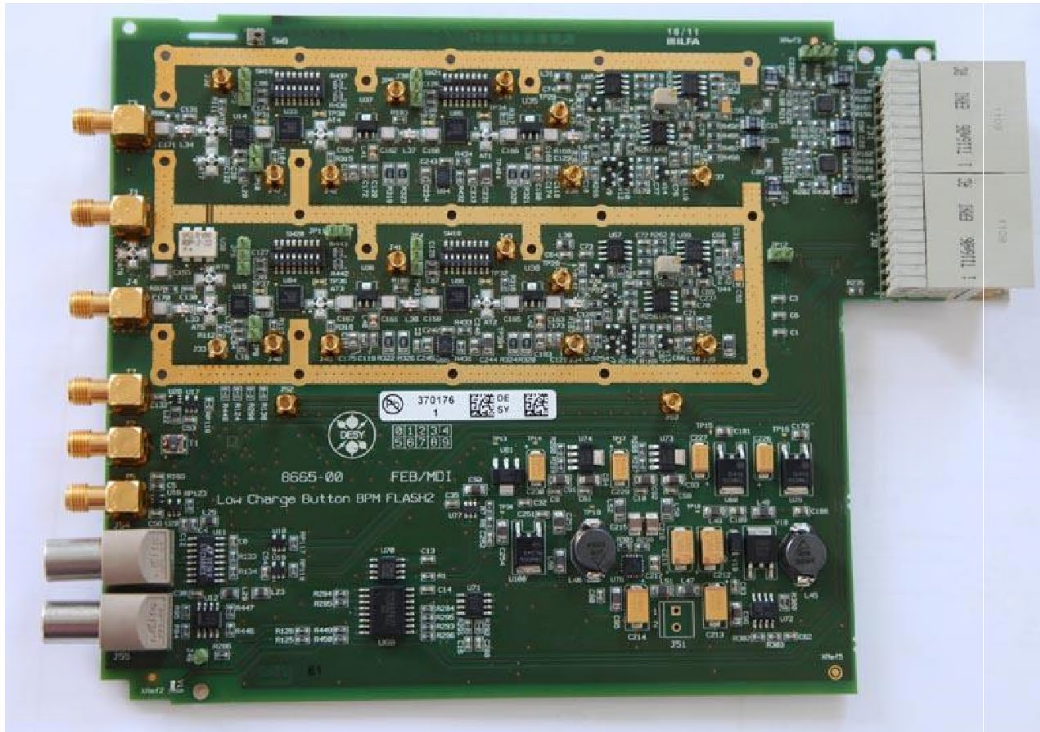
DESY FLASH

SIS8300-L2/DESY Interleaving RTM

ESS

SIS8300-KU/DWC10LF

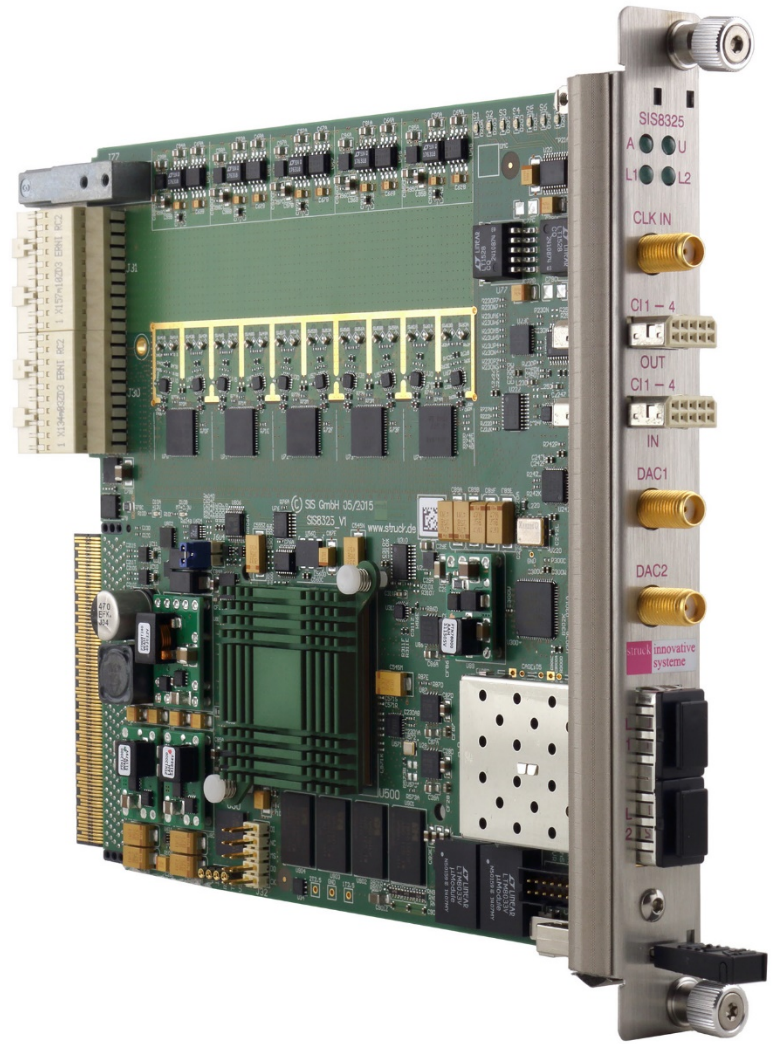
DESY BPM RTM



Interleaved Sampling
50 pC resolution target
Frank Schmidt-Föhre, Bastian Lorbeer

SIS8325 250 MSPS 16-bit Digitizer (Helmholtz Validation fund project)

- MTCA.4
- 4 lane PCI Express Connectivity
- 10 Channels 250 MS/s 16-bit ADC
- 10 MS/s to 250 MS/s Per Channel Sampling Speed
- AC and DC Input Stage
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Gigabit Link Port Implemenation to Backplane
- Twin SFP Card Cage for High Speed System Interconnects
- Virtex 6 FPGA
- One GSample Memory (flexible partitioning scheme)
- In Field Firmware Upgrade Support

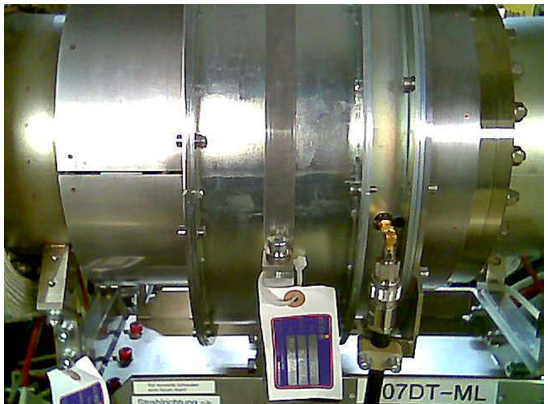


Application FAIR FCT (Fast Current Transformer)

- Test System with SIS3350 500 MSPS 12-bit VME Digitizer
- Development of new MTCA FMC Carrier and 2.5 GSPS 14-bit Digitizer FMC

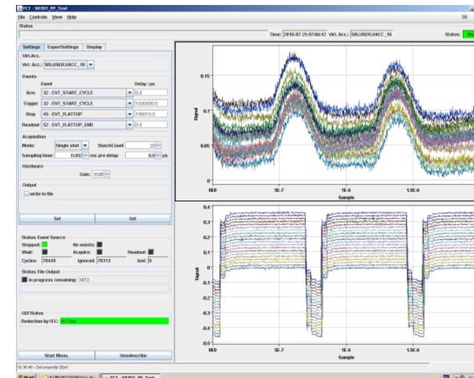
Measurements in the SIS 18. Setup (courtesy GSI)

Detector in SIS tunnel, view 1



Detector in SIS tunnel, view 2

GUI in control room

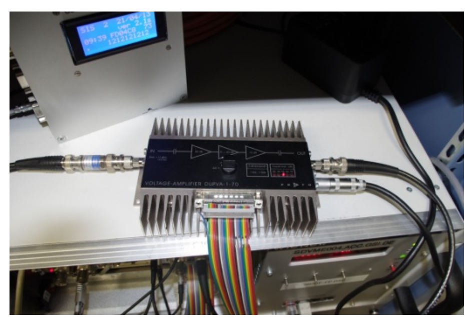


~100m cable

Electronic room

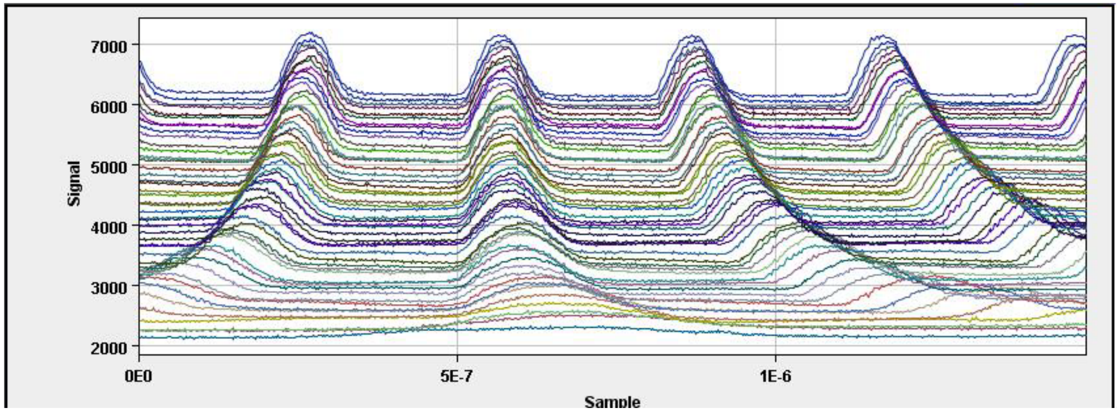
Signal output

Amplifier



VME DAQ

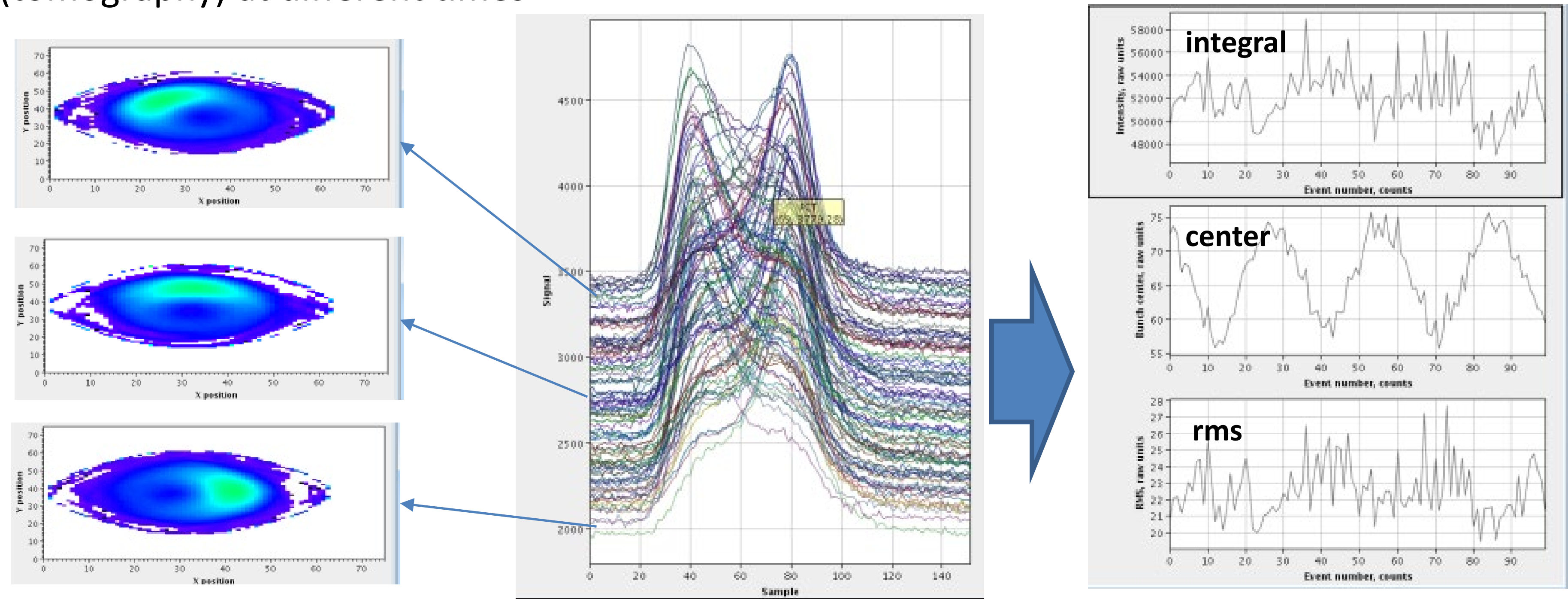
Observation of the signal during different processes
(below is the FCT signal “waterfall” plot measured during frequency ramp)



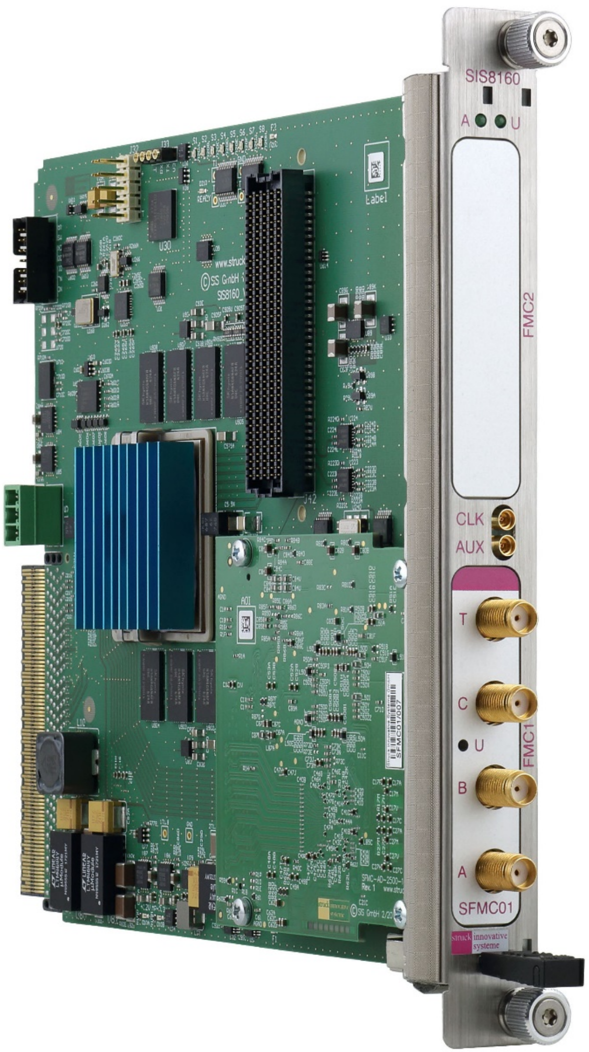
Applications

Bunch phase space reconstruction (tomography) at different times

Observation of the single bunch parameters in time during unstable behavior

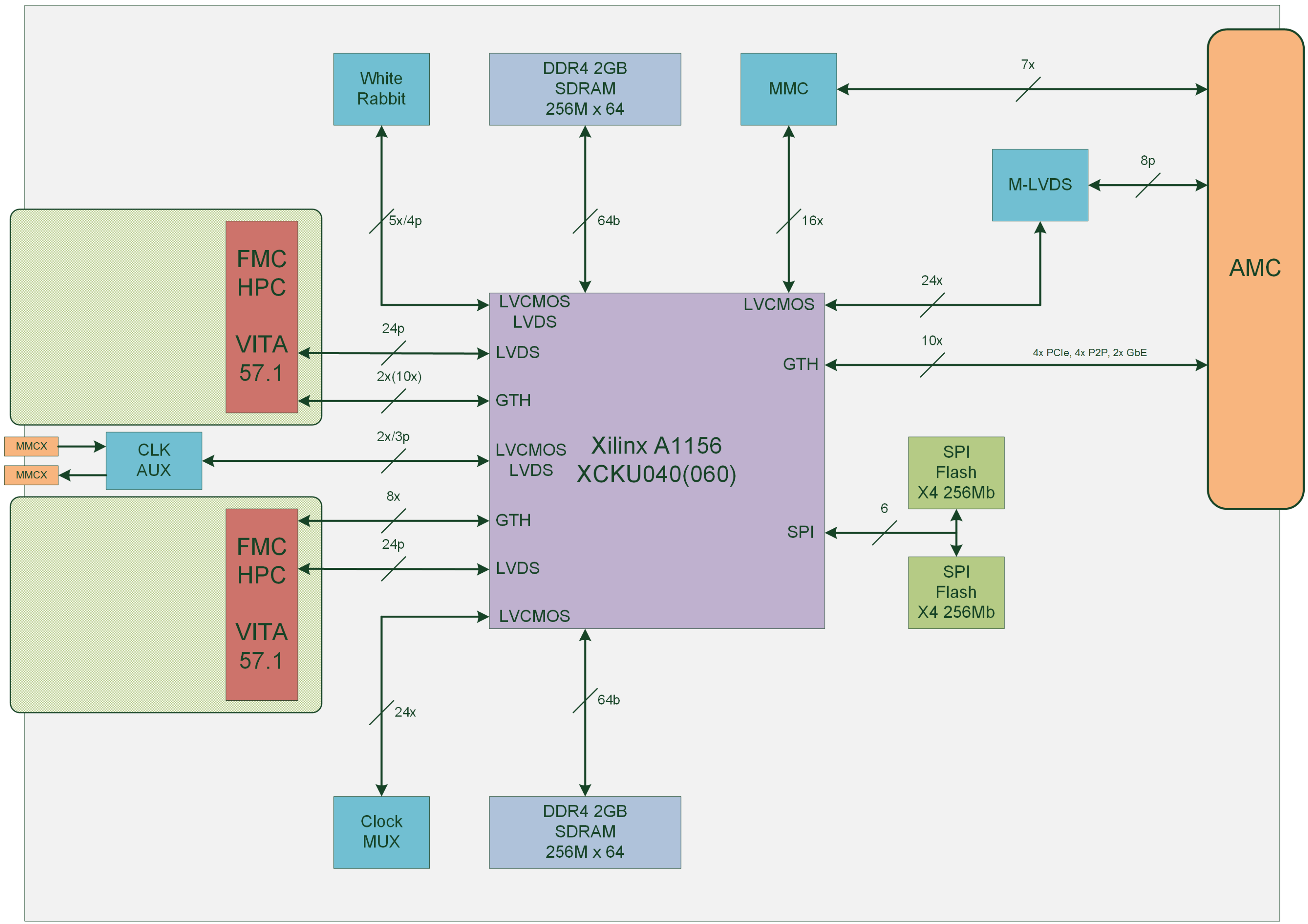


SIS8160 Dual FMC Carrier AMC

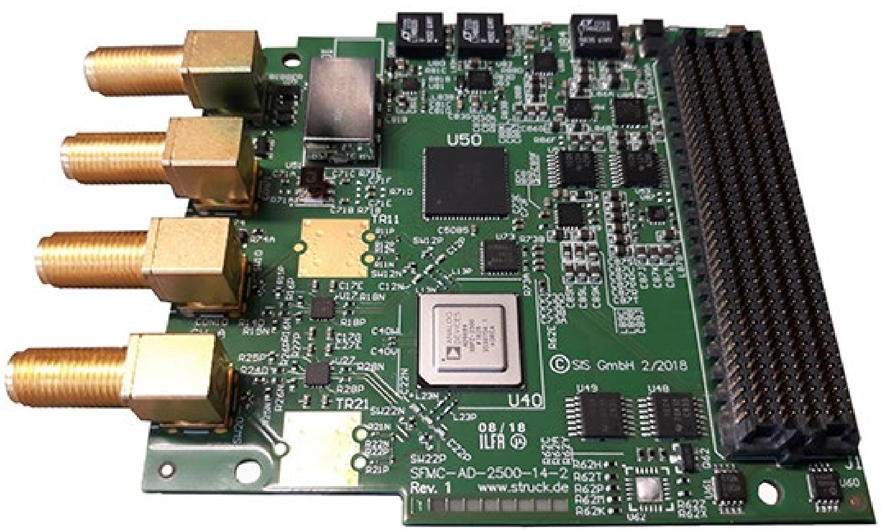


- 4-lane PCI Express Gen3 Connectivity
- Xilinx XCKU40- or XCKU060-1FFVA1156C Kintex Ultrascale FPGA
- Dual Boot
- Front Panel MMCX Clock Input
- Front Panel MMCX Digital In-/Output (HW Configuration)
- Point to Point Links
- 4 MLVDS µTCA Ports (AMC Ports 17-20) → 8 MLVDS lines
- 2 HPC FMC Sites
- Variable FMC VADJ (1,0V - 1,8V)
- Low Jitter Clock Generation and Management
- 2 x 2 GByte DDR4 Memory with two Memory Controllers
- White Rabbit Option (over FMC 2)
- Stand Alone Operation Option
- MMC1.0 under DESY LV91

SIS8160 Block Diagram

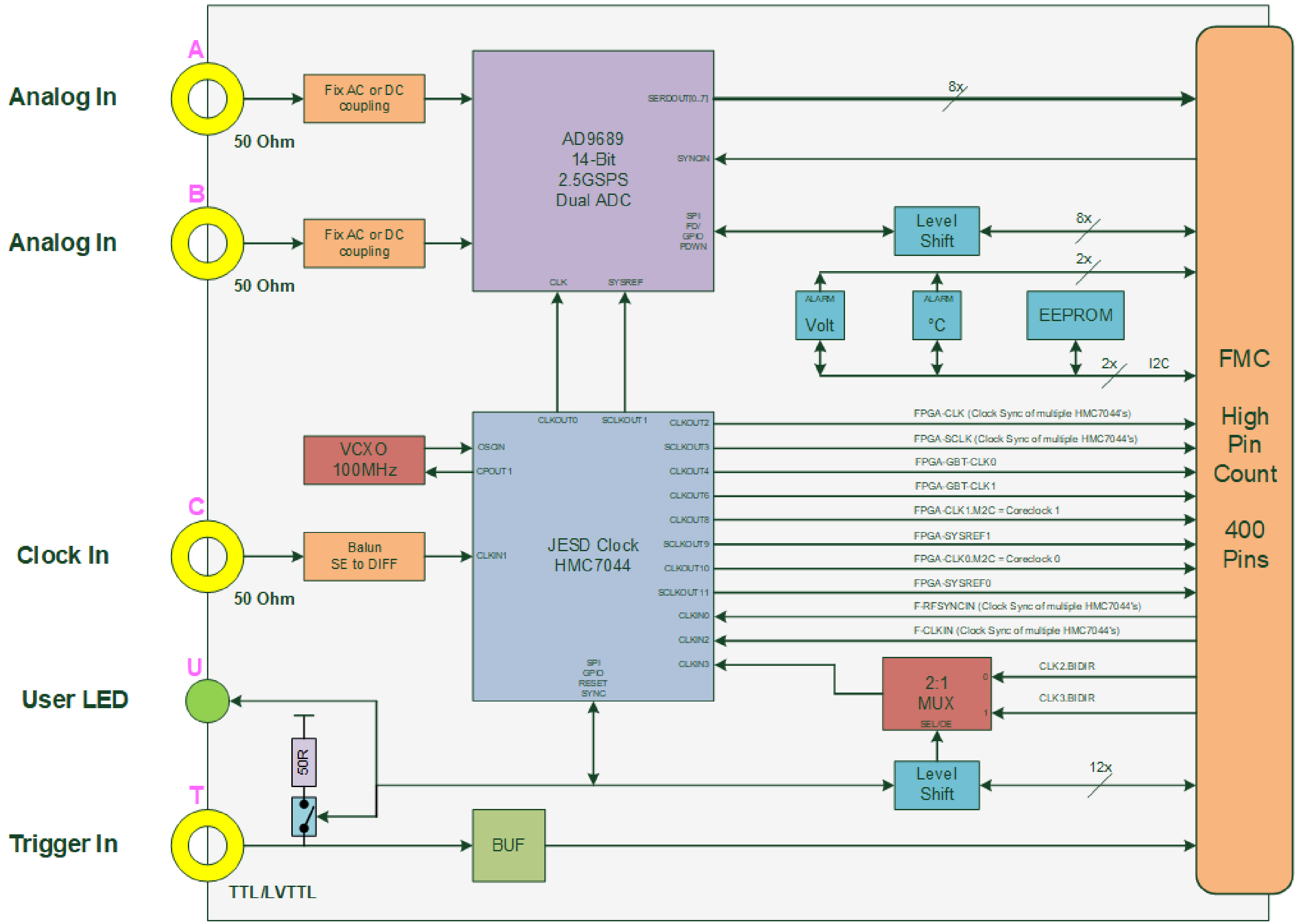


SFMC01
2 Channel 2.5 GSPS 14-Bit

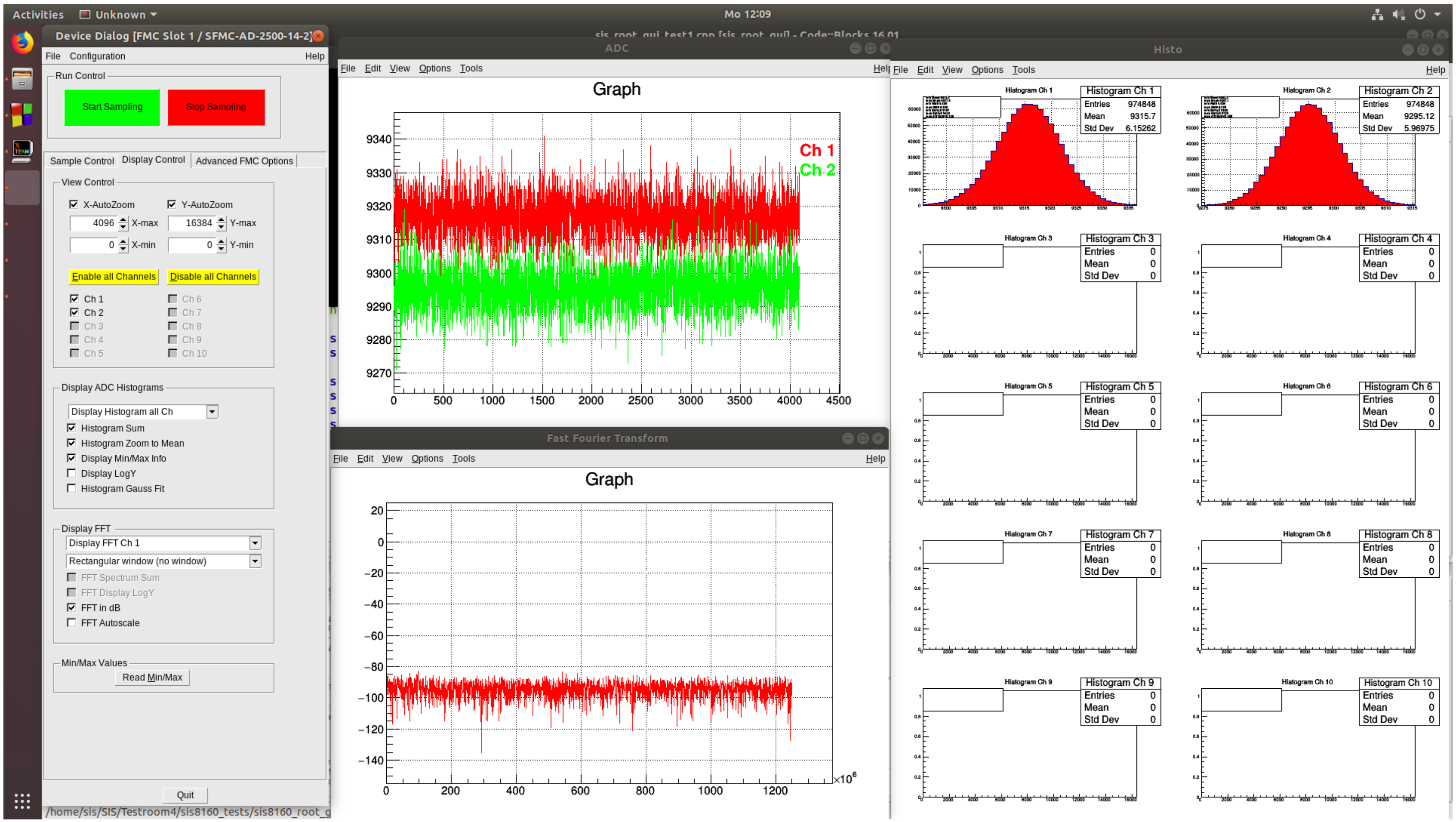


- Single width, 10mm stacking height, air cooled commercial grade HPC FMC Module
- Analog front-end factory configurable for DC- or AC (Balun) input coupling
- Up to 5 GHz AC Analog BW
- Up to 1 GHz DC Analog BW
- Dual channel 14-Bit, 2.5 GSPS with JESD204B Interface
- 50 Ohm Input Termination
- 4 Front panel SMA Inputs for Analog A/B, Clock and Trigger
- Ultra low phase noise 100 MHz on board clock source
- High performance jitter attenuating frequency generator for JESD204B
- one green Front panel user LED
- System management EEPROM and Temperature Sensor with Thermal Watchdog

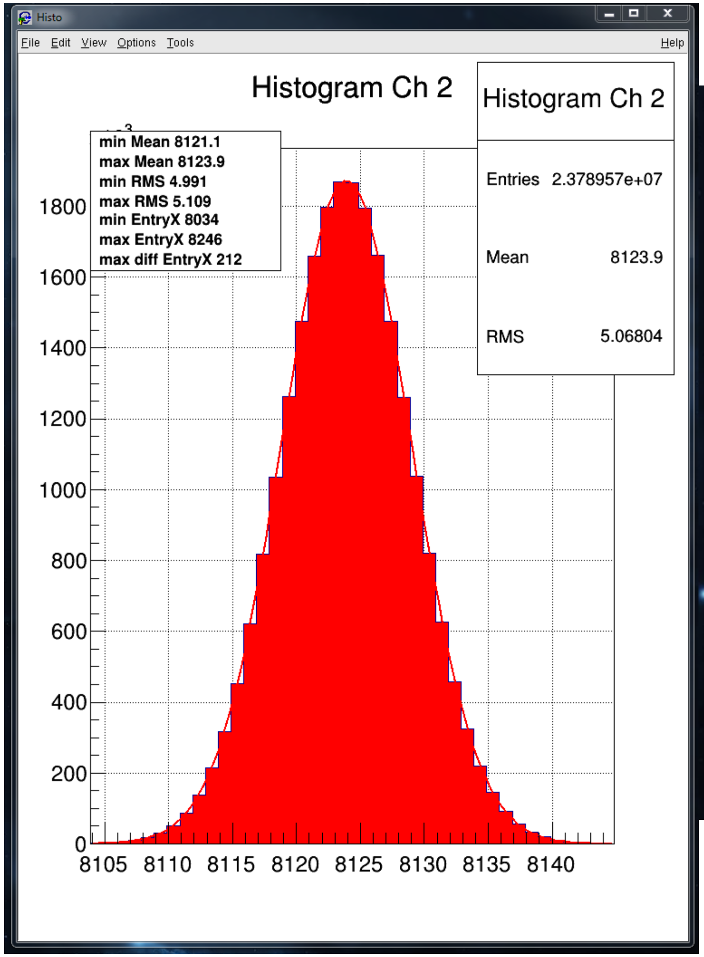
SFMC01
2 Channel 2.5 GSPS 14-Bit

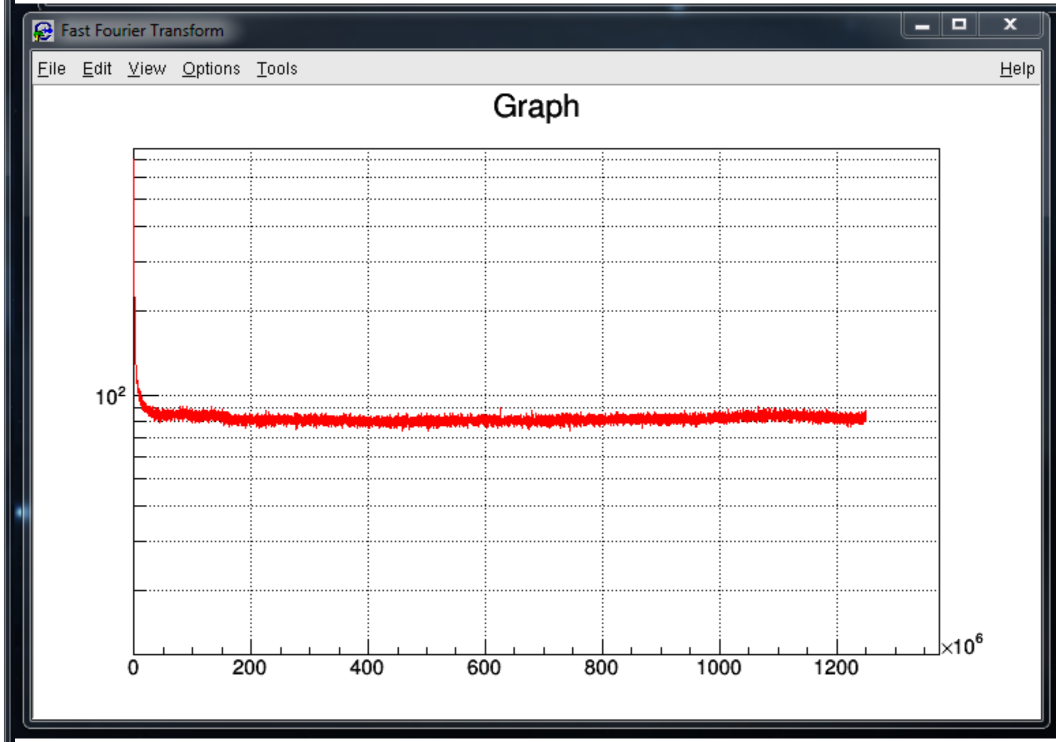


SIS8160/SFMC01 RROT GUI DC Configuration 1 GHz BW

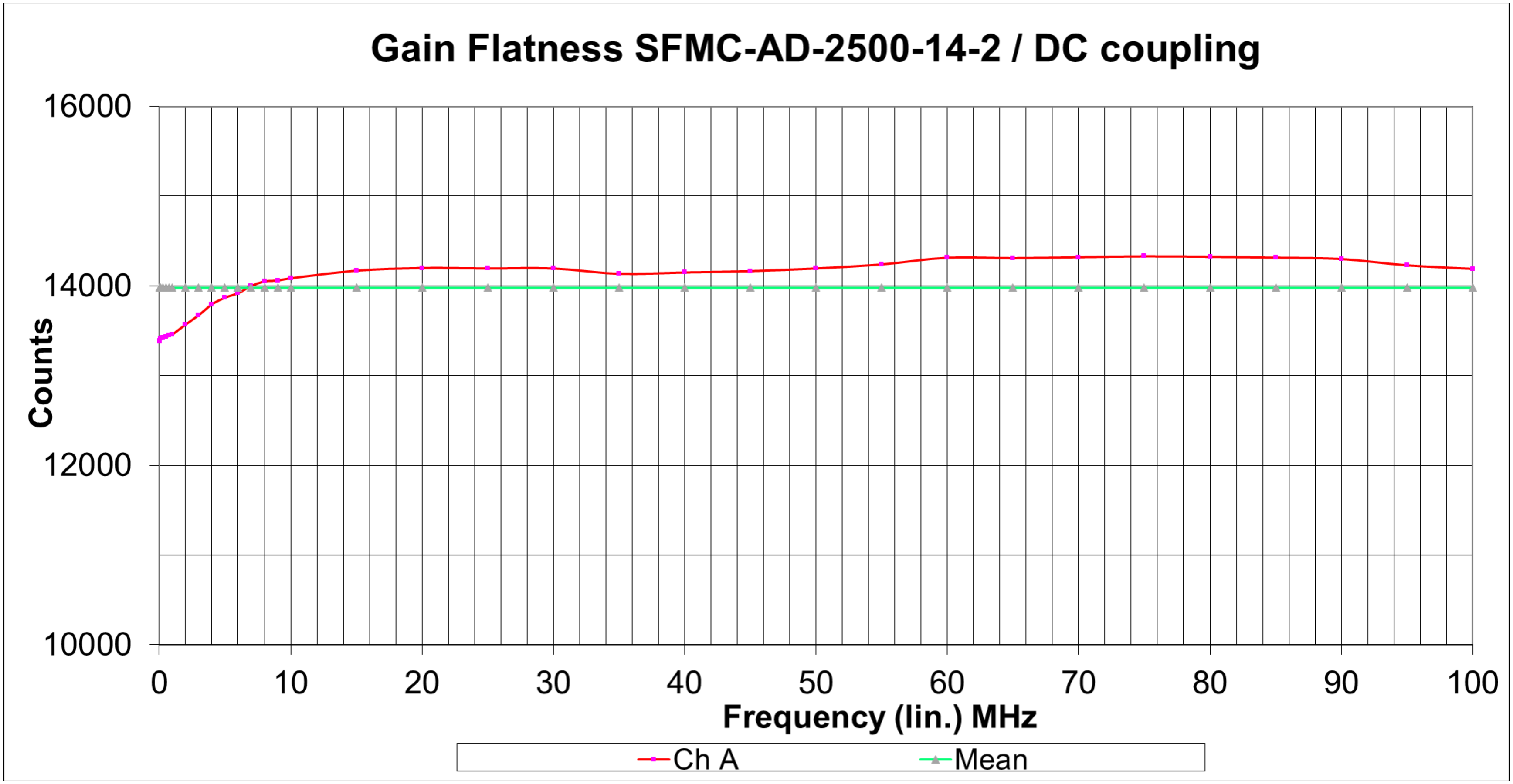


SFMC01 AC 5 GHz BW Open Input





SFMC01 Gain Flatness request: +/- 0,5 dB 0-100 MHz



Possible next FMC JESD Developments

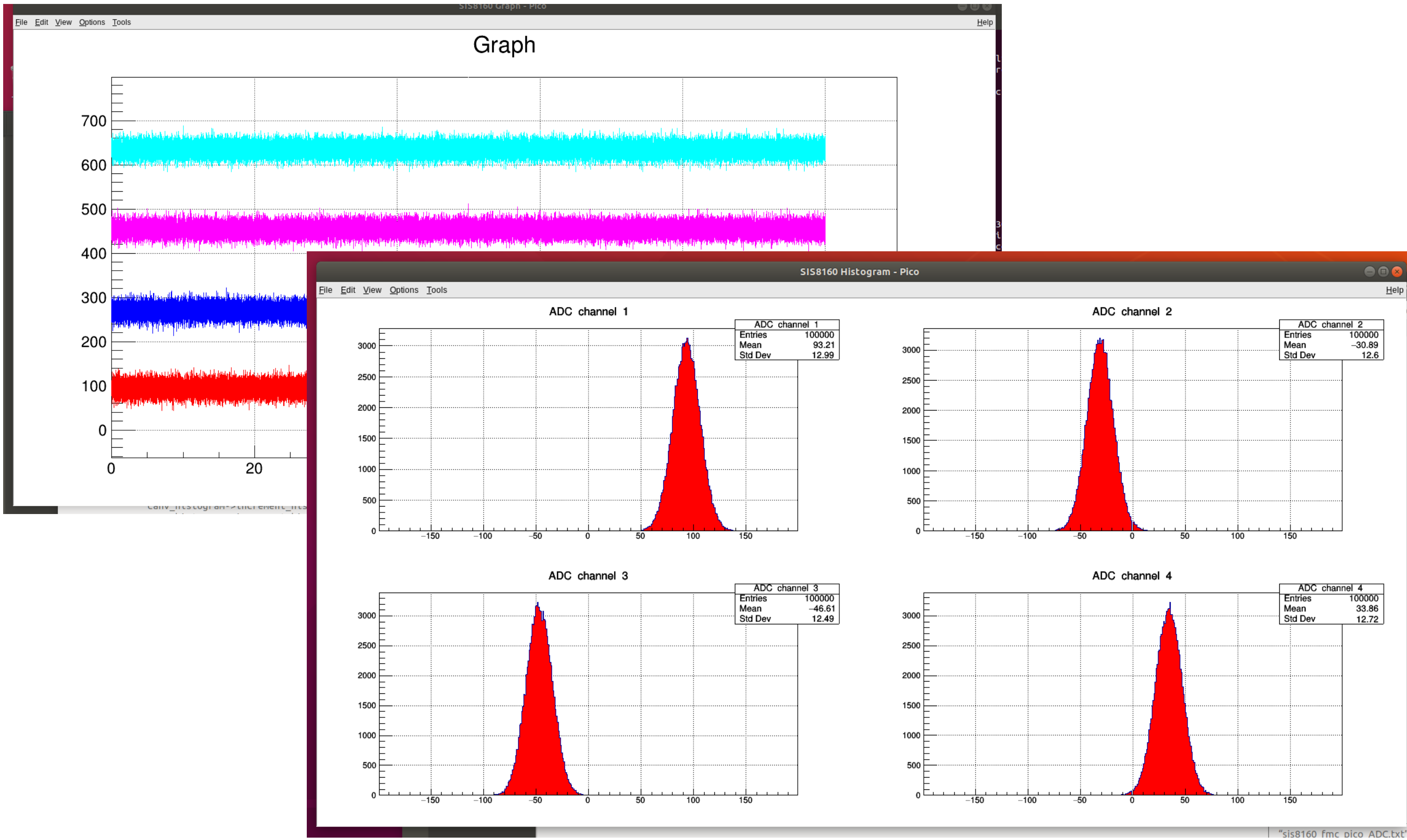
- 4 Channel GSPS 16-bit Digitizer
- 8 Channel 500 MSPS 14-bit Digitizer
- Project Driven …
- ADC/DAC Combination …

SIS8160 Application
CAENELS FMC-Pico-1M4(-C3)

- 4 Channel Pico Ammeter
- 20-Bit 1 MSPS (BW 10/C3 300 KHz)
- RNG0: ± 1 mA, RNG1: ± 1 µA
- C3: RNG0: ± 10 mA, RNG1: ± 500 µA
- BPM, SR Beamline,…
- SIS8300-KU like FW framework
- Vivado upgrade path to older carrier HW

Picture courtesy CAENELS

SIS8160/FMC Pico Noise Distribution (reminder 20-bit)



SIS8864 64 channel LVTTL Digital I/O AMC

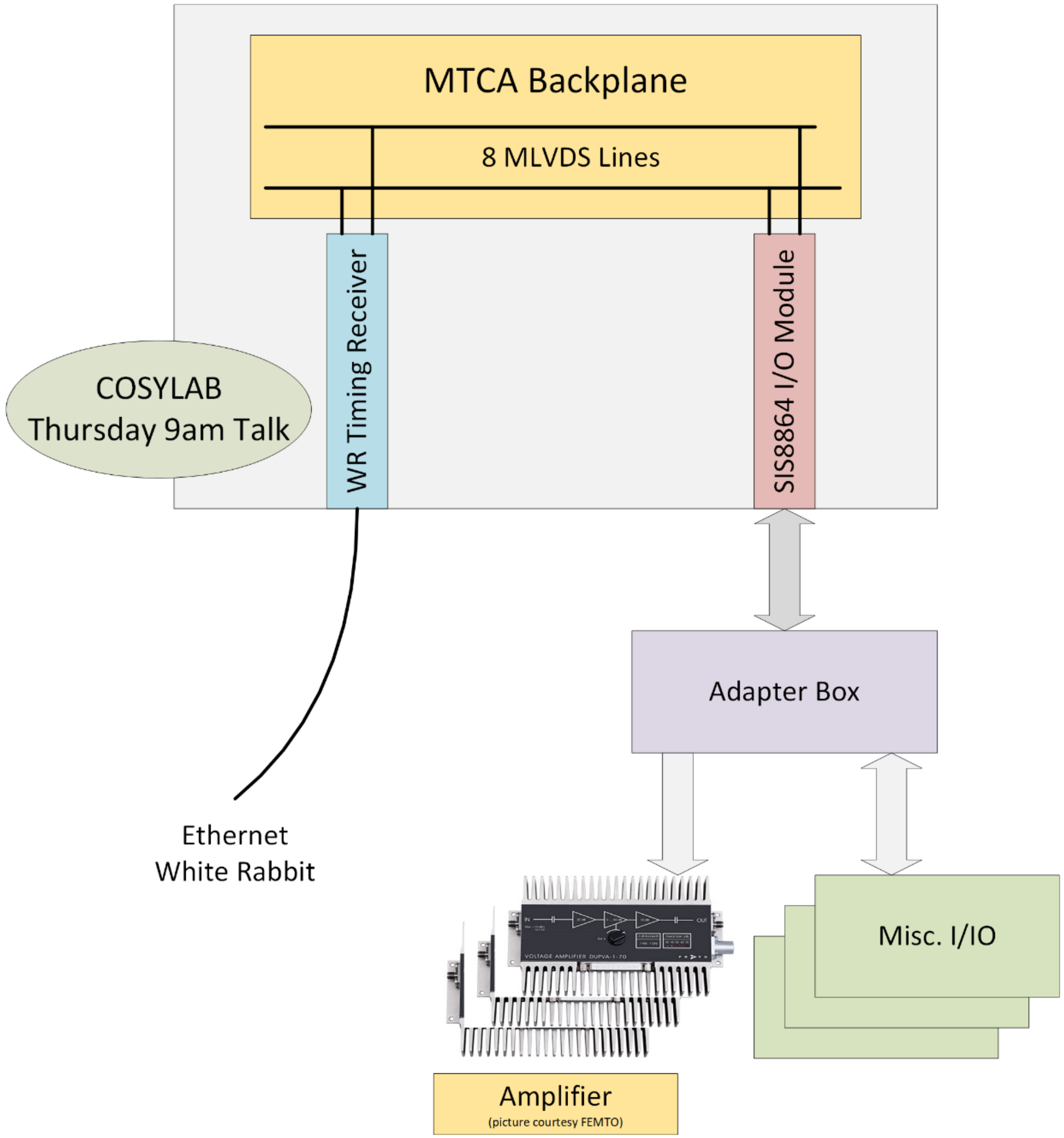
- Machine cycle dependent & generic ouput pattern with digital input
- Alternative to OHWR FMC carrier and two I/O FMC's
- Ready to run firmware
- Application specific firmware adaptations

SIS8864 64 channel LVTTL Digital I/O AMC Properties

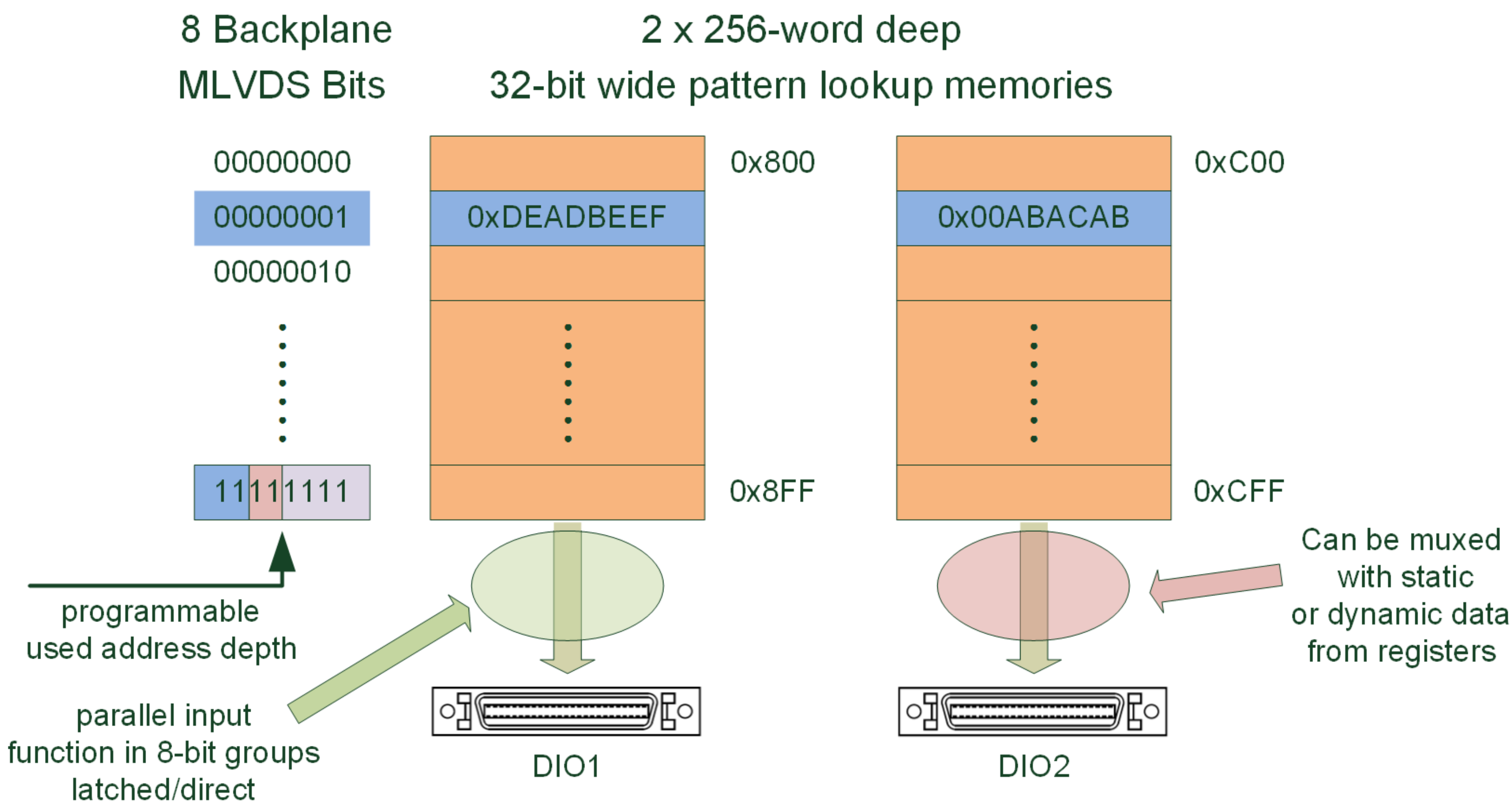
- AMC with Double Width Mid-Size form factor
- Xilinx XC7A15T-2FGG484C Artix-7 FPGA
- Single lane PCI Express Gen2 Interface
- 1 AMC Port GbE
- 2 AMC Ports Point-to-Point Serial Link
- 4 AMC Ports MLVDS (8 MLVDS lines)
- 2 Front panel 32 data I/O: Mini D Ribbon (MDR) (TTL/LVTTL)
- I/O direction programmable in 8-Bit Groups
- 1 Front panel control Input: LEMO (TTL/LVTTL)
- 1 Front panel control Output: LEMO (LVTTL)
- In field firmware upgrade capability
- Module Management Controller ATxmega128A1U, IPMB-L interface
- DESY MMC1.0 (under LV 91)

Status: 2nd batch in production

Typical FAIR SIS8864 Digital I/O Use Case



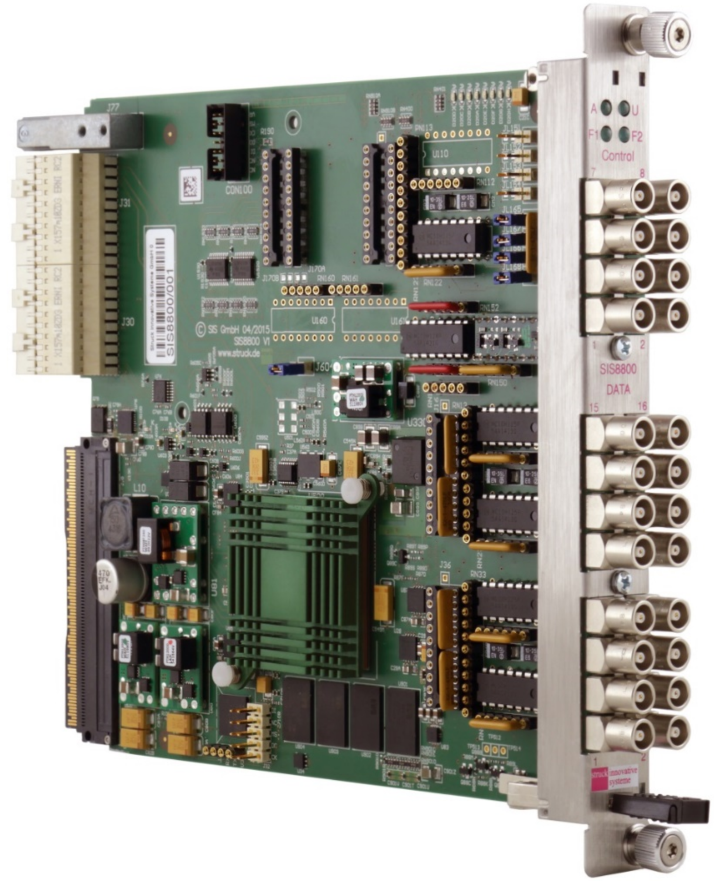
SIS8864 Digital I/O Firmware Detail
Event Receiver/MLVDS → Pattern Memory



SIS8800 Multi Purpose Scaler

Functionality

- MTCA.4 AMC
- 4 Lane PCI Express connectivity
- XC6VLX130T-2FFG1156C Xilinx
- Dual boot
- Redundant PCIe implementation
- 2 GByte DDR3 memory
- 16 front inputs NIM or TTL/LEMO, TTL,ECL or LVDS/flat cable
- 200 MHz count rate (NIM/ECL)
- 4 control in-/4 control front outputs
- Zone 3 Class D1.1 compatible
- MMC 1.0 under DESY license LV91



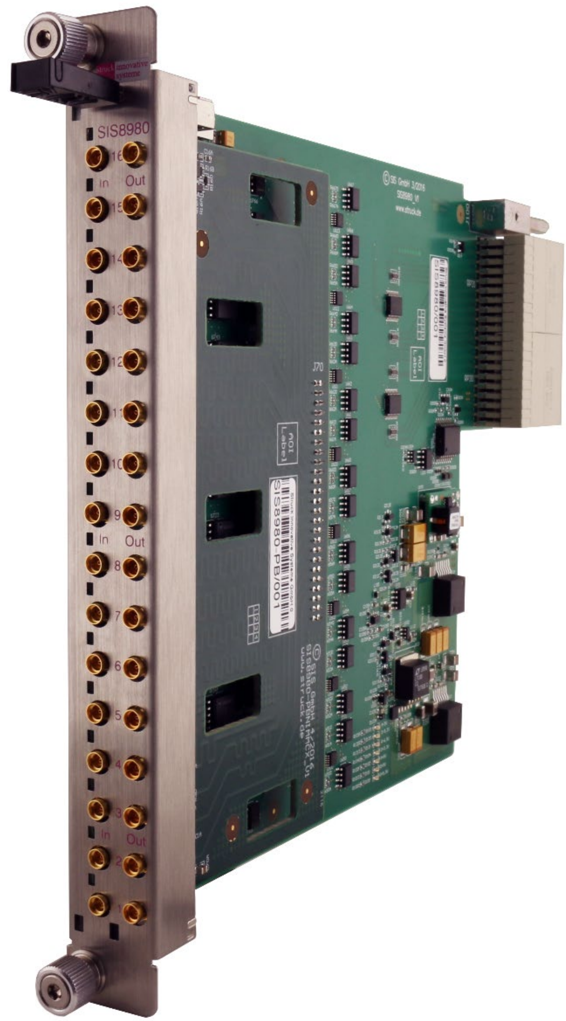
→ good fit for SRI (Synchrotron Radiation Instrumentation) also (talk by Martin Tolkiehn)

SIS8890 Discriminator RTM for SIS8800 Multi Purpose Scaler

Functionality

- MTCA.4 RTM
- 16 Discriminator Inputs, Connector Type MMCX
- Leading Edge
- 50 Ω Input Termination
- 14 Bit Threshold DAC for each Channel, 0.4 mV/Step
- 16 Outputs to Zone 3 (to Scalers on SIS8800)
- 16 Front Outputs, Connector Type MMCX
- Programmable Pulse Width 10 ns -250
- Zone 3 Class D1.1 Compatible
- MMC1.0 Compatible

SIS8980 in NIM/MMCX Configuration



MTCA.4 Relevance, current Struck user base

AU	Australian Synchrotron
BR	LNLS
CH	CERN
CN	IHEP Beijing, SINAP, USTC, IMP
CZ	ELI (Inst of Physics, Praha)
DE	DESY, HZDR, PTB, MPG, KIT, HZB, GSI, DESY Zeuthen, HMI
ES	ESS Bilbao, GMV
FR	ITER, Saclay
GB	Diamond, STFC
IN	TIFR
JP	KEK, SPring-8
KR	PAL
RU	ITER, JINR (Techlab/Bevatech)
SE	ESS, Lund University
TR	TARLA
TW	NSRRC
US	SLAC, NSCL/FRIB, ANL, ORNL

Conclusion

- MTCA(.4) standard widely adopted
- COTS hardware for a variety of applications
- Increasing number of in house designs
- Companies and MTCA Techlab as incubators

Questions/Discussion

partner