Status of Digital Pixel

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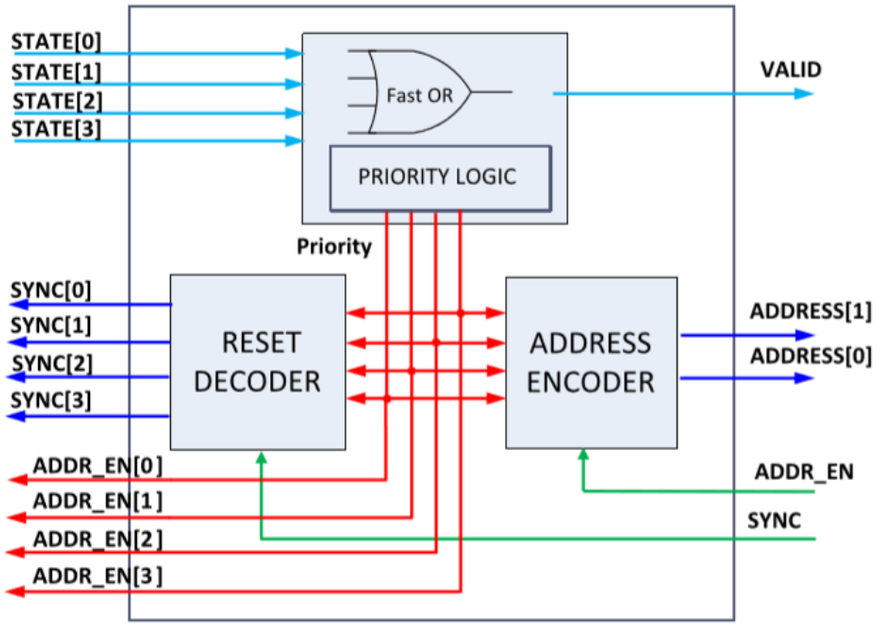
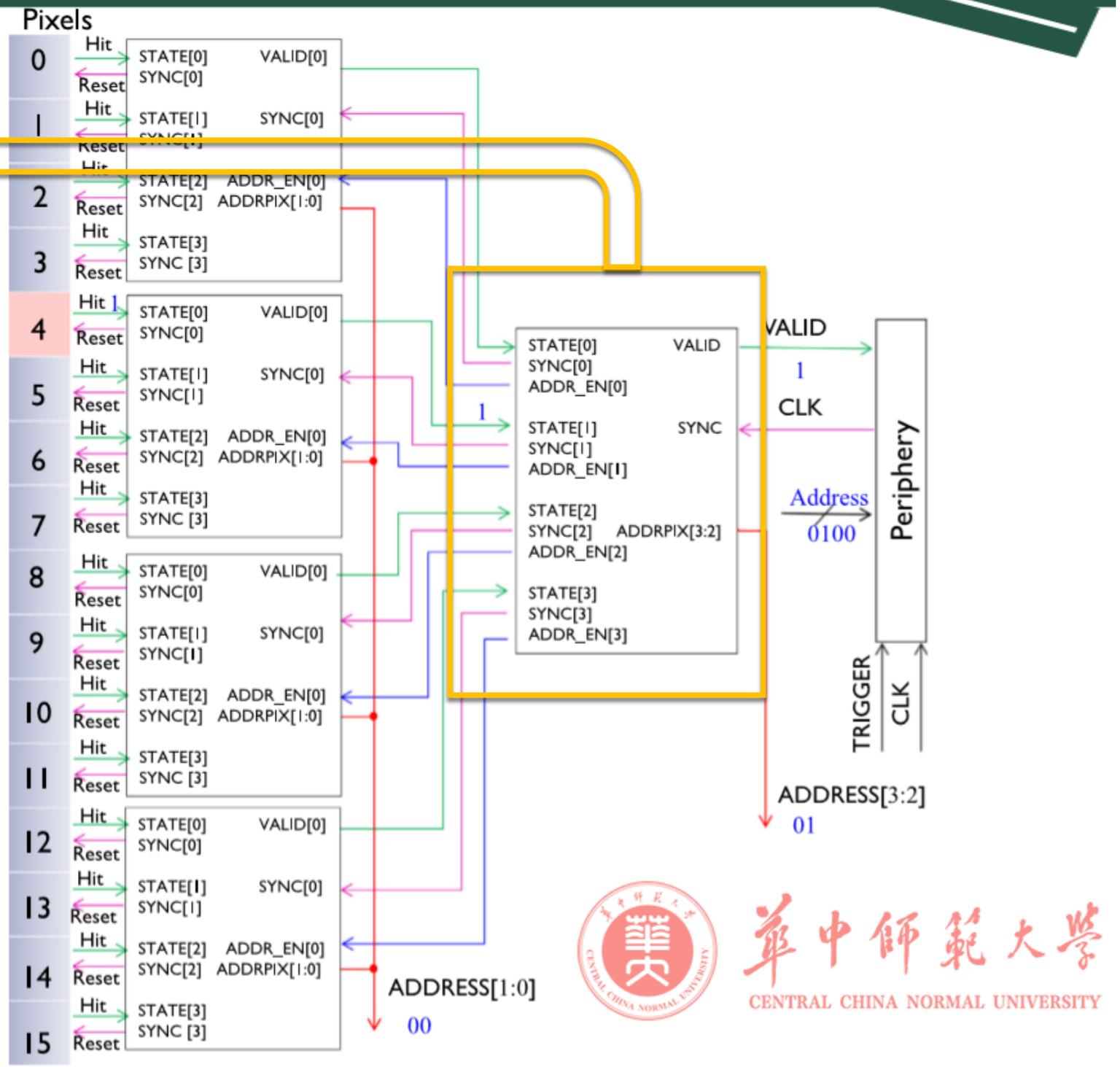
OUTLINE

- Boosting speed AERD block
- Simulation results of the new method
- Simulation results of the other schemes
- Outlook

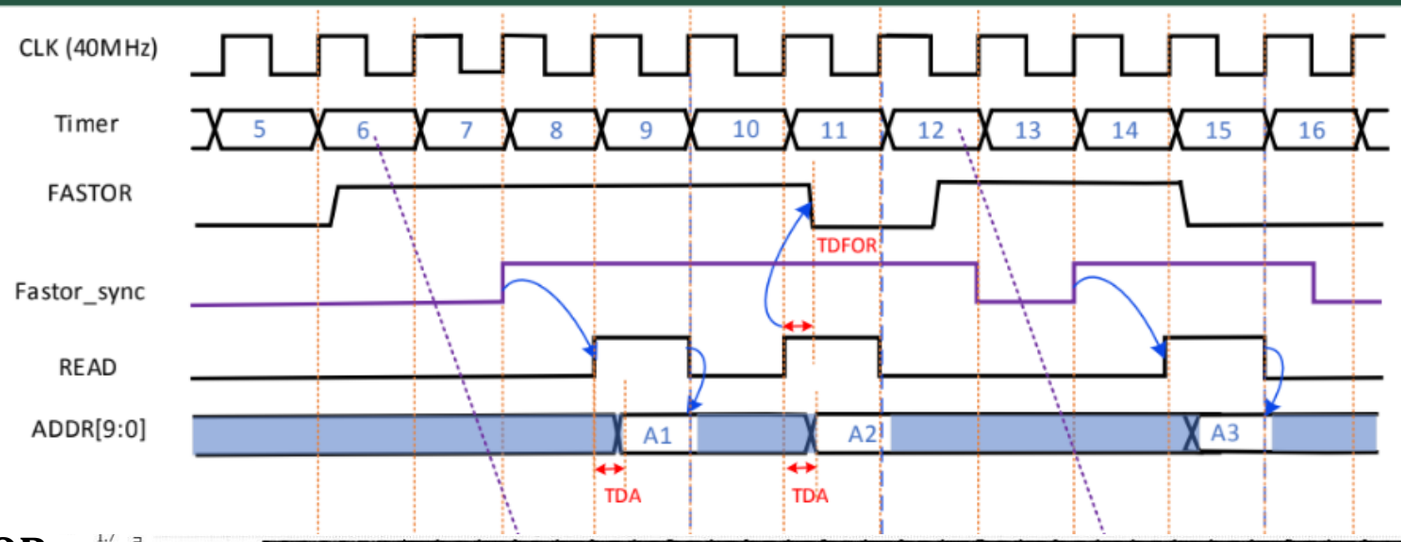
Boosting speed AERD block



The proposed structure of the basic AERD block to boost the speed.

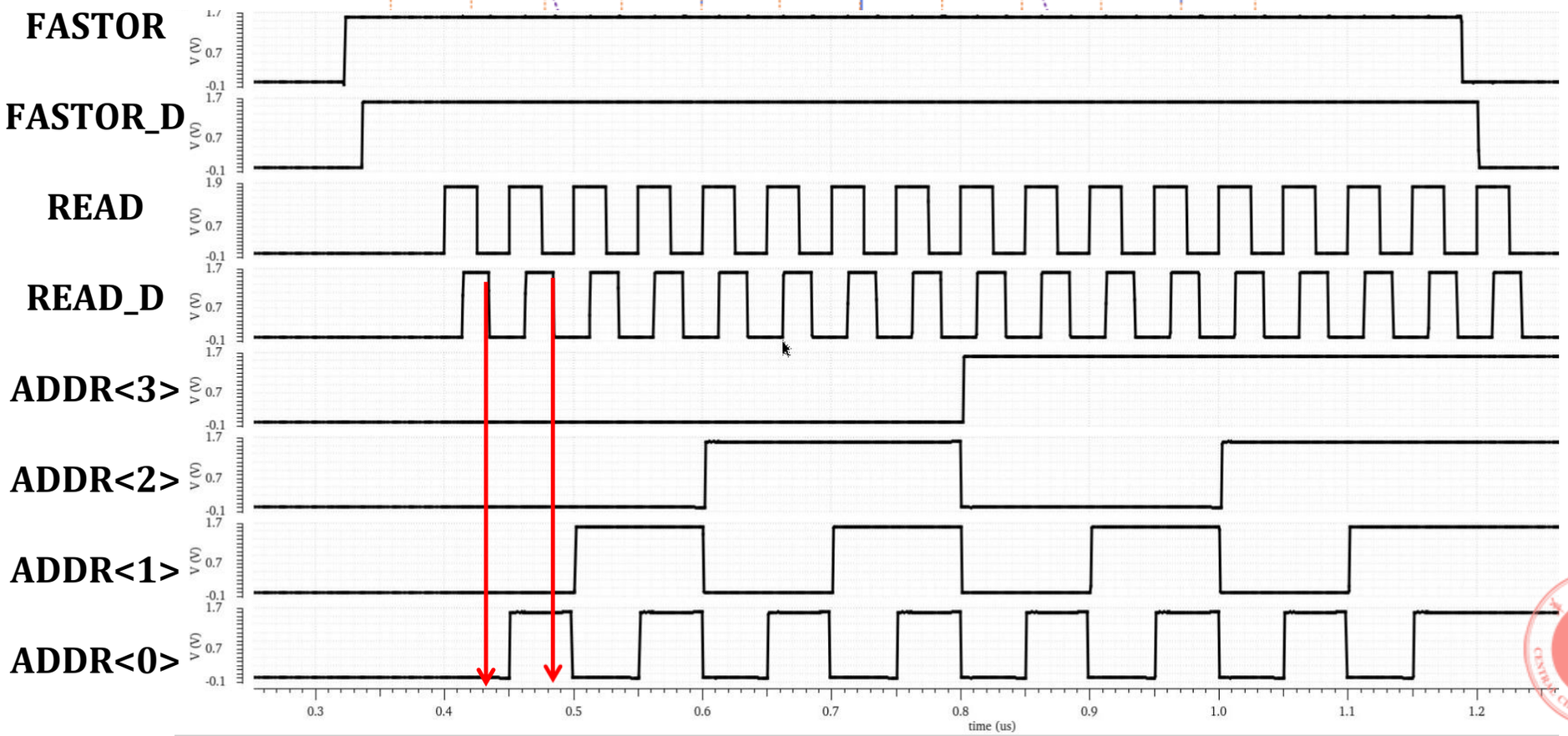


Simulation of boosting speed AERD



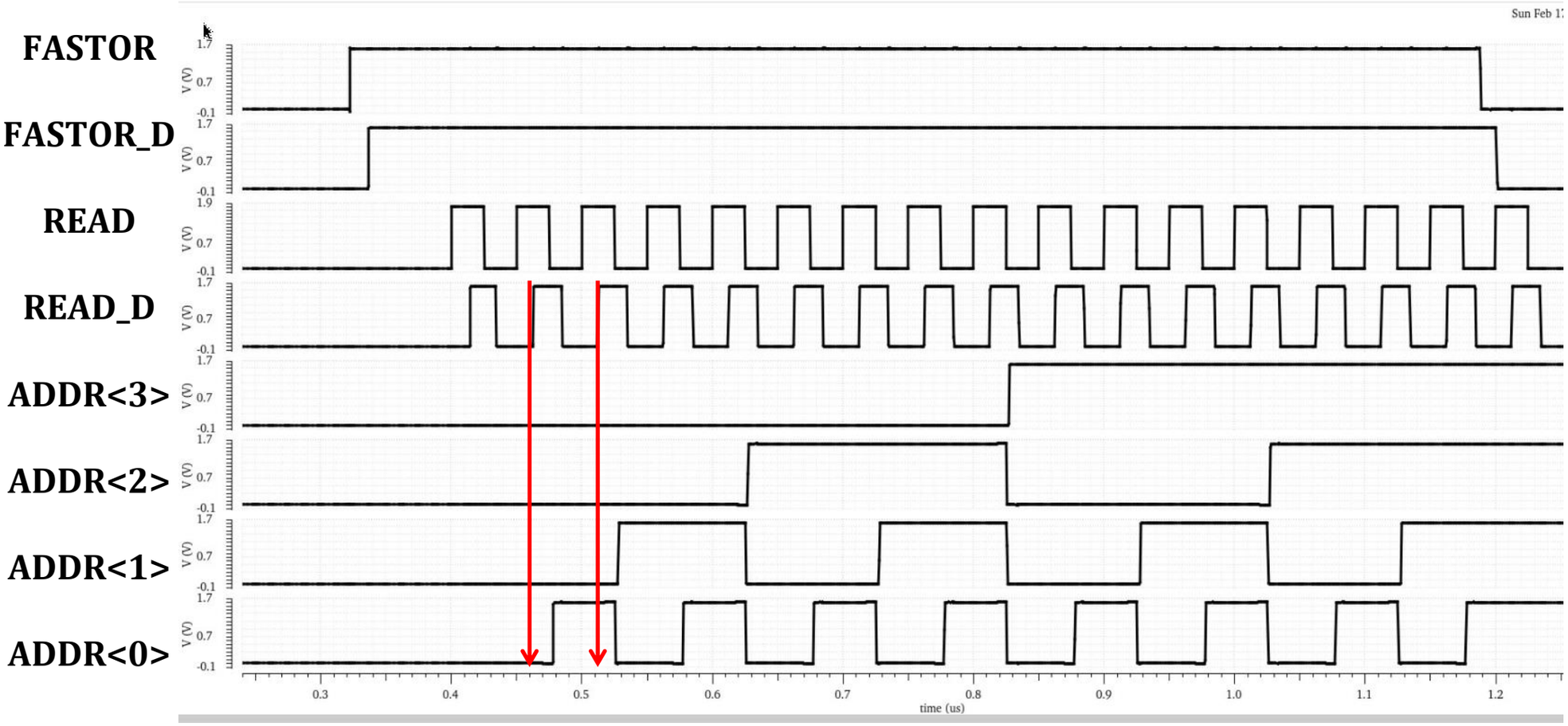
TT ; 1.8V ; 27℃	
Signal	Delay
FASTOR	9.7ns
READ	9.7ns
TDA	19.7ns
TDFOR	10ns

SS ; 1.6V ; 50℃	
Signal	Delay
FASTOR	14.3ns
READ	14.3ns
TDA	25.5ns
TDFOR	1.3ns



The address encoder will work at falling edge . And the worst case will increase the delay from the long metal line.

Simulation of normal AERD

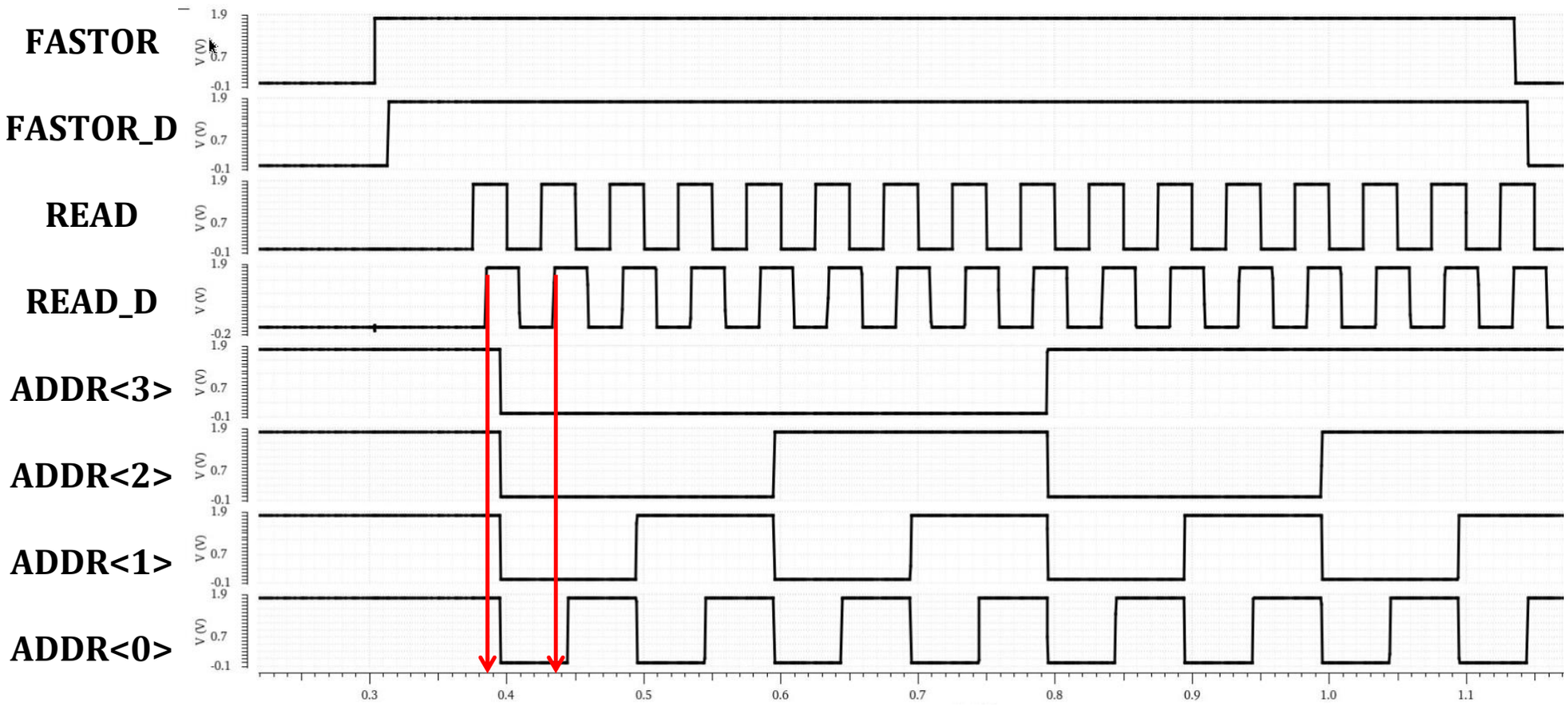


TT ; 1.8V ; 27℃	
Signal	Delay
FASTOR	9.7ns
READ	9.7ns
TDA	19.4ns
TDFOR	10ns

SS ; 1.6V ; 50℃	
Signal	Delay
FASTOR	14.3ns
READ	14.3ns
TDA	28ns
TDFOR	1.3ns

The address encoder will work at rising edge . And the worst case will increase the delay from the long metal line.

Simulation of FE-I3



TT ; 1.8V ; 27℃	
Signal	Delay
FASTOR	9.7ns
READ	9.7ns
TDA	20ns
TDFOR	10ns

SS ; 1.6V ; 50℃	
Signal	Delay
FASTOR	14.4ns
READ	14.4ns
TDA	27.8ns
TDFOR	14 ns

The address encoder will work at rising edge . And the worst case will increase the delay from the long metal line.

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Conclusion and OUTLOOK

Conclusion:

- The boosting speed scheme read data half a cycle in advance, at the falling edge.
- It will cost more logic gates.
- Insert buffer at the end of the column, it seems there is no high Z condition.

Next tasks to do：

- Decide the final digital pixel circuits.
- Simulate the full column and submit it.

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Thanks for your attention.

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