Status of Digital Pixel

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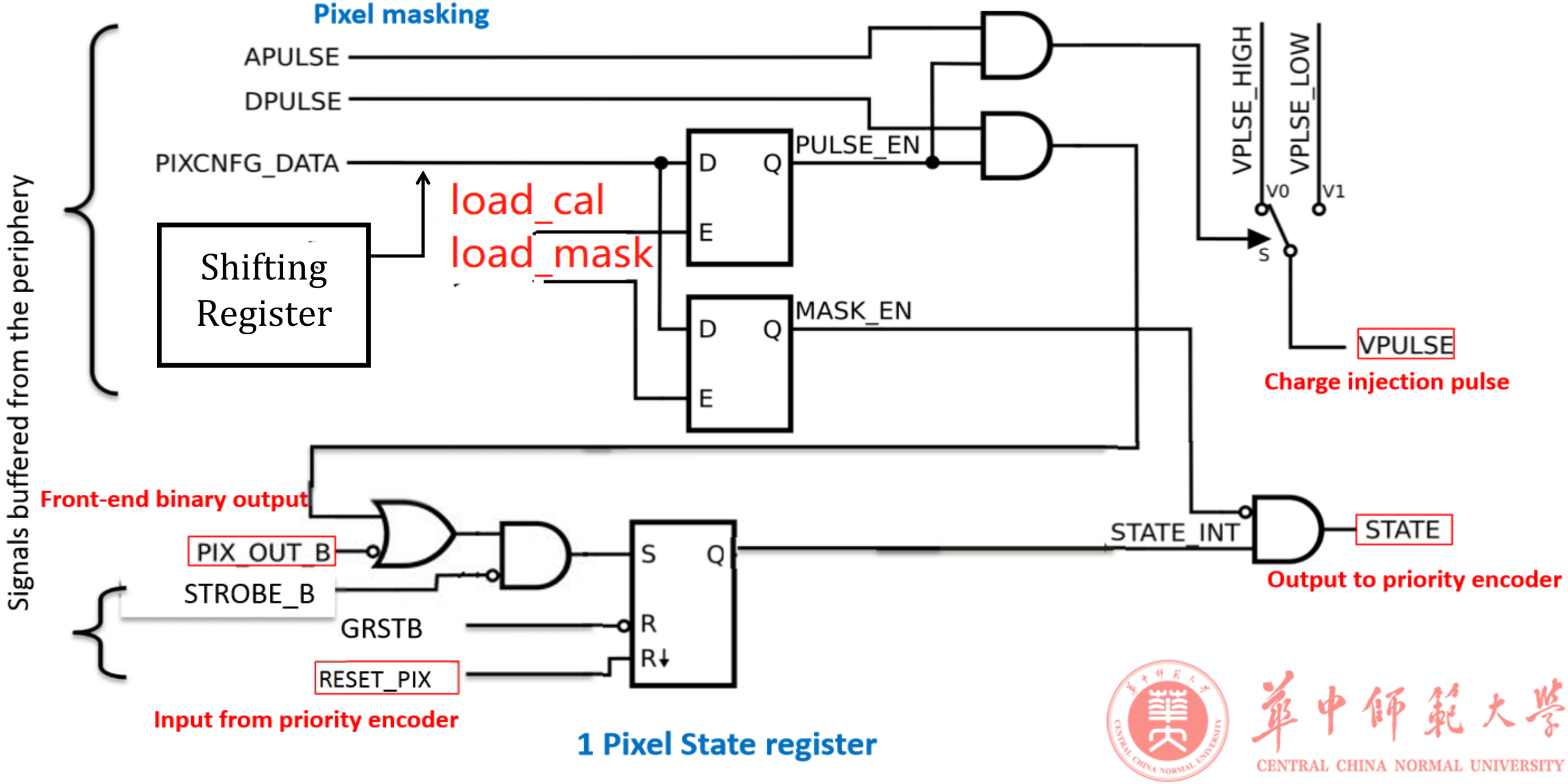
OUTLINE

- ALPIDE logic block
- FE_I3 logic block
- Outlook

ALPIDE Digital Cell

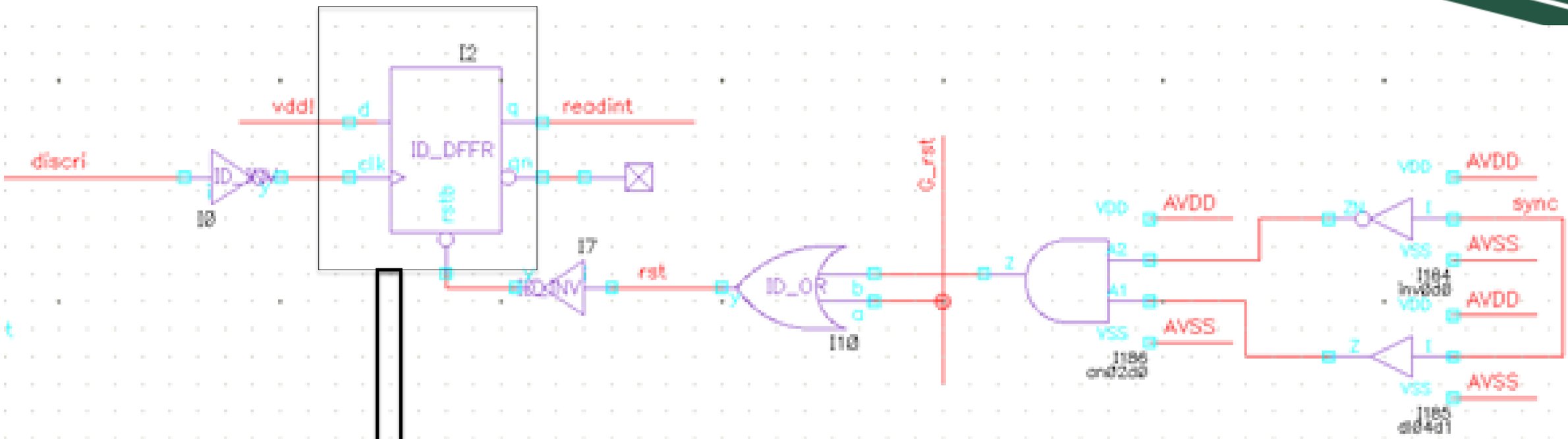
2 Configuration bits:
Pixel pulsing
Pixel masking

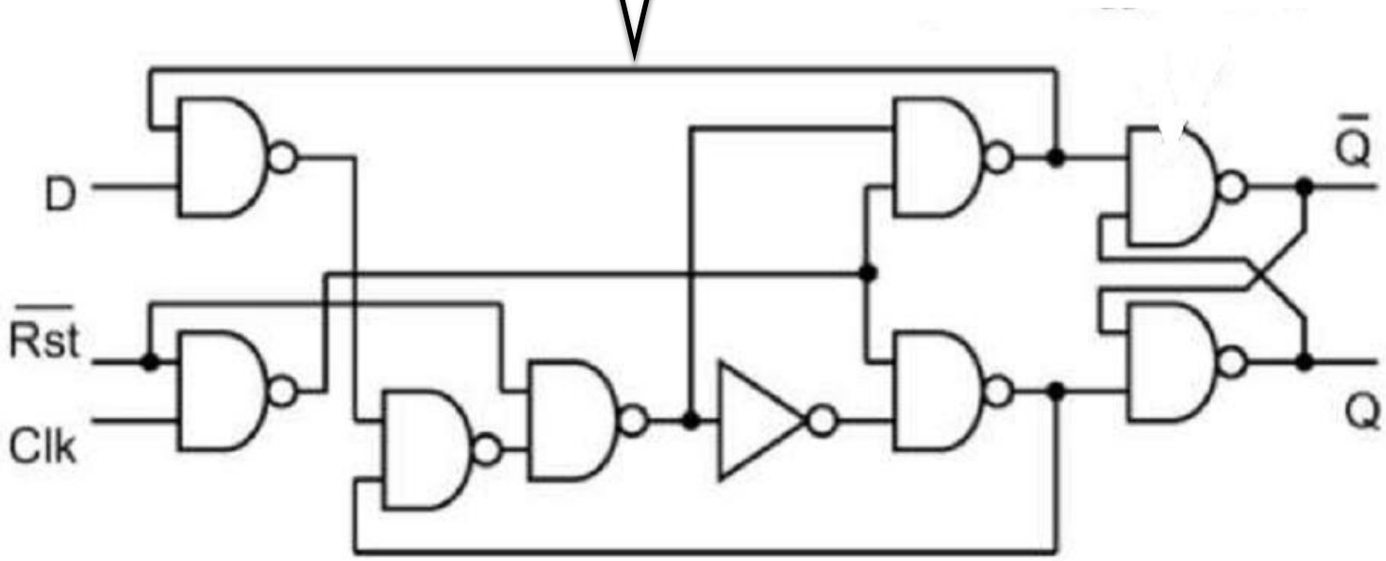
It will cost around 60 transistors.



1 Pixel State register

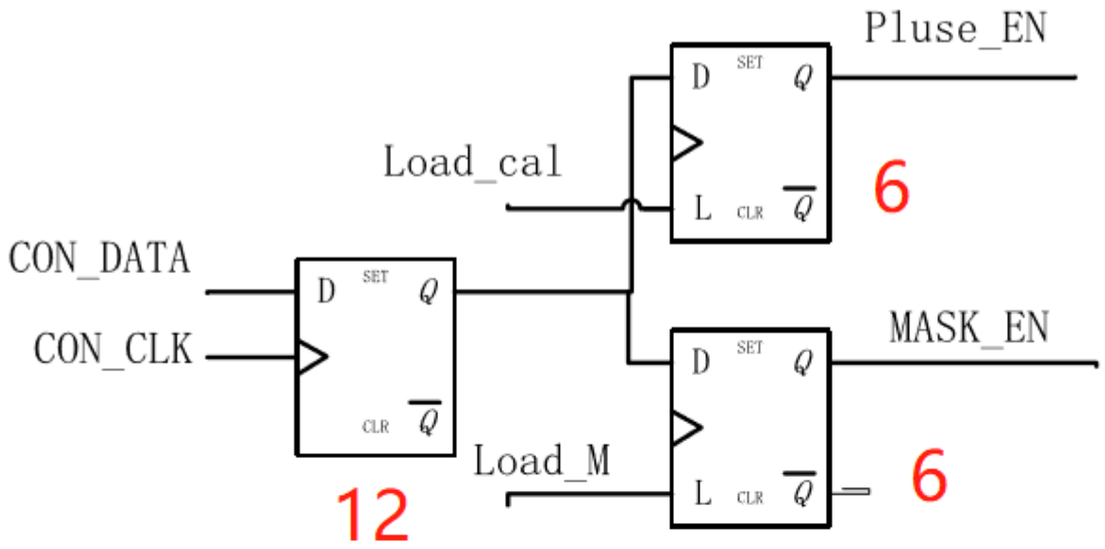
Optional Digital Cell

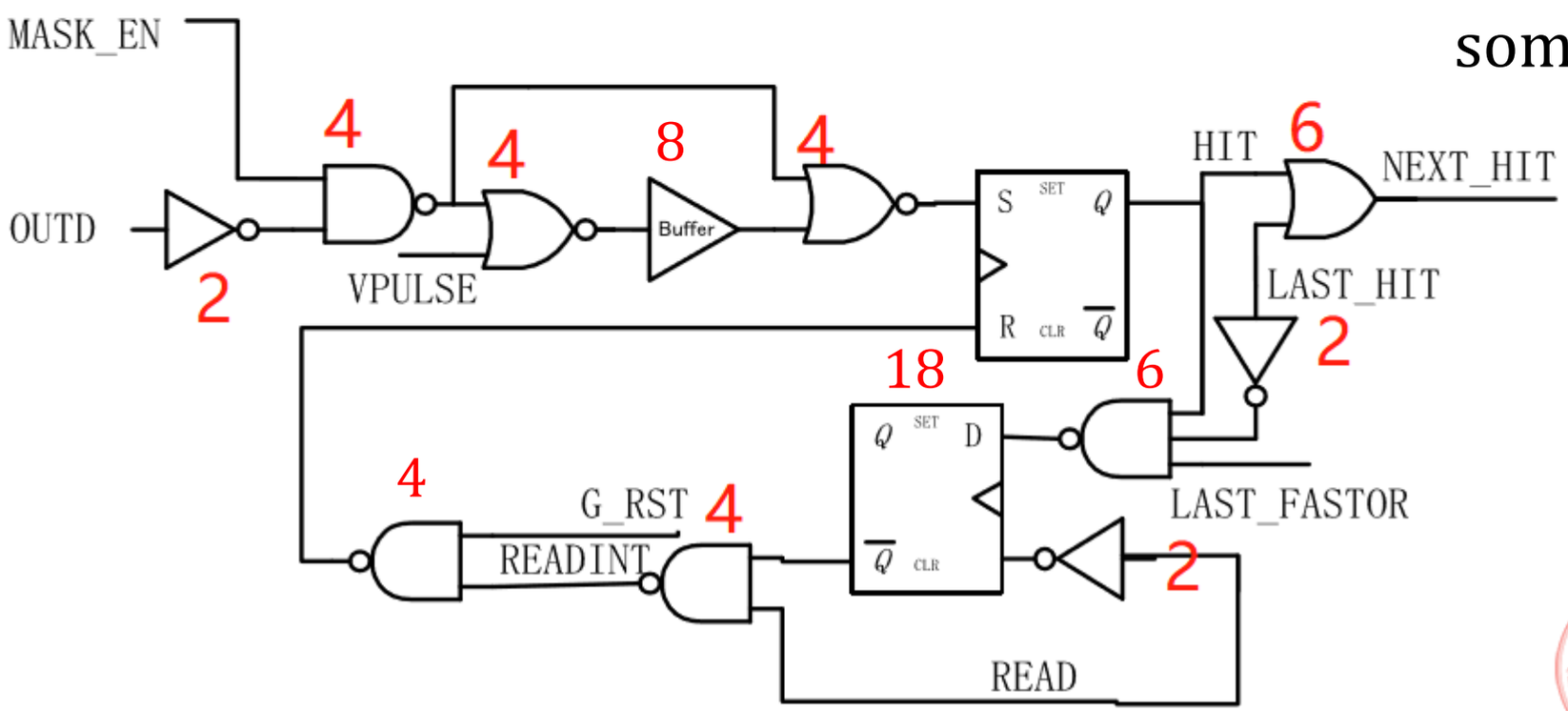




It will cost around 96 transistors.
Including Masking and Analog Calibration circuits.
This is not the best choice.

FE-I3 Digital Cell





It will cost around 104 transistors, including the Analog calibration block.
But the address encoder part will save some area than ALPIDE

Conclusion and OUTLOOK

Conclusion:

- From my simulation result, the ALPIDE structure will need a trigger latency signal (Strobe) more to reduce the effect of analogue pulse duration.
- Both of them are working fine with the external configuration bits.

Next tasks to do：

- Do the standard cell layout.
- Simulate the full column and submit it.

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Thanks for your attention.

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