山东大学
SHANDONG UNIVERSITY

粒子物理与粒子辐照
教育部重点实验室

Design of Current DAC & Voltage DAC

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on behalf of SDU group

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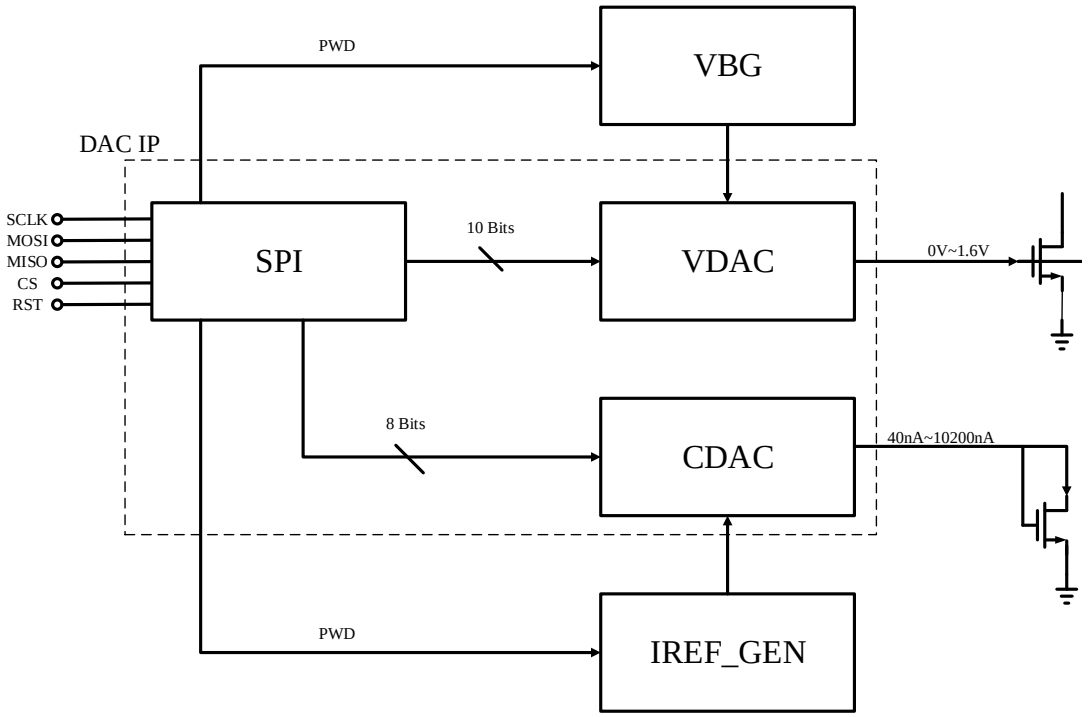
Structure of DAC

- **Structure of the DAC**
  - SPI
  - Voltage DAC (VDAC)
  - Current DAC (CDAC)

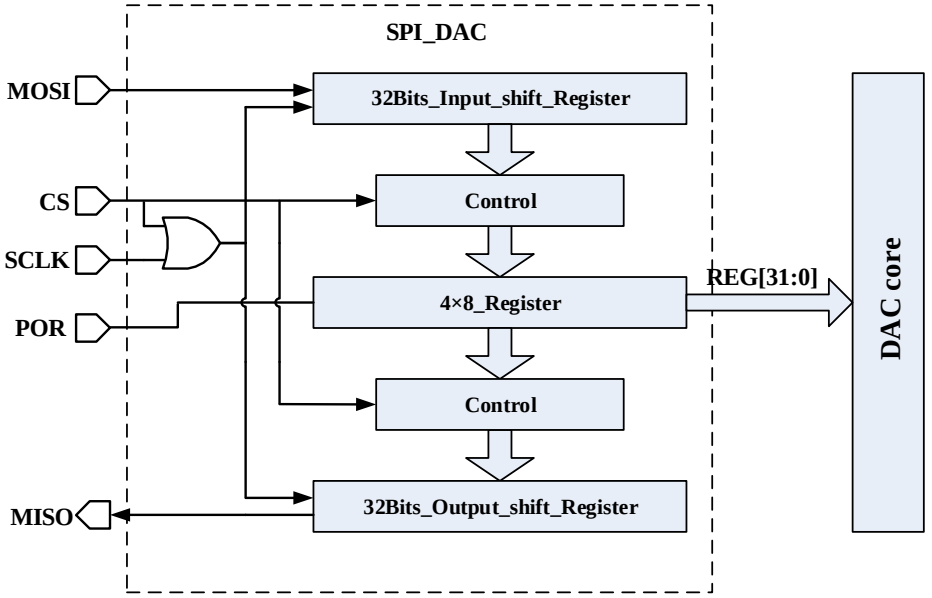
- **Characteristics**
  - SPI
    - SPI register 32 bits (4 byte)
    - Clock ~ 10 MHz
  - Voltage DAC (VDAC)
    - 10 bit
    - LSB: 1.56 mV
    - Range: 0 – 1.6 V
    - Reference voltage: 0.8 V
  - Current DAC (CDAC)
    - 8 bit
    - LSB: 40 nA
    - Range: 0 nA ~ 10.2 µA



Architecture of the top DAC

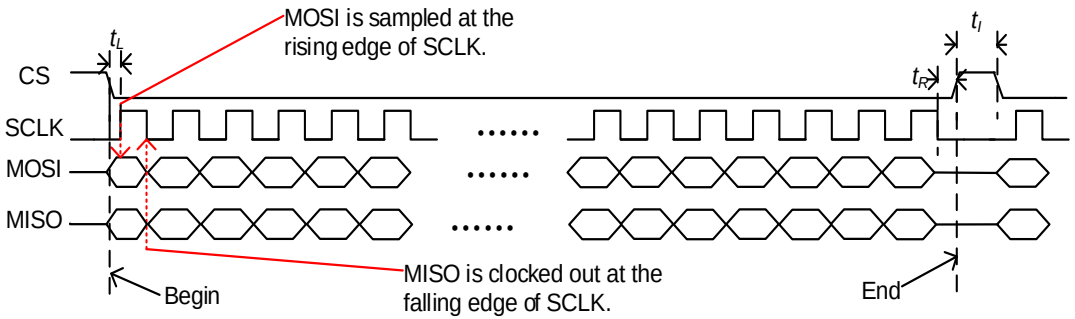
Structure of SPI

- **I/O**
  - Inputs
    - MOSI (serial input)
    - CS
    - SCLK (clock)
    - POR (clean register)
  - Outputs
    - MISO (serial output)



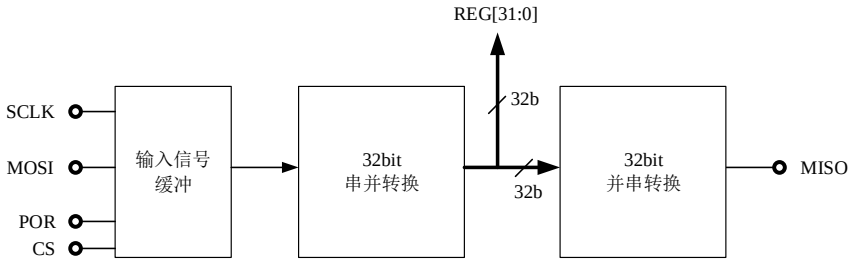
Architecture of the SPI (serial peripheral interface)

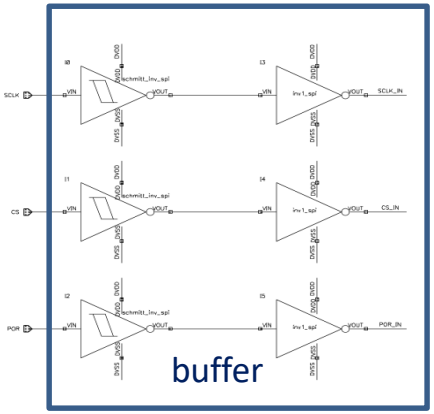
- **Timing**
  - Input: REG[N] → REG[0]
  - Output: REG[N] → REG[0]

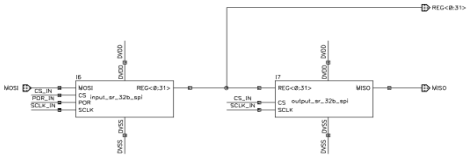


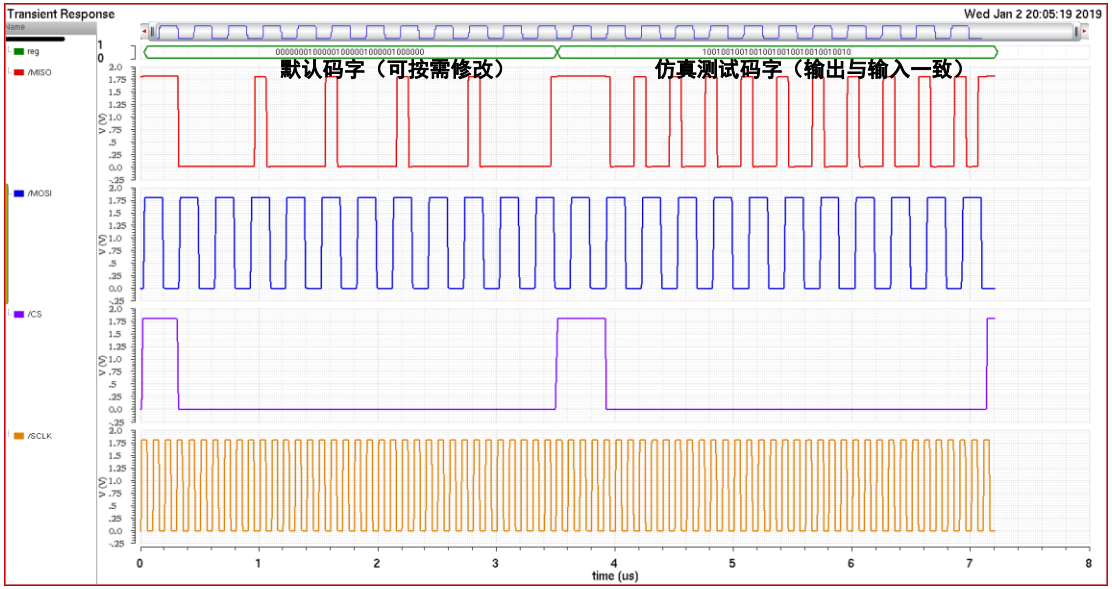
Timing of the SPI

Structure of SPI





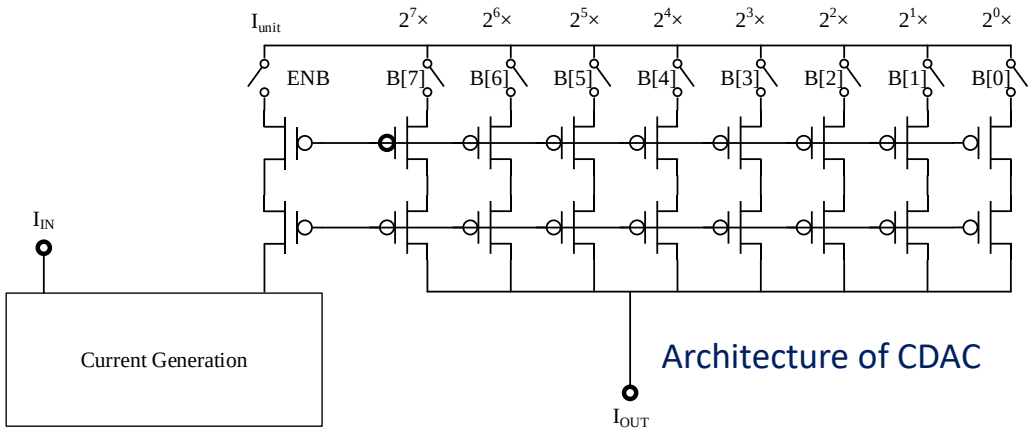




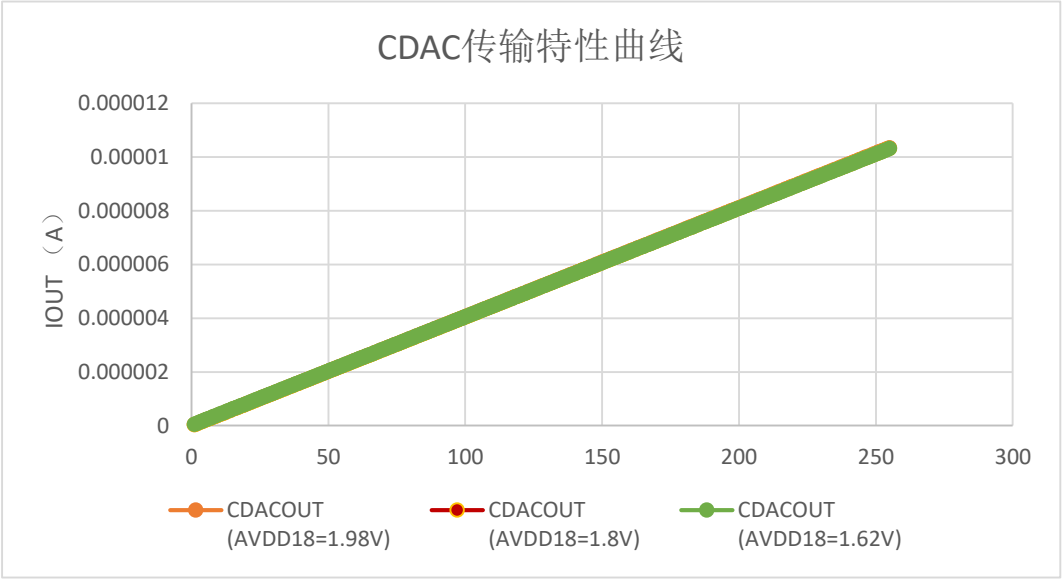
Simulation results of SPI (clock @ 5M Hz)

Structure of Current DAC (CDAC)

- **Current DAC**
  - Current mirror
  - Segmented architecture
    - 4 most significant bits (MSB)
      - ★ thermometer decode
    - 4 least significant bits (LSB)
      - ★ binary weighted
  - Output impedance
    - Min: 104KΩ
    - Max: 43 MΩ

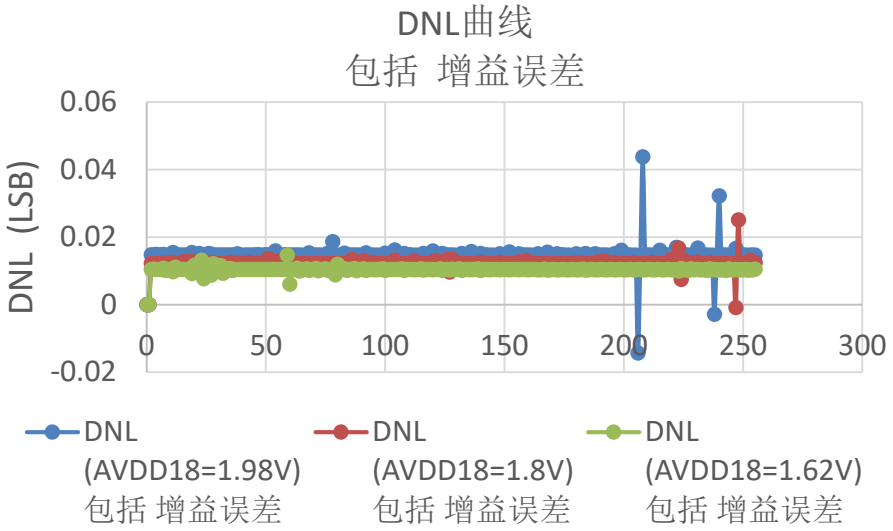


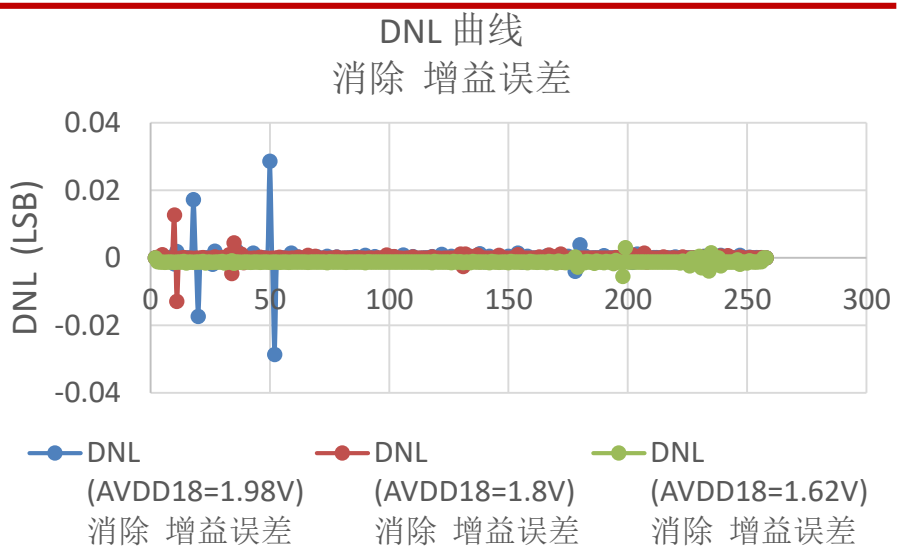
Architecture of CDAC

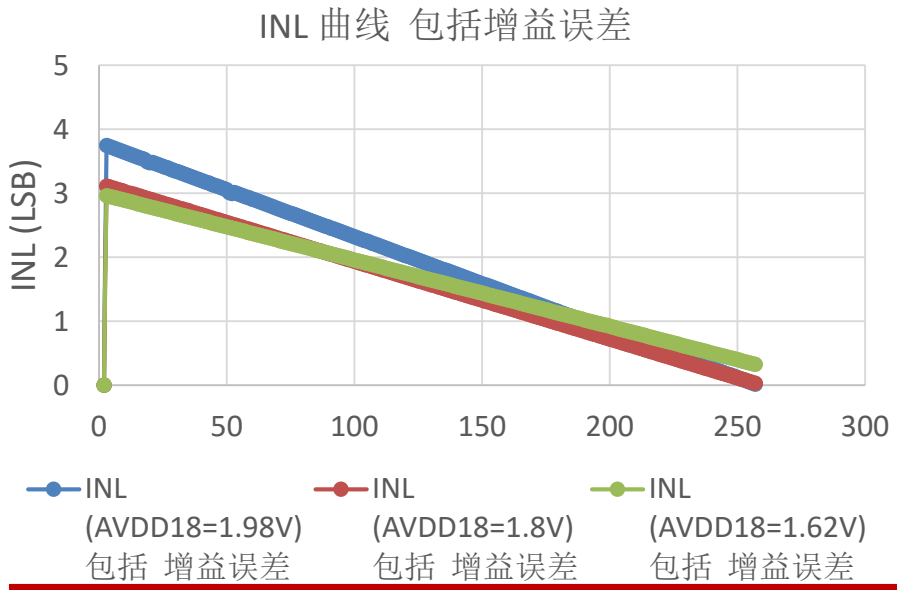


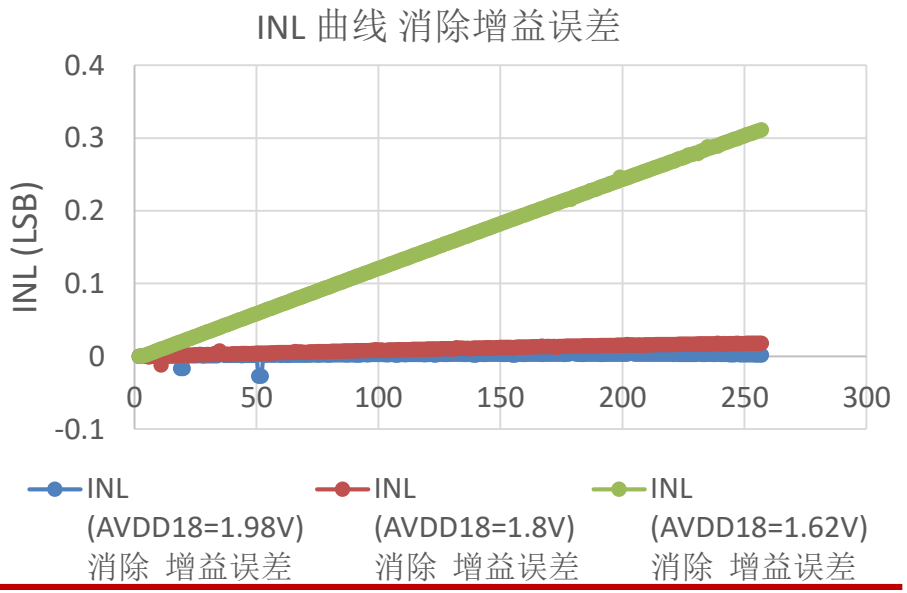
Characteristic curve of the CDAC

Simulation results of Current DAC (CDAC)



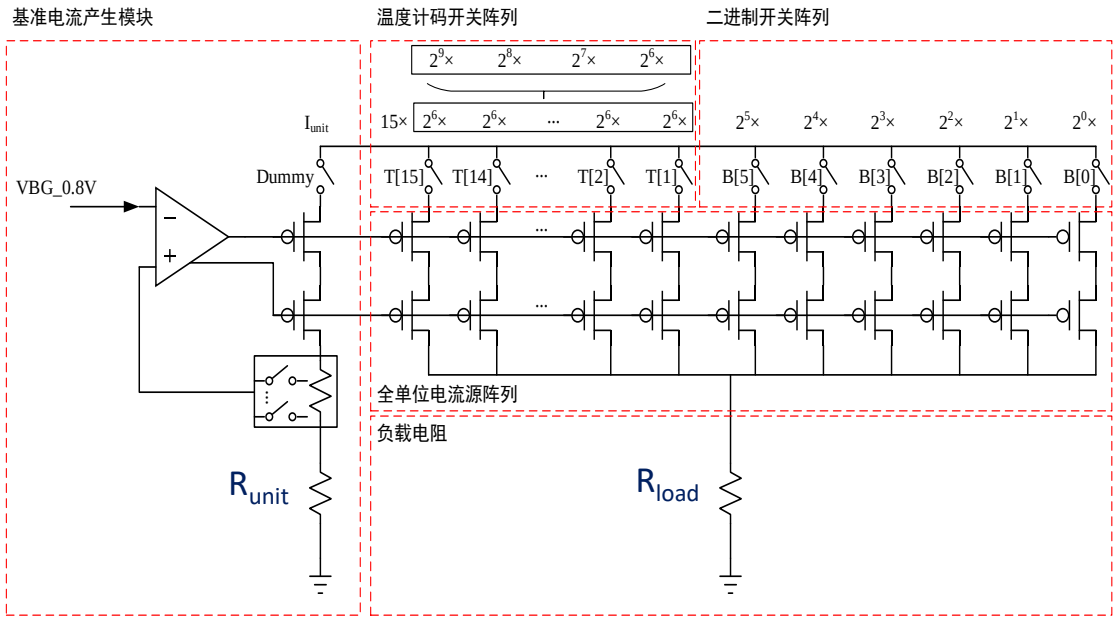






Structure of Voltage DAC (VDAC)

- **Voltage DAC**
  - Current bias generation block
    - VBG: output of bandgap ~ 0.8 V
    - I_{unit} ~ 20 μA
  - Negative feedback to stabilize VBG @ 0.8 V V_{FB}
  - Current mirror with resistor load
  - Segmented architecture
    - 4 most significant bits (MSB): thermometer decode
    - 6 least significant bits (LSB): binary weighted



Architecture of CDAC

$$V_{DAC} = Weight(Code[9:0]) \times I_{unit,mirror} \times R_{load}$$

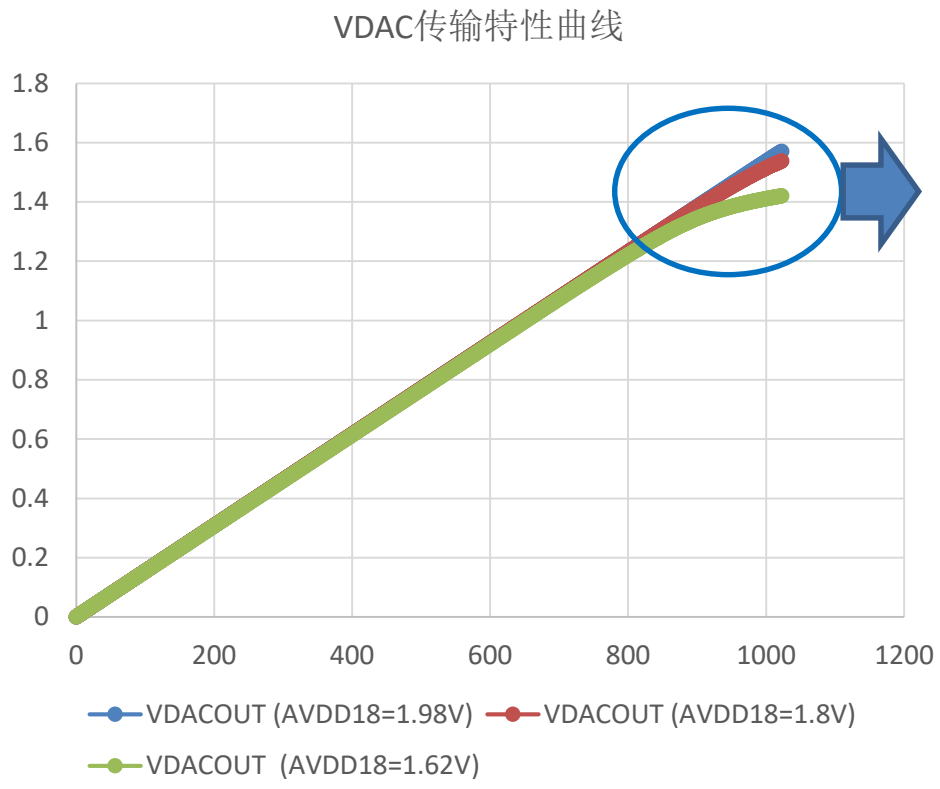
$$= Weight(Code[9:0]) \times \left(\frac{1}{4} \times I_{unit,ref} \times \frac{1}{4} \times R_{unit}\right)$$

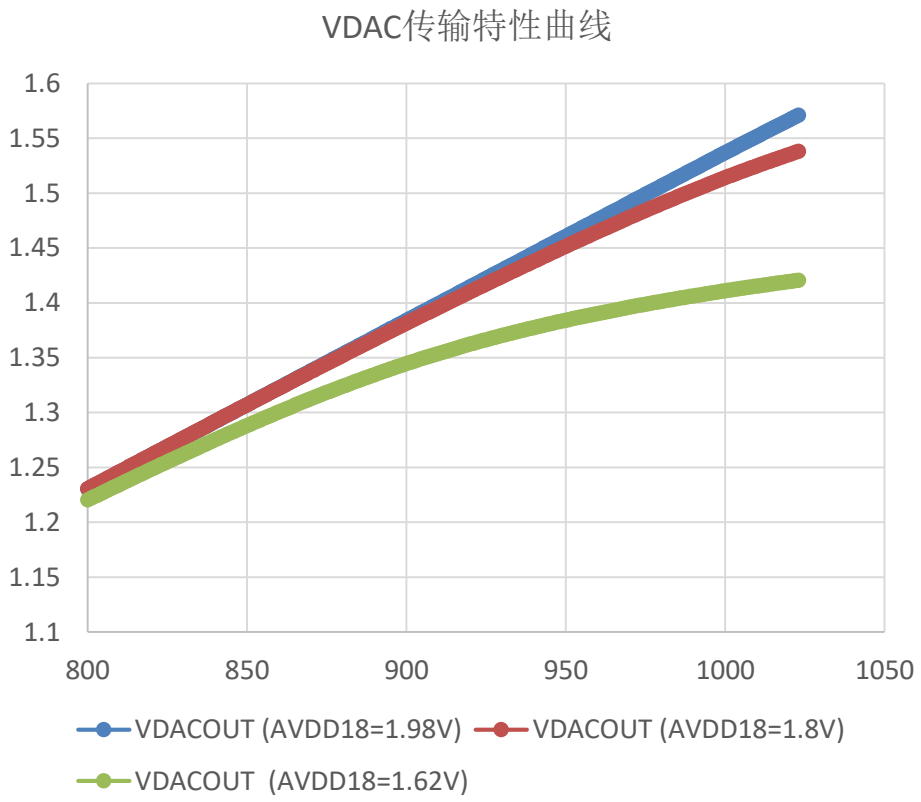
$$= \sum_{i=0}^{9} 2^i \cdot Code[i] \times \left(\frac{1}{4} \times I_{unit,ref} \times \frac{1}{4} \times R_{unit}\right)$$

$$= \sum_{i=0}^{9} 2^i \cdot Code[i] \times \frac{1}{512} \times V_{FB}$$

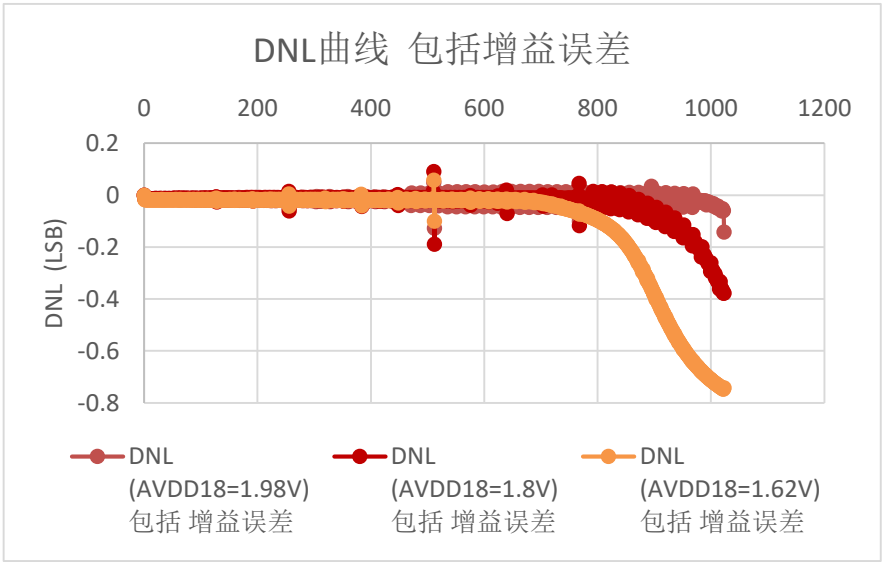
$$= \sum_{i=0}^{9} 2^i \cdot Code[i] \times V_{LSB}$$

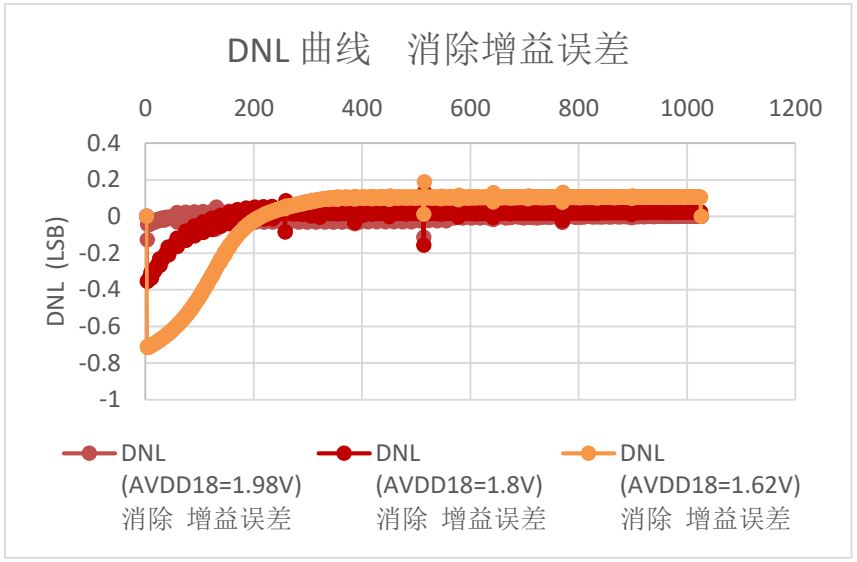
Structure of Voltage DAC (VDAC)

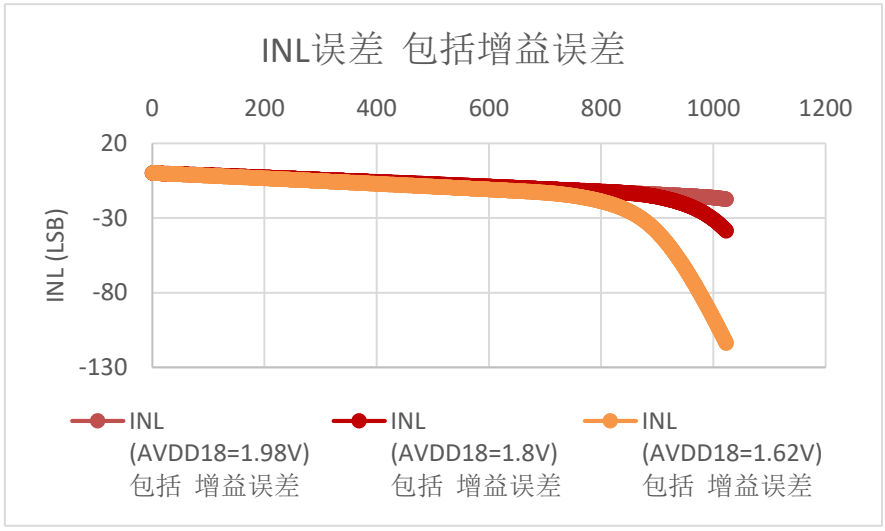


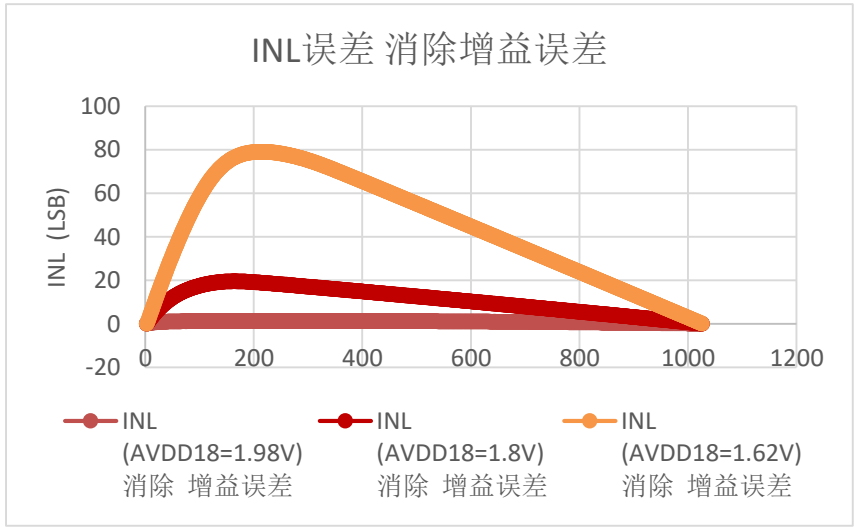


Simulation results of Voltage DAC (VDAC)









Thanks for your attention