Status of Digital Pixel

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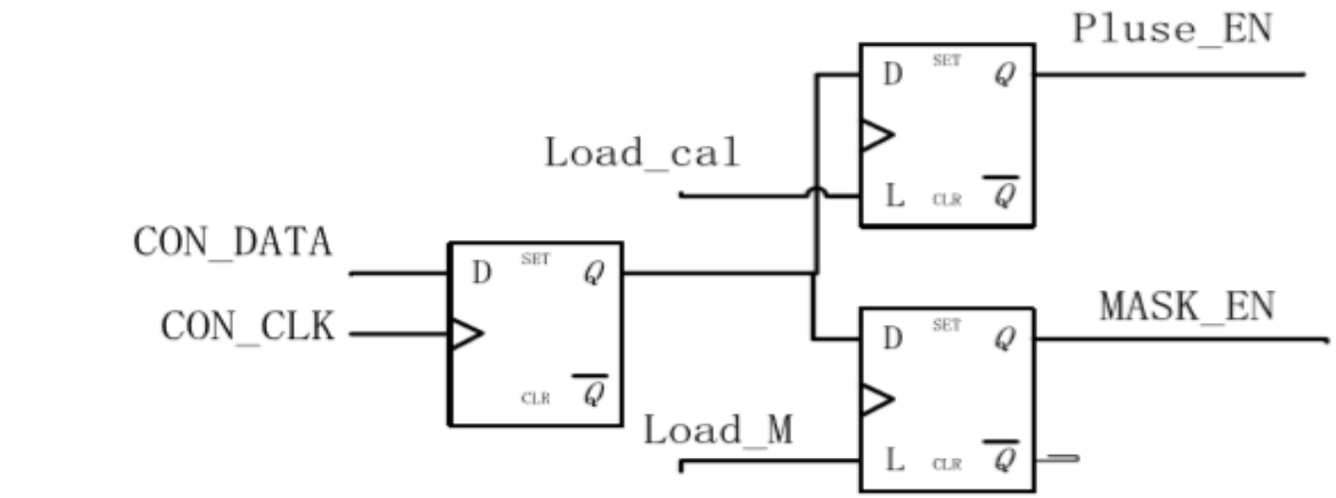
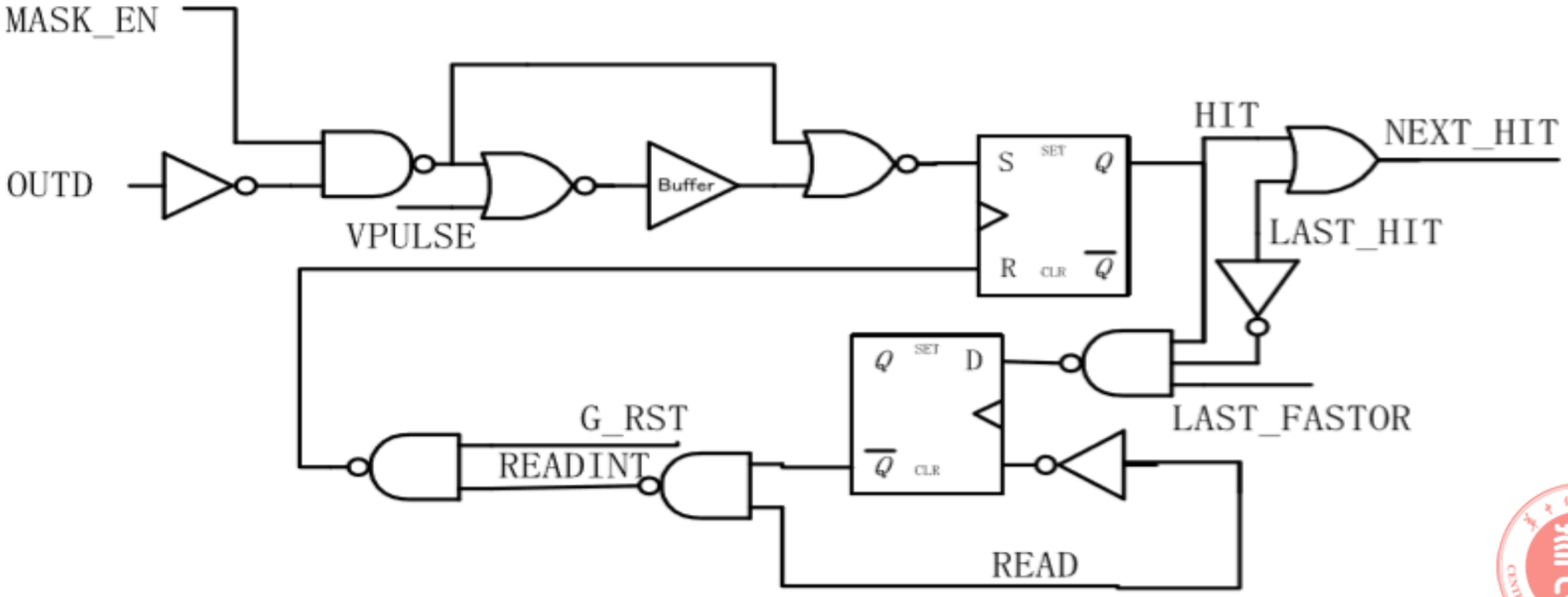
FE-I3 digital logic block





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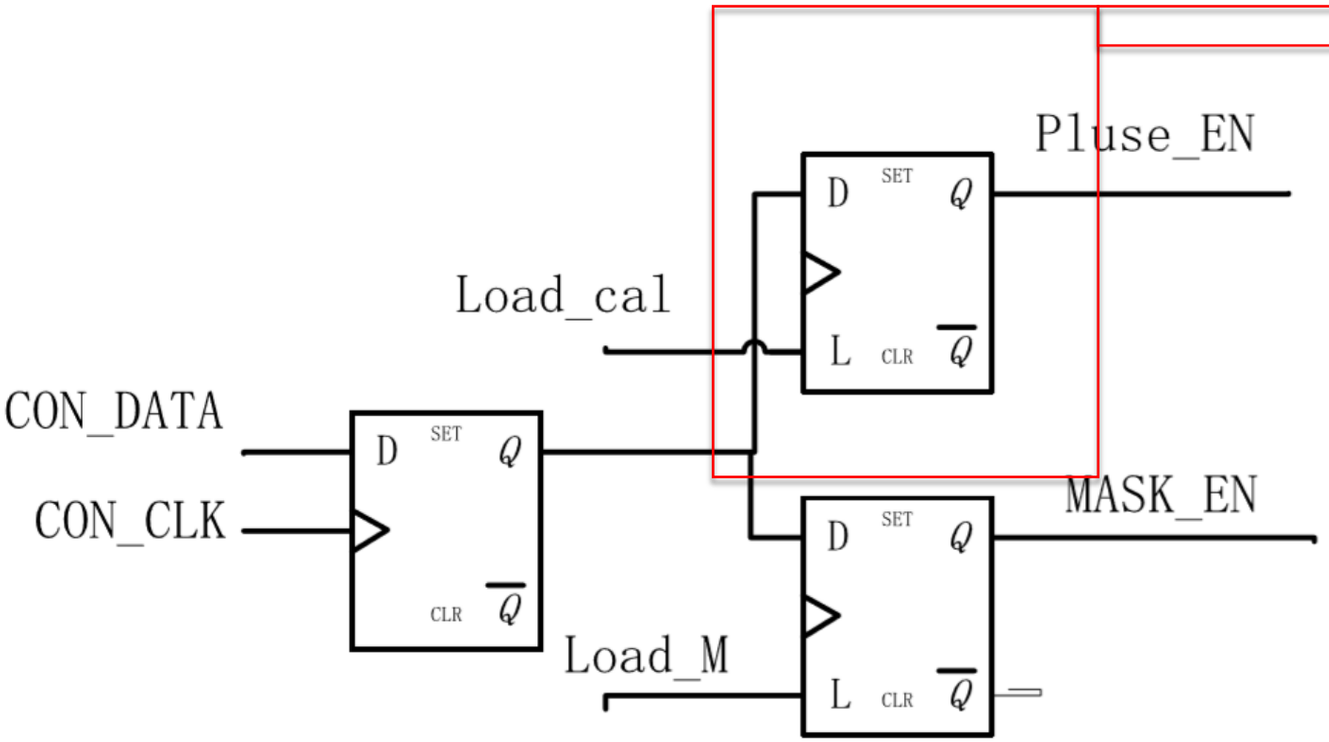
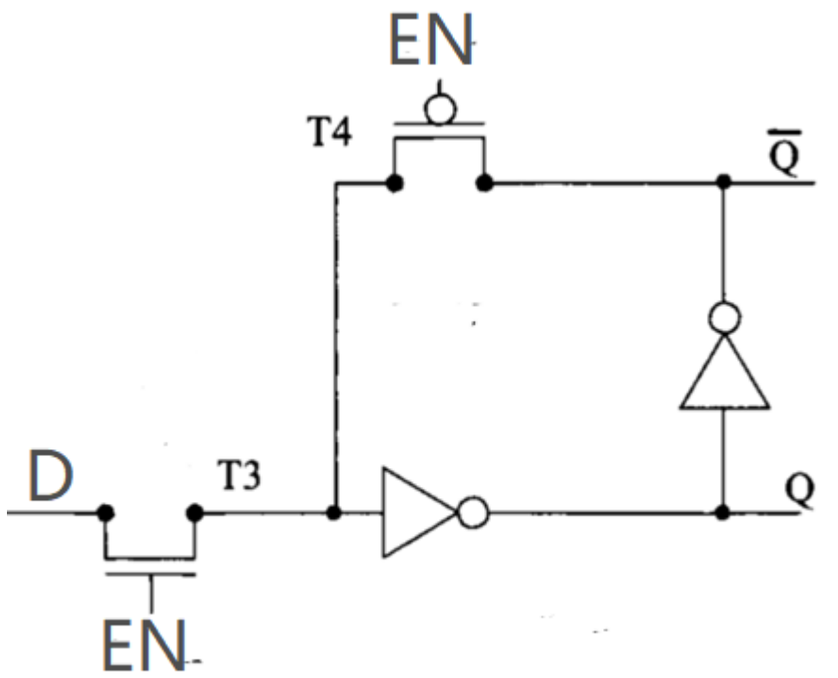
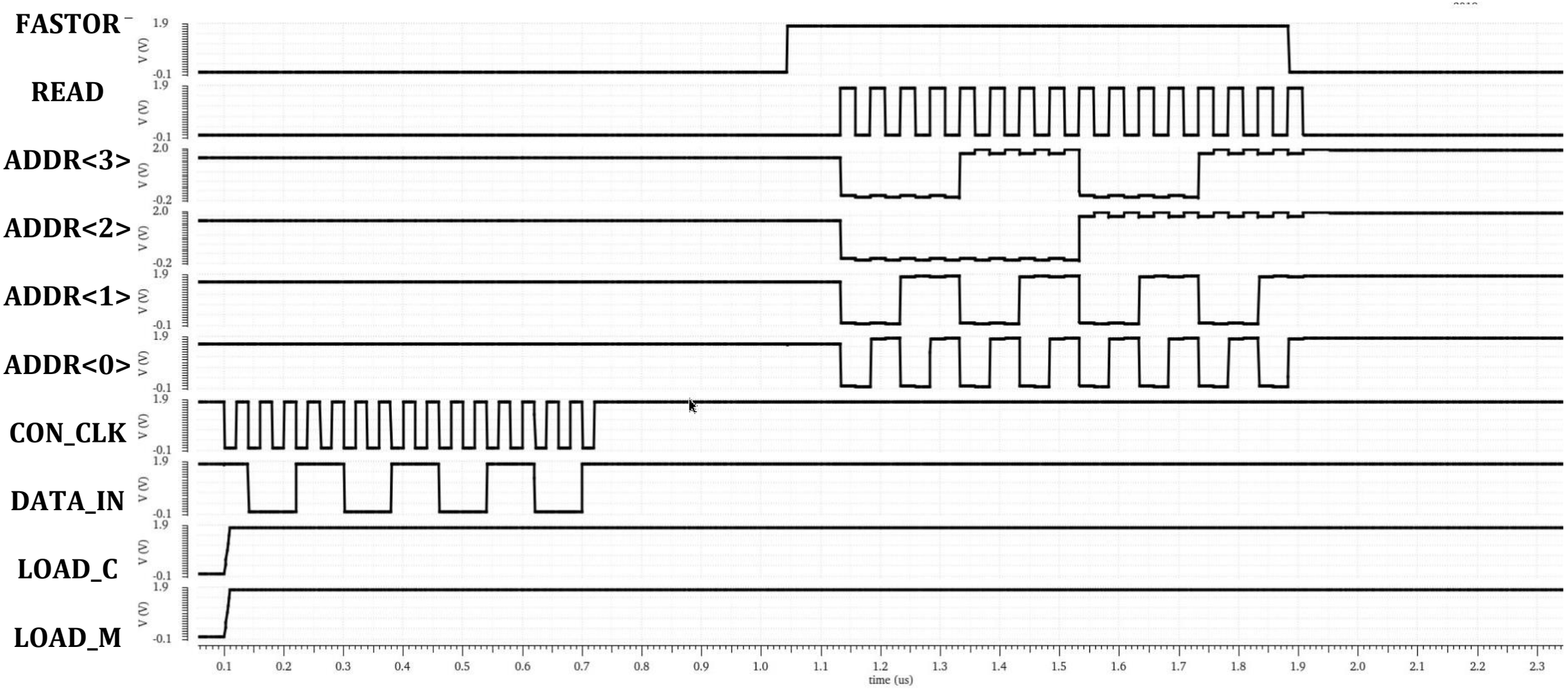
FE-I3 digital logic block





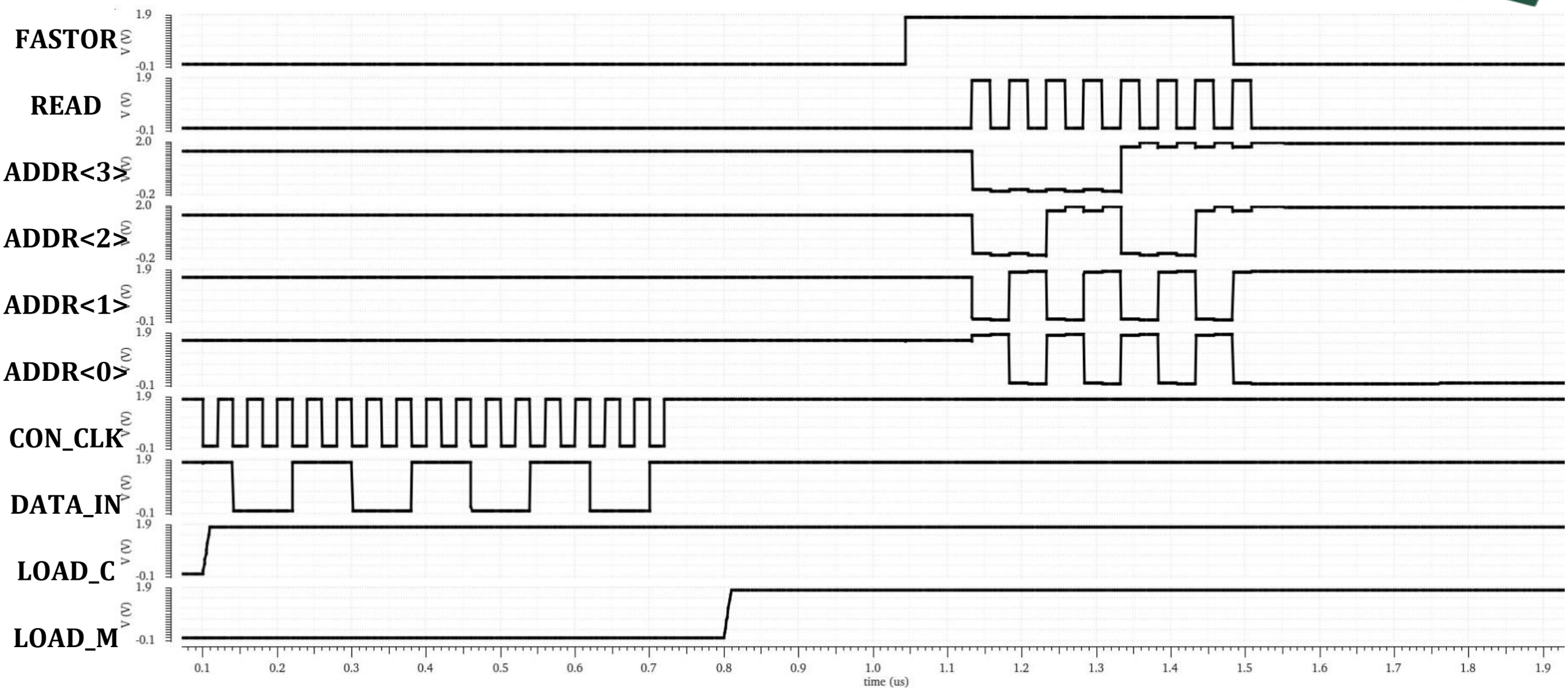
D	EN	Q	QB
0	0	1	0
1	0	0	1
0	1	latch	latch
1	1	latch	latch

FE-I3 timing diagram (default)



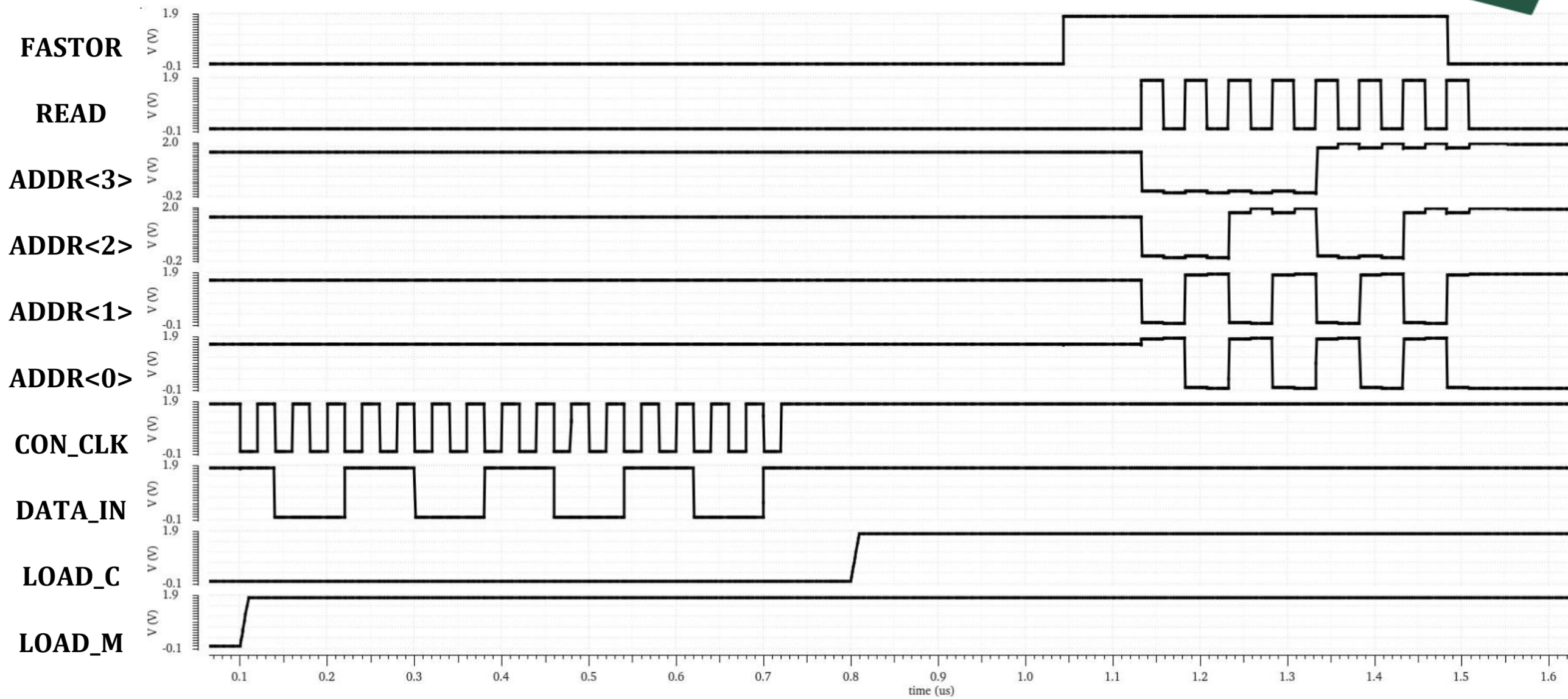
When load_c and load_m step to high level, the latch will have a stable output where keep the last state.

Masking bit test



LOAD_M will latch the data after all the masking bits configured.

Analog Calibration bit test



LOAD_C will latch the data after all the masking bits configured.

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Thanks for your attention.

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