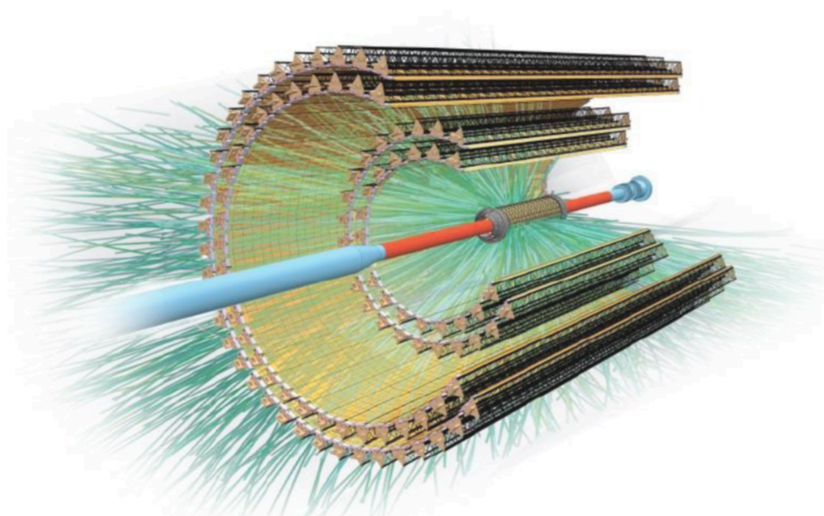
ALICE Inner Tracking System Upgrade

Biao Zhang

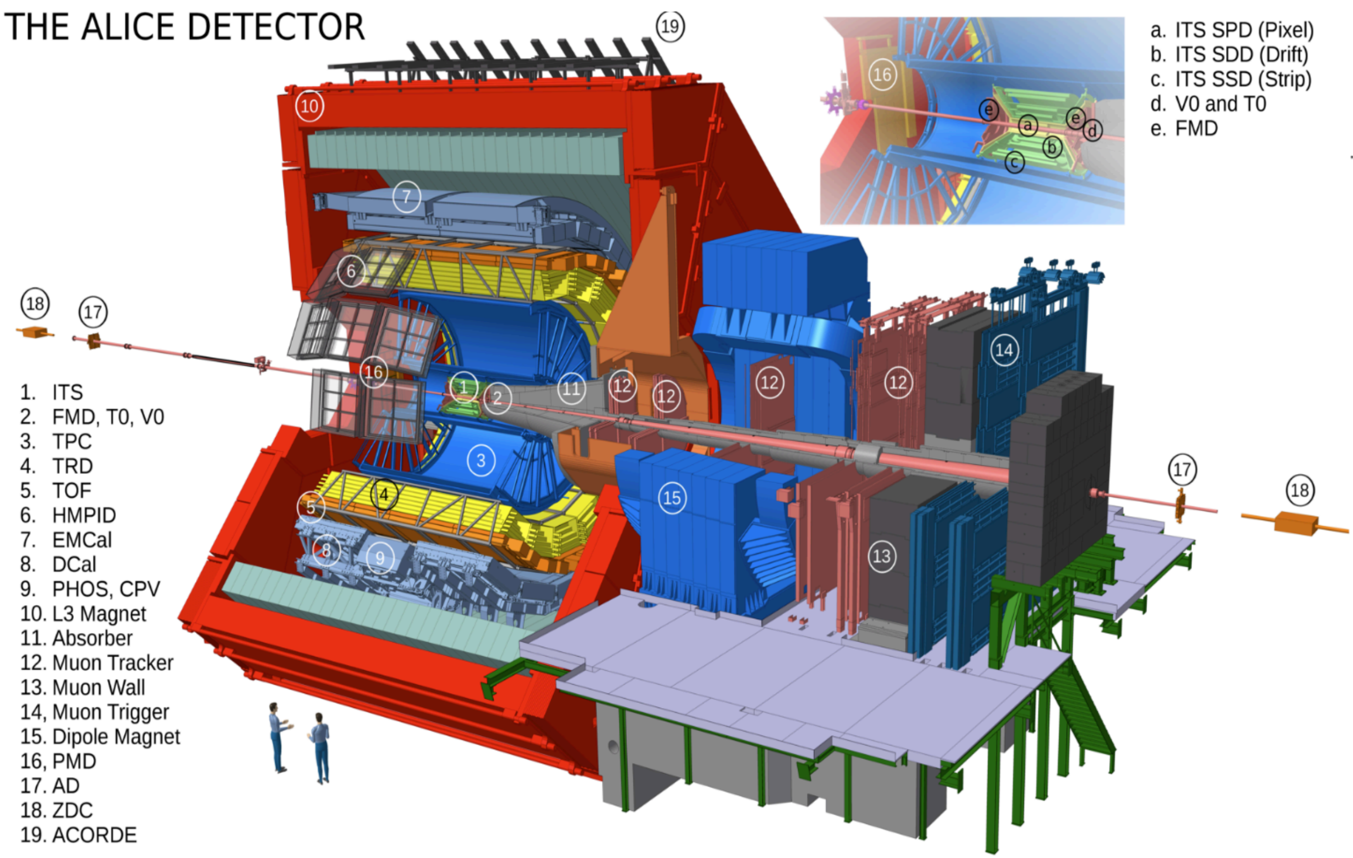
Central China Normal University



Outline

- **Physics motivation**
- **ALICE ITS Upgrade**
  - ✓ **ALPIDE Pixel Chip**
  - ✓ **New ITS layout and components**
  - ✓ **Assembly and commissioning**
- **OB HIC assembly and testing at CCNU**
- **Summary and outlook**

Current ALICE Detector



Run 1 (2009 – 2013)
Pb-Pb @ $\sqrt{s_{NN}}$ = 2.76 TeV
p-Pb @ $\sqrt{s_{NN}}$ = 5.02 TeV
pp @ $\sqrt{s}$ = 0.9, 2.76, 7, 8 TeV

Run 2 (2015 – 2018)
Pb-Pb @ $\sqrt{s_{NN}}$ = 5.02 TeV Xe-Xe @ $\sqrt{s_{NN}}$ = 5.44 TeV
p-Pb @ $\sqrt{s_{NN}}$ = 5.02, 8.16 TeV
pp @ $\sqrt{s}$ = 5, 13 TeV

ALICE Detector:

- ✓ Central Barrel: $|\eta| < 0.9$
- ✓ Muon spectrometer: $-4.0 < \eta < -2.5$
- ✓ Forward detectors: trigger, centrality

Operation in Run 1 and Run 2:

- ✓ Tracking and PID in large kinematic range
- ✓ High resolution vertex reconstruction

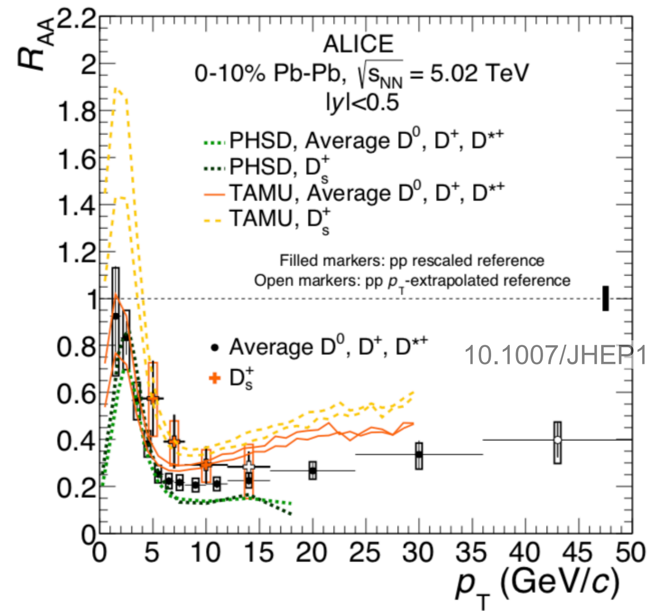
Physics Motivation

– Current ALICE detector:

- ✓ integrated luminosity ~ 0.1 nb^{-1}
- ✓ Max readout rate ~ 1 kHz (ITS and TPC)

– Present limits:

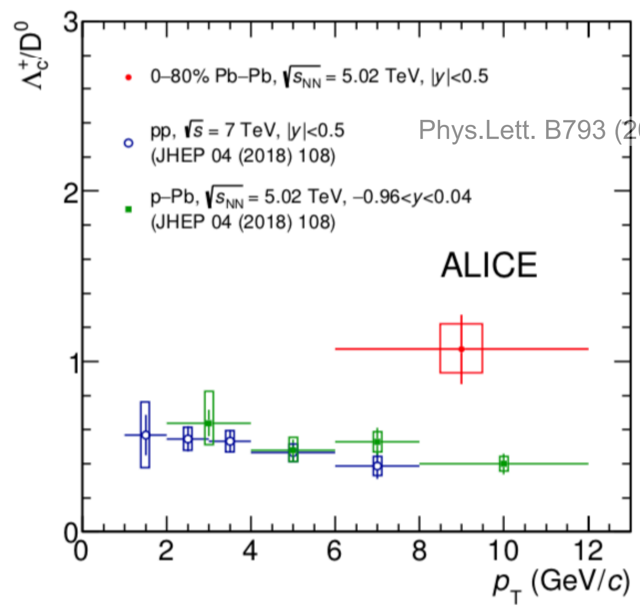
- ✓ Heavy flavour and quarkonia at very low p_T
- ✓ Vector mesons and low-mass dileptons
- ✓ Light nuclei and hypernuclei



10.1007/JHEP10(2018)174

ITS upgrade in LS2(Run3+Run4):

- ✓ **Integrated luminosity ~ 10 nb^{-1}**
- ✓ **Max readout rate ~ 100 kHz (Pb-Pb)**



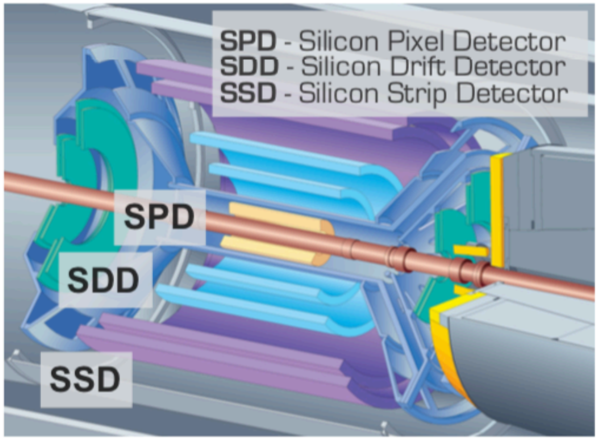
Phys.Lett. B793 (2019) 212-223

More statistics + High resolution !!

New ITS Performance

1. Improve impact parameter resolution
   - Get closer to IP (position of first layer)
   - Reduce material budget
   - Reduce pixel size
2. Improve tracking efficiency and p_T resolution at low p_T
3. Increase read-out capabilities

ITS (Run1/Run2)

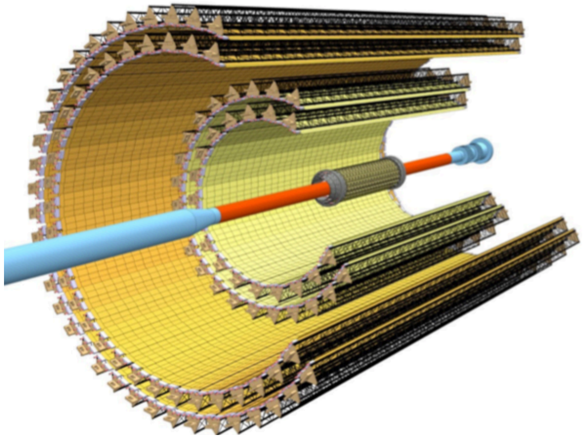


	ITS (Run1/Run2)	ITS Upgrade
Number of layers	6 (pixel, drift, μstrip)	7 (MAPS*)
Rapidity range	$\|\eta\| < 0.9$	$\|\eta\| < 1.3$
Material budget per layer	1.14% (SPD)	0.35% (IL)
Distance to interaction point	39 mm	22 mm
Pixel size	50 x 425 μm^2	29 x 27 μm^2
Spatial resolution	12 μm x 100 μm *	5 μm x 5 μm
Max. readout speed Pb-Pb	1 kHz	100 kHz

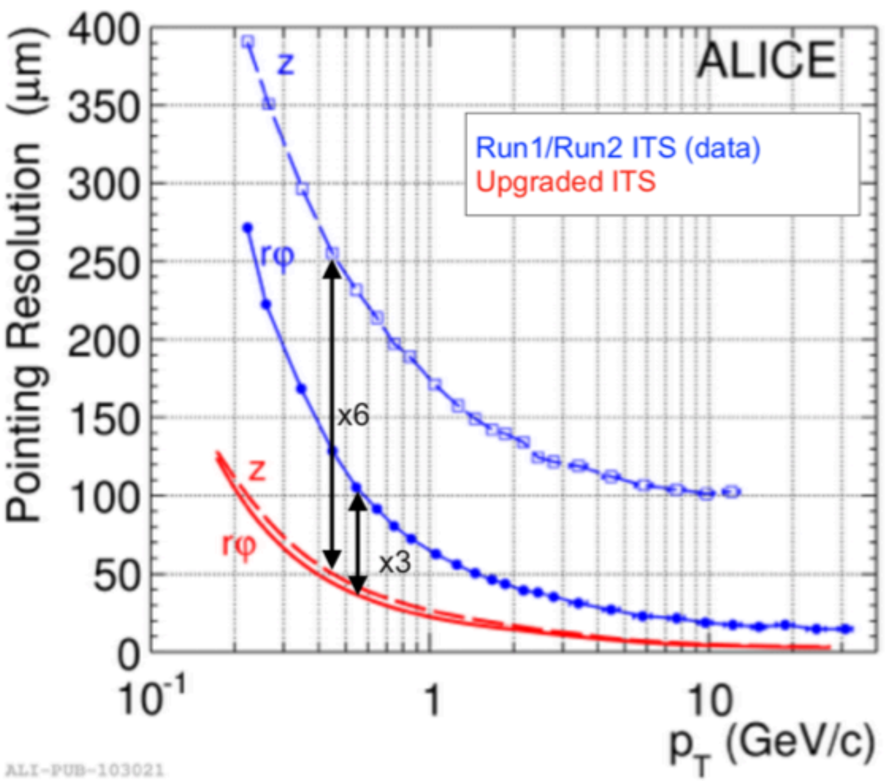
* SPD

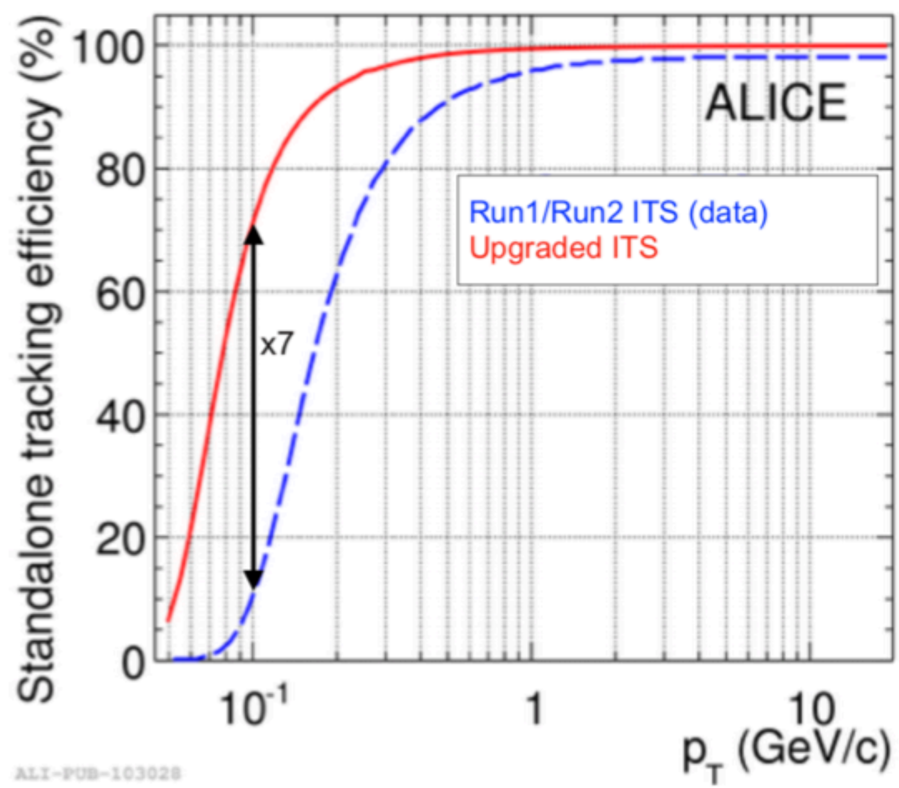
* Monolithic Active Pixel Sensors

ITS Upgrade



New ITS Performance



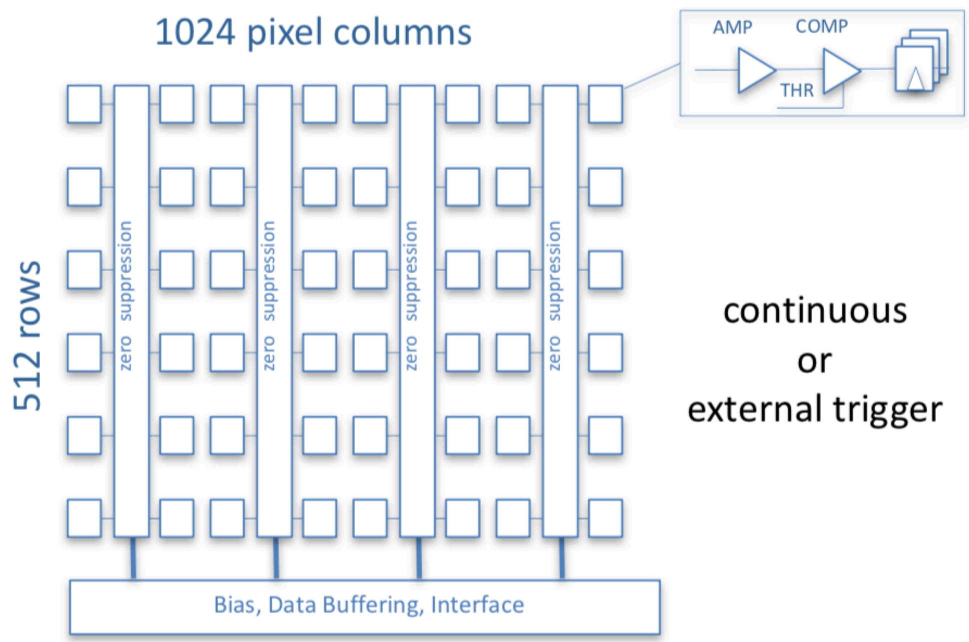


» Pointing resolution improved by

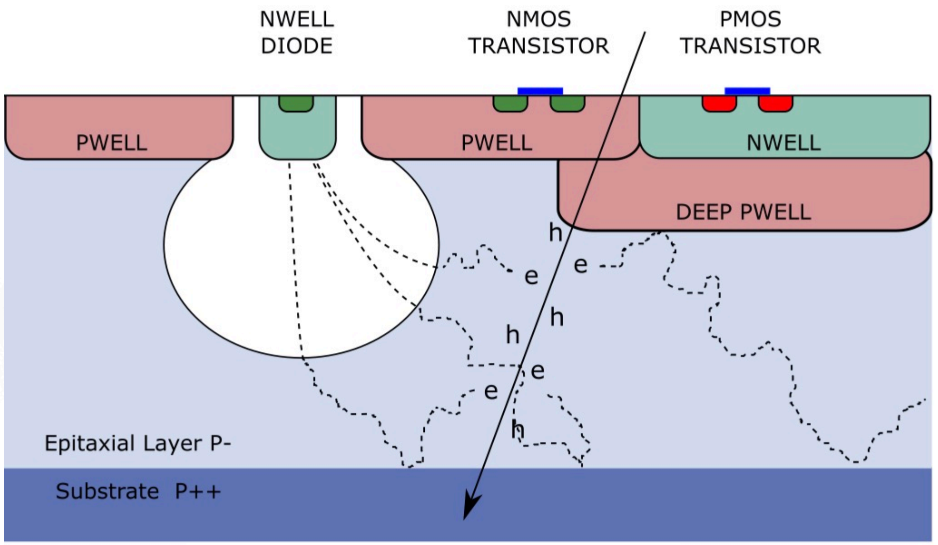
- 6 times in z direction for $p_T < 1$ GeV/c
- 3 times in $r\phi$ direction for $p_T < 1$ GeV/c

» ITS standalone tracking efficiency significantly increased for $p_T < 1$ GeV/c

ALIPIDE pixel chip

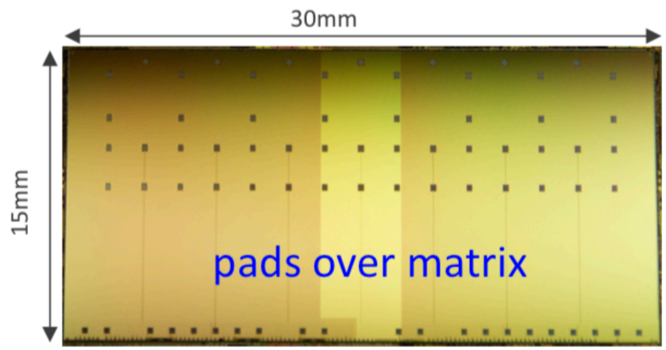


continuous
or
external trigger



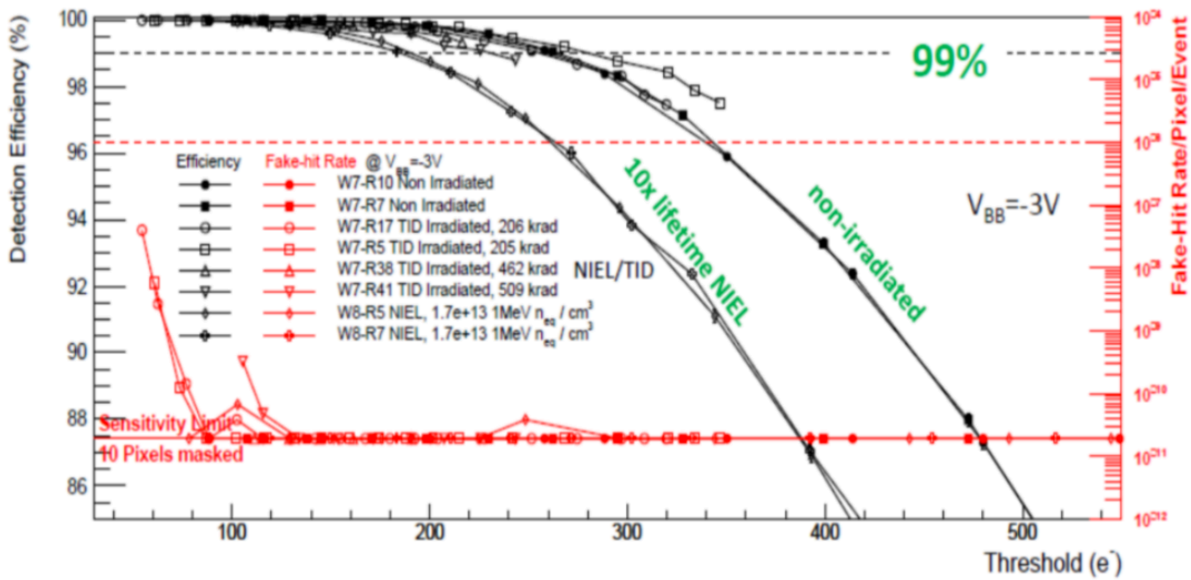
MAPS manufactured in Tower-Jazz 180 nm CMOS

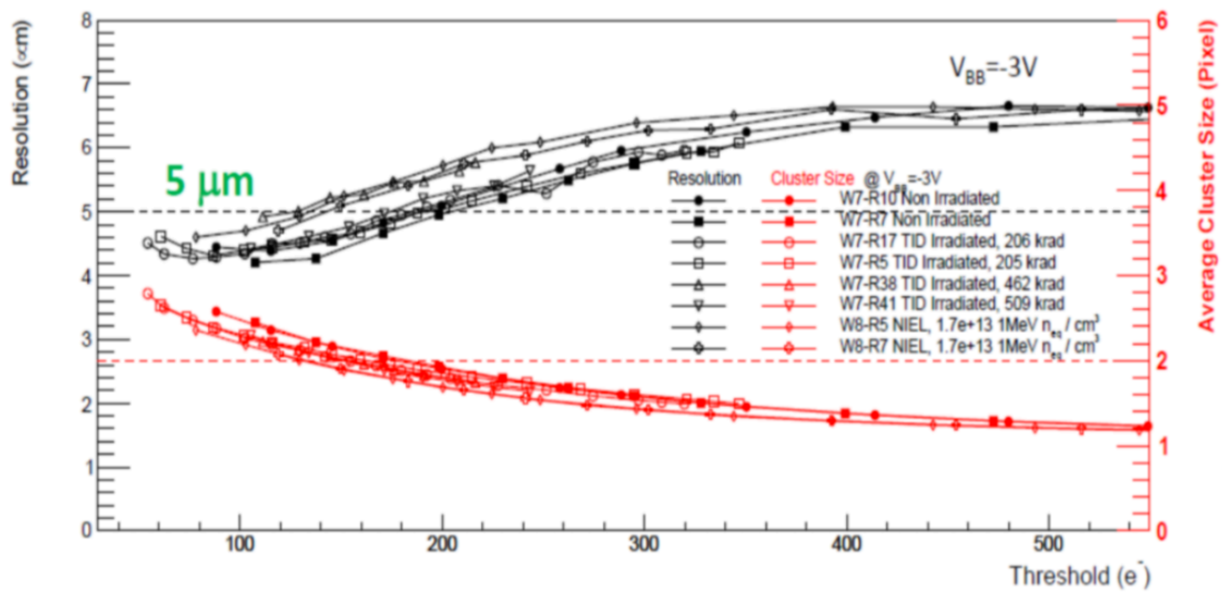
ALPIDE (ALICE PIxel DEtector)
(IB: 50 μm thick; OB: 100 μm thick)



- ✓ 130,000 pixel/cm^2
- ✓ Spatial resolution: ~5 μm (3-D)
- ✓ Integration time: < 10 μs
- ✓ Fake-hit rate: ~10^{-10} pixel/event
- ✓ Power: ~ 300 nW/pixel

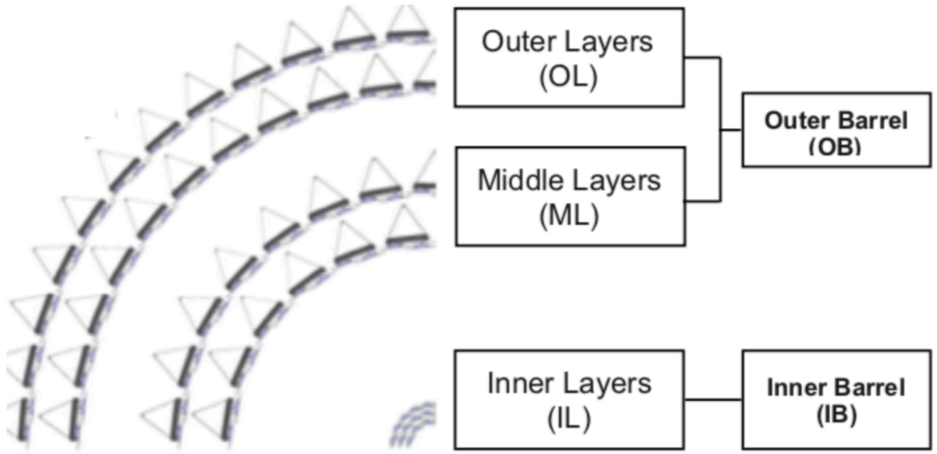
ALPIDE beam test





- Detection efficiency stays at 100% over wide range of threshold value
- Fake-hit rate is below 10^{-11} /pixel/event (requirement 10^{-6})
- Average cluster sizes vary between 1 and 3 pixels (for MIPs)
- Resolution of ~5μm at a threshold of 200 electrons
- Irradiated chips (NIEL/TID) show no degradation in resolution/efficiency

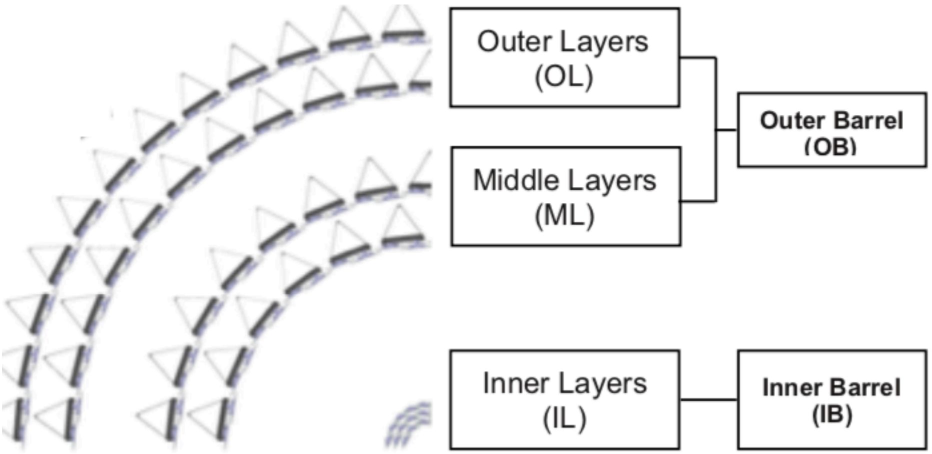
New ITS layout and components



7-layer barrel geometry based on MAPS

- Inner Barrel (**IB**) : 3 layers
- Outer Barrel (**OB**) : 4 layers
- r coverage: (min) 22 – (max) 394 mm
- η coverage: (min) 1.3 – (max) 2.5
- 12.6 Gigapixels
- Total active area ~ 10 m^2

New ITS layout and components

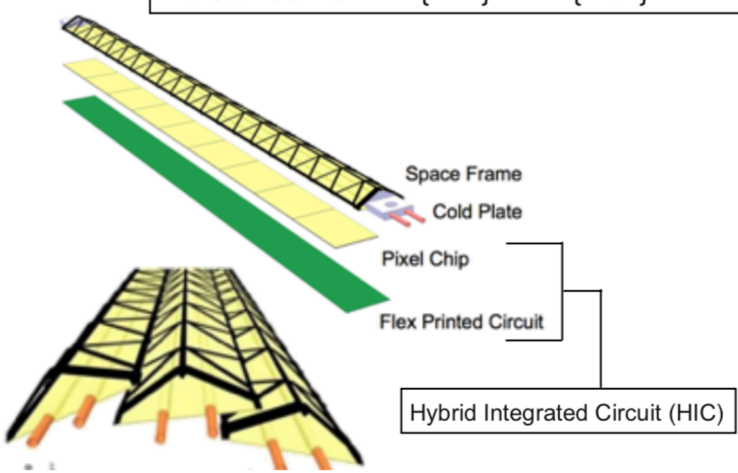


7-layer barrel geometry based on MAPS

- » Inner Barrel (**IB**) : 3 layers
- » Outer Barrel (**OB**) : 4 layers
- » r coverage: (min) 22 – (max) 394 mm
- » η coverage: (min) 1.3 – (max) 2.5
- » 12.6 Gigapixels
- » Total active area ~ 10 m²

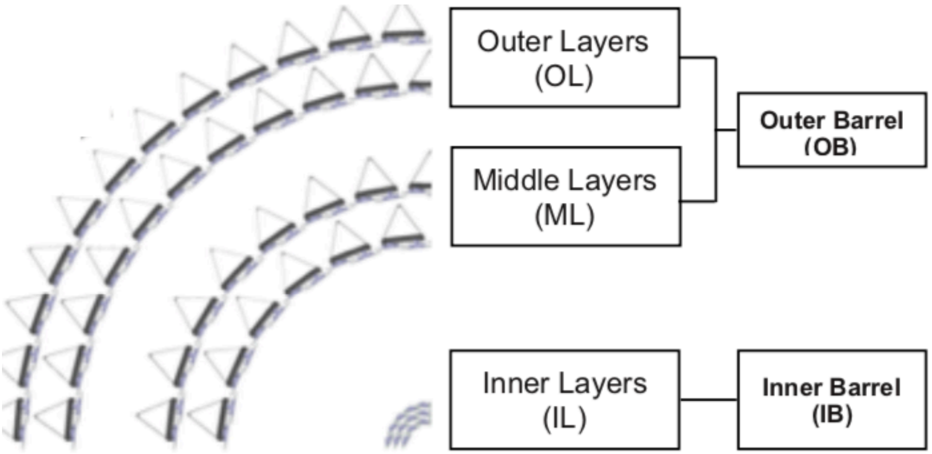
Inner Barrel

- » 48 staves
- » 9 ALPIDE chips on 1 row per stave
- » chip thickness: 50 μm
- » stave length: 290 mm
- » distance from IP: (min) 22 – (max) 42 mm



Tilted staves with overlap

New ITS layout and components

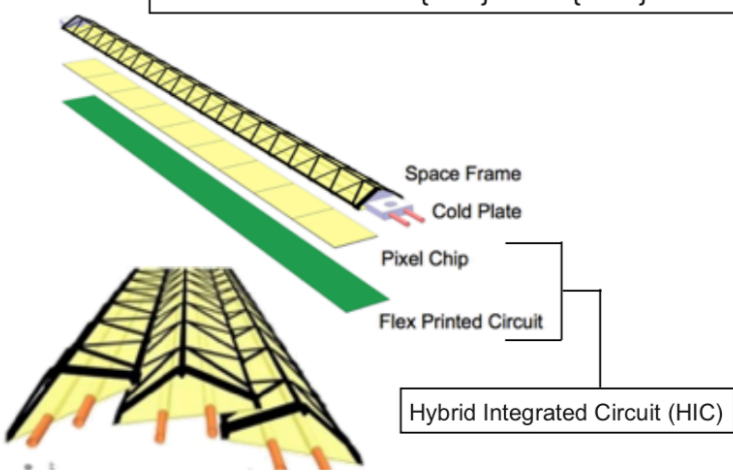


7-layer barrel geometry based on MAPS

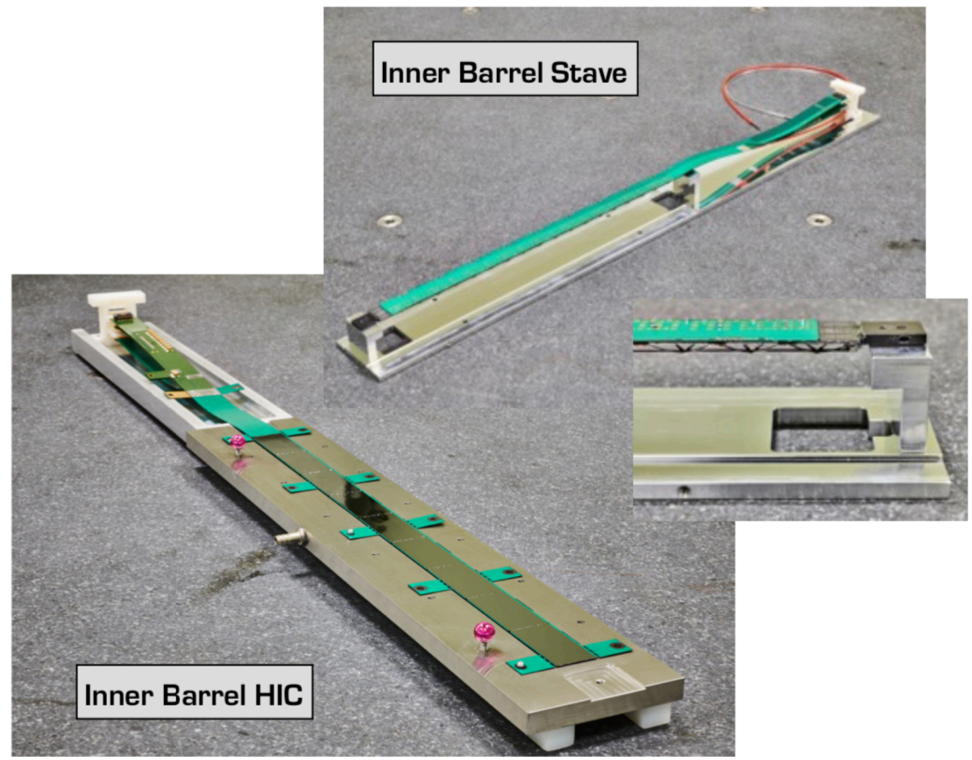
- Inner Barrel (**IB**) : 3 layers
- Outer Barrel (**OB**) : 4 layers
- r coverage: (min) 22 – (max) 394 mm
- η coverage: (min) 1.3 – (max) 2.5
- 12.6 Gigapixels
- Total active area ~ 10 m^2

Inner Barrel

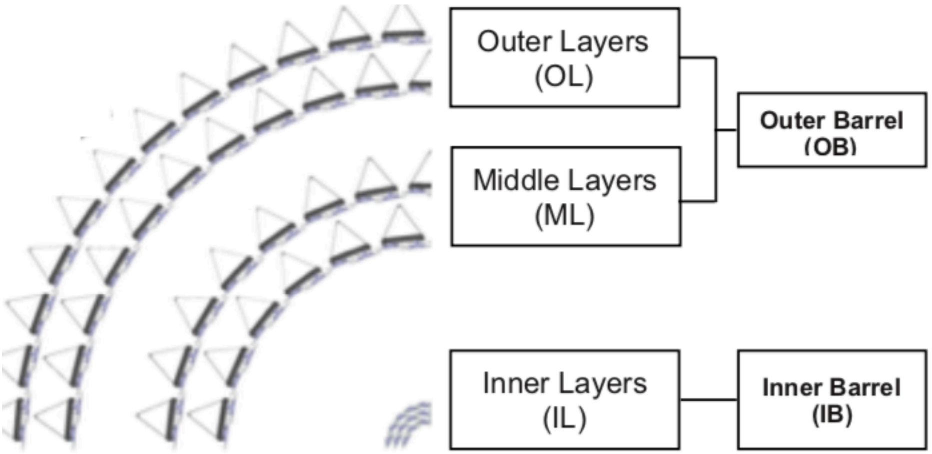
- 48 staves
- 9 ALPIDE chips on 1 row per stave
- chip thickness: 50 μm
- stave length: 290 mm
- distance from IP: (min) 22 – (max) 42 mm



Tilted staves with overlap



New ITS layout and components

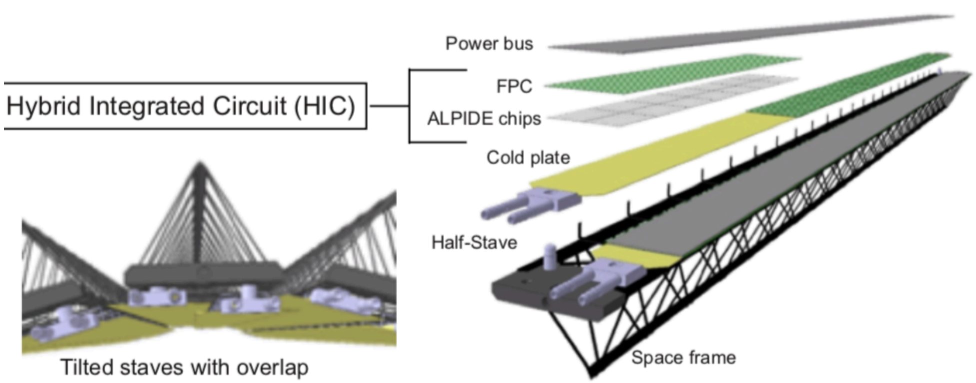


7-layer barrel geometry based on MAPS

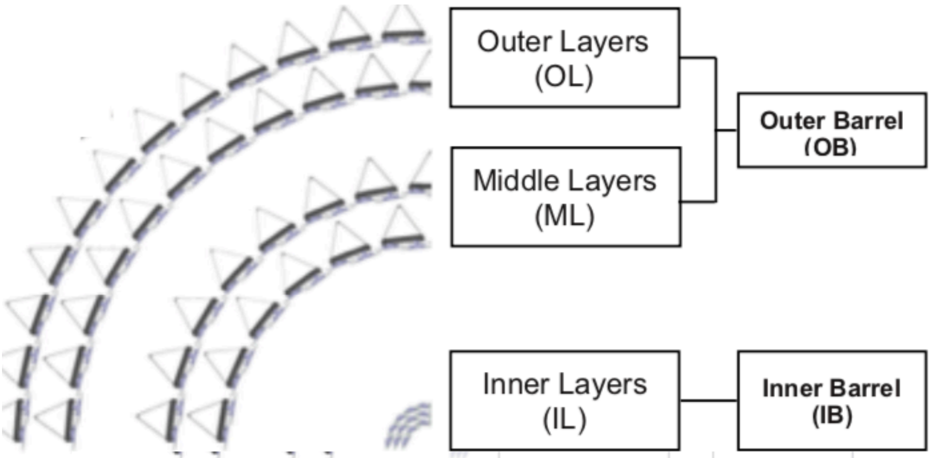
- » Inner Barrel (**IB**) : 3 layers
- » Outer Barrel (**OB**) : 4 layers
- » r coverage: (min) 22 – (max) 394 mm
- » η coverage: (min) 1.3 – (max) 2.5
- » 12.6 Gigapixels
- » Total active area ~ 10 m^2

Outer Barrel

- » 54 staves in ML + 90 staves in OL
- » ML: 56 ALPIDE chips on 2 rows per stave in ML
- » OL: 98 ALPIDE chips on 2 rows per stave in OL
- » chip thickness: 100 μm
- » stave length: 843 – 1473 mm
- » distance from IP: (min) 194 – (max) 394 mm



New ITS layout and components

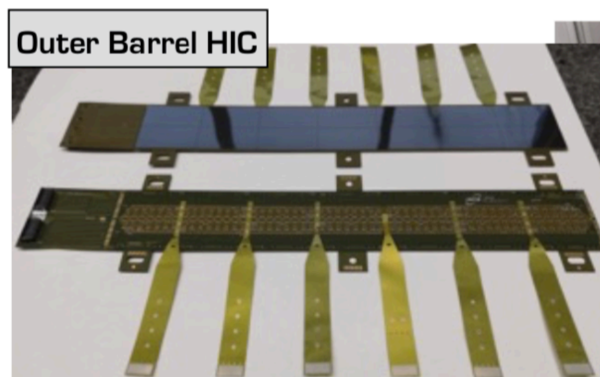


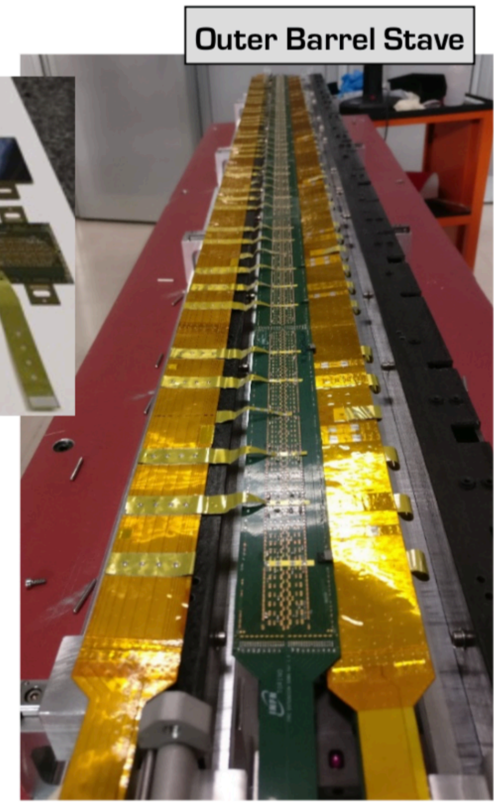
7-layer barrel geometry based on MAPS

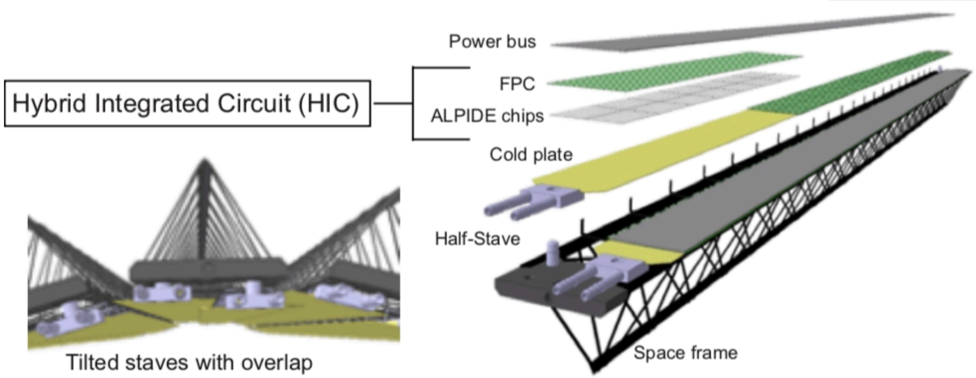
» Inner Barrel (**IB**) : 3 layers
» Outer Barrel (**OB**) : 4 layers
» r coverage: (min) 22 – (max) 394 mm
» η coverage: (min) 1.3 – (max) 2.5
» 12.6 Gigapixels
» Total active area ~ 10 m²

Outer Barrel

» 54 staves in ML + 90 staves in OL
» ML: 56 ALPIDE chips on 2 rows per stave in ML
» OL: 98 ALPIDE chips on 2 rows per stave in OL
» chip thickness: 100 μm
» stave length: 843 – 1473 mm
» distance from IP: (min) 194 – (max) 394 mm







Progress of ITS upgrade project

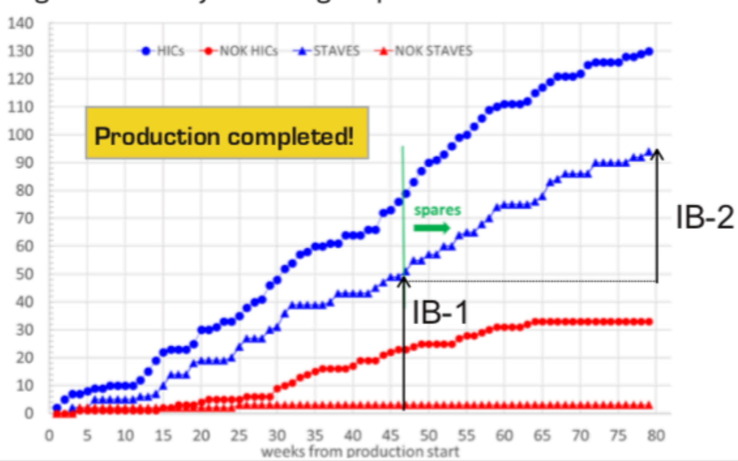
ALPIDE chips

» Institutes:
50 μm: CERN
100 μm: Yonsei, Pusan

» Total # of chips tested: ~70000
» Total # of wafers: ~1700
» Total yield: 63.7%
» Series test ended in mid 2018

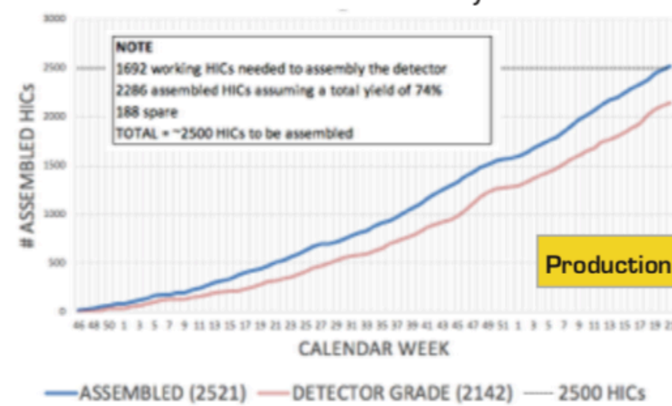
Inner Barrel HICs and Staves

» Institutes: CERN
» 95 staves assembled with a yield of 73%
  » Enough for 2 fully working copies of IB

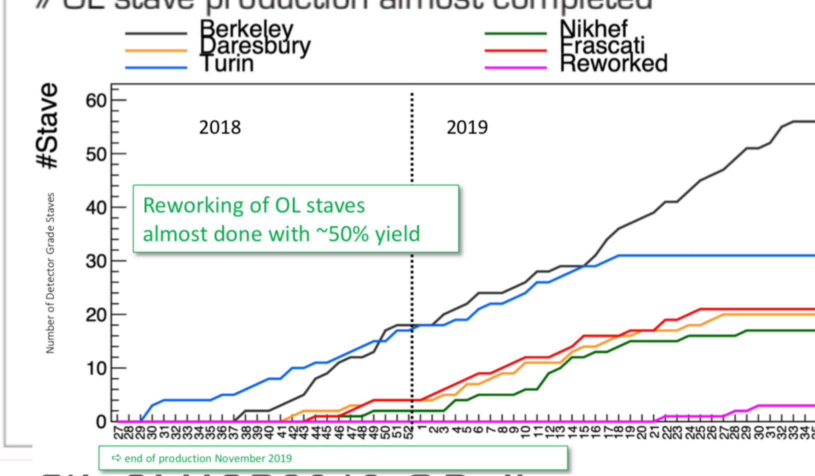


Outer Barrel HICs and Staves

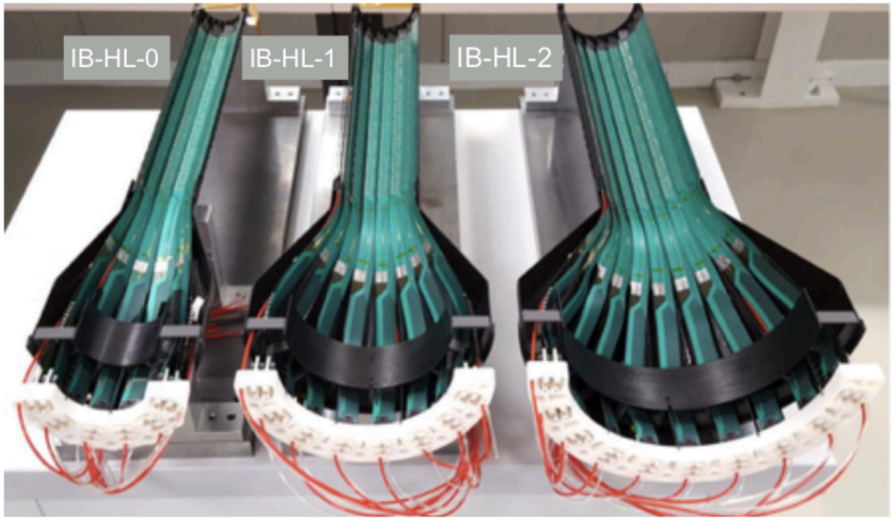
» HIC institutes:
Bari (IT), Liverpool (UK), Pusan (KR), Strasbourg (FR), Wuhan (CN),
» ~2500 HICs assembled with a yield of 85%

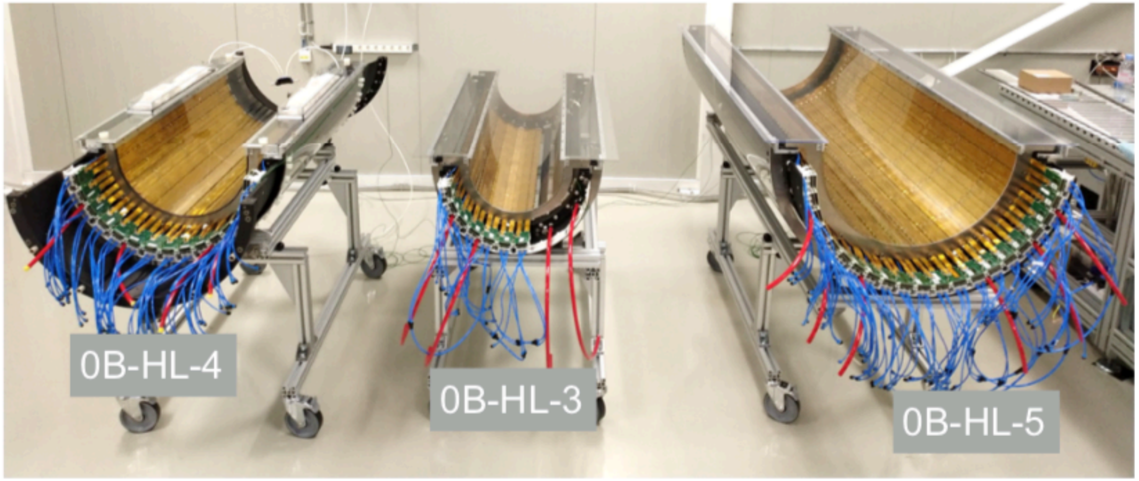


» Stave institutes:
Berkeley (US), Daresbury (UK), Frascati (IT), Nikhef (NL), Turin (IT)
» Yield above 90%
» OL stave production almost completed



Commissioning

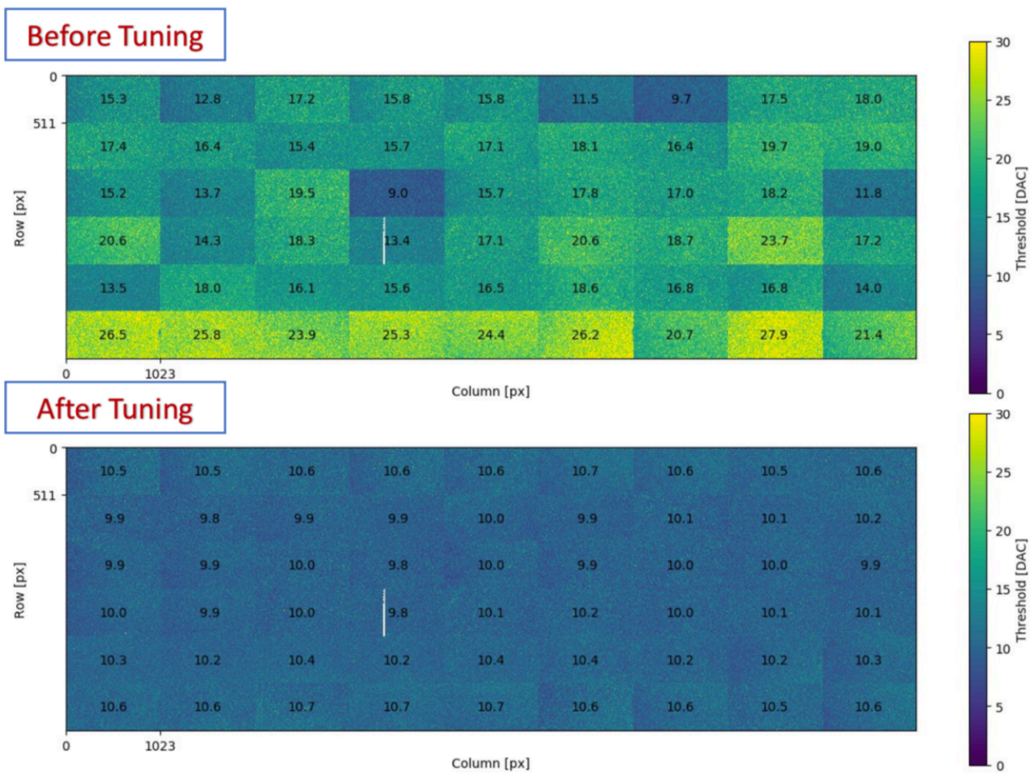


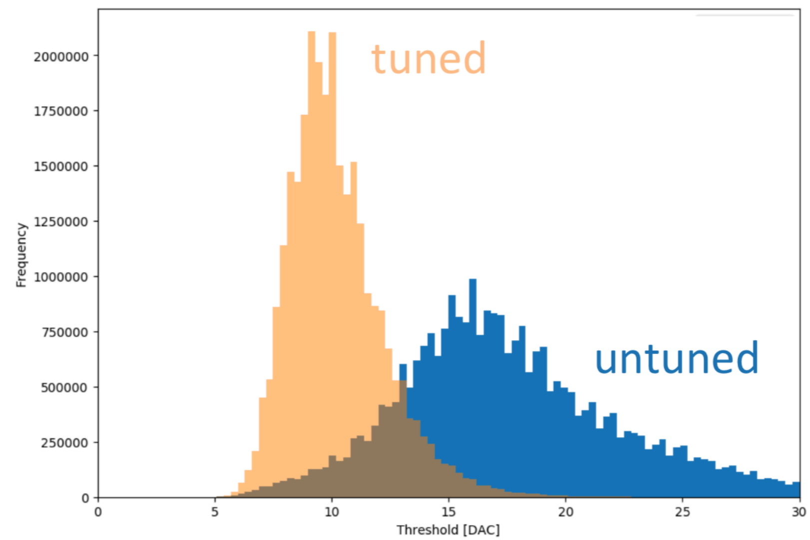


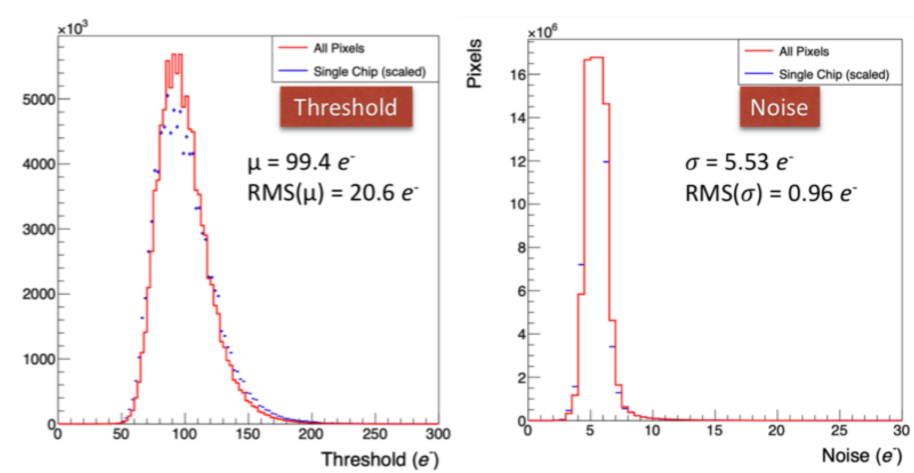
- ✓ Cooling plant, Power and Read-out racks, Trigger and DAQ system be constructed for testing
- ✓ DCS and DAQ systems: development of full functionalities ongoing
- ✓ Commissioning before installation: data taking with cosmic rays and calibration scans
- ✓ **It have started in May.2019, and scheduled to be completed in May 2020**
- ✓ **Installation, and 6-months global alignment from June 2020 to Feb 2021**

Commissioning(threshold tuning)

- Adjustment of front-end parameters to equilibrate the charge thresholds
- Achieving uniform response across the detector, verified on a spare IB half-layer

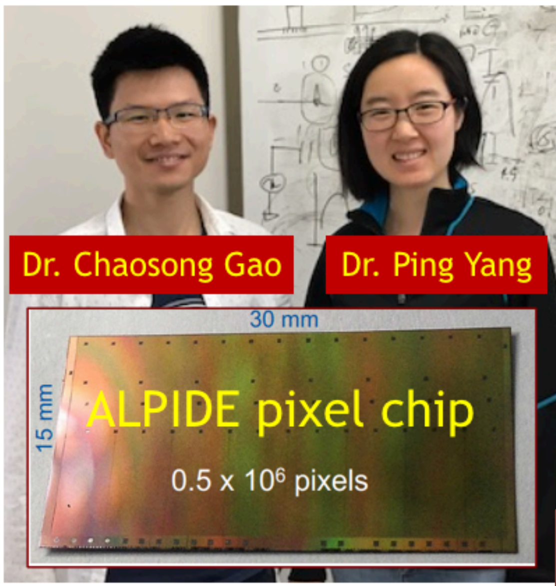




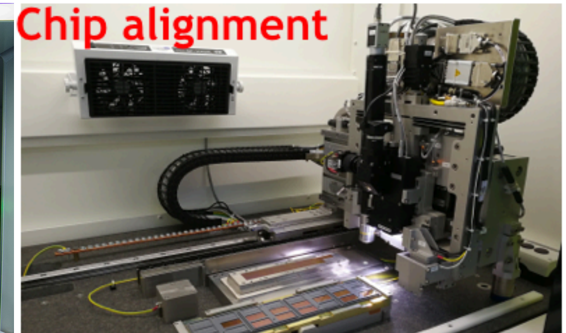


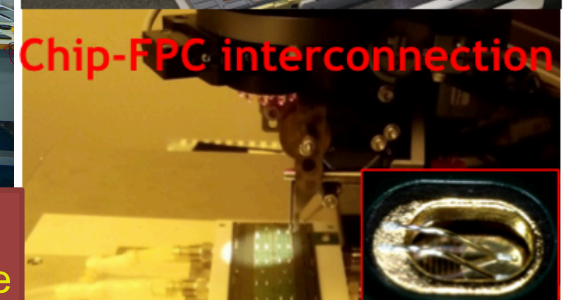
Threshold and noise after tuning for an OL Stave (~100M pixels) compared with a single chip test data

Effort from CCNU on ALICE/ITS



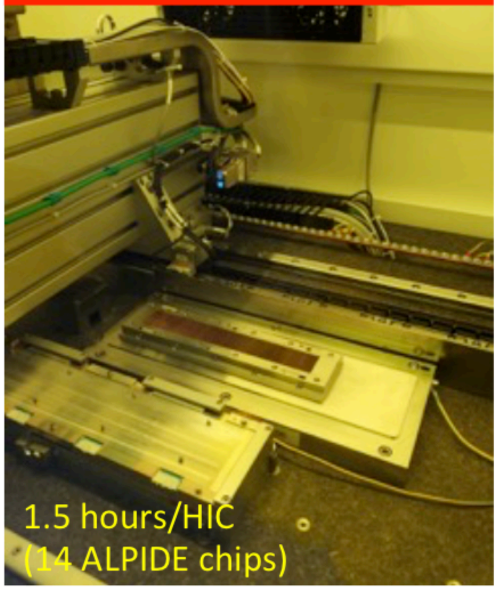
Liang、Yalei、Wenjing、Wenjing、Biao
Kai、Jun、Yaping (CCNU coordinator on the ITS OB HIC production)、Daming



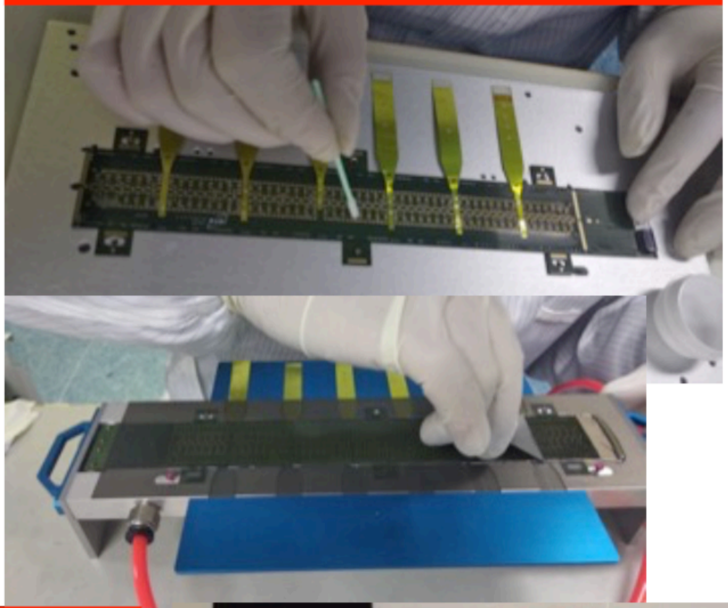


Effort from CCNU on ALICE/ITS:OB HIC assembly test

1. Chip Alignment

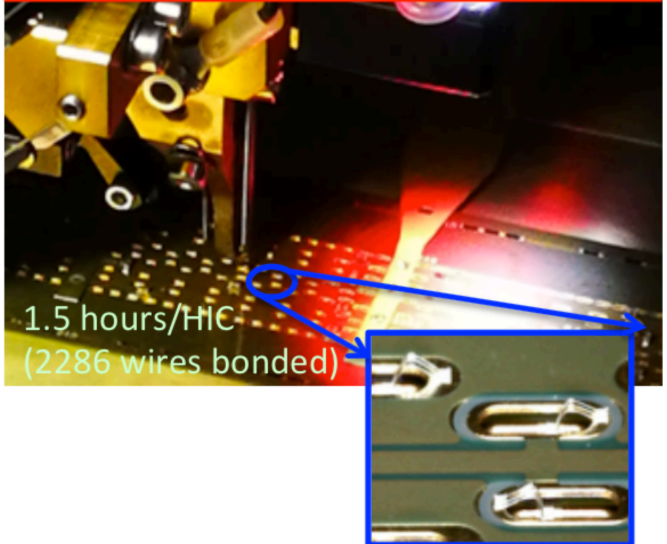


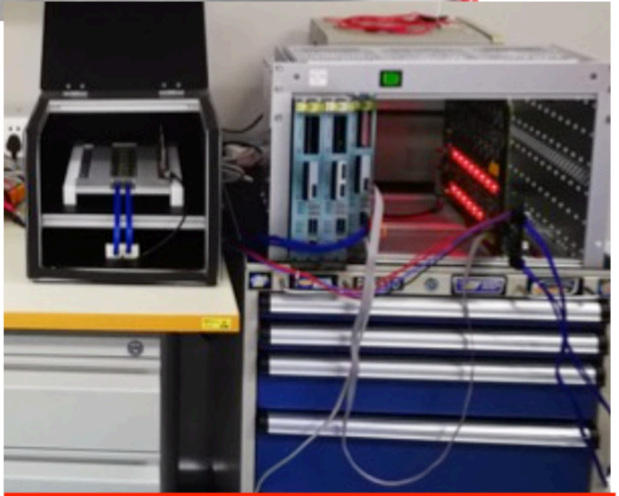
2. FPC preparation & glue spreading



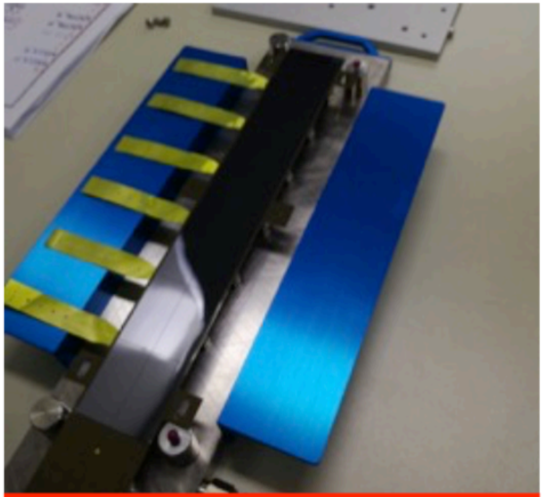
3. Pre-curing & fully curing

4. Wire-bonding





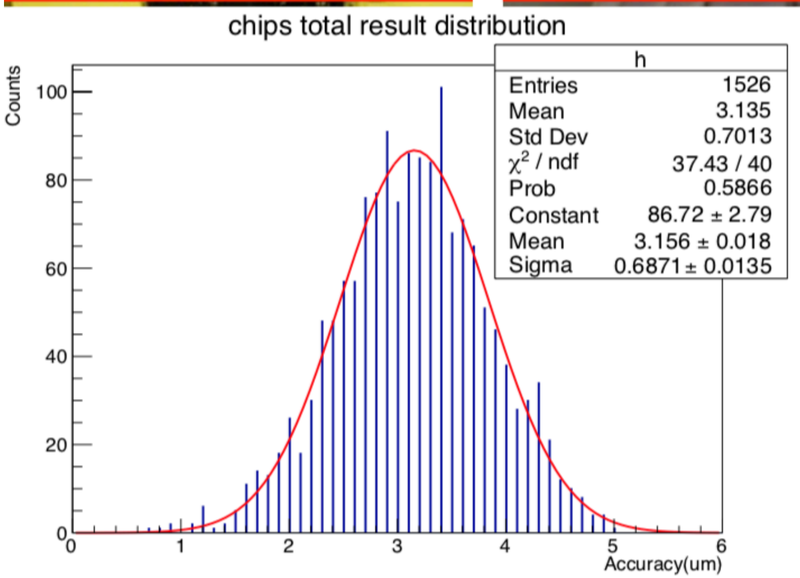
5. Qualification & endurance testing



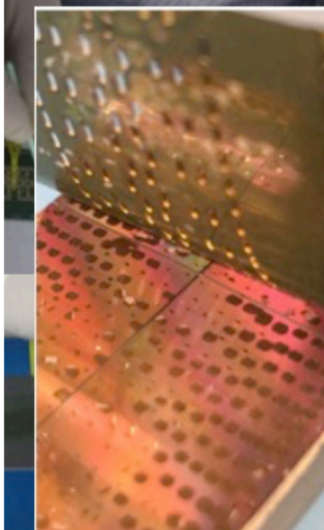
6. Qualified ITS OB HIC

Effort from CCNU on ALICE/ITS:OB HIC QA

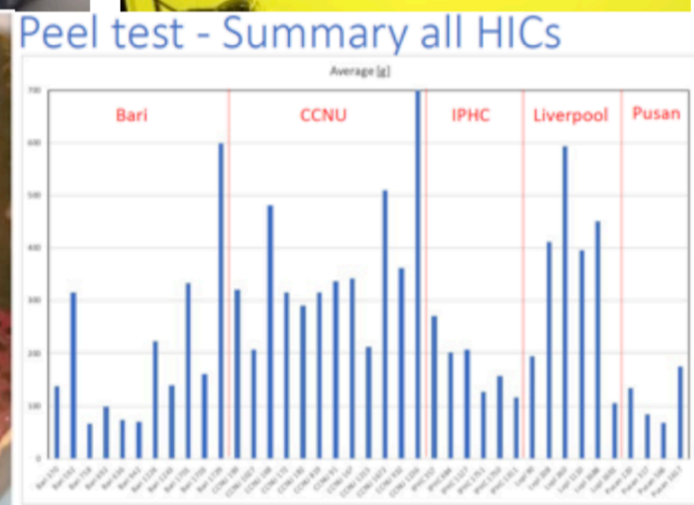
1. Chip Alignment



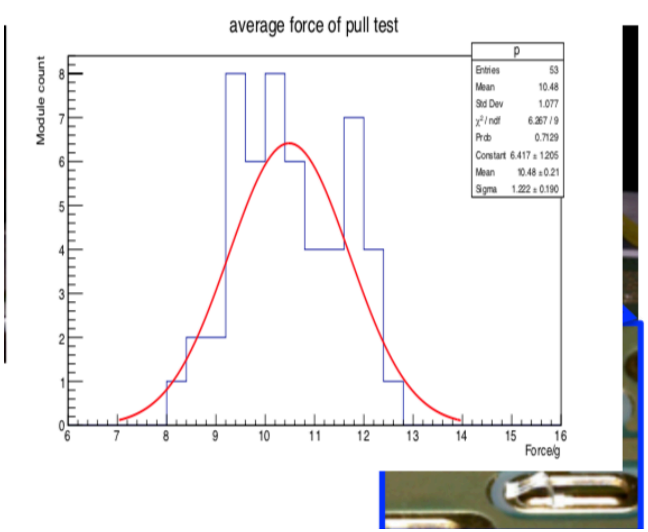
2. FPC preparation & glue spreading

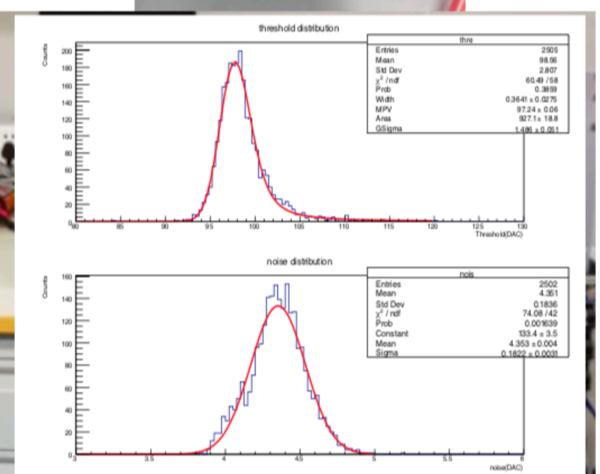


3. Pre-curing & fully curing

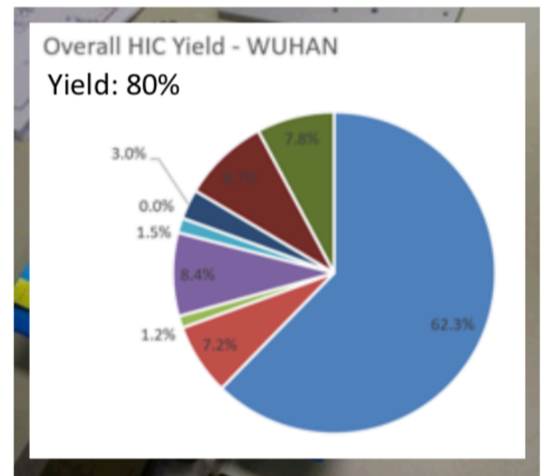


4. Wire-bonding



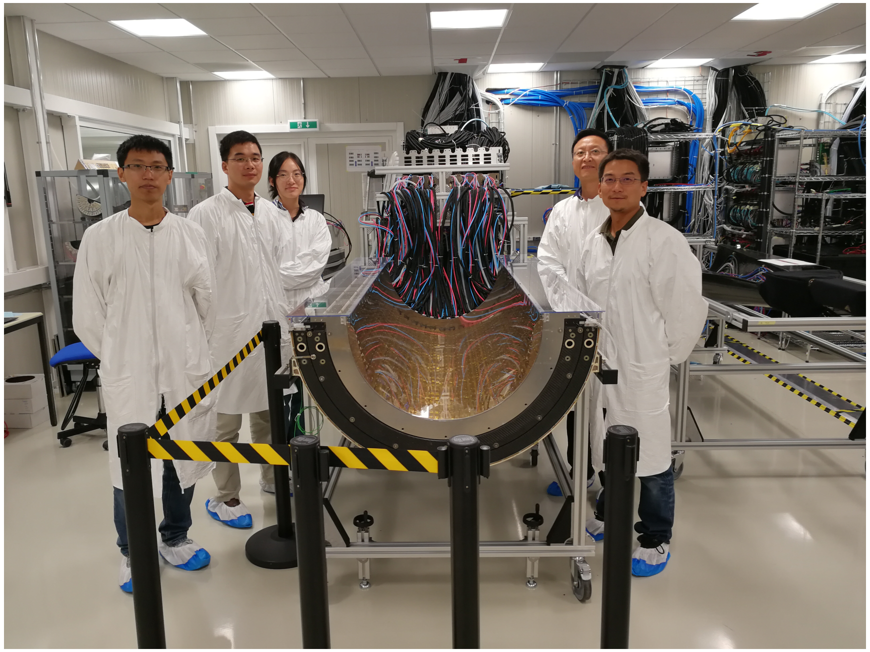


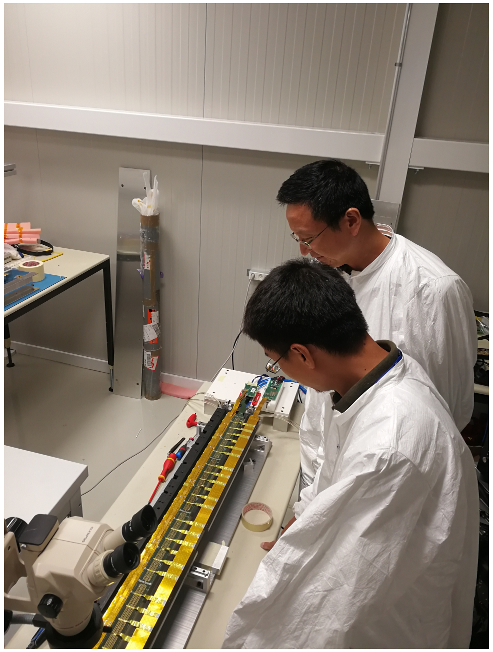
5. Qualification & endurance testing

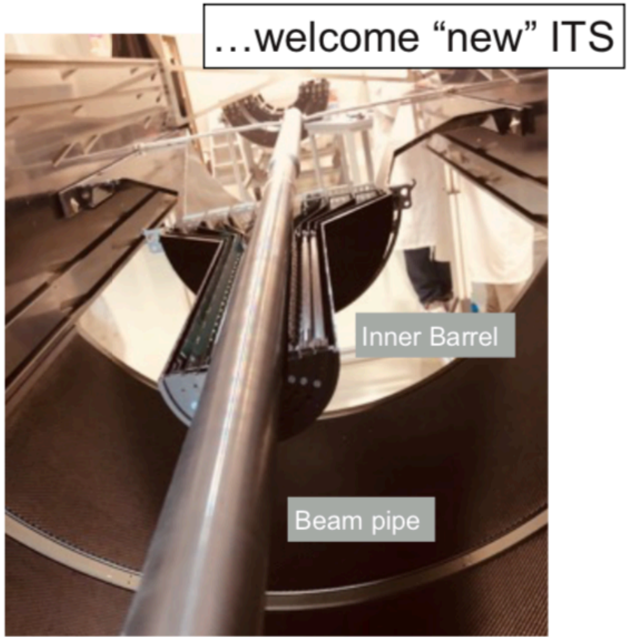


6. Qualified ITS OB HIC

Effort from CCNU on ALICE/ITS







- **Efforts on ALPIDE chip design since 2012**
- **Take charge of 20% ALICE/ITS OB HIC module assembly and test (~10000 ALPIDE chips)**
- **Pre-series production started in Dec. 2017**
- **Series production started in April, 2018, and have been completed in June, 2019**
- **450 HICs have been constructed and tested, production yield around 80%**
- **Calibration, alignment and commissioning are ongoing at CERN**

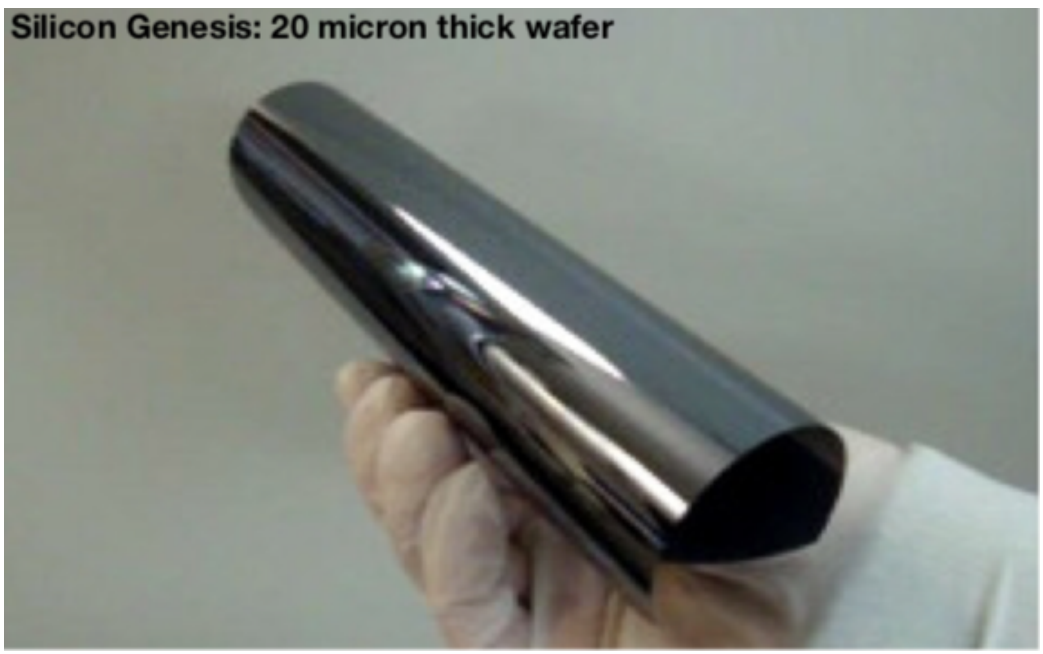
Summary

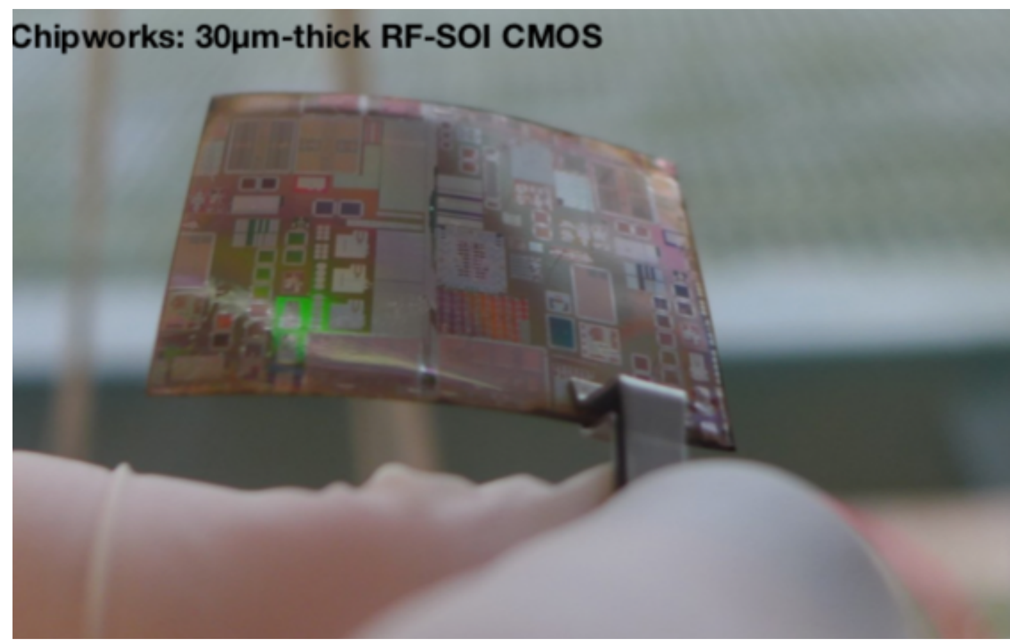
- **Requirements of the new ITS**
  - ✓ Improve vertex and tracking performance
  - ✓ Enable Pb-Pb collision readout rate at 100 kHZ
- **ALICE ITS upgrade project**
  - ✓ Staves of IB and OB have been constructed
  - ✓ Commissioning and calibration are ongoing
- **OB HIC production and testing at CCNU**
  - ✓ Series production ended successfully at the end of June
  - ✓ All qualified HICs have been delivered to stave construction site, production yield ~80%
  - ✓ Continue to put effort on the ITS commissioning & calibration
  - ✓ Contribute to development next generation MAPS chip of ultra-thin wafer -scale

Thank you for your attention!

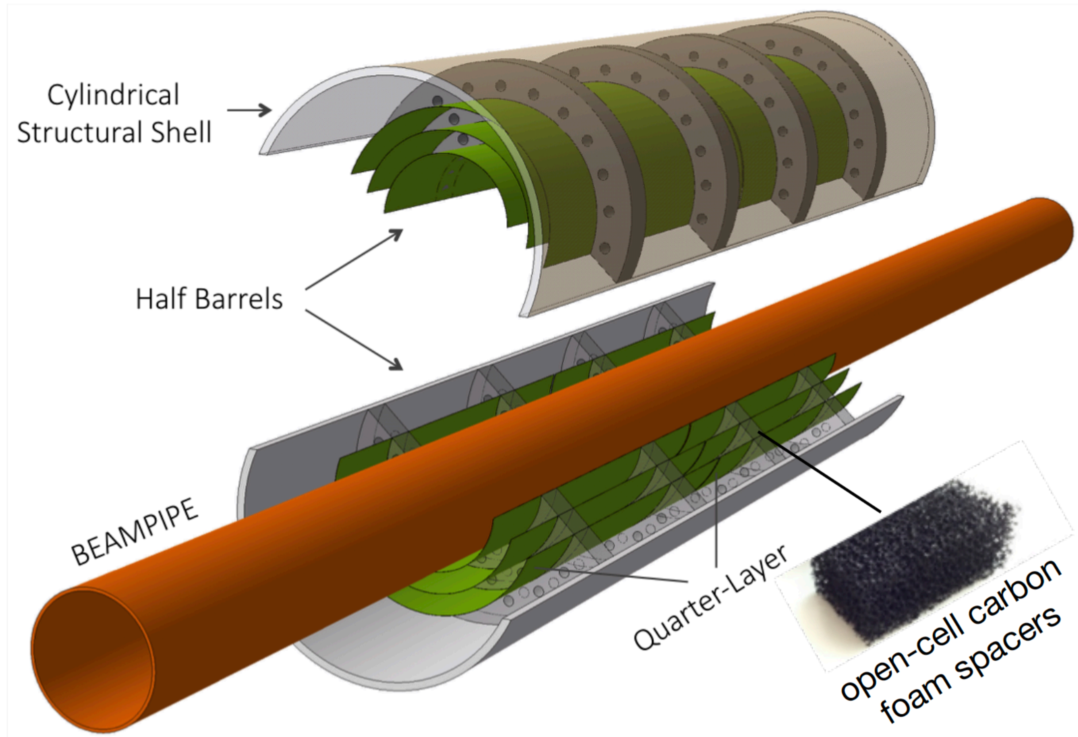
Outlook: Bending silicon!

- **Driving requirements of ITS2 upgrade**
  - Reduce material budget
  - Move closer to beam-line
- **can be pushed further using technologies that are quickly becoming mature**
  - Silicon stitching a sensors of ~ 10x10 cm2
  - Thinning to ~30 μm a cylindrical sensors





Outlook: Bending silicon!



Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensors dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

Thank you!