華中師範大學

SiPM readout ASICs for Calorimeter of High Energy Physics

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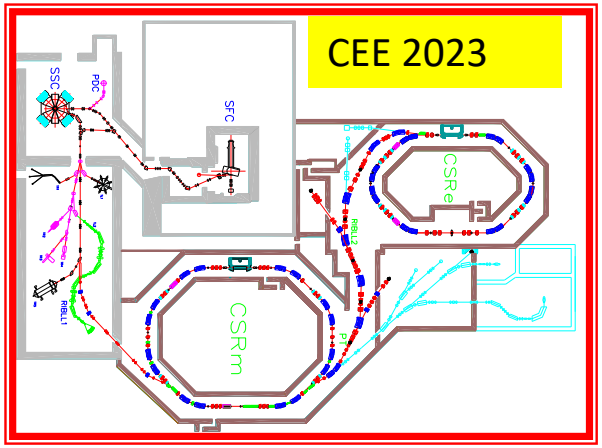
Outline

- ✓ Introduction on HIRFL/CSR Calorimeter detector
- ✓ SiPM features and first readout prototype
- ✓ Blocks optimization
  - Timing： discriminator and jitter
  - Energy： TOT and high speed ADC
- ✓ Summary and outlook

HIRFL/CSR Calorimeter detector

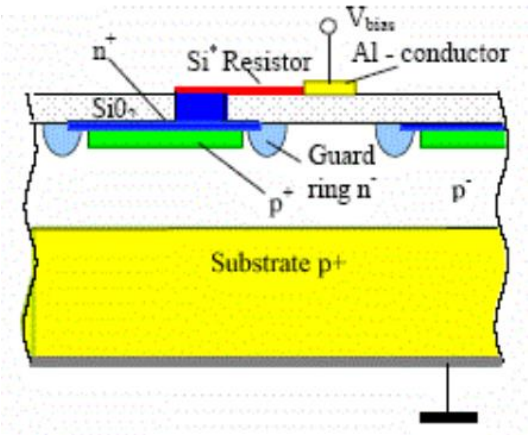
Hua Pei's talk 25th pm

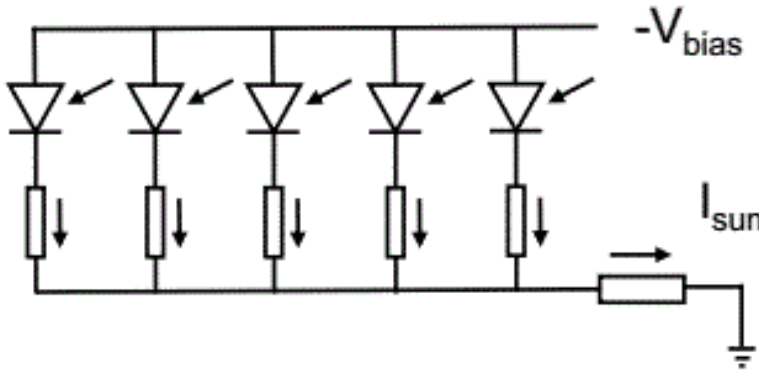
CEE key prameters: (500-1000MeV/u)
- Momentum resolution: ⩽ 5%
- Space resolution: ⩽ 50ps
- Event rate: ⩾ 10^4/s
- Date writing rate: ⩾ 500MB/s



- Can be as a trigger detector, require fast discriminator response
- Event rate > 10 MHz
- Fast discriminate time < 500 ps
- Energy resolution < 20% / √E(GeV)

SiPM features





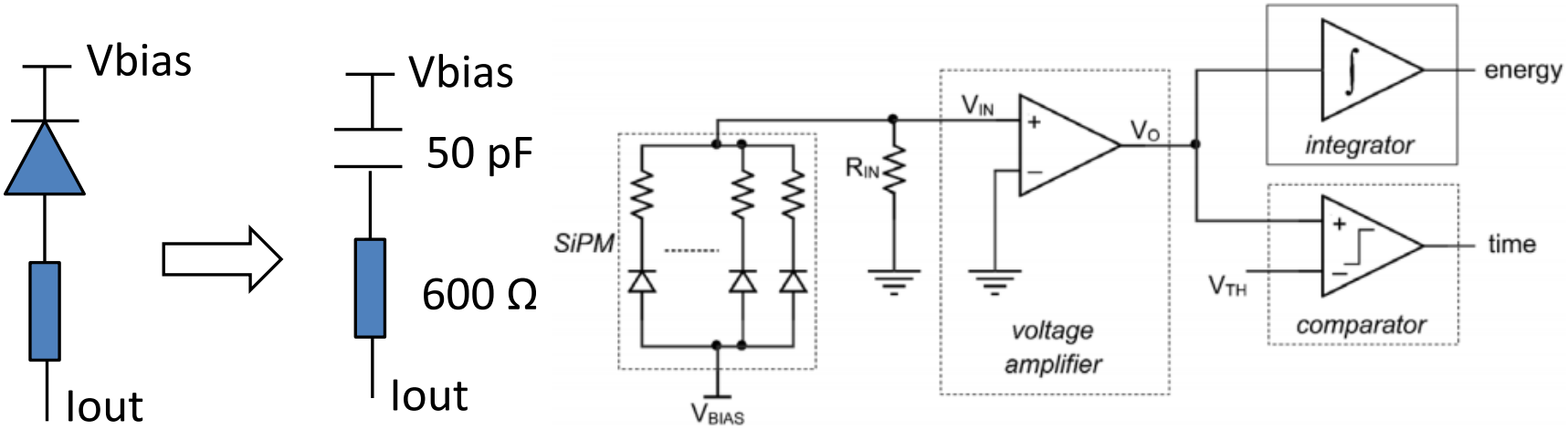
~90000 G-APD cells in parallel

BNU SiPM 11-3030C

- Fast timing response : < 200 ps
- High gain : > 2 x 10^5
- Sensor is small : effective area ~3 x 3 mm^2, pitch 10 μm
- Low breakdown voltage : 27.5±0.4 V
- Not sensitive to magnetic field
- Ultra-high single photon resolution

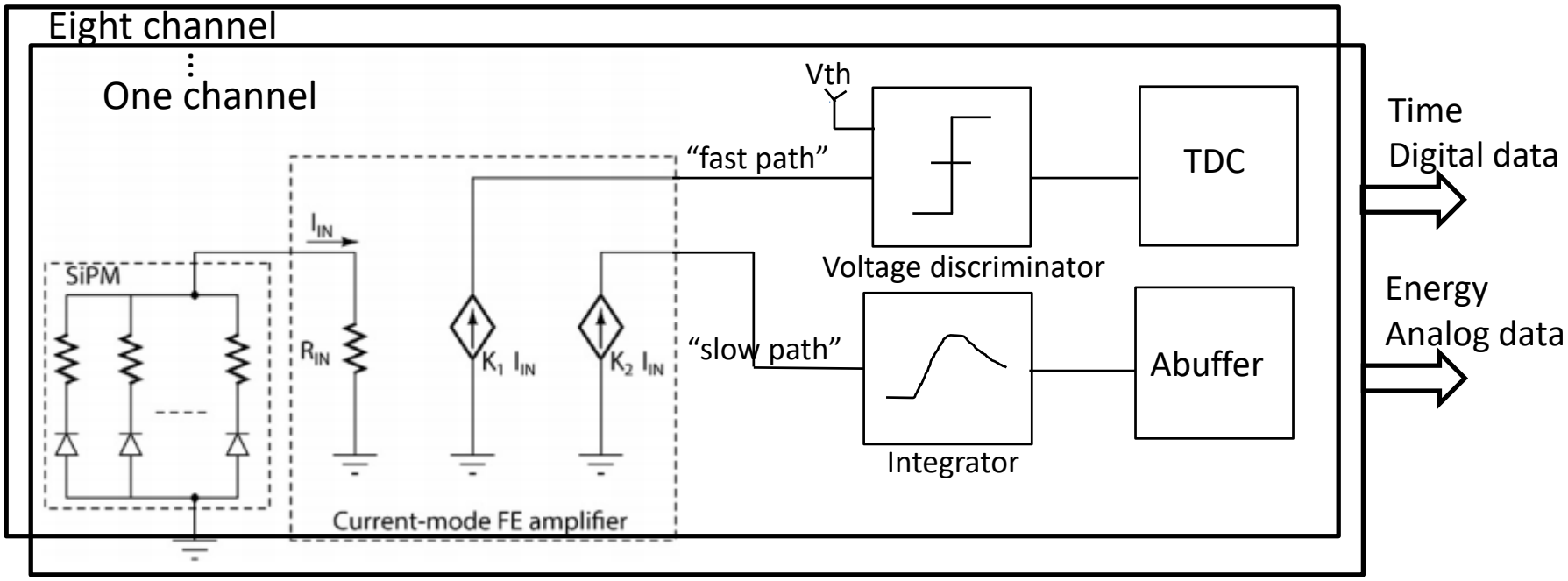
SiPM features

SiPM simplified equivalent model



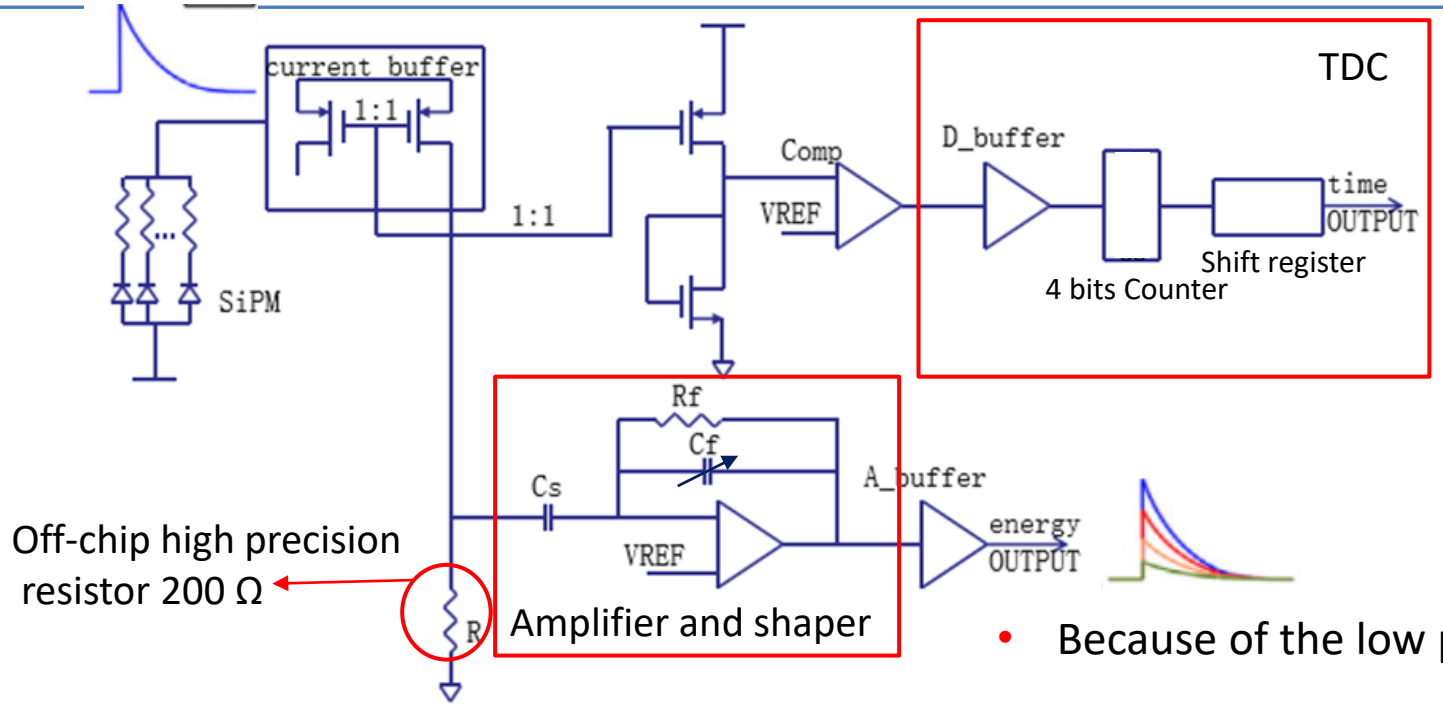
- For such a large capacitance, traditional voltage mode is slower than current mode when the same current is used
- Charge Sensitive Amplifier(CSA) is not suitable because of the high gain of SiPM
- Current mode is used to improve the time response

First readout prototype design



- GSMC 130 nm process, power supply 1.2 V, standard CMOS process is fine
- Current conveyor divides the input current into "fast" time measurement and "slow" energy measurement
- 8 channels, linear input current : 20 μA-3mA, 2.4M-500M e-

First readout prototype design



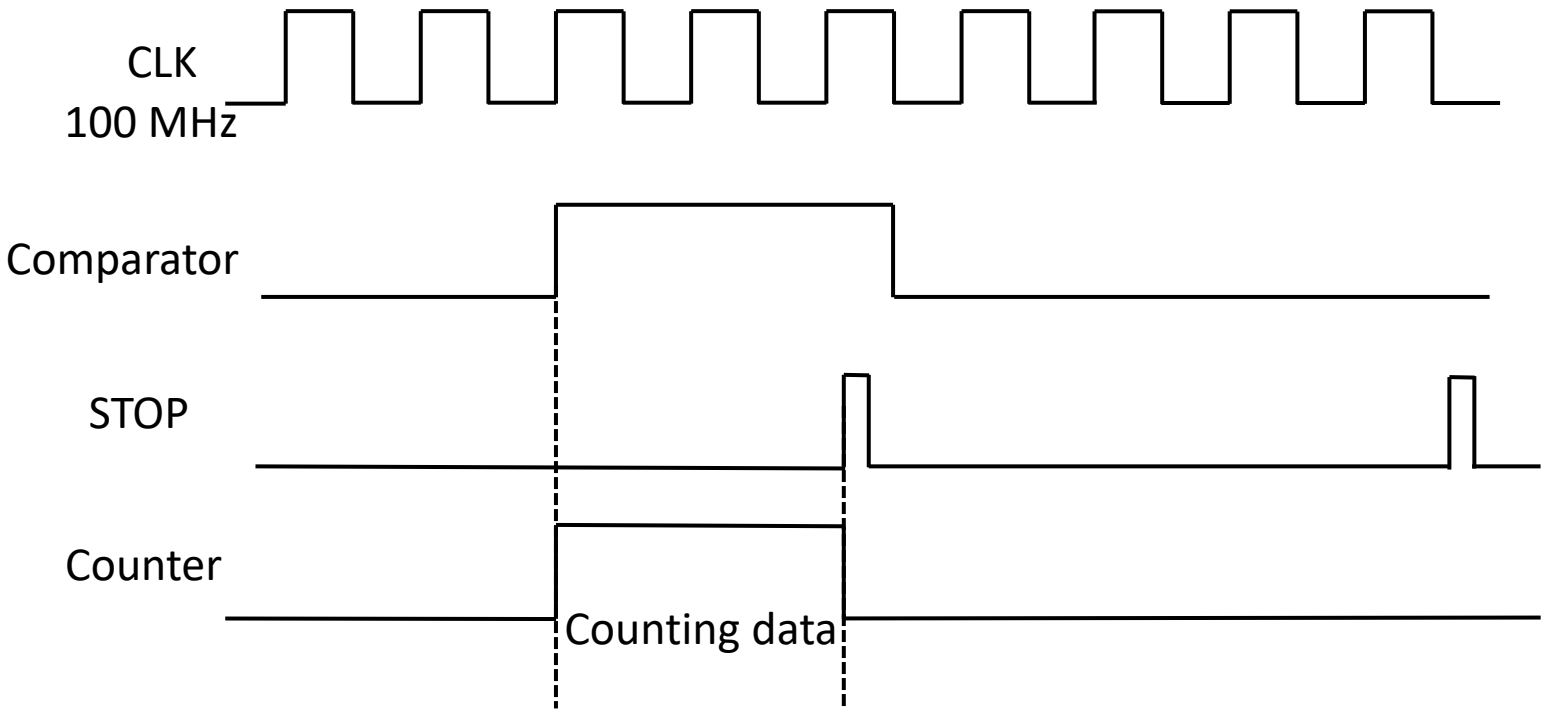
Cs	Cf	K1	K2	K3	In	Out
200f	16f	0	1	1	20uA	25mV
200f	16f	0	1	1	100uA	110mV
200f	100f	1	0	1	100uA	34mV
200f	100f	1	0	1	501uA	174.6mV
200f	600f	1	1	0	501uA	34.7mV
200f	600f	1	1	0	3mA	201.4mV

- Because of the low power supply voltage, add gain-selector switch to improve the input range
- The linear range of the input signal is 20 μA to 3 mA
- Peaking time ~14 ns

  decay time ~50ns

First readout prototype design

TDC timing diagram

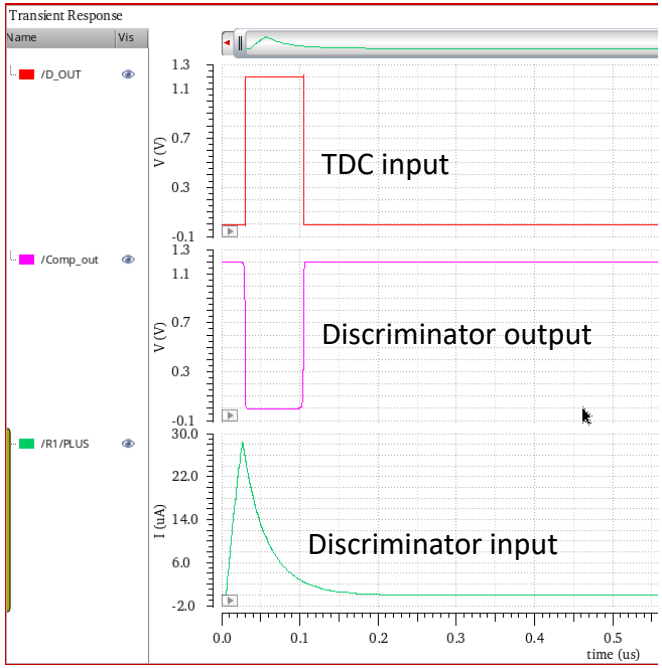


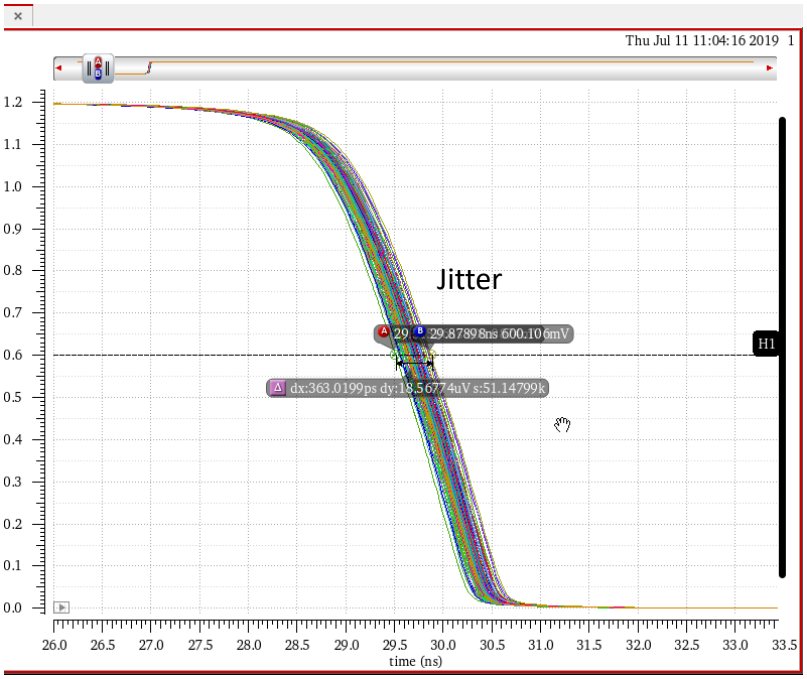
arrival time = STOP time – counter data* CLK cycle

- Increase CLK frequency can improve TDC accuracy
- 100 MHz CLK frequency, 10 MHz event rate, 4 bits counter is enough

First readout prototype design

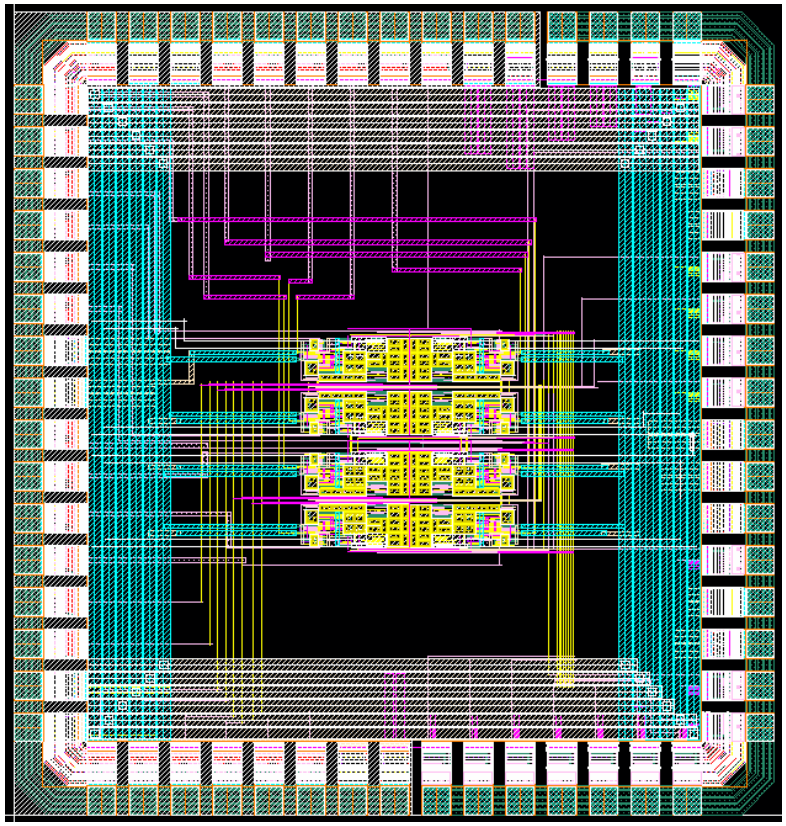
Discriminator jitter simulation





- Rising time of the discriminator < 1.5 ns
- Jitter < 400 ps, jitter affect the time measurement accuracy

First readout prototype design

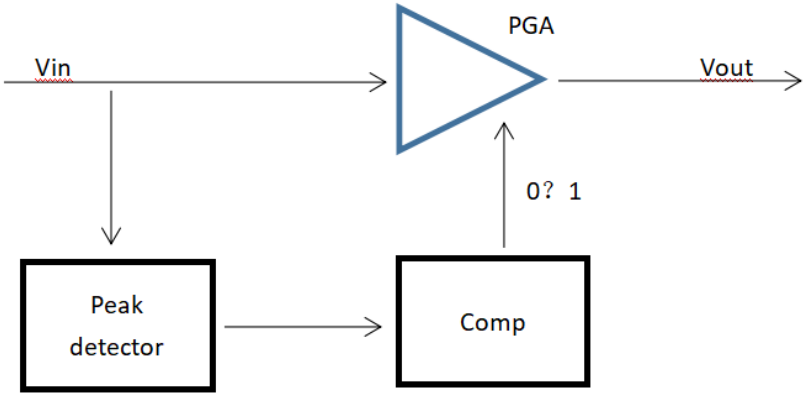


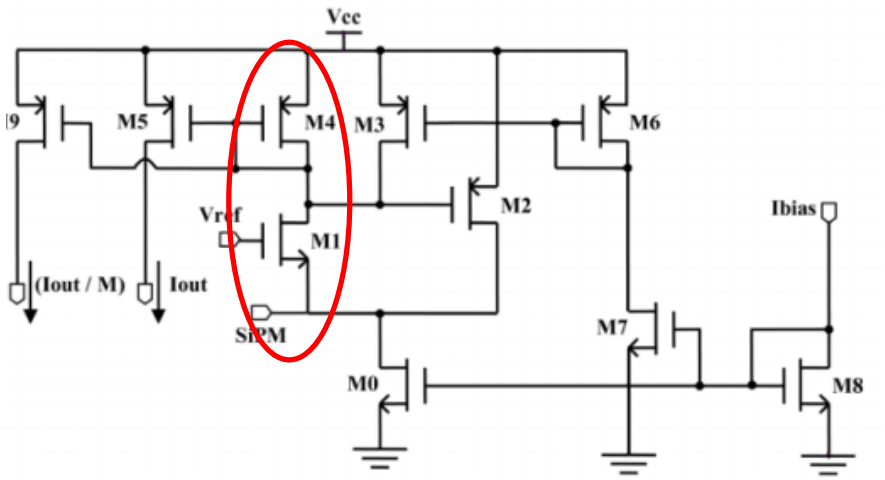
- Chip area 2 mm x 2 mm
- Tapeout June 2019, will be back Nov 2019
- Test board is ready to tape out will be back in two weeks

Module	Current value
Current conveyer	100 uA
Amplifier_CS	1.2 mA
A_Buffer	1.6 mA
Comp	450 uA

Blocks optimization

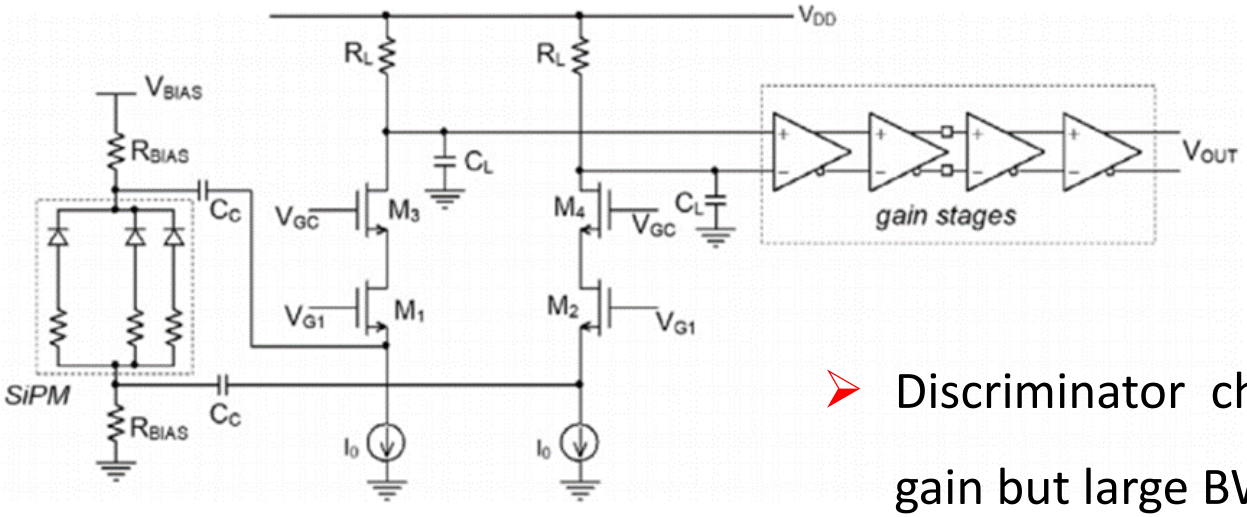
Blocks optimization: input range

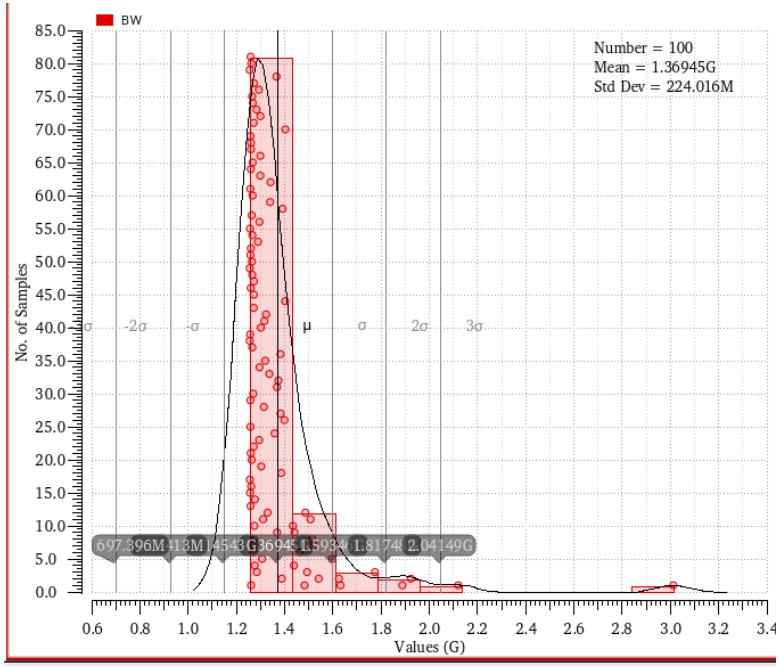




- If the input dynamic range is more than two orders of magnitude, need PGA(Programmable Gain Amp) to adjust the optimal output range
- PGA need feedback, feedback may slow down the circuit
- Optimize the input current conveyer, change the input two transistors to low Vth ones, and increase the power consumption, improve the input range to 10 μA – 10 mA

Blocks optimization: timing test



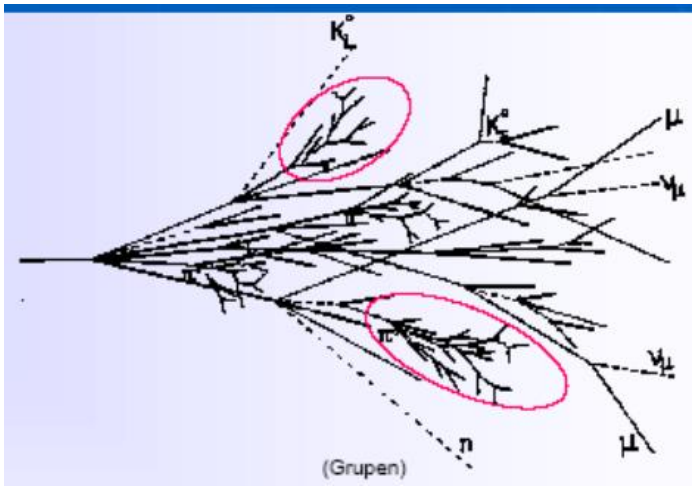


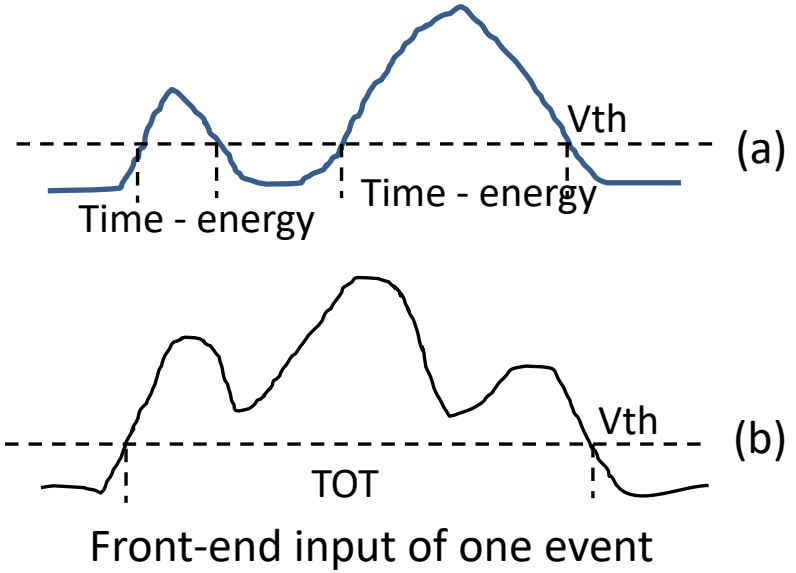
- Discriminator changes to multiple low gain but large BW amps
- Four stages, minimum BW is 1.2 GHz, for a large signal, jitter < 25 ps
- High power consumption

Current input	Jitter(rising)
100 uA	170 ps
720 uA	23 ps
3 mA	15 ps

Blocks optimization: Energy test

Energy test error sources

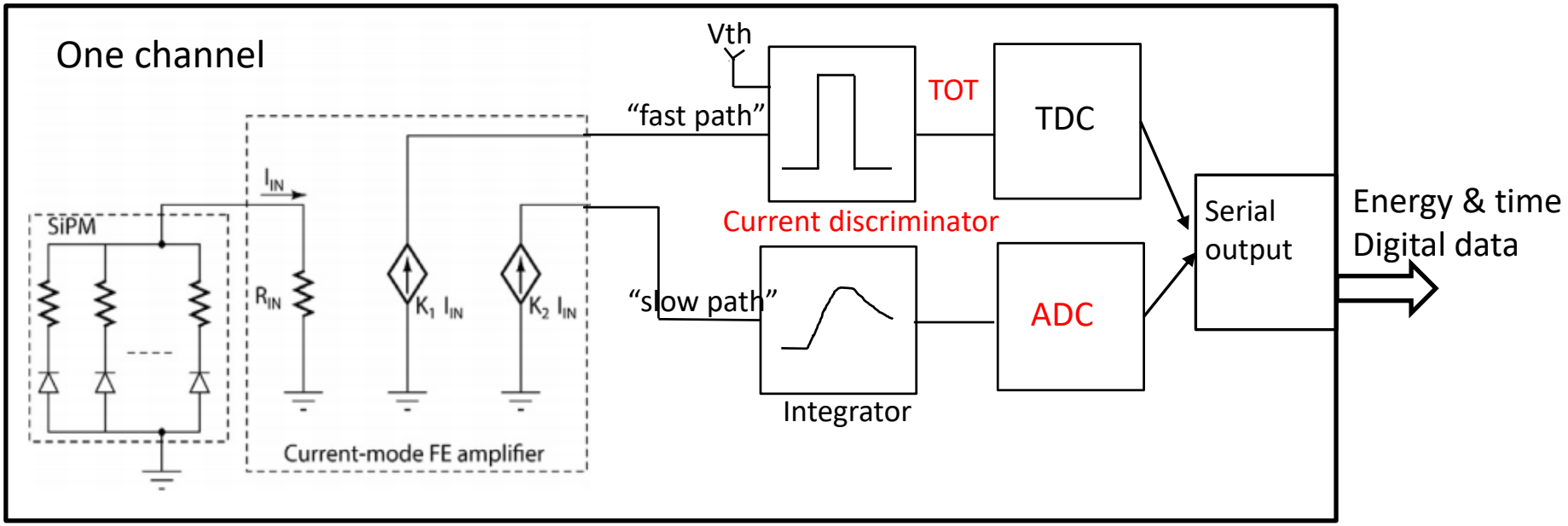




Front-end input of one event

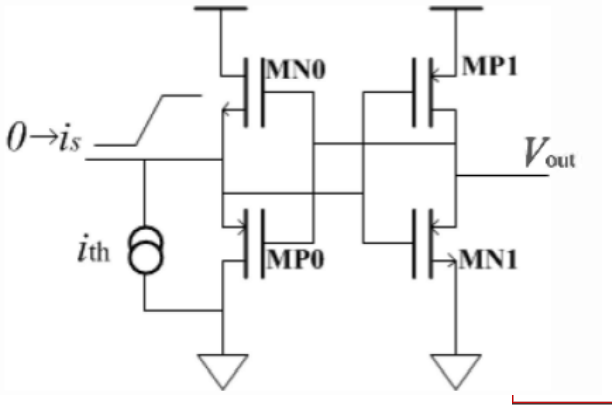
- High energy hadrons interact strongly with the nuclei of the medium through the medium to produce several secondary hadrons -> large energy fluctuations
- After optical fiber, one event will create multiple peak values
- TOT and high speed ADC both used to measurement the energy

Blocks optimization: Energy test

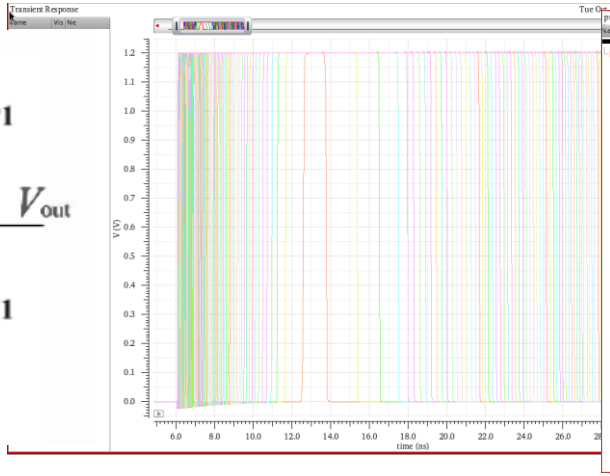


- Current discriminator has fast rising and falling time, low jitter
- High speed sampling ADC
- TOT also used for energy measurement

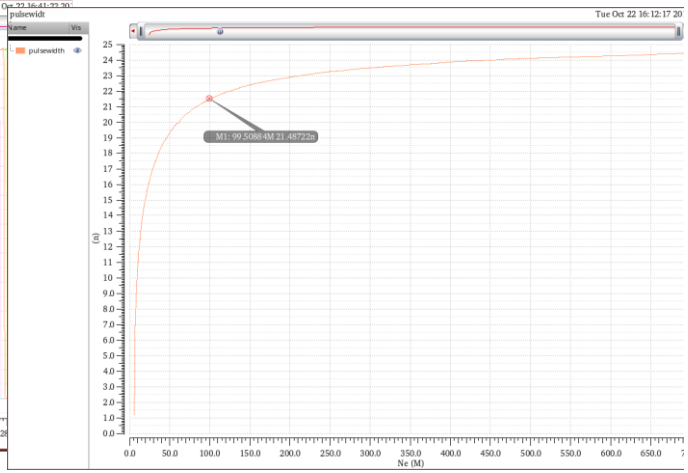
Blocks optimization: Current discriminator



Comp



Time-walk



Output pulse width vs input charge

- Inverter-based current discriminator
- For energy measurement, errors from: different input charges cause different flip time called time-walk; circuit noise called jitter
- Simulation result: 3 ns time-walk, 500 ps rising/falling time @ 100uA
- Need high time resolution TDC ~ 20 ps

Summary and outlook

Summary

- First prototype chip of SiPM readout is taped out and will be test soon, using GSMC 130 nm 1.2V process
- Timing and energy measurement are both included

Outlook (next submission will be the beginning of 2020)

- Blocks are optimized for the next submission
  - Improve the input range
  - Improve the timing response: current discriminator
  - Improve the energy measurement using TOT and ADC
  - Pipeline ADC and TDC are under designing

Thank you very much for your attention!