Scintillator Fibre Tracker for the LCHb Upgrade I

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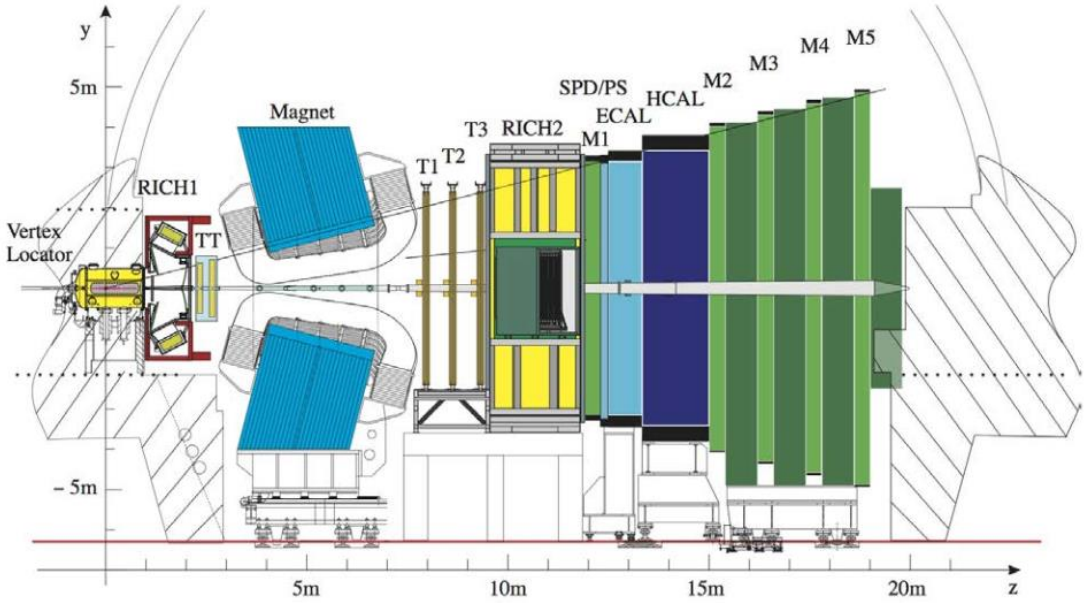
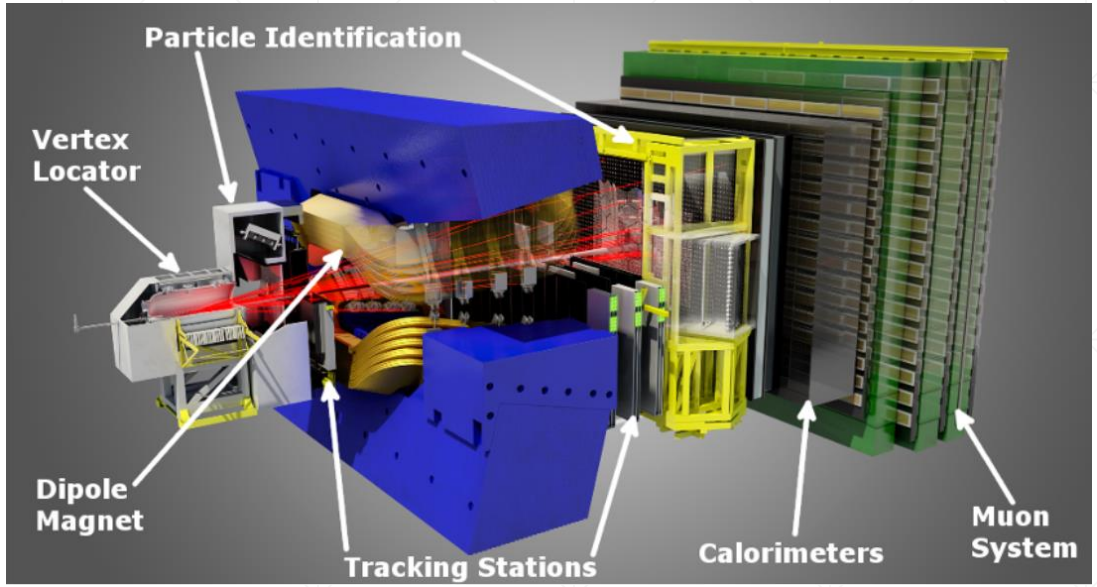
CLHCP 2019

大连 2019.10.26

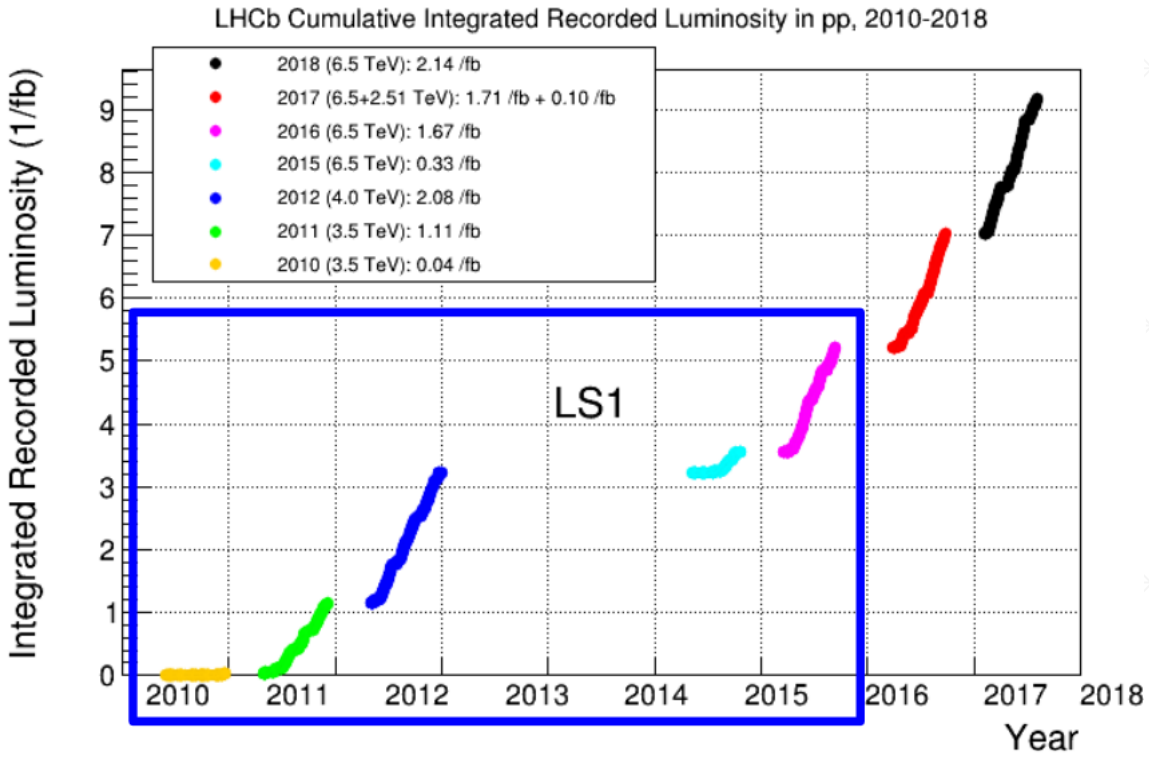
LHCb 主要科学目标与探测器



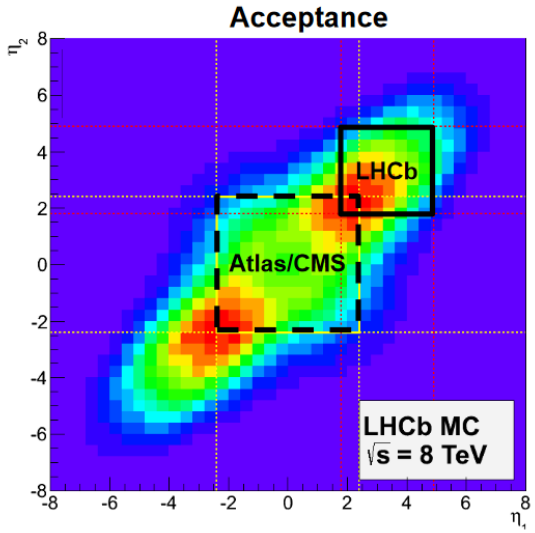


- **理解正反物质不对称：CP破坏**
- **间接发现新物理：稀有衰变**
- **理解强相互作用机制：强子性质，新强子态**
- **其它：电弱物理，重离子物理，…**

LHCb Run 2

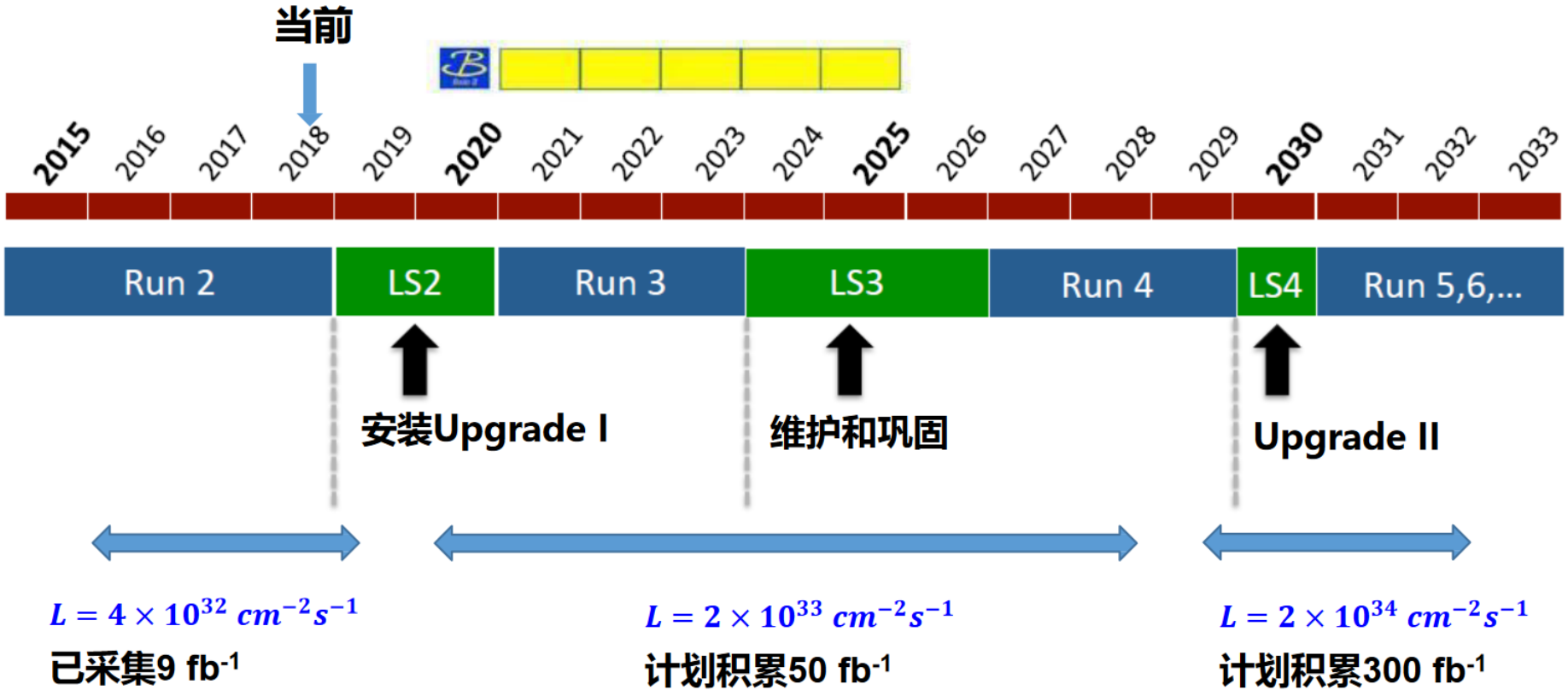


LHCb proved itself to be the Forward General–Purpose Detector at the LHC

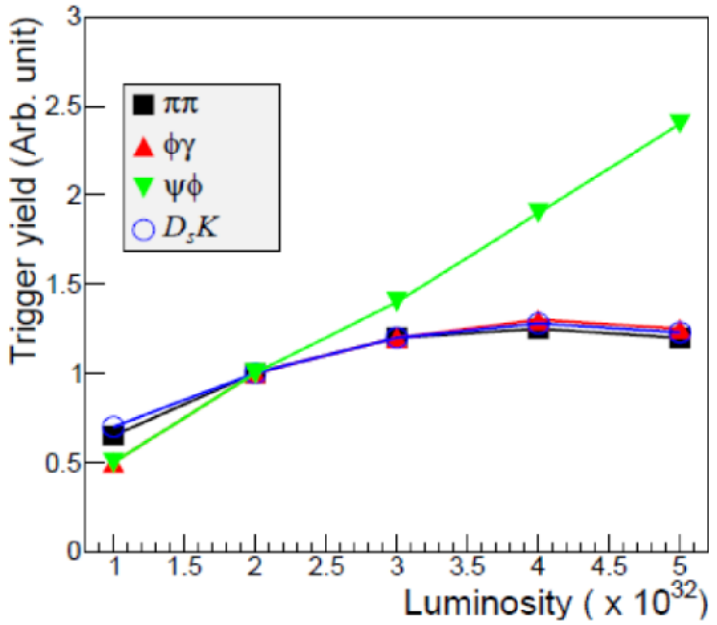


- **运行亮度达到$4 \times 10^{32}\ cm^{-2}s^{-1}$, 两倍于设计指标**
- **积分亮度超过$9fb^{-1}$**

LHCb 未来升级计划


当前
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
Run 2
LS2
Run 3
LS3
Run 4
LS4
Run 5,6,...
安装Upgrade I
维护和巩固
Upgrade II
$L = 4 \times 10^{32}\ cm^{-2}s^{-1}$
已采集9 fb-1
$L = 2 \times 10^{33}\ cm^{-2}s^{-1}$
计划积累50 fb-1
$L = 2 \times 10^{34}\ cm^{-2}s^{-1}$
计划积累300 fb-1

LHCb Upgrade Motivation

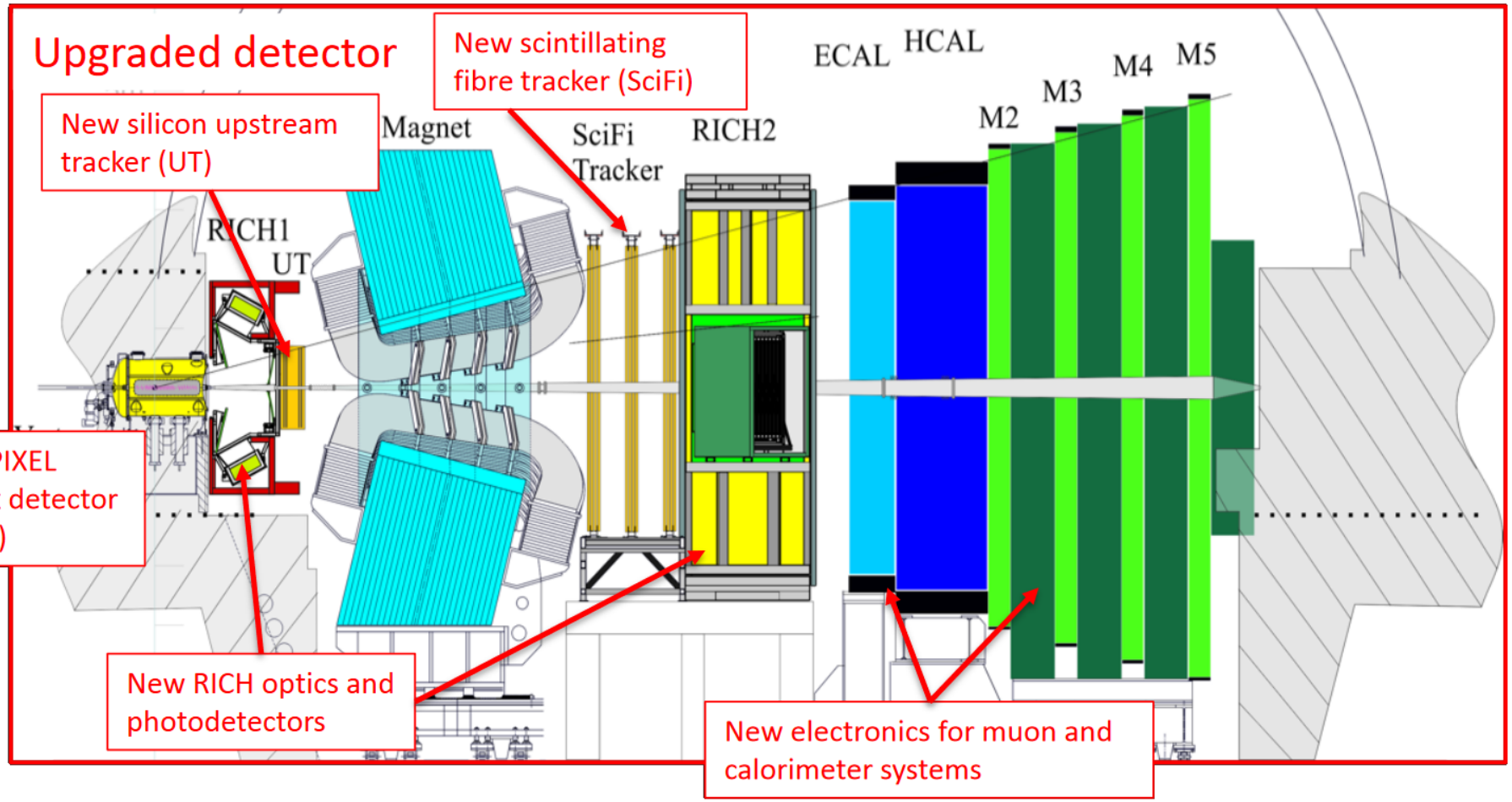


Present L0 hardware trigger (max rate 1 MHz) saturates at high luminosity for hadronic final state modes

LHCb Upgrade I, with installing in 2019-2020 (LHC LS2) and first data-taking in Run 3 (2021-2023).

- ❖ Goal: increase statistics by more than ×10
- ❖ Raise operational luminosity by factor of five to $2\times10^{33}cm^{-2}s^{-1}$
- ❖ Triggerless 40MHz readout (Full software trigger)
- ❖ Necessitates redesign of several sub-detectors and overhaul of readout (40MHz readout rate)
- ❖ Replace tracking detectors (finer granularity to cope with higher particle density)

LHCb Upgrade I



All sub-detectors read out at 40 MHz for a fully software trigger.

LHCb Upgrade I: Tracking - SciFi

Current: IT & OT

3 stations with 4 layers each

→ silicon micro-strips in innermost region

→ straw drift tubes in outer region

→ 130 k + 54 k readout channels

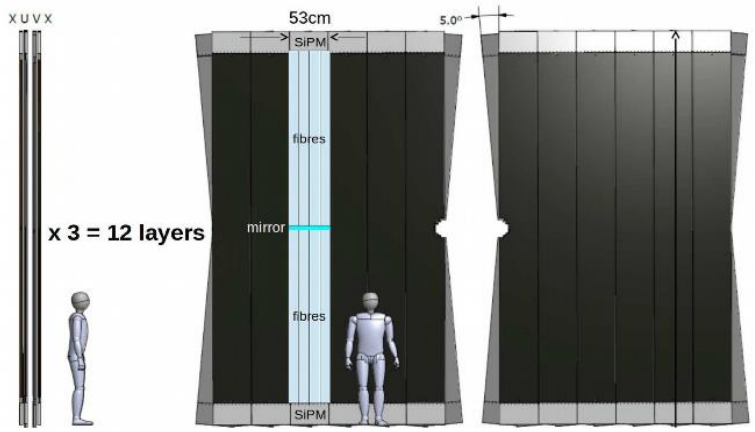
Upgrade: SciFi

3 stations of scintillating fibres

→ 2.5 m long, 250 μm diameter

→ read out with silicon photomultipliers

→ 590 k readout channels



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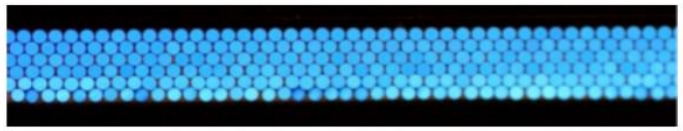
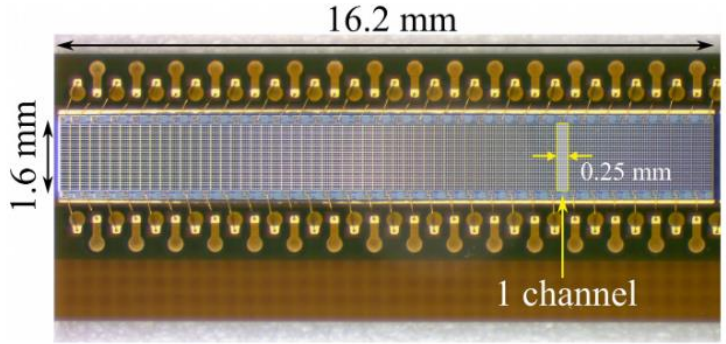


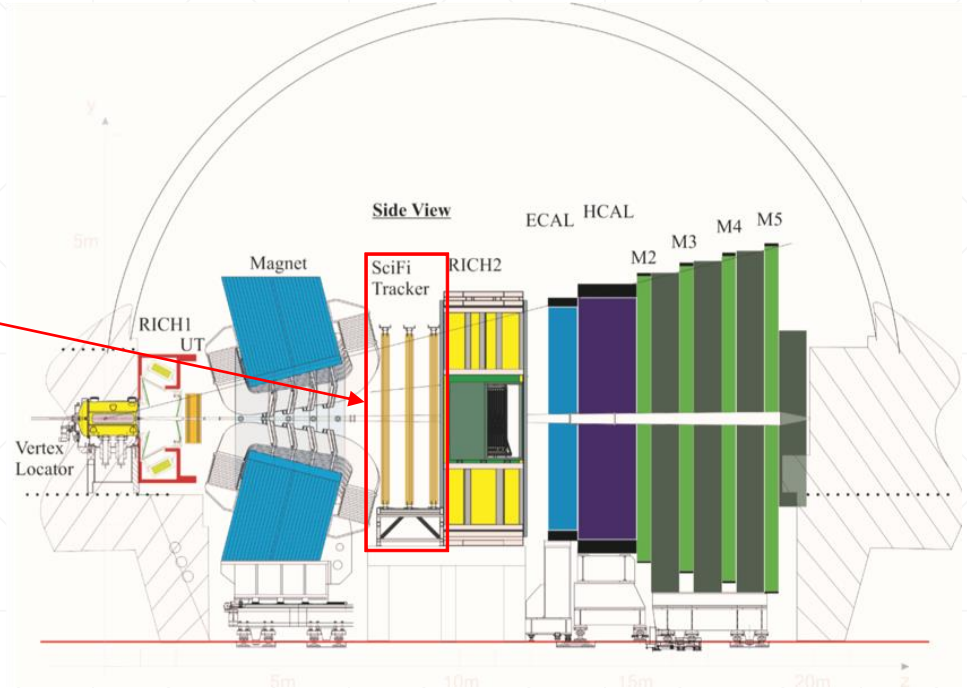


LHCb Upgrade I: SciFi

LHCb Upgrade I: SciFi

- ❖Goal: increase statistics by more than ×10
  - ✓ Operate at $2\times10^{33}cm^{-2}s^{-1}$ → 50 fb^{-1}
  - ✓ Triggerless 40MHz readout

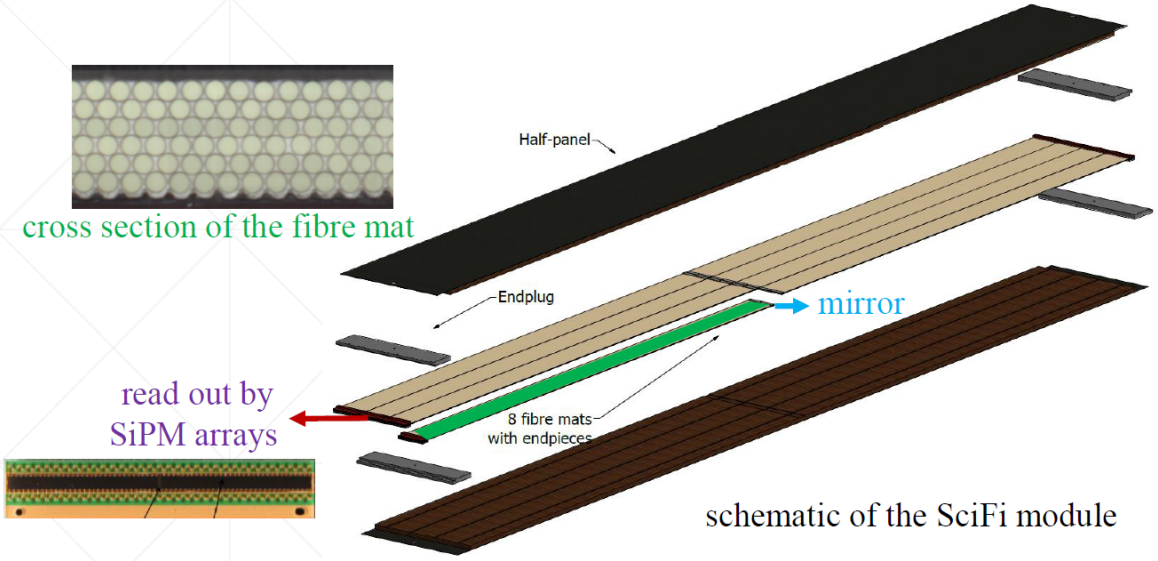
- ❖Scintillating Fibre (Sci-Fi) Tracker
  - ✓ Fast, high efficiency (~99%)
  - ✓ High granularity (250μm)
  - ✓ High resolution (<100μm)
  - ✓ Low mass (<1% X_0/layer)
  - ✓ Radiation hardness (up to 35kGy)



Schematic view of the current LHCb detector

SciFi – Fibre Mat & Module

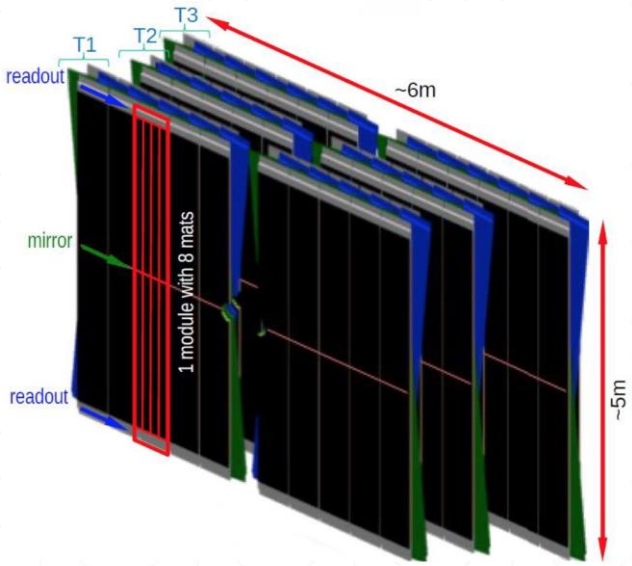
- 250μm diameter scintillating fibre wound into a 6-layer 2.4m-long fibre mat
  - ✓ one end equipped with a mirror
  - ✓ read out by 4× SiPM arrays
- 8 × fibre mat + honeycomb = sandwich-structure 0.5m × 5m module

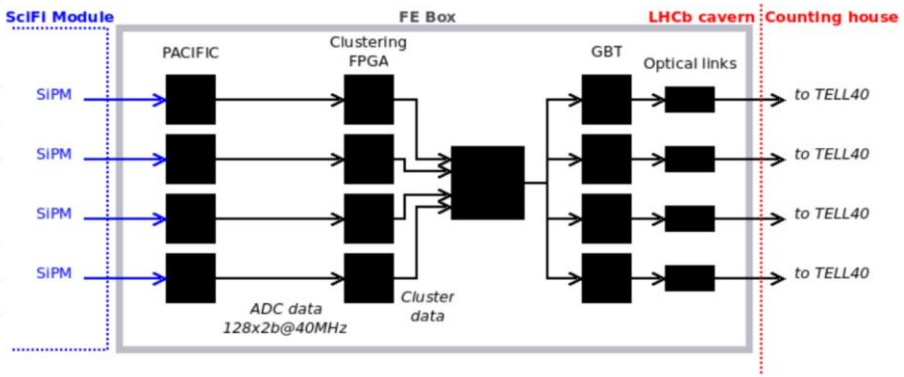


Sci-Fi readout electronics (FE)

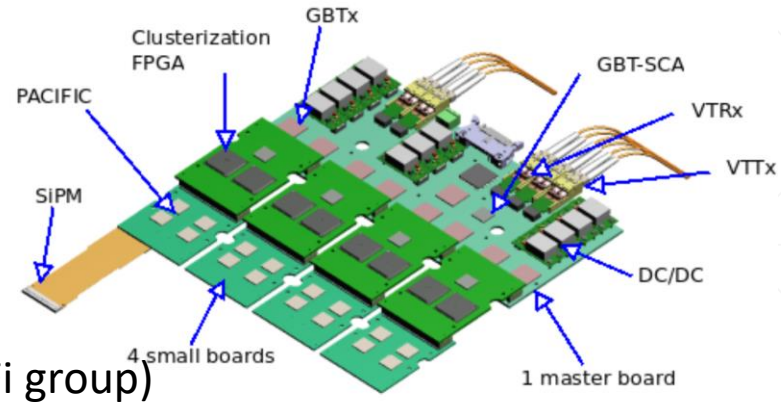
❖Tracker structure:
- ✓ 3 Tracking Stations
  - ✓ 12 detector layers (X-U-V-X, 5°)
    - ✓ 144 modules

❖Electronics design:
- ✓ ~340m^2 total active surface
- ✓ 590,000 SiPM channels
- ✓ 12,000 PACIFIC chips needed
- ✓ 2,500 Frontend Electronic Boards



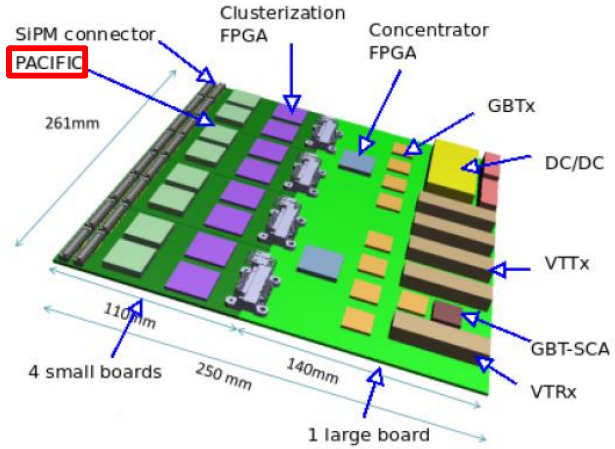


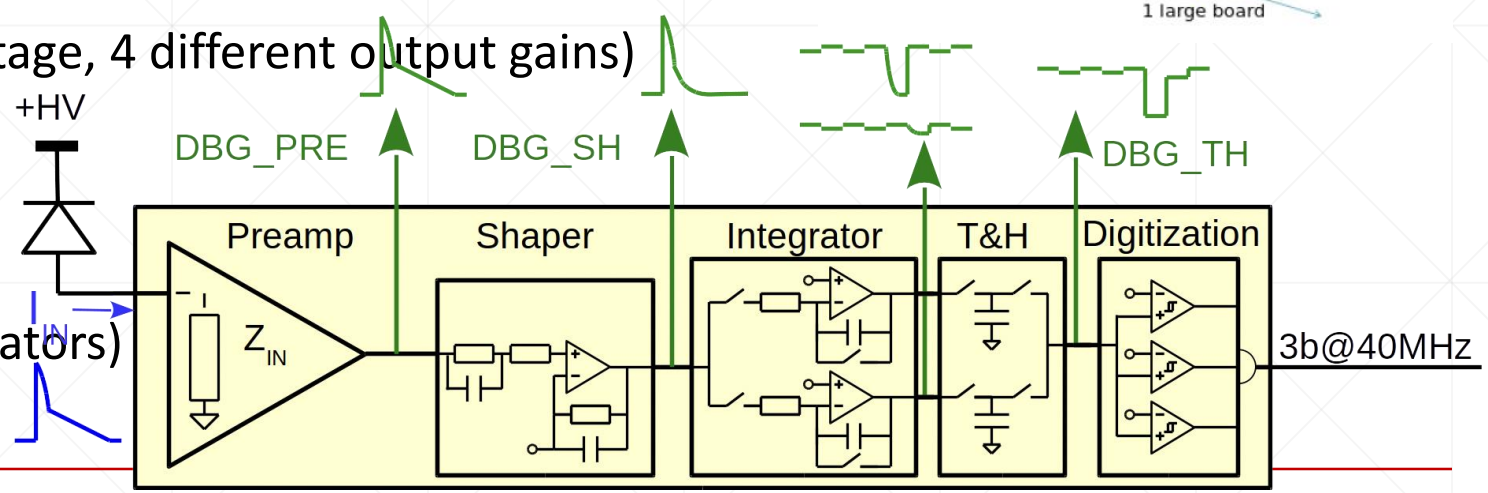
❖LHCb China Group 2016~2018:
- ✓ Co-design Sci-Fi Frontend Electronic Boards
- ✓ Manufacturing all Frontend Boards in China, testing a part
- ✓ Sci-Fi Readout Electronics Quality Assurance System (For chips and boards)
- ✓ Readout Electronics for Detector Performance Evaluation (>20 setups in Sci-Fi group)



PACIFIC5

- ❖64-channel SiPM readout ASIC for the Sci-Fi Tracker
- ❖Current mode input
- ❖Low input impedance (≈50Ω)
- ❖High Bandwidth preamplifier (≈250MHz)
- ❖Output：8bit×16pair@320MHz
- ❖Main functional blocks:
  - ✓Pre-amplifier(Current->Voltage, 4 different output gains)
  - ✓Shaper
  - ✓Offset trim
  - ✓Integrators×2 (20MHz)
  - ✓Track & Hold
  - ✓Digitization (with 3 comparators)

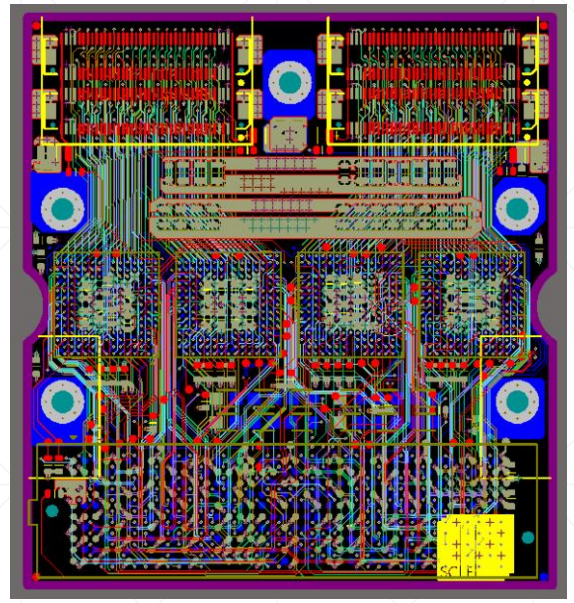




PACIFIC Frontend Board

We decided to re-optimize the routing of the PACIFIC Frontend Board

- 4 × PACIFIC ASICs (196-pin BGA packaged)
- 4 × temperature measurement circuits (voltage divider circuits with NTC , 2 for SiPMs, 2 for the ASICs)
- 4 × SiPM bias voltage measurement circuits (voltage divider circuits)
- 1 × BoardID IC (DS2401 64-bit unique, factory-lasered silicon serial number, no permanent damage up to 140Gy)
  http://radwg.web.cern.ch/RadWG/Pages/showExternal.aspx?GotoUrl=https://twiki.cern.ch/twiki/bin/viewauth/Main/TulliosPreferredPartList
- 4 × SiPM flex cable connectors (Hirose DF12(3.0)-80DS-0.5V)
- 1 × FMC connector (ASP-134602-01)



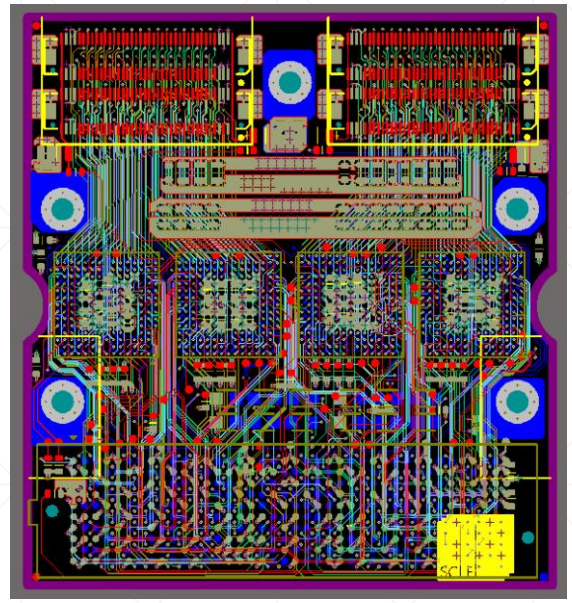
re-optimised PACIFIC Frontend Board r4

Redesign of PACIFIC Frontend Board

We decided to re-optimize the routing of the PACIFIC Frontend Board

- for a higher production yield
- more strict routing constrains, to gain some margin for the sampling window size

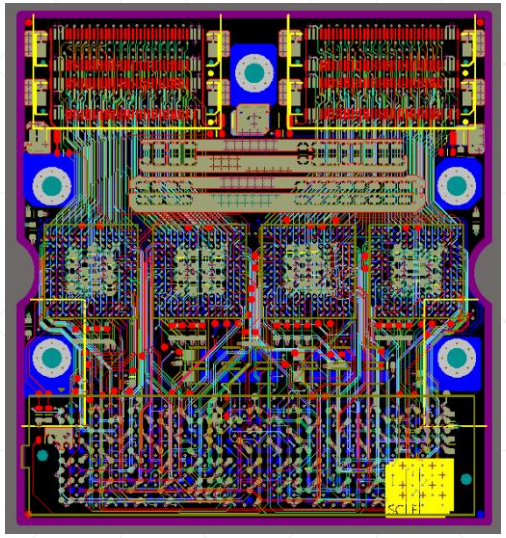
- 4 pairs of PACIFIC Clock lines (CLKIN_0~3) : routing length match < 1mm
- 4 SYNC lines (SYNC_0~3): routing length match < 1mm
- 64 pairs of data lines (DATA_0~3_X) : routing length match <3mm.
- well seperate the analog input signals and the output data lines, the CLOCK lines
- from 8-layers to 14-layers
- Calculate impedance for Halogen Free (TU-862HF), and keep thickness 1.7mm

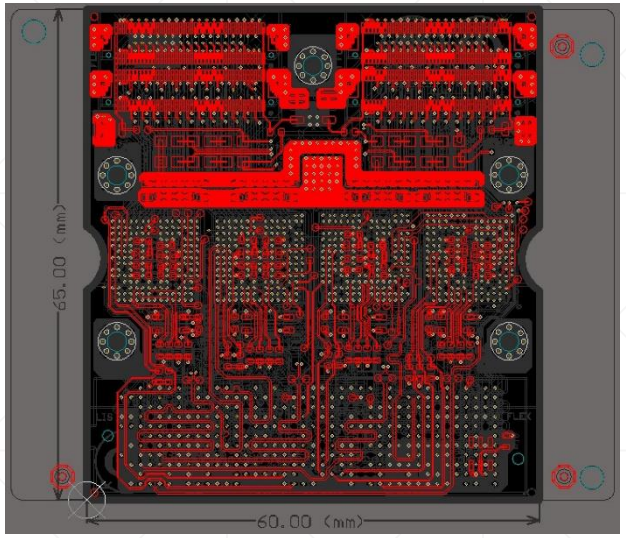


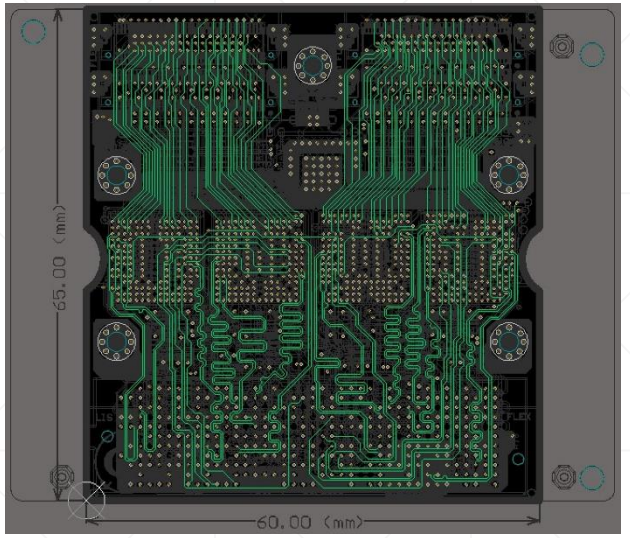
re-optimised PACIFIC Frontend Board r4

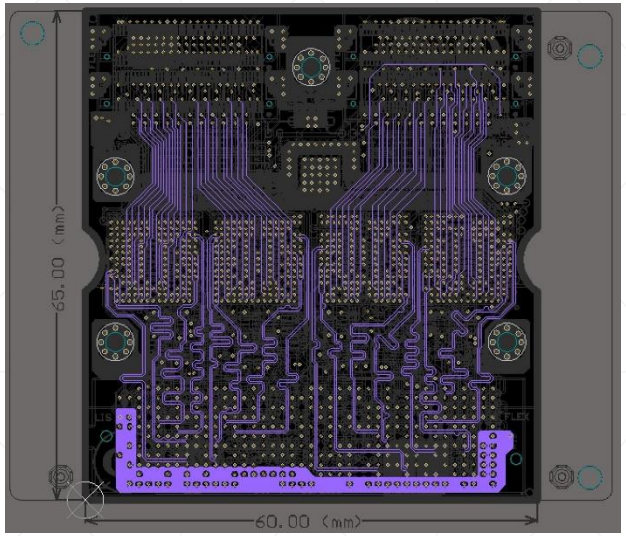
The design has been complete.
For the first 250 PACIFIC Frontend Boards, we will assemble first 10 PCBs, check with the SciFi full electronics (MB+CB) to make sure everything works fine after this optimization.

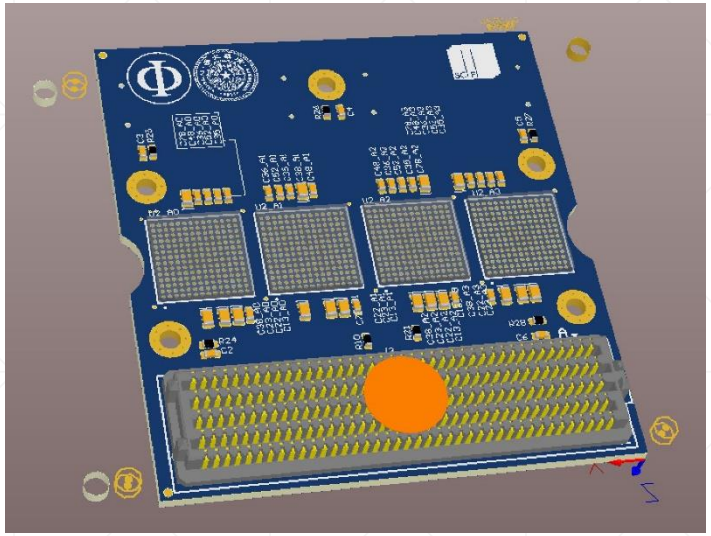
Redesign of PACIFIC Frontend Board

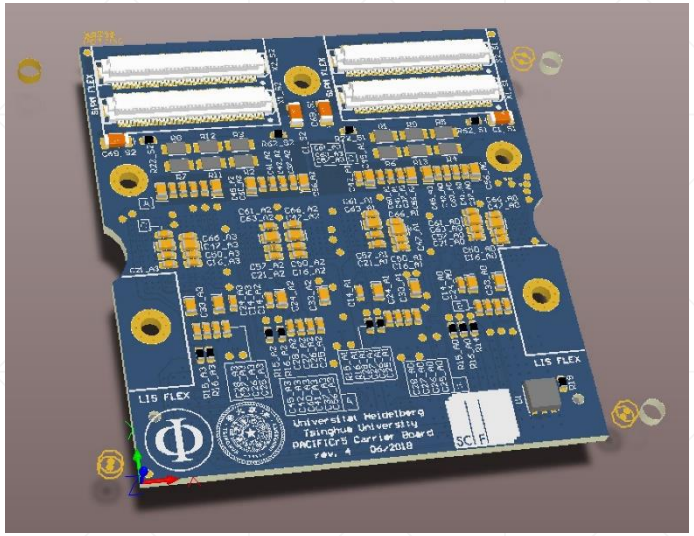






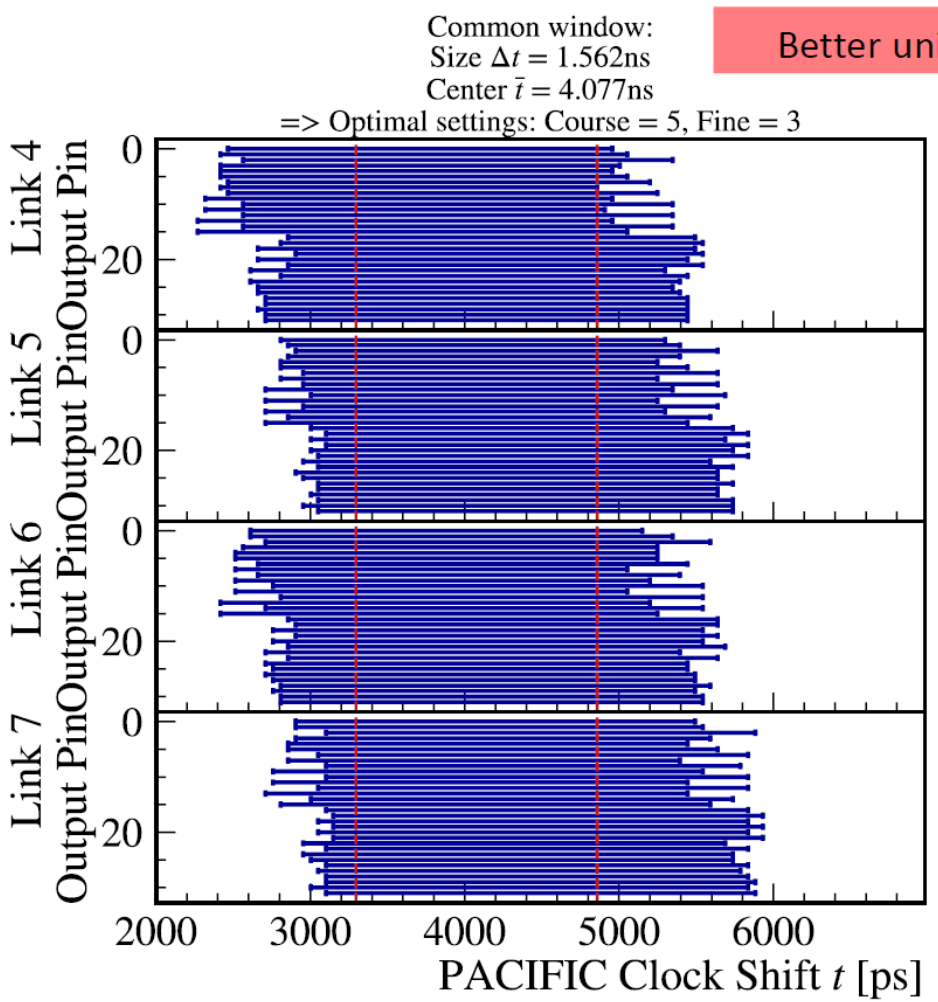




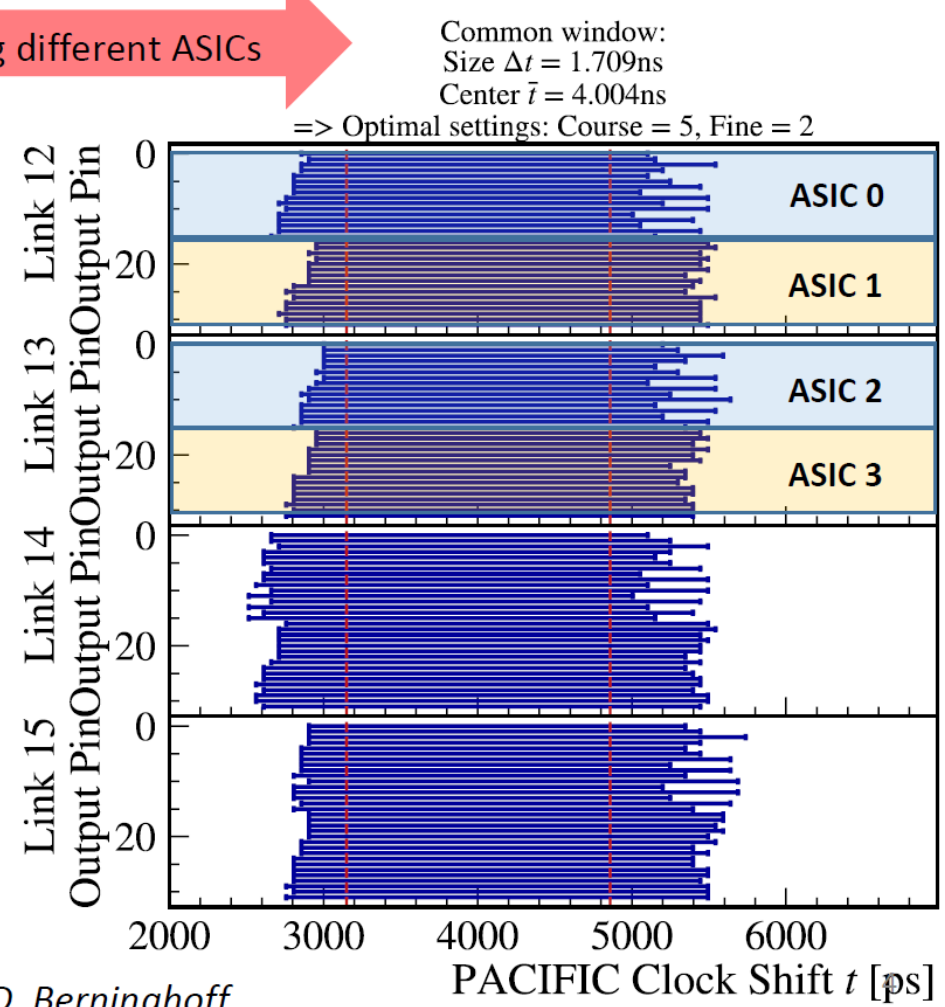


BER test with SciFi FE

- Position: Master Board 0, PBs 2+3, old design
- Position: Master Board 1, PBs 2+3, **new design**

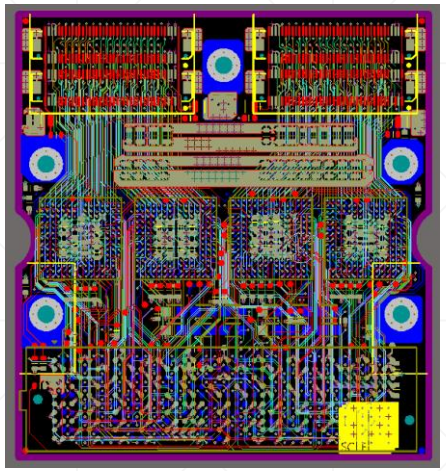


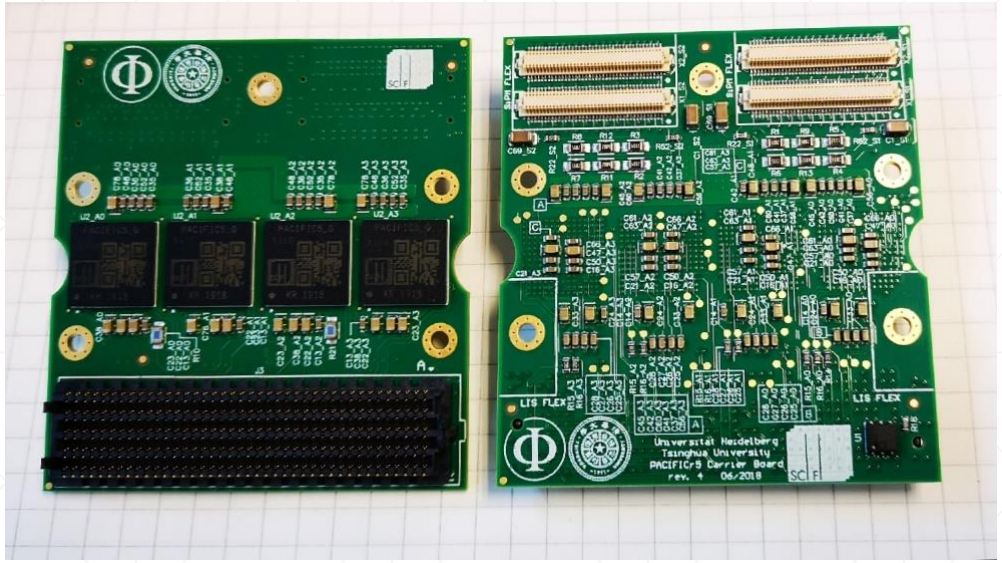
Better uniformity among different ASICs

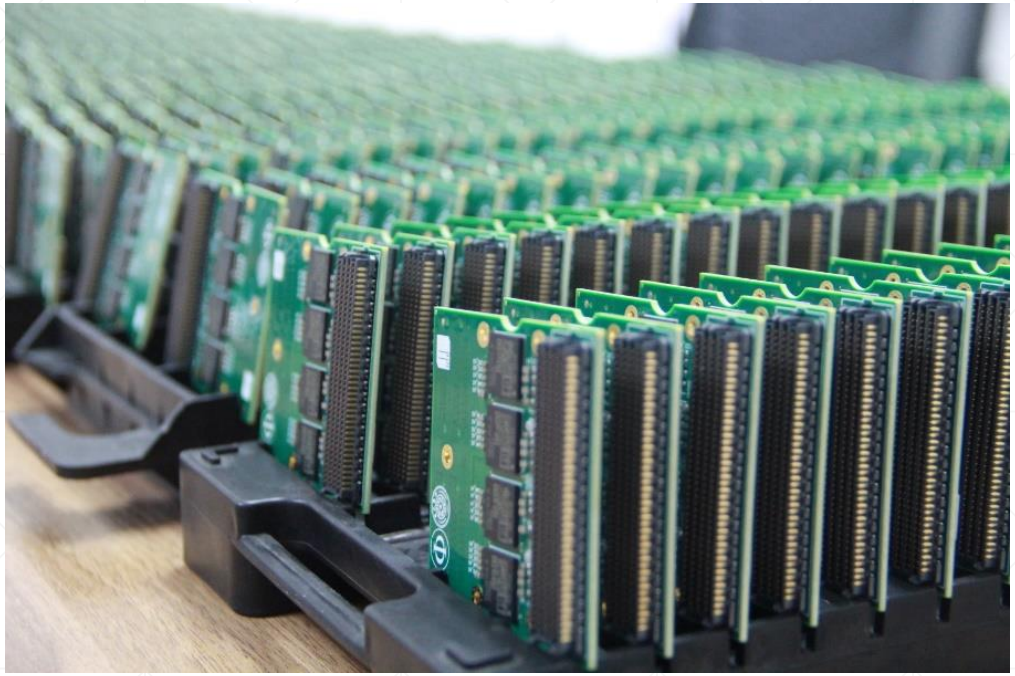


Result from D. Berninghoff

Redesign of PACIFIC Frontend Board & Mass Production



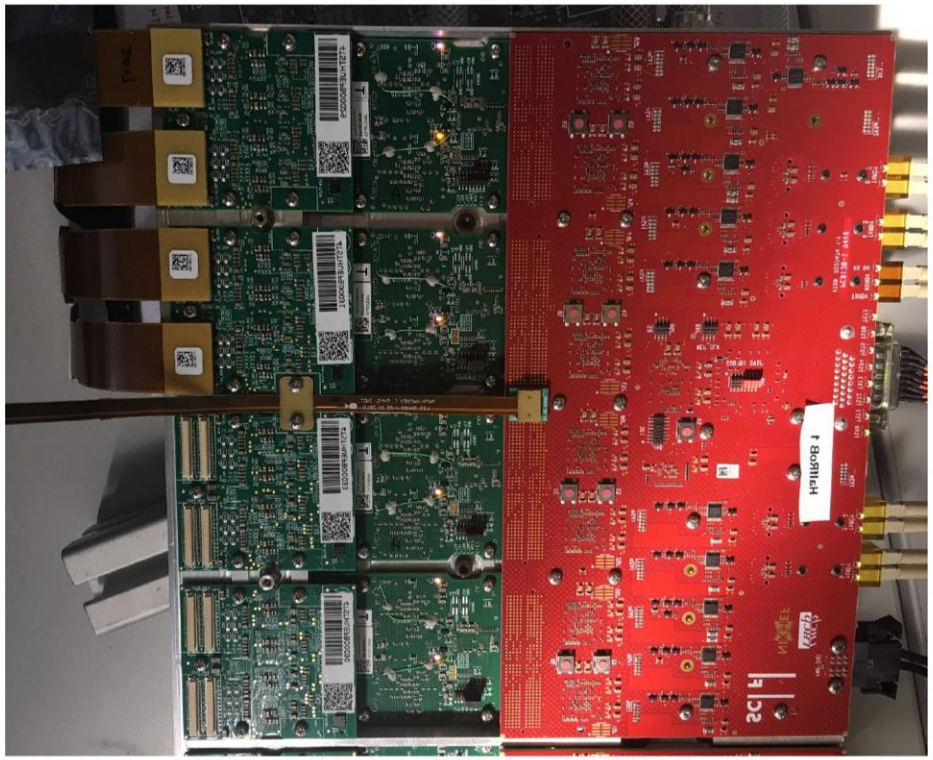




2018.09 - First 250 PACIFIC Frontend Boards finished !
(for first C-Frame of SciFi)

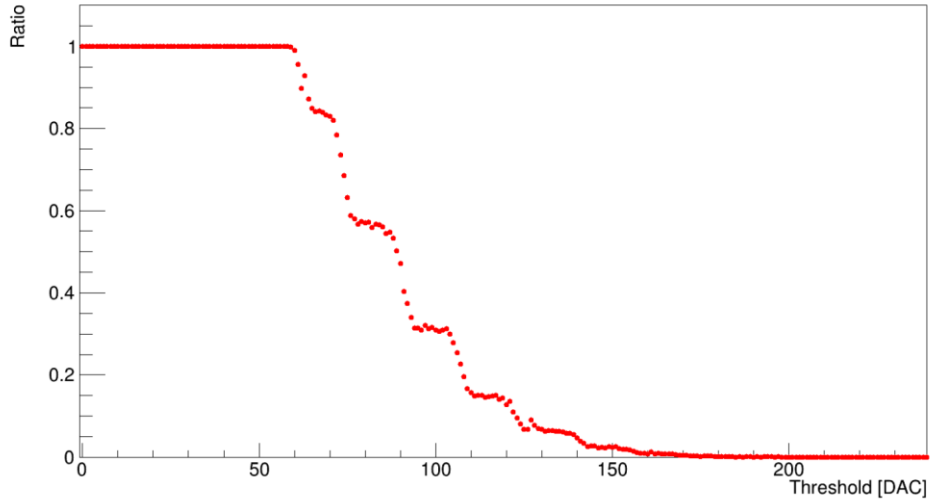
2019.09 – Finished all 2,300 PACIFIC Frontend Boards !

First Setup of SciFi C-Frame



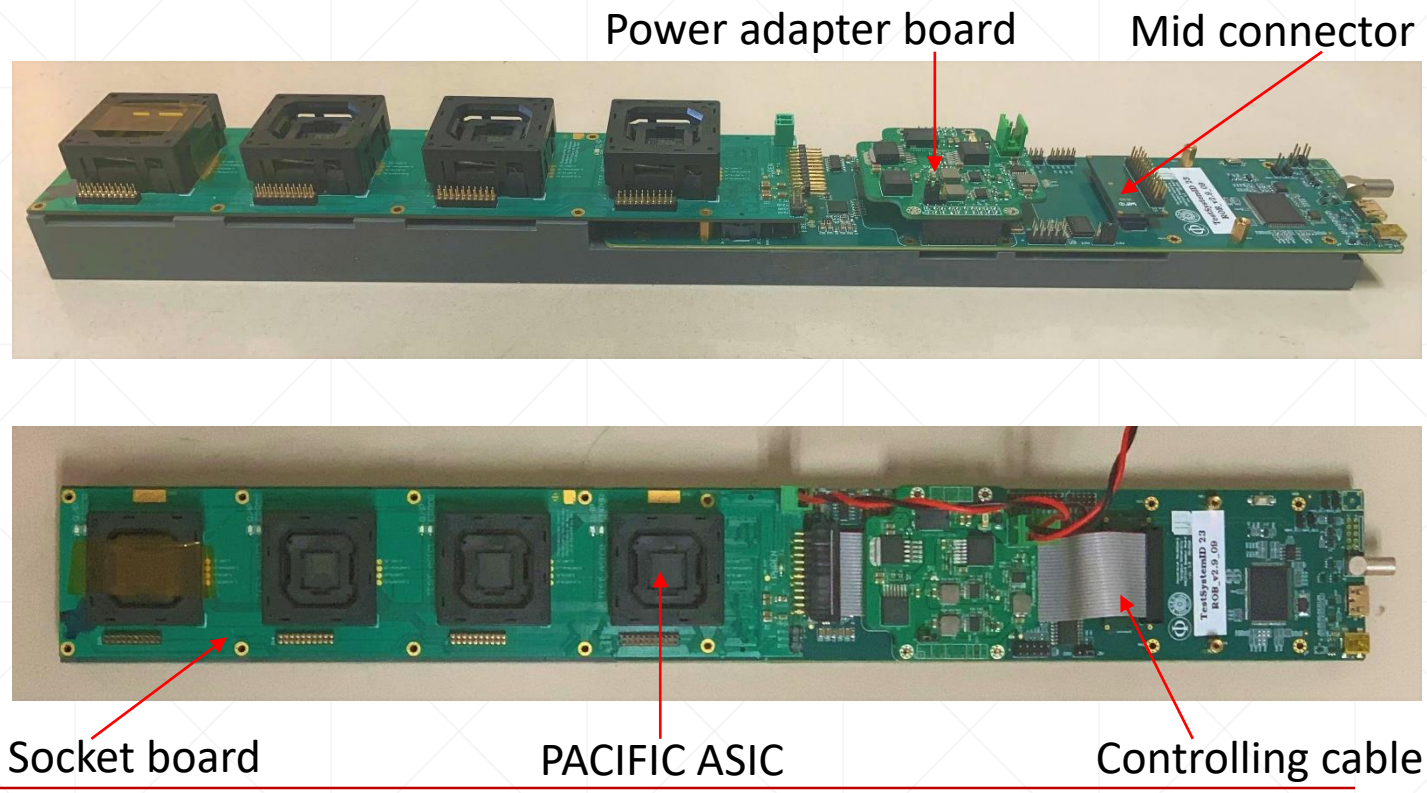
First Setup of SciFi C-Frame
(Sci-Fi milestone of 2018)

Test with SiPM + Light Injection System



QA System for PACIFIC chips

- ❖Custom designed test DAQ (PACIFICROB): [fully tested, 4 for Heidelberg, 3 for Barcelona, 3 for Valencia]
  - ✓ Altera Cyclone FPGA (clock generation, ASIC configuration, data process, sensor readout ...)
  - ✓ precision clock conditioner to fine tune the clock for each ASIC
  - ✓ (LVDS-SLVS convertor)
  - ✓ 8-channel, 12-bit ADC
  - ✓ USB interface to PC
- ❖Socket Board:
  - ✓ 4 sockets to nip chips
  - ✓ Connected with FMC & controlling cable
- ❖DC power supply
  - ✓ Output 5V/3A at least
- ❖Linux PC
- ❖Robot arm (Barcelona)



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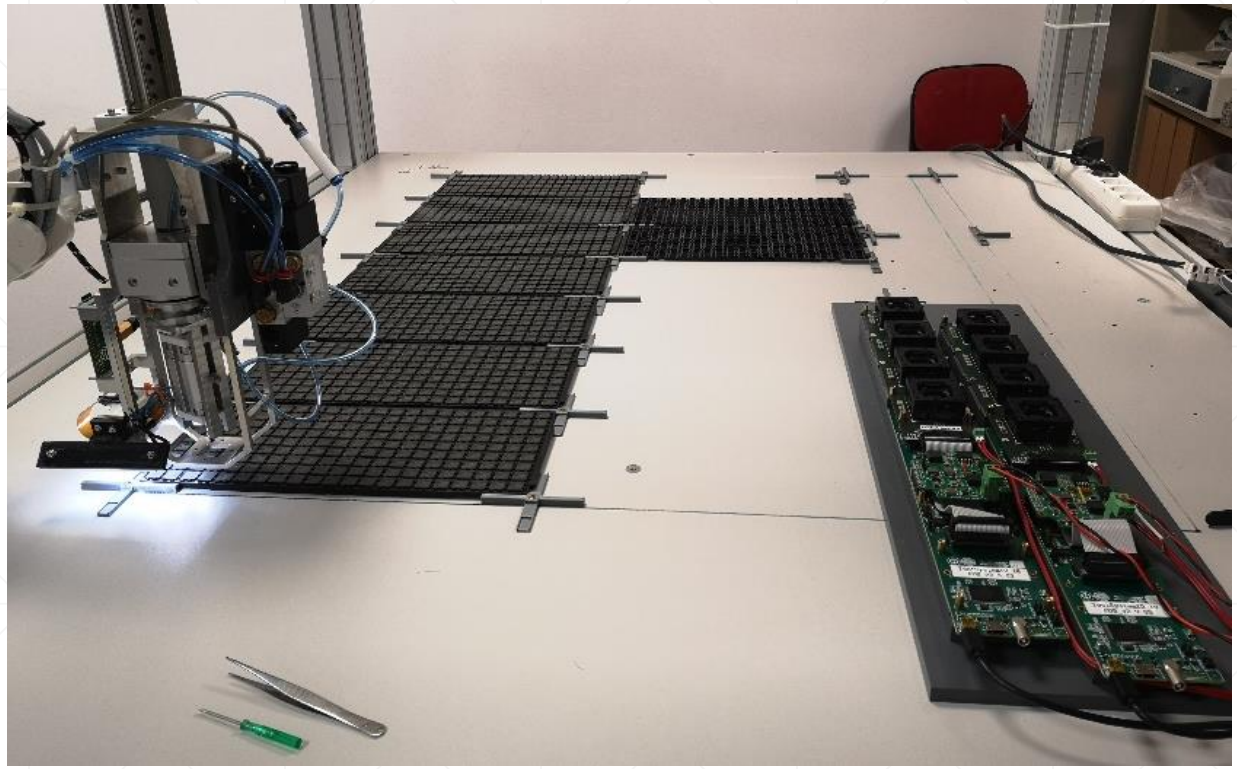
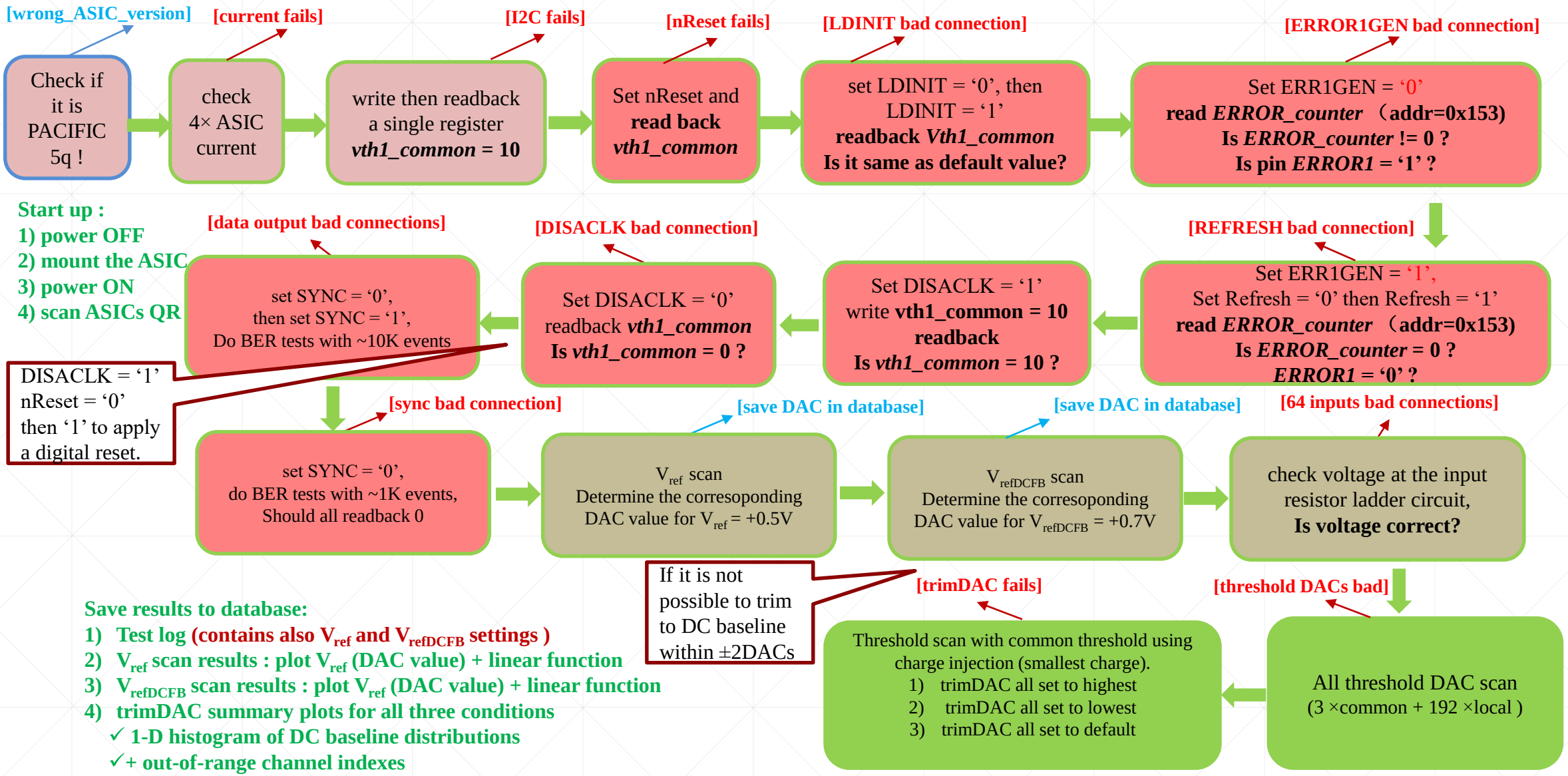




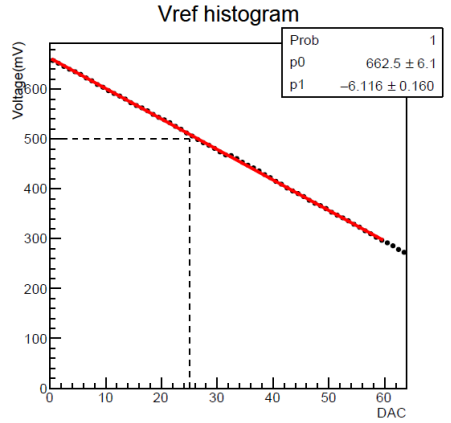
Save results to database:

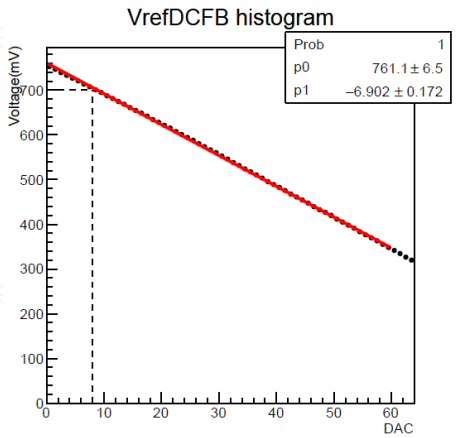
1) **Test log (contains also V_{ref} and $V_{refDCFB}$ settings)**
2) **V_{ref} scan results : plot V_{ref} (DAC value) + linear function**
3) **$V_{refDCFB}$ scan results : plot V_{ref} (DAC value) + linear function**
4) **trimDAC summary plots for all three conditions**
   - ✓ **1-D histogram of DC baseline distributions**
   - ✓**+ out-of-range channel indexes**

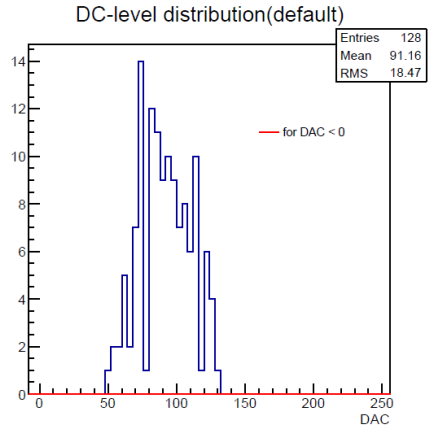
PACIFIC ASIC QA test routine

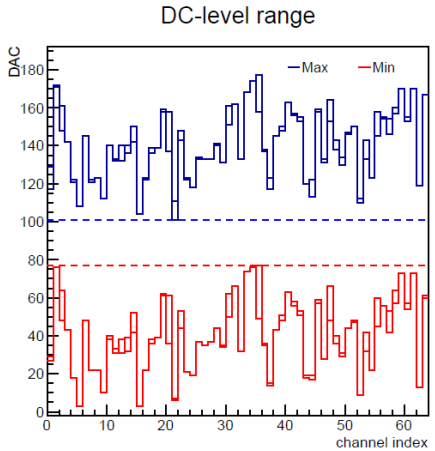
Raw data from all the scans will be save into one file to reproduce the results.

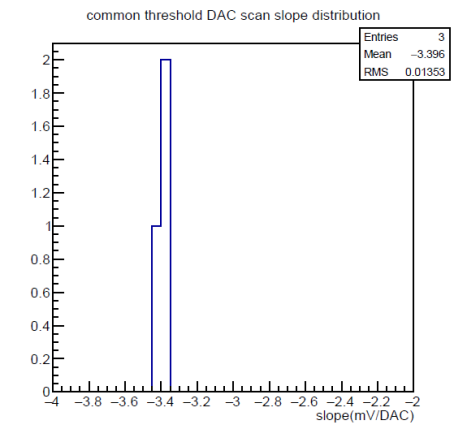
Main features of test results for one chip

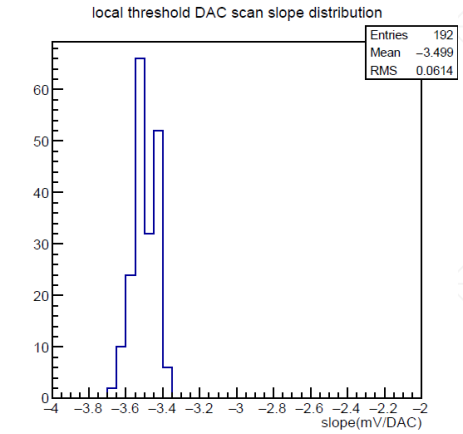






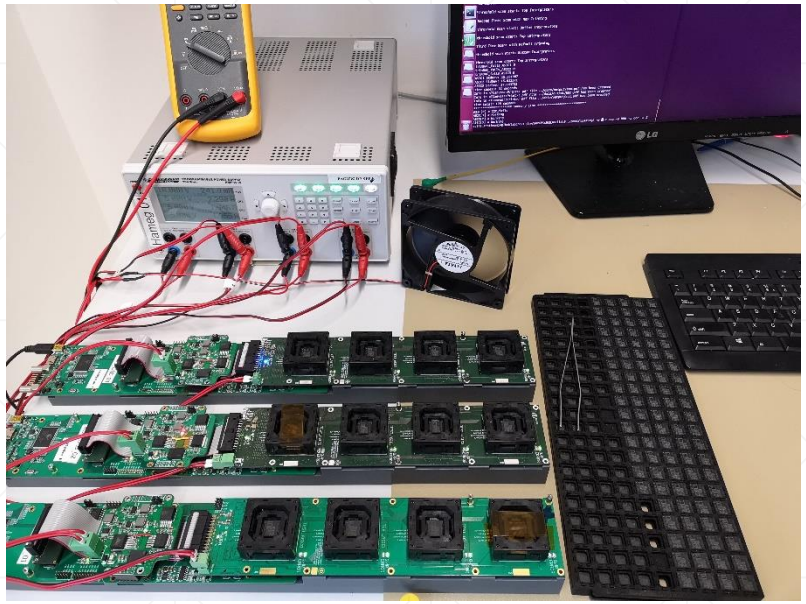




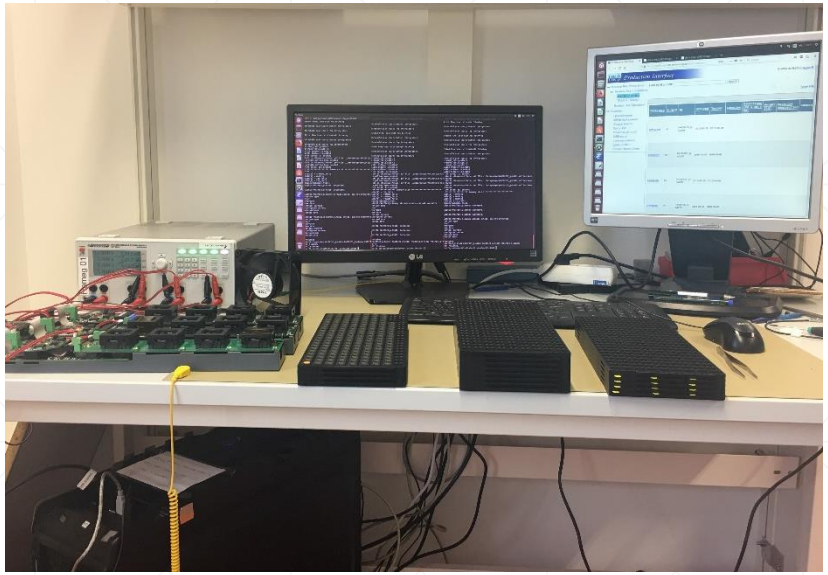


test automatically update result to DB

final check the QA test routine



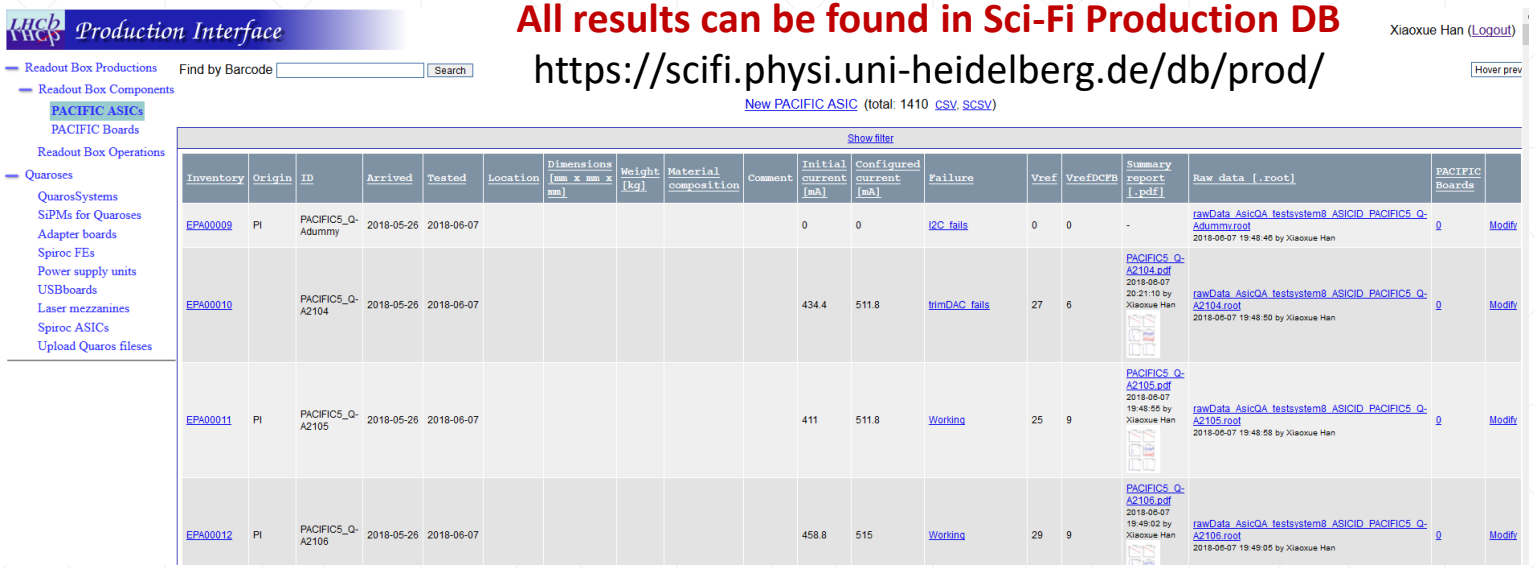
QA test running : 10 ASICs/run , ~100ASICs/hour



finish all 1st batch 1420 PACIFIC5q test

All results can be found in Sci-Fi Production DB

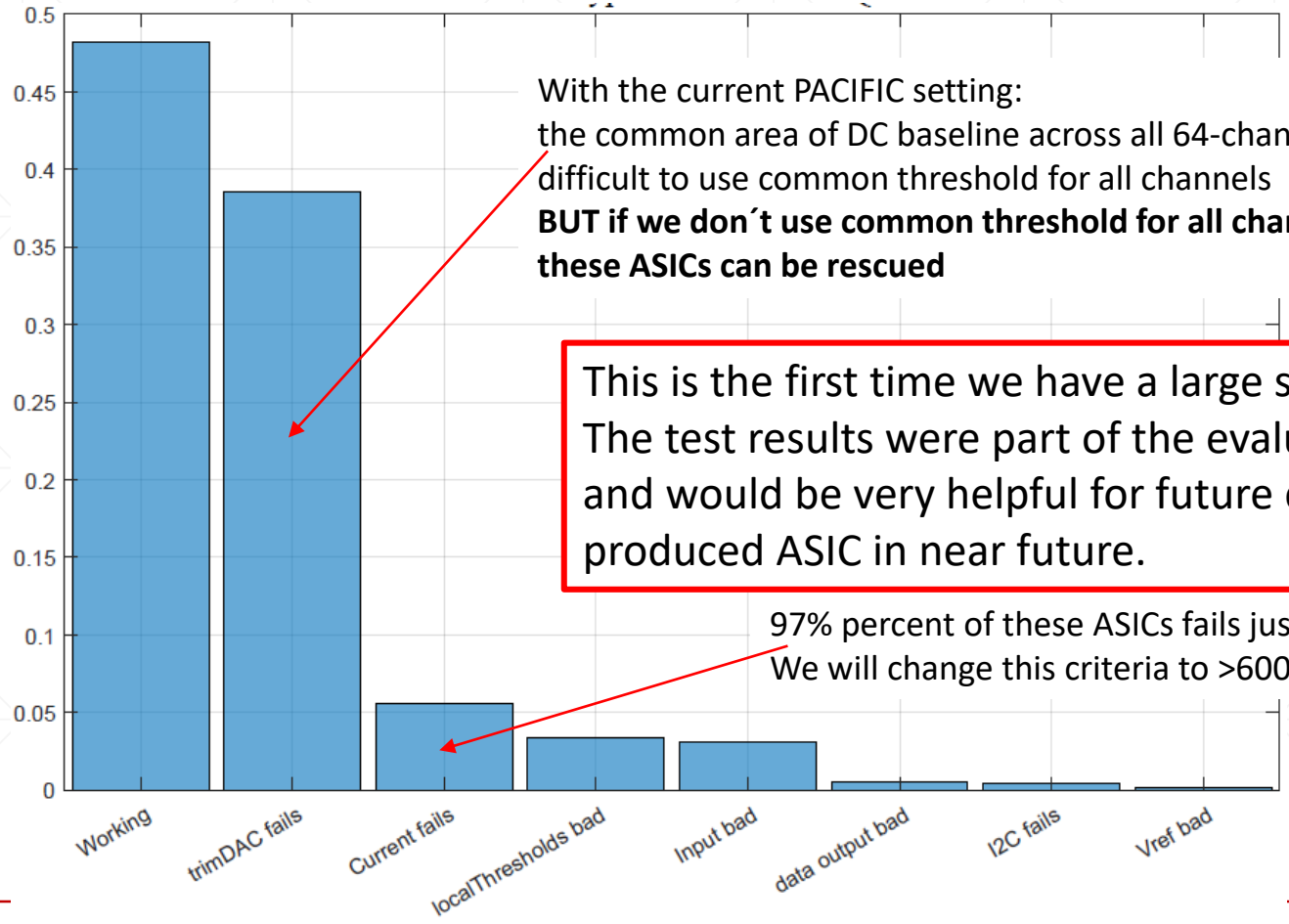
https://scifi.physi.uni-heidelberg.de/db/prod/



QA test for 1st batch of packaged PACIFIC5q

1st batch of 1420 chips

2018 Summer



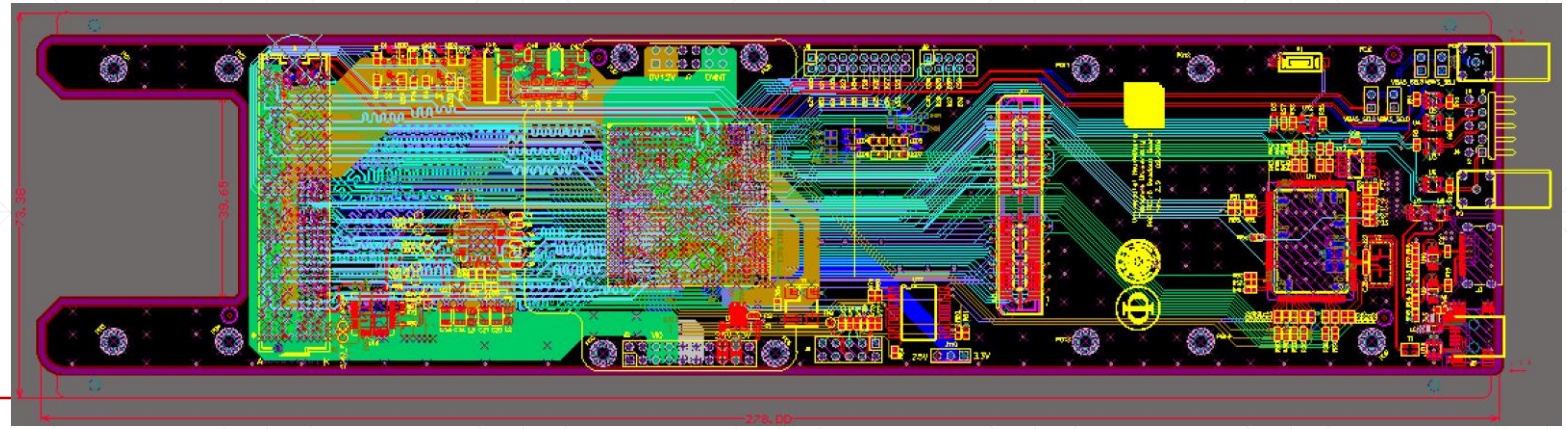
With the current PACIFIC setting:
the common area of DC baseline across all 64-channels is less than 4DACs,
difficult to use common threshold for all channels
BUT if we don´t use common threshold for all channels or tune the PACIFIC settings , these ASICs can be rescued

This is the first time we have a large statistical sample of the ASICs. The test results were part of the evaluation of the Sci-Fi electronics and would be very helpful for future classification of mass-produced ASIC in near future.

97% percent of these ASICs fails just because the initial current > 500mA
We will change this criteria to >600mA and re-measure these ASICs

QA System for Frontend Boards

- ❖Custom designed test DAQ (PACIFICROB): [fully tested, 3 for Heidelberg (delivered), 3 for Barcelona, 3 for Valencia]
  - ✓ Altera Cyclone FPGA (clock generation, ASIC configuration, data process, sensor readout ...)
  - ✓ precise clock conditioner to fine tune the clock for each ASIC
  - ✓ LVDS-SLVS convertor
  - ✓ 8-channel, 12-bit ADC
  - ✓ USB interface to PC
- ❖FMC connector intermedia board:
  - ✓ Simple pin-to-pin adapter PCBs
  - ✓ To avoid broken FMC connectors
- ❖Charge injection board
- ❖DC power supply
  - ✓ Output 5V/3A at least
- ❖Arbitrary waveform generator
- ❖Linux PC



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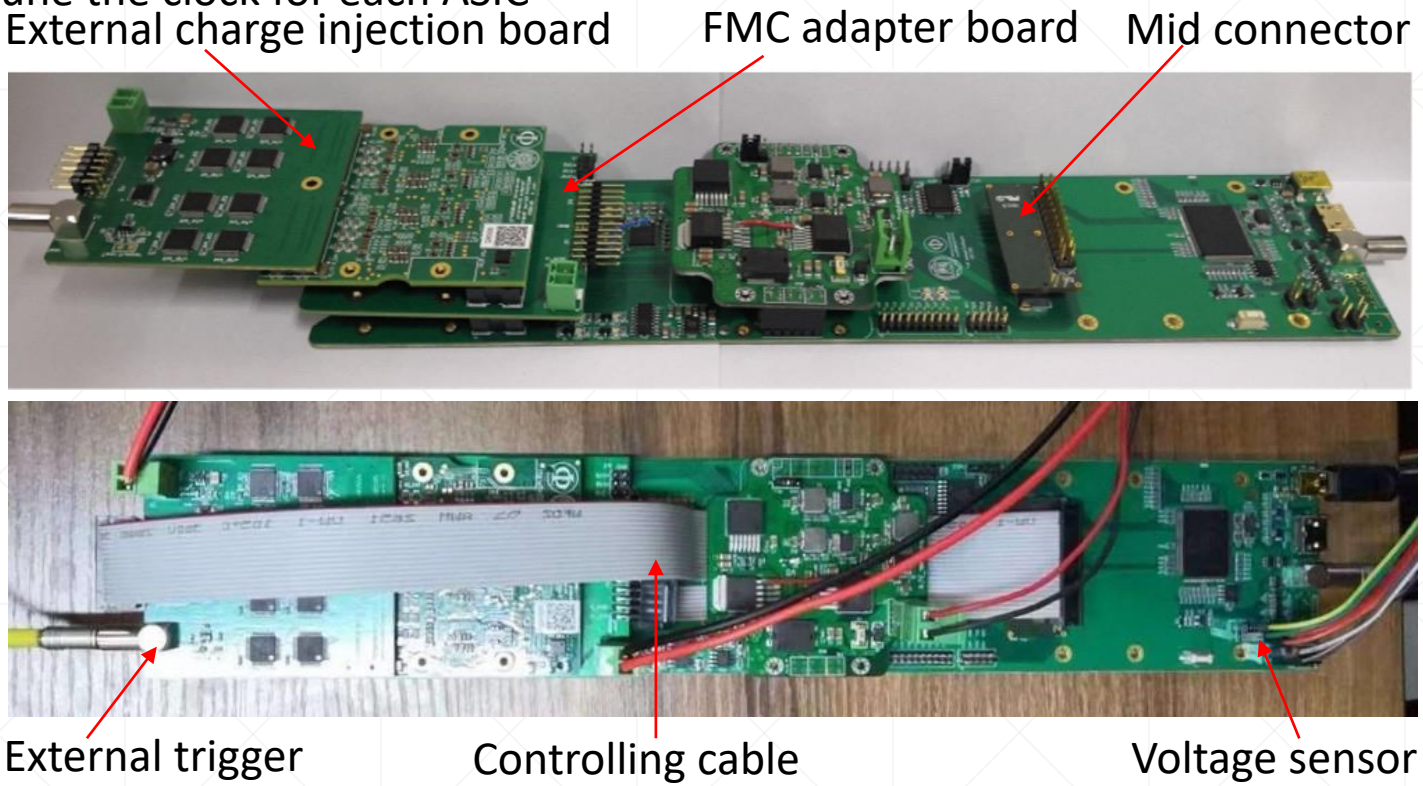
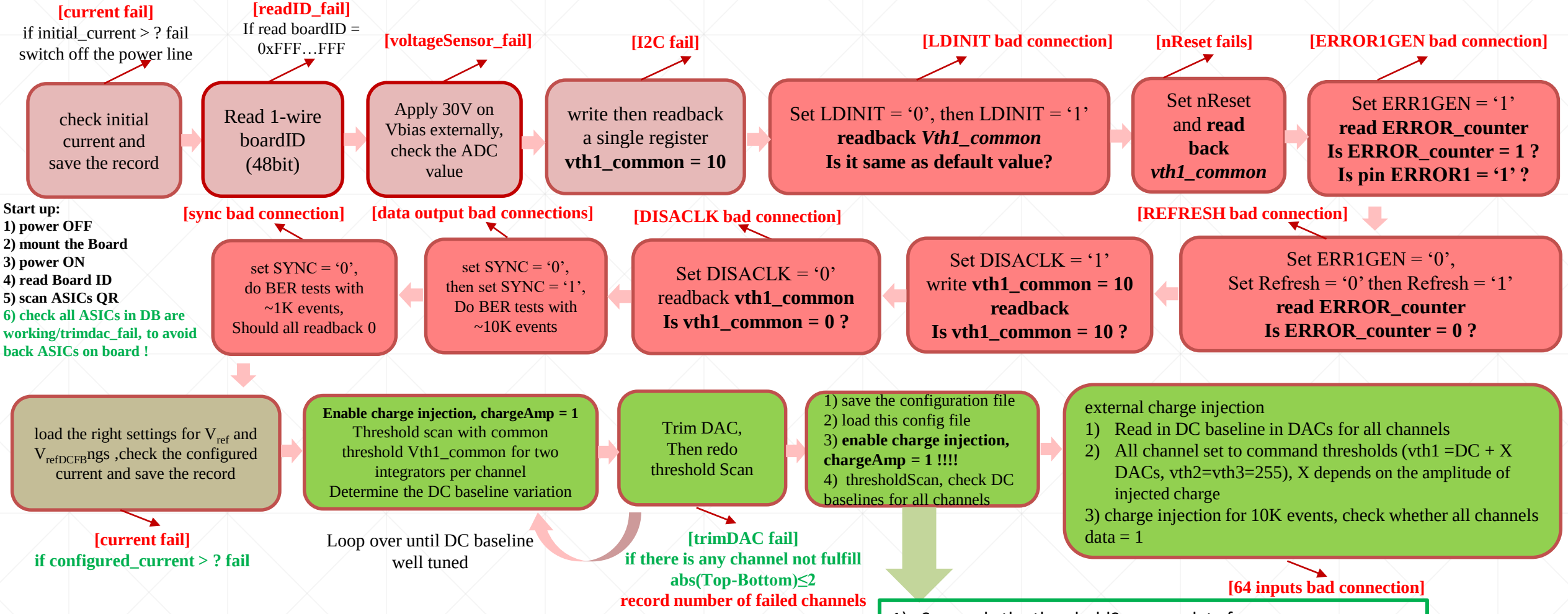


PACIFIC Frontend Board QA test routine



Save results to database:

1) test log

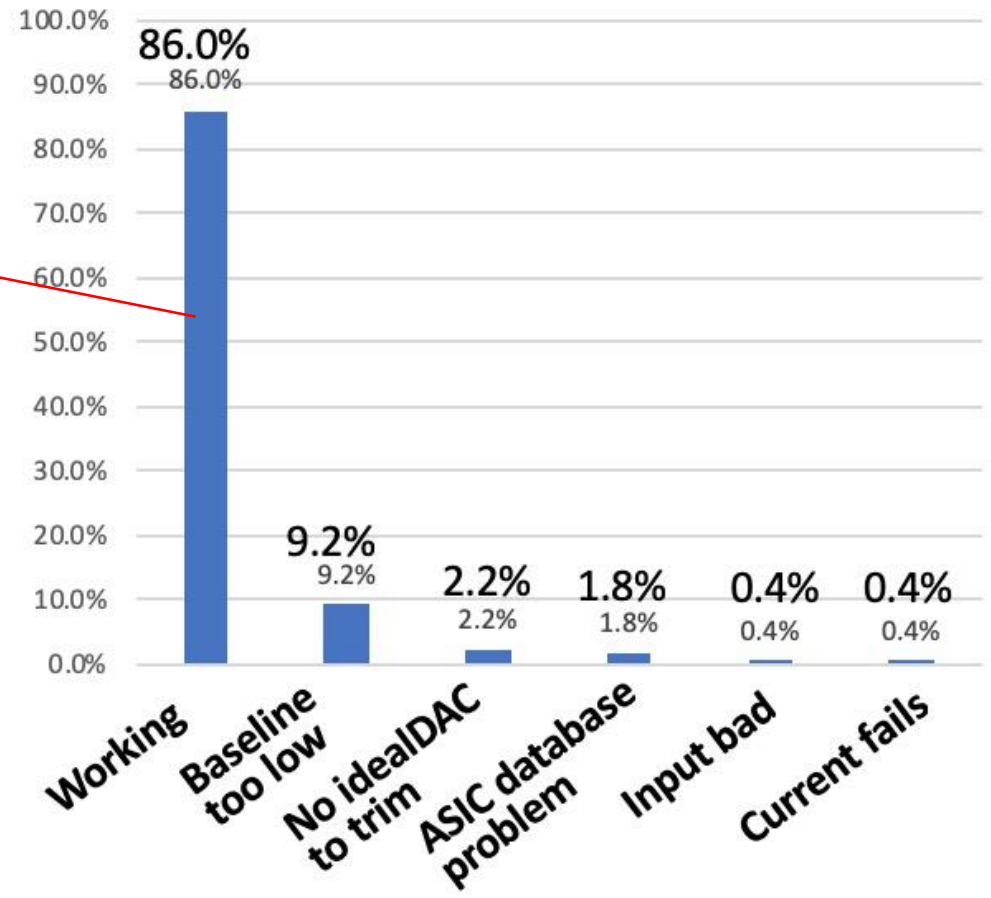
2) all parameters into a configuration file: PB_XX.conf, which can be read later by SciFi readout system.

3) after trimming DC-baseline distribution

- ✓ **1-D histogram of 0.5ratio-transition-DAC value for all channels (both Top and Bottom DAC) for each ASIC**
- ✓ **1-D histogram of difference of Top and bottom DAC within the same channel for each ASIC**

First 250 PACIFIC Frontend Boards Tested

- ❖86.0% Working
- ❖14.0% Failed:
  - ✓ Baseline too low
  - ✓ No ideal DAC to trim
  - ✓ ASIC database problem
  - ✓ Input bad
  - ✓ Current fails

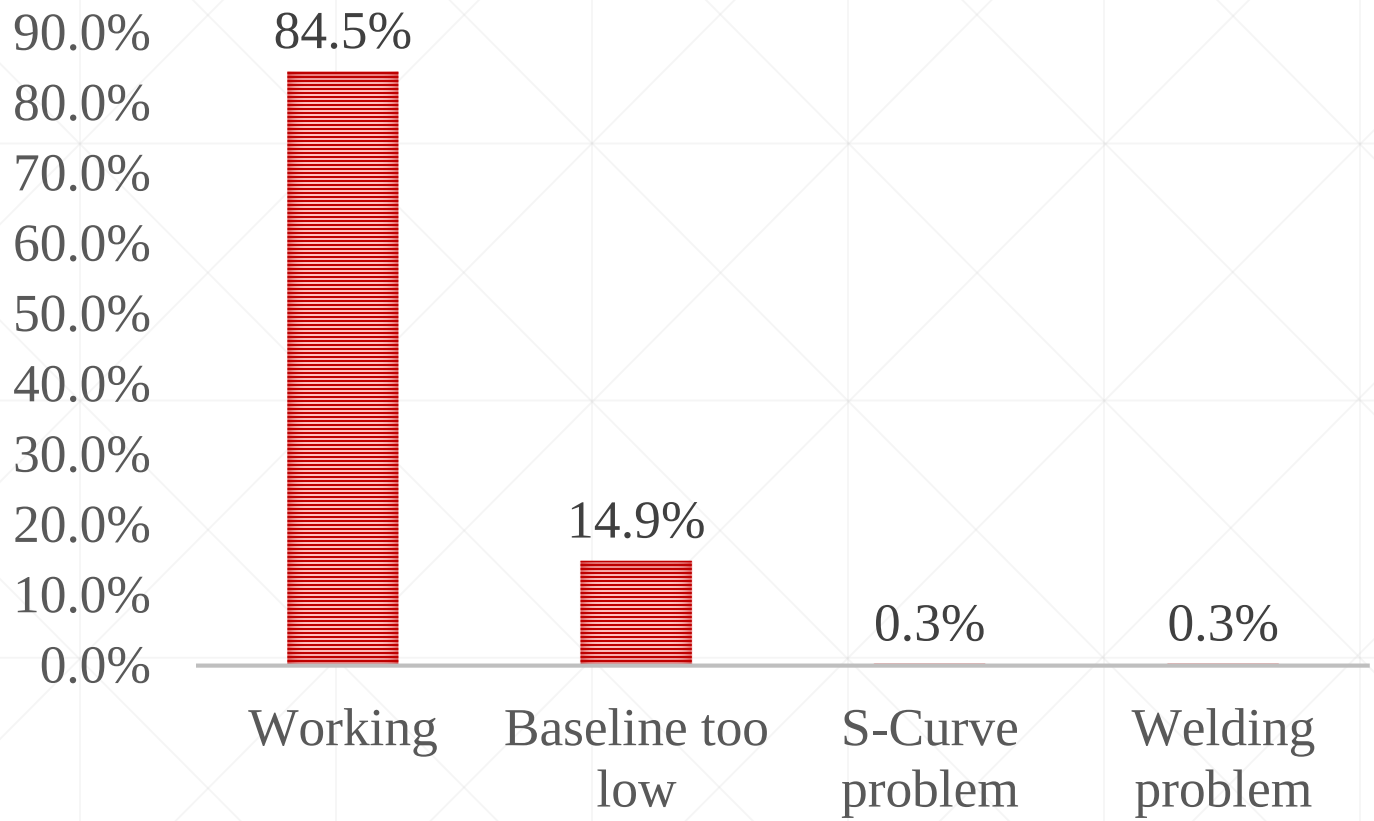


Updated test result for 2nd batch in Tsinghua

- Solved the current fail problem and retested several boards
- 362 boards:
  - Working: 305
  - Baseline too low: 54
  - S-Curve problem: 1

  (not uploaded to database)
  - Welding problem: 1

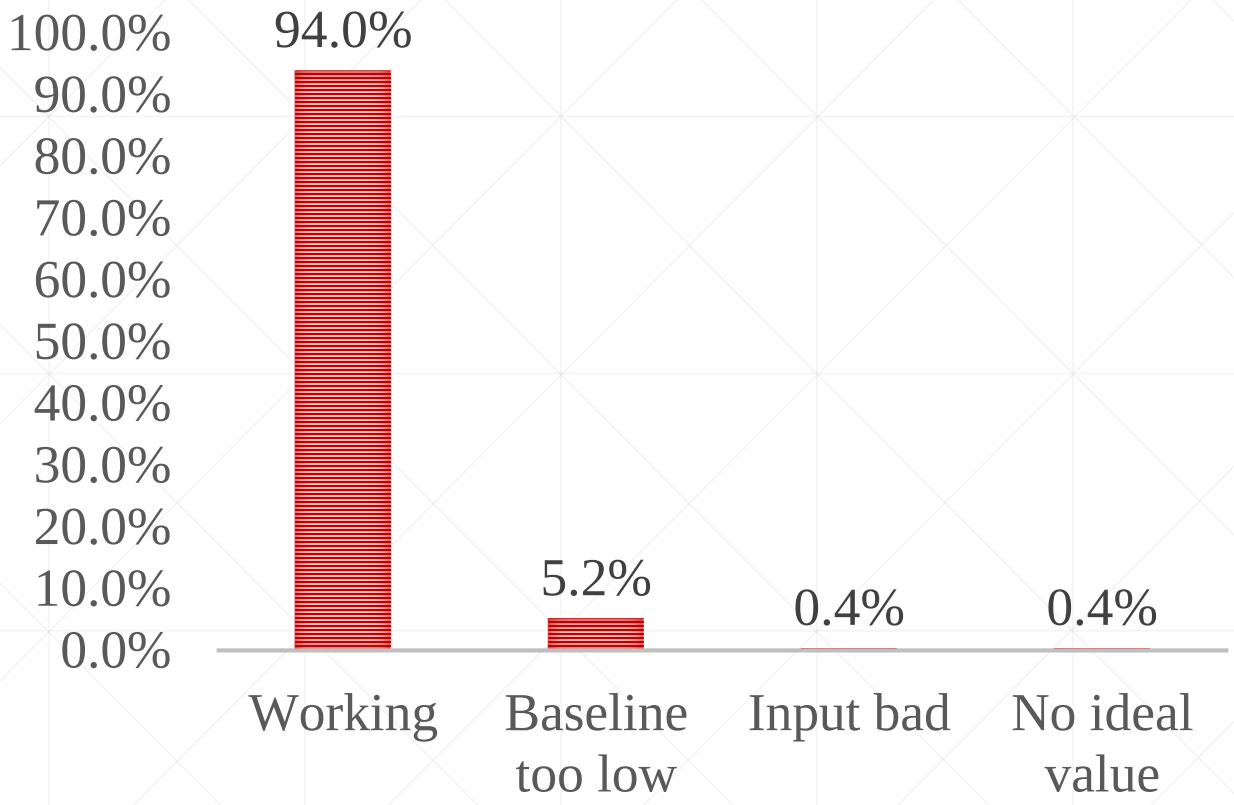
  (not uploaded to database)



Updated test result for 3rd batch in Tsinghua

- Solved the current fail problem and retested several boards

- 250 boards:
  - Working: 235
  - Baseline too low: 13
  - Input bad: 1
  - No ideal value: 1

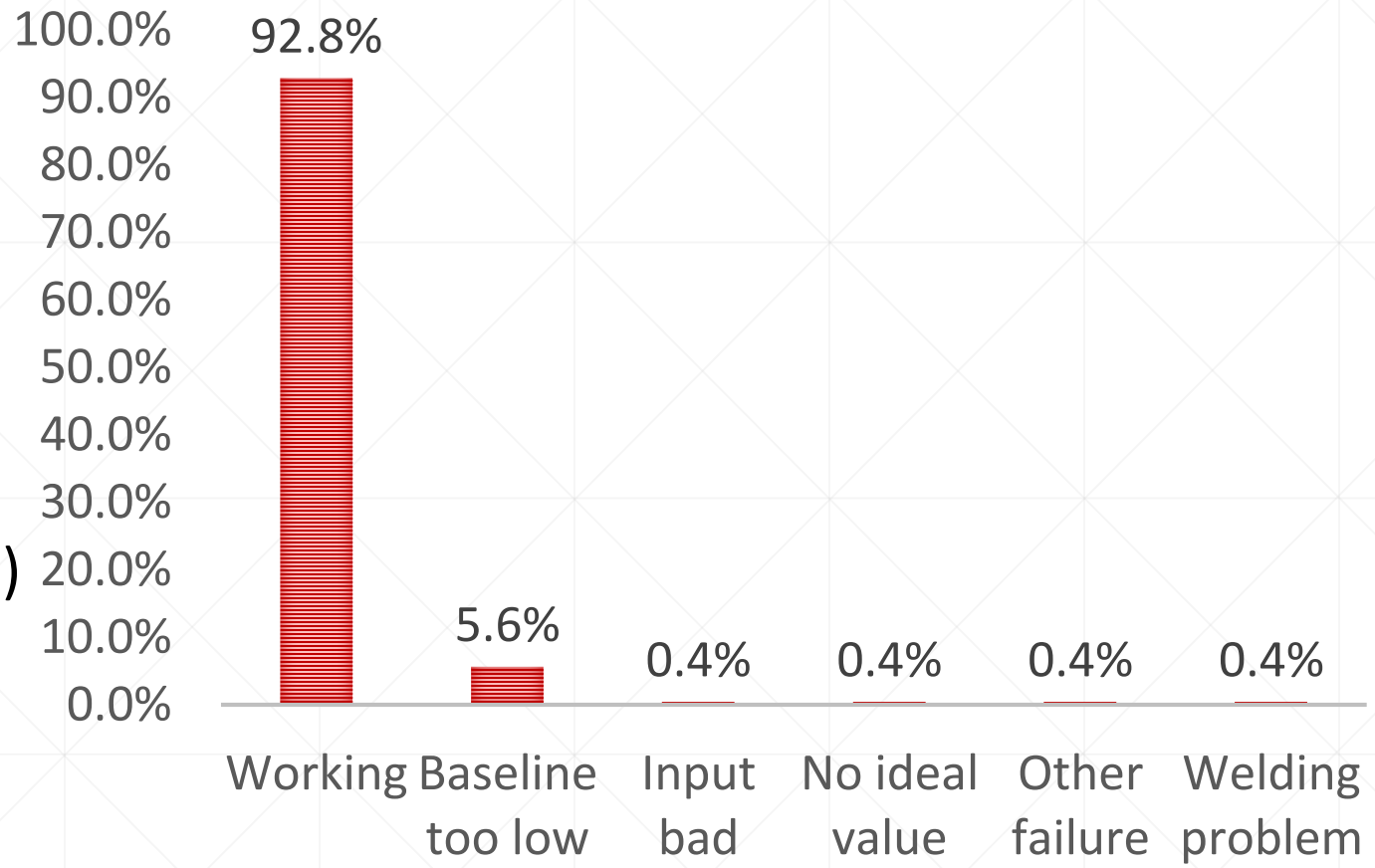


Test result for 4th batch in Tsinghua

- 250 boards:
  - Working: 232
  - Baseline too low: 14
  - Input bad: 1
  - No ideal value: 1
  - Other failure: 1

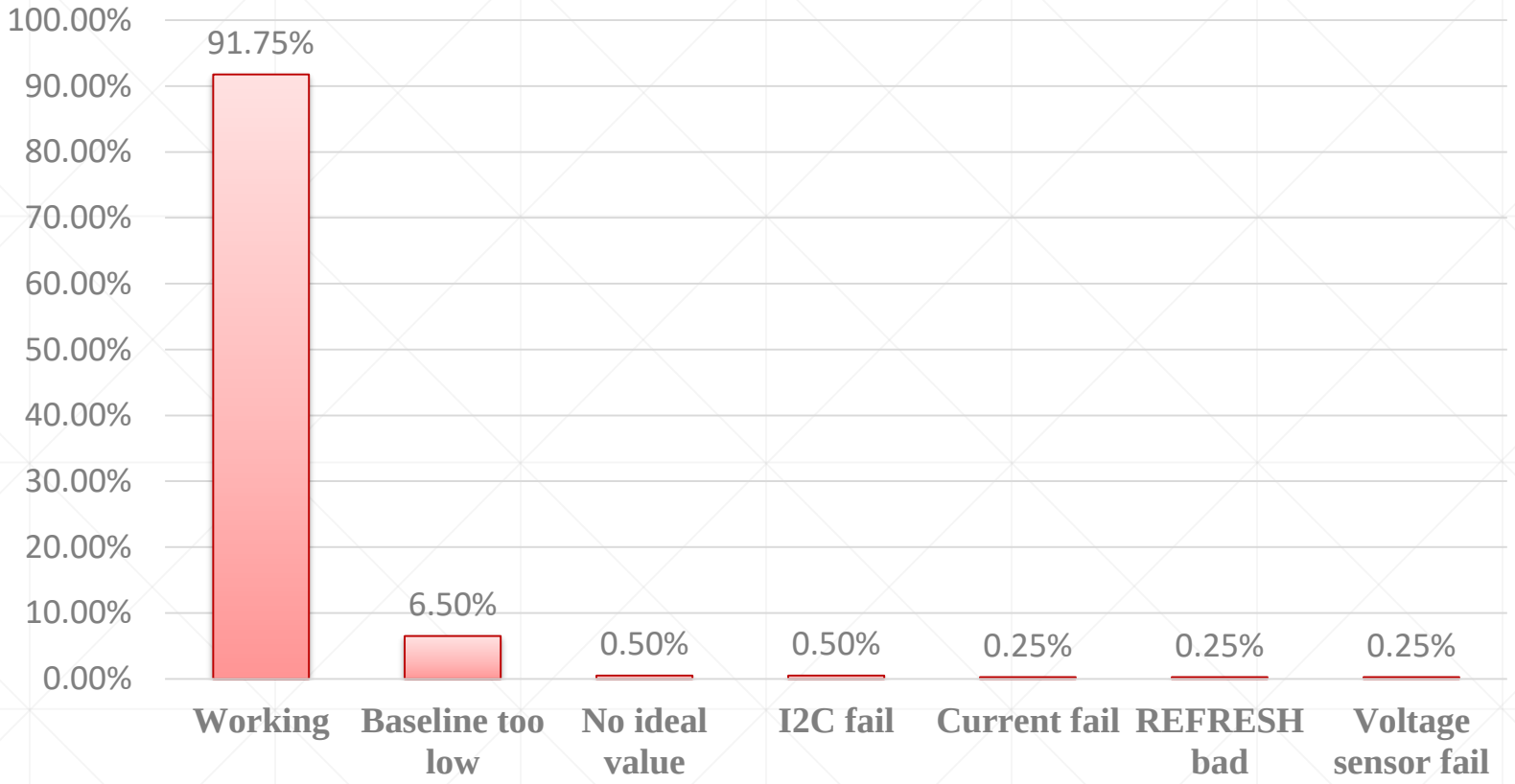
  (SiPM connector possible defect)
  - Welding problem: 1

  (not uploaded to database)

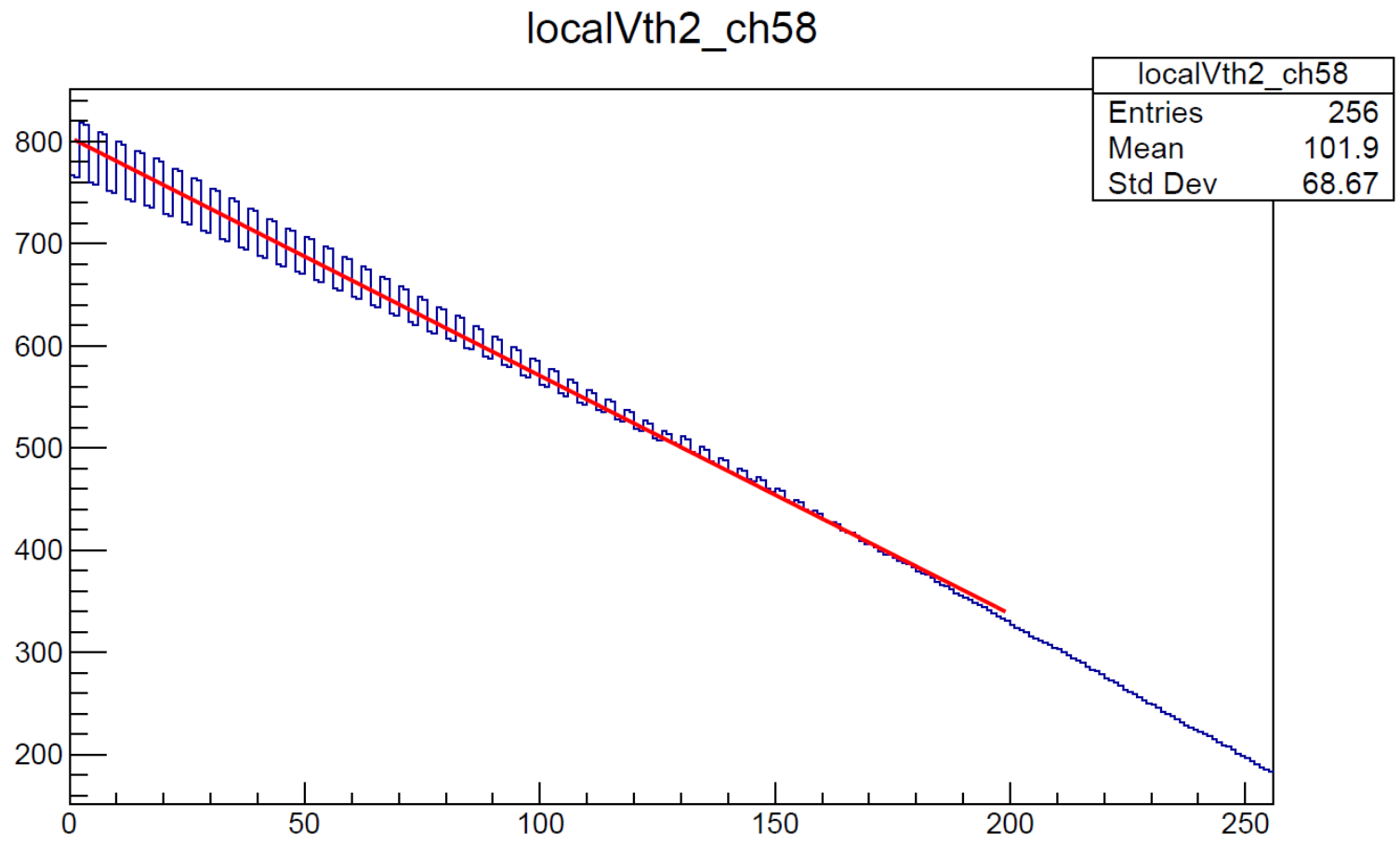


Test result of 5th batch in Tsinghua: Total

- 400 boards:
  - Working: 367
  - Baseline too low: 26
  - I2C fail: 2
  - No ideal value: 2
  - Current fail: 1
  - REFRESH bad: 1
  - Voltage sensor fail: 1



Main features of test results for one chip



LHCb Upgrade I: SciFi

From SciFi IB

Production:

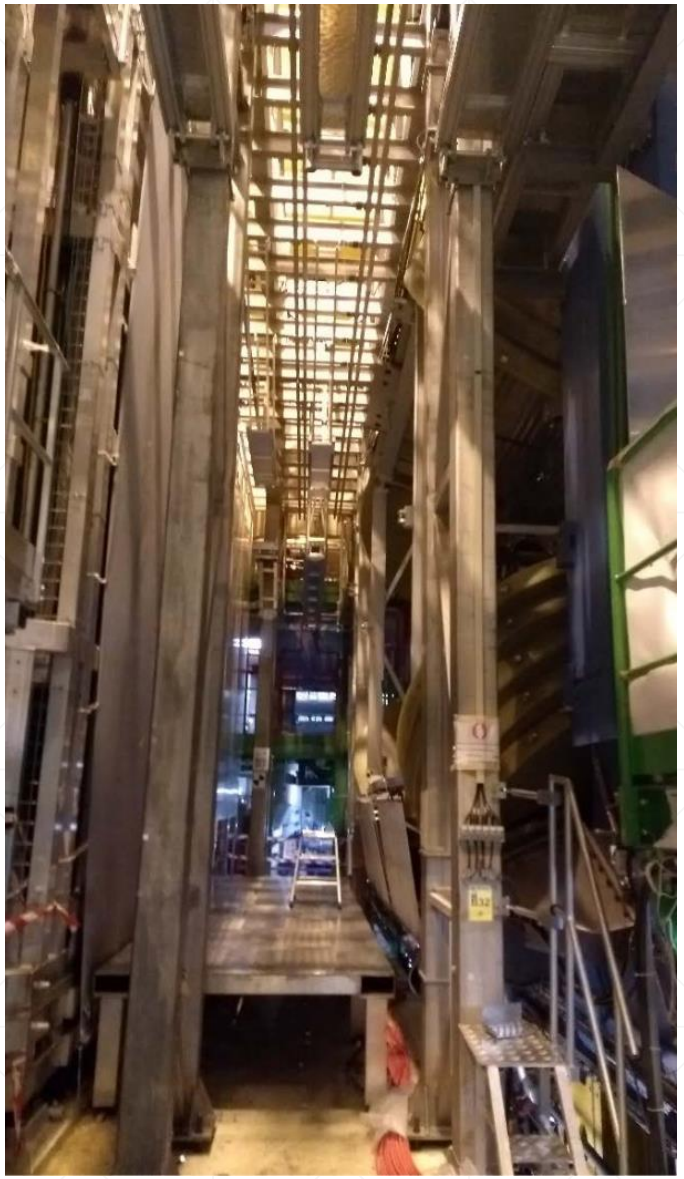
PACIFIC Chip	100% produced and tested
PACIFIC Board	100% produced and tested
Cluster Board	100% prodcued and tested
Master Board	Preseries 50 MBs: ok Main production (570 boards): Batch 1: 96 MBs in July Batch 2: 104 MBs in Aug Batch 3: 100 MBs in Sep Next batches: 08 Nov, 06 Jan
Mechanical Parts	100% produced

Congratulations to
- Tsinghua, Valencia, HD
- Clermont-Ferrand

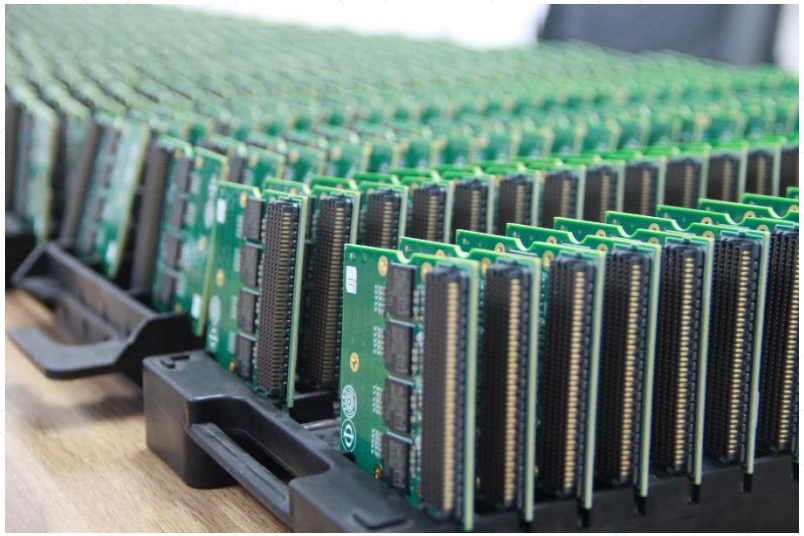
Front-end boxes	Preseries (23) ready → frame1 Batch 1: 30 boards at CERN Batch 2: expected this week Next batches: 30 FEBs/3 weeks

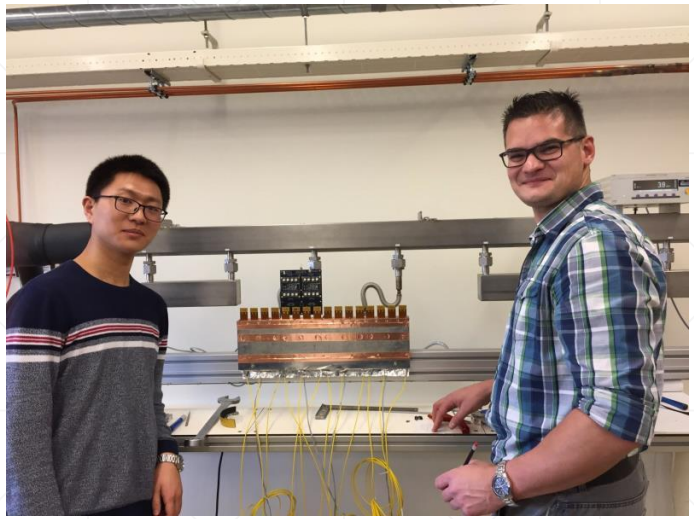
FEB finishing determined by MB schedule: Significant delays, however in shadow of delays of C-frames

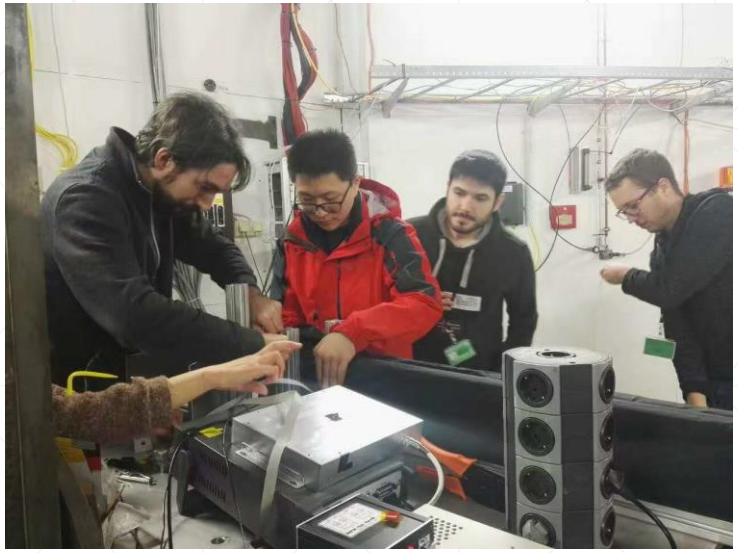
Very detailed test of FEBs at CERN, progressing very well (Massa + students).



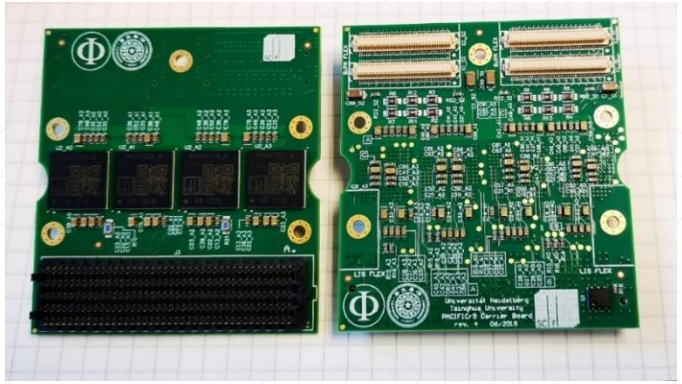
LHCb SciFi China Group

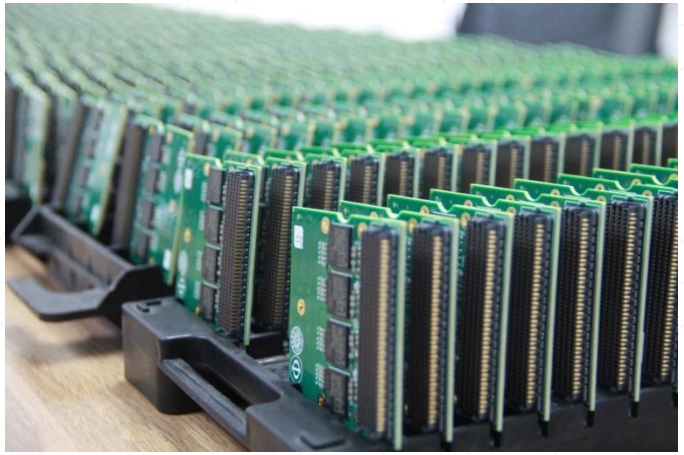






LHCb Upgrade I: SciFi (LHCb China Group)





- **SciFi : 524,000 SiPM Channels**
- **PACIFIC – 64 channel SiPM readout ASIC**
- **LHCb SciFi China Group :**
  - **Co-design the PACIFIC Board (with Heidelberg)**
  - **Manufacture all 2,300 PACIFIC Boards (Finished in 2019)**
  - **Test 1/2 of the PACIFIC Boards (another ½ @Valencia)**
  - **Quality Assurance System for PACIFIC chip selection**

    (6 setups @Tsinghua, Barcelona and Heidelberg)
  - **Quality Assurance System for PACIFIC Board**

    (5 @Tsinghua, Valencia and Heidelberg)
  - **Software: Build new sequence for SciFi specific processing of Testbeam data.**
  - **Commissioning in 2020 ……**

Thank you!

Questions?

References:

- https://cds.cern.ch/record/2630472/files/passaleva-ichep%2007.07.pdf
- https://cds.cern.ch/record/2650584/files/181206_Kruger.pdf
- https://cds.cern.ch/record/2648754/files/grauges-LHCb-NagoyaHfNPFP.pdf
- ……