ATLAS Muon Detector Phase-II Upgrade

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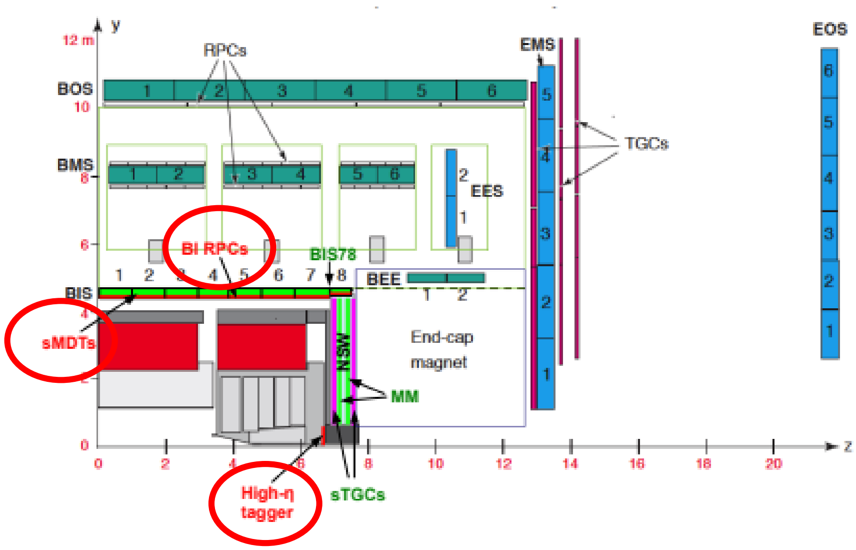
Outline

- ➢BI RPC upgrade
- ➢BI sMDT frontend electronics upgrade
- ➢High-eta tagger
- ➢Summary



BI RPC upgrade

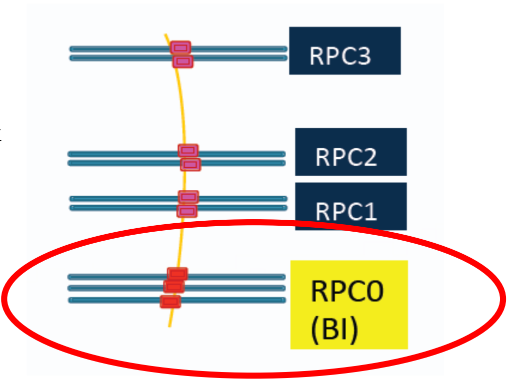
Introduction: BI RPC and Improvement

➢ Problem of current RPC in ATLAS

- Exceed their service time (10 years @ LHC)
- Rate capability limited: 20 Hz/cm^2
- Work under lower voltage → 15-35% eff. Lost

➢ The solution

- Add BI RPC layers (3 layers of RPC)
- Improvement of rate, longevity, time & spatial resolution.



- 9 layers instead of 6

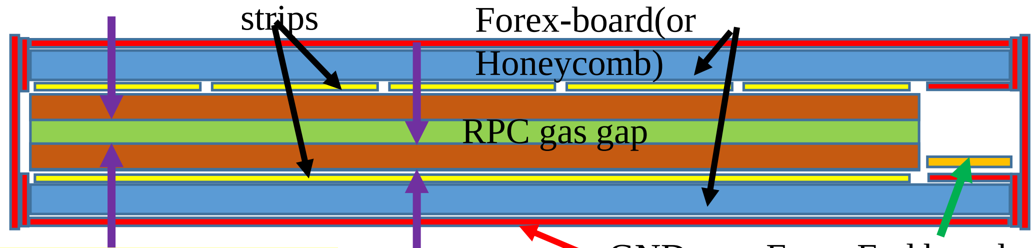
Improvement of RPC gas gap:

➢ Reduced gap size:
  - Less charge produced per event → improve longevity, rate capability
  - Less high voltage applied but higher field → better time resolution

➢ Reduced bakelite thickness:
  - Less voltage loss in bakelite → improve the rate capability

➢ New generation FE electronic:
  - Higher amplification factor and high S/N ratio to compensate the less gas amplification.

➢ Improved readout panel and method
  - Better mechanics structure, better signal transmission and good spatial resolution.

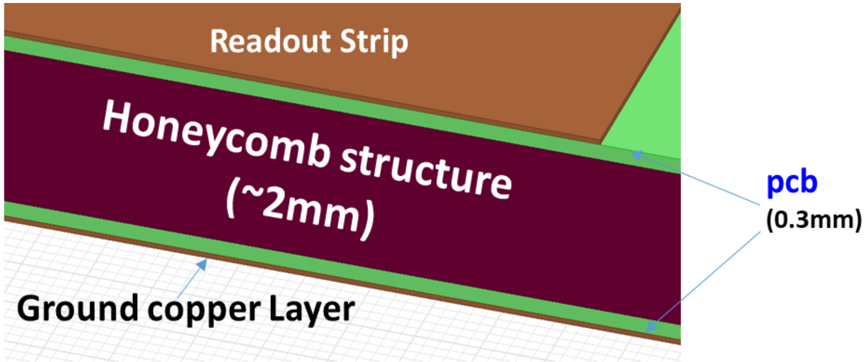


Gap size: 2mm→1mm

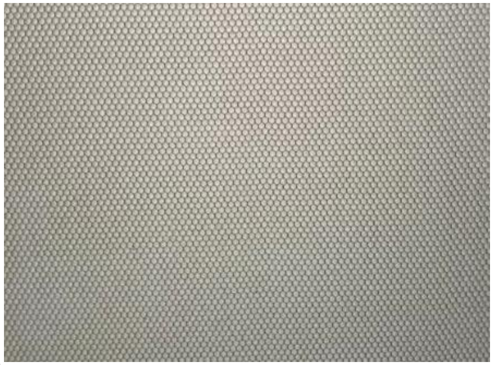
Bakelite: 1.8mm→1.2mm

New material of readout panel

- Main considerations of material: Dielectric constant (ε_r) , weight, rigidity
- Old design: foam-like material (low ε_r, fragile and soft)
- New design: honeycomb board (low ε_r and hard)



- Design and parameter of honeycomb read panel
- 2 layers of PCB as readout strip and ground
- ~2 mm honeycomb plate as medium
- Characteristic impedance: ~19 ohm
- Good performance tested in the double-end readout test

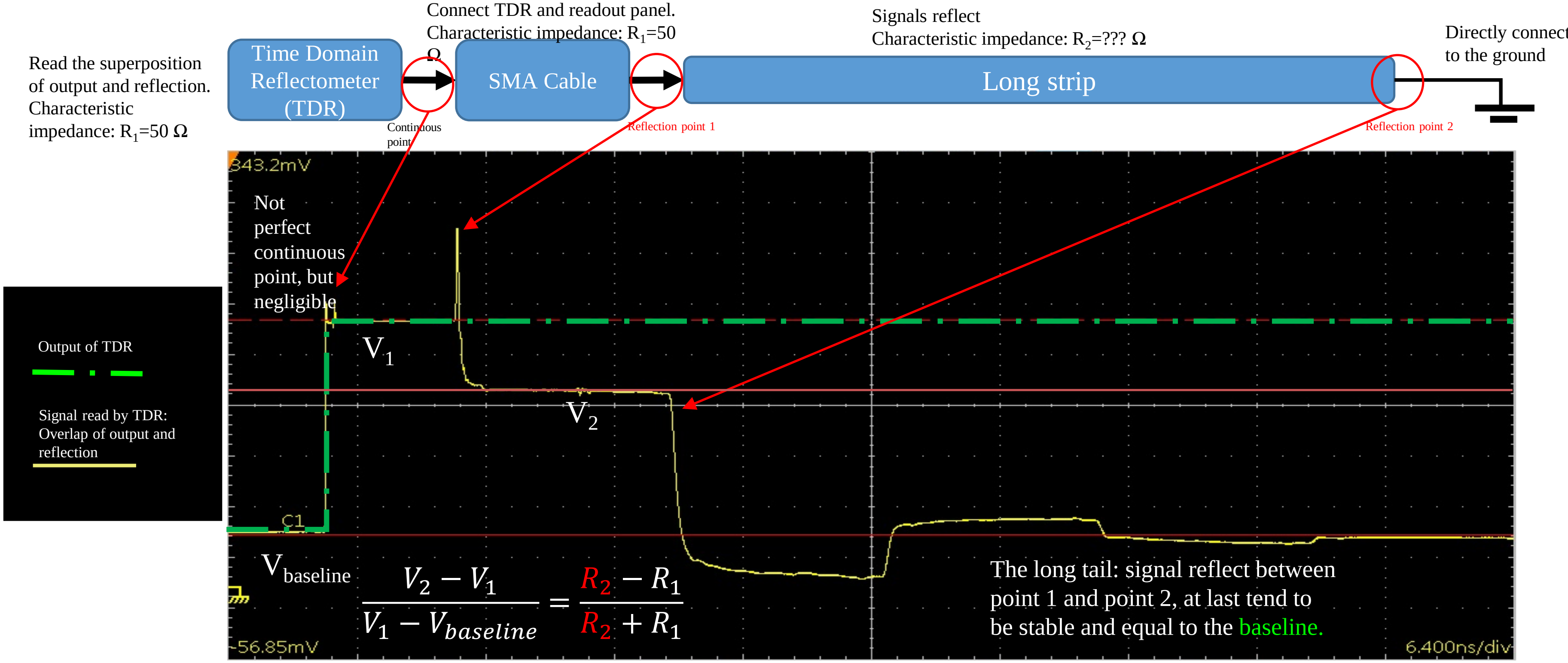


Raw honeycomb board

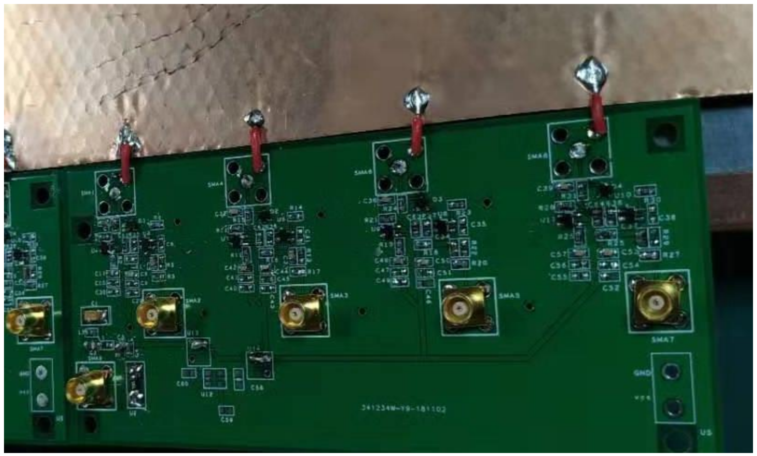
Completed honeycomb readout panel

Measurement of characteristic impedance

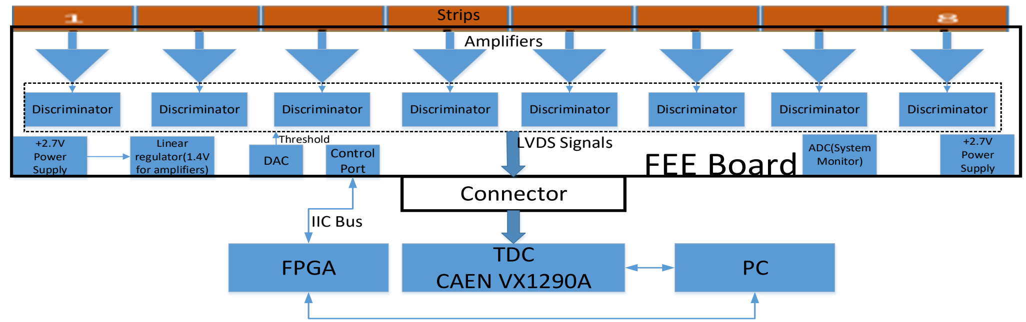
Precise measurement of characteristic impedance. This is necessary in the test of BI RPC during chamber assembly and in the measurement of new panel.

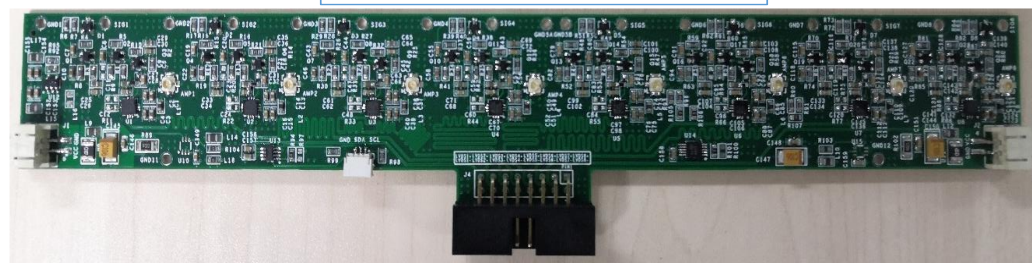


New FEE Board designed by USTC



Version 1 of FEE board(only amplifier):



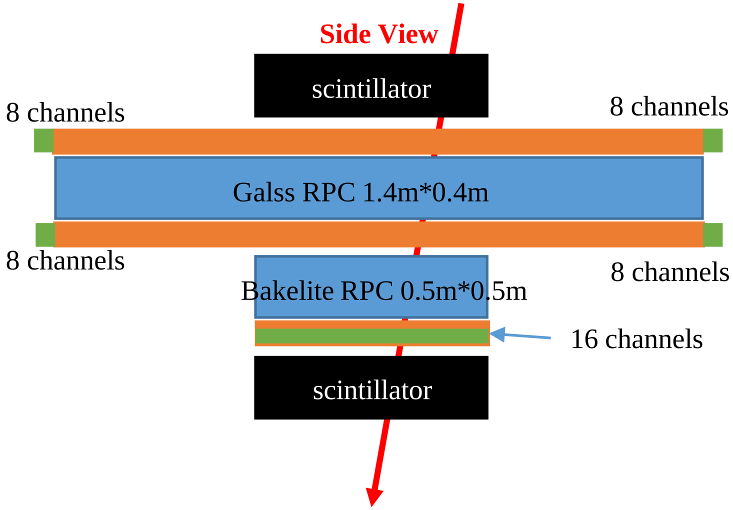


Version 2 of FEE board(amplifier-discriminator-LVDS converter):

- Two versions of FEE boards were designed by USTC.
- Compared with that of INFN, USTC FEE board has larger gain, wider bandwidth and lower power consumption.
- Current and voltage could be monitored by software.
- Now the second version of FEE board is under testing in USTC.

Double-ends Readout Method

- Trigger: coincidence of 2 scintillators
- Bakelite RPC used as reference and speed calibration.
- Signal read from both front end and back end of panel
- Hit position(HP) ∝ (T_frontend – T_backend)
- HP1 and HP2 reconstructed by panel1 and panel2.
- Histogram filled by (HP1 – HP2): Gaussian distribution
- Spatial resolution: $\sigma/\sqrt{2}$



System setup

- Fig (a): Scatter plot of 2 hit positions found by bakelite RPC and reconstructed by glass RPC. Transmission speed: 19.69 cm/ns.
- Fig (b): Distribution of (HP1 – HP2). The best spatial resolution: 0.998 cm. Meet the requirement of Phase II Upgrade.

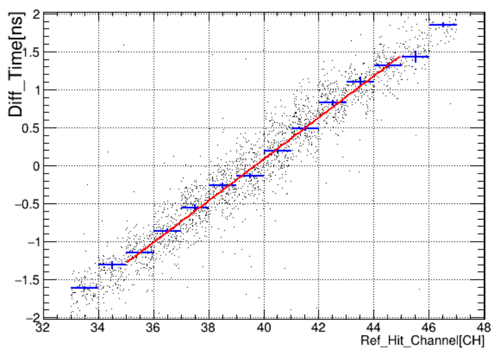


Fig (a)

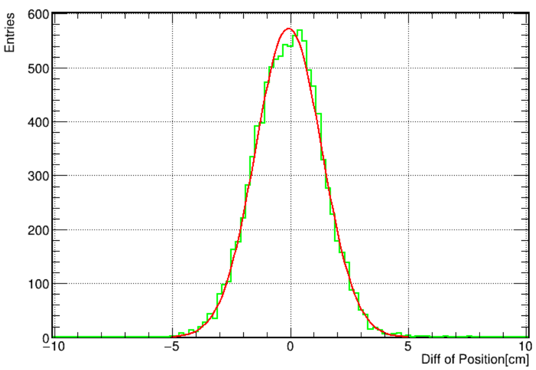
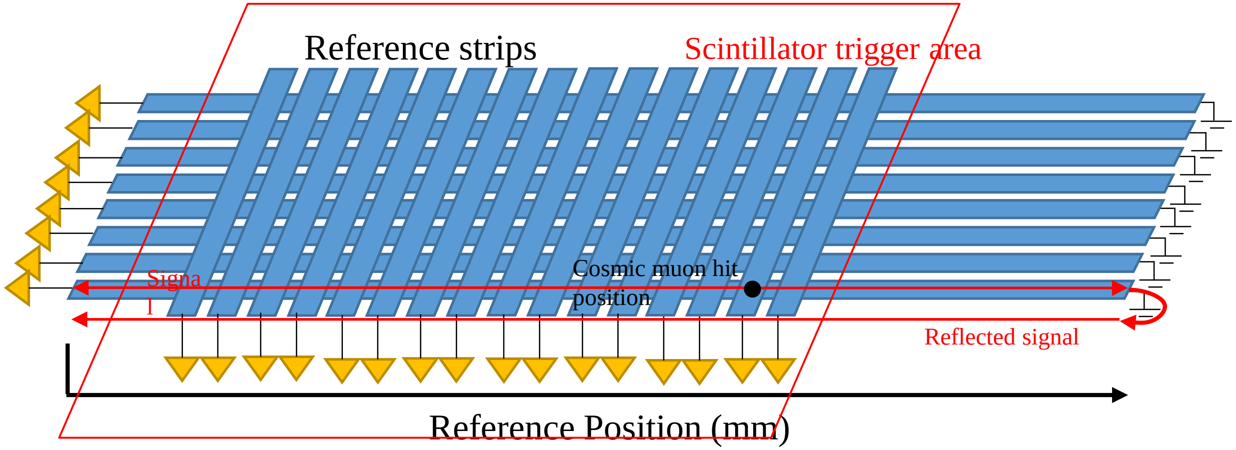


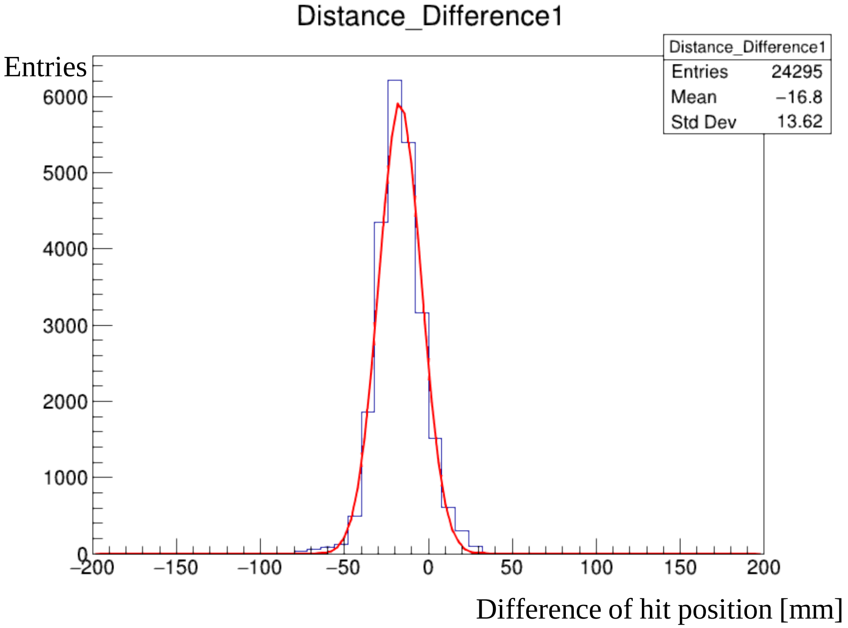
Fig (b)

Hypothesis: Single-end reflection readout



Gas gap/Strip size: 100cm * 50cm
Strip width: 25mm
Strip gap width 2mm

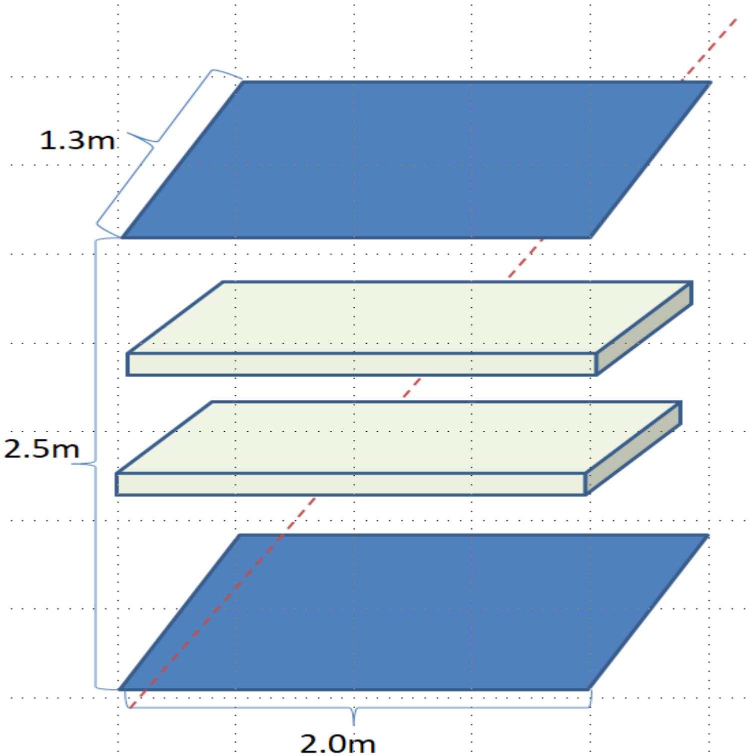
- ➢ An advancing improvement:
- The backend of strips are open or connect to ground directly.
- FEE board read signal and reflected signal from single end of the strips.
- Hit position can be reconstructed by time difference between signal and reflected signal.
- Measured result: 1.015 cm.



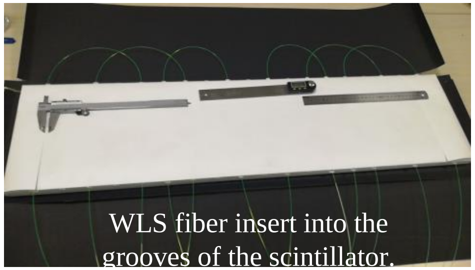
Big area trigger detector design (by SDU)

➢Trigger detector of the future RPC test system:

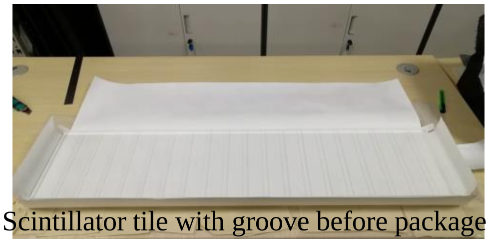
- BIS RPC max area：
  - 1820mm*1096mm
- Trigger detector sensitive area:
  - 2000mm*1300mm
- Light tight box of the trigger detector:
  - 2200mm*1350mm*50mm



Trigger detector assembly(SDU)

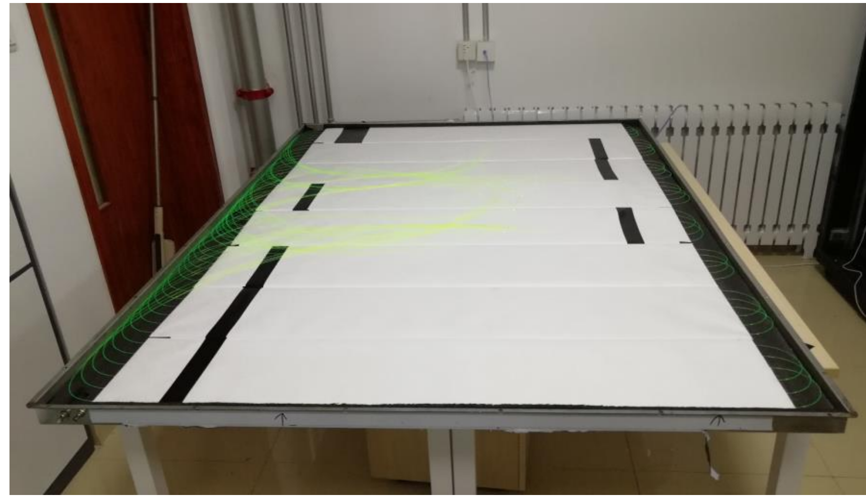


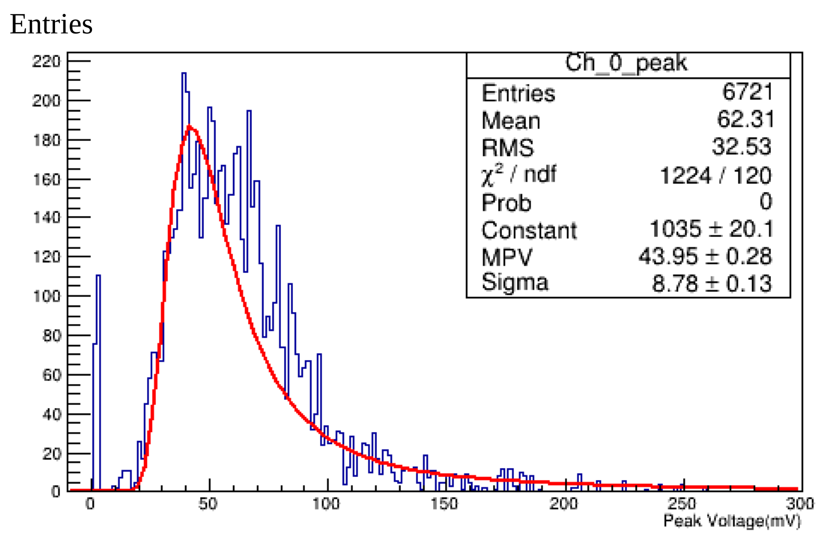
WLS fiber insert into the grooves of the scintillator.



Scintillator tile with groove before package with tyvek paper.

PMT





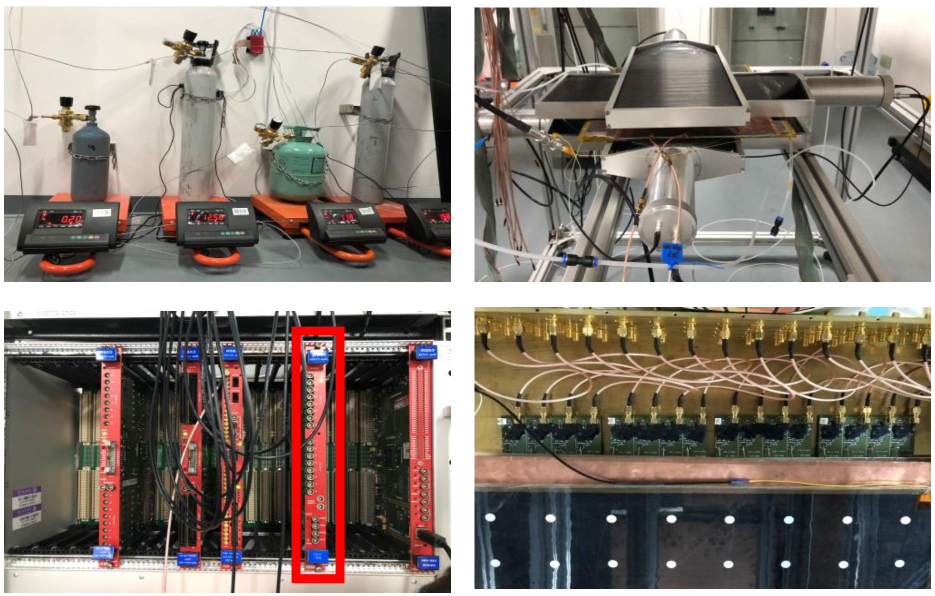
Amplitude of signal from scintillator

- ✓ 8 piece scintillators install in one light tight box
  - Each scintillator insert 6 WLS fibers
  - One PMT couple to all the fibers
- ✓ Quality of signal is good.
- ✓ Waiting more scintillators for another detector.

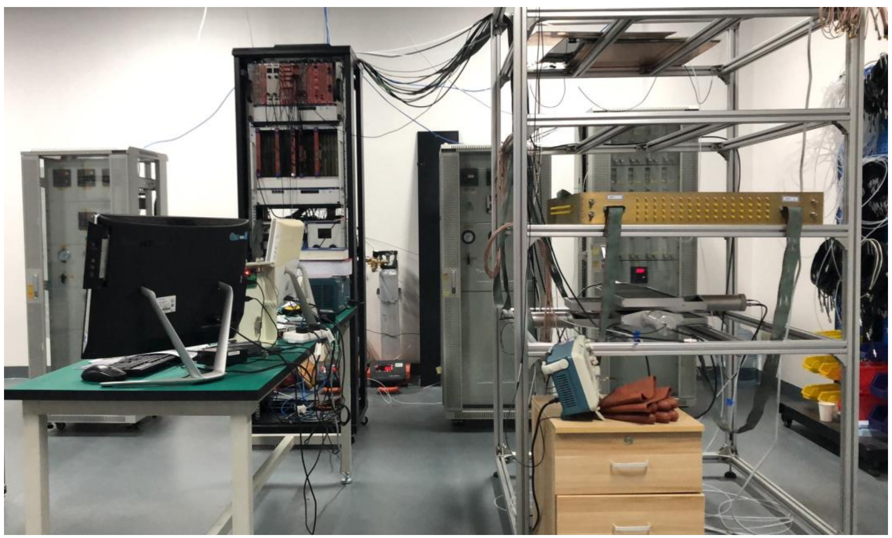
RPC Detector Laboratory in SJTU

The RPC detector test platform was built, including the gas distribution system, the trigger system, the test system and the readout system.

- Gas system： Gas components(**C_4H_{10},SF_6, R134a, N_2**)， Gas mixture, Gas distributor.
- Trigger system： **Scintillator, photomultiplier tube (PMT), and trigger module unit (TDC)** for signal discrimination and selection.
- Test system： **High voltage module, gas channel, Faraday cage, RPC to be tested** for the RPC performance testing.
- Readout system： **Sensitive detection unit (sensing strip), front-end electronics, analog-to-digital converter ADC, DAQ system.**



Gas, trigger, test and readout system



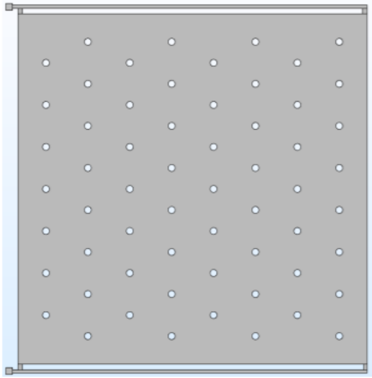
RPC detector test platform

Gas Flow Simulation on RPC detector (by SJTU)

◆RPC model construction

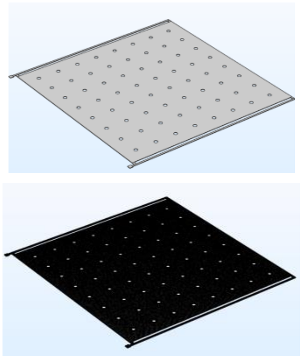
RPC size	Spacer placement	Inlet and outlet	Intake velocity
50cm*50cm*1mm	Alignment/ Misplacement	one in one out / one in multiple out on the same side /symmetrical on both sides	0~2m/s
20cm*20cm*1mm			

Different RPC design and simulation parameters

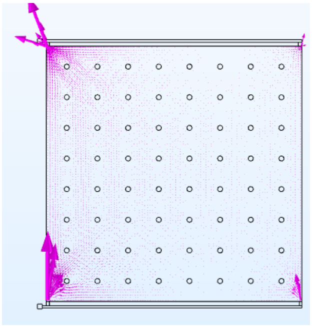


Misplacement of the spacer

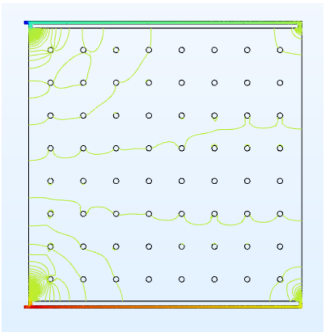
◆Simulation and analysis



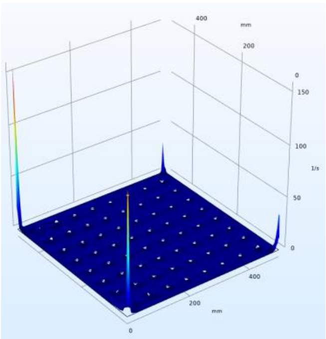
RPC structure design and meshing



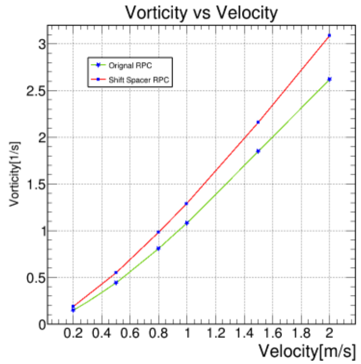
velocity distribution



Pressure distribution



Vorticity distribution



Average vorticity corresponding to the two spacer placement methods

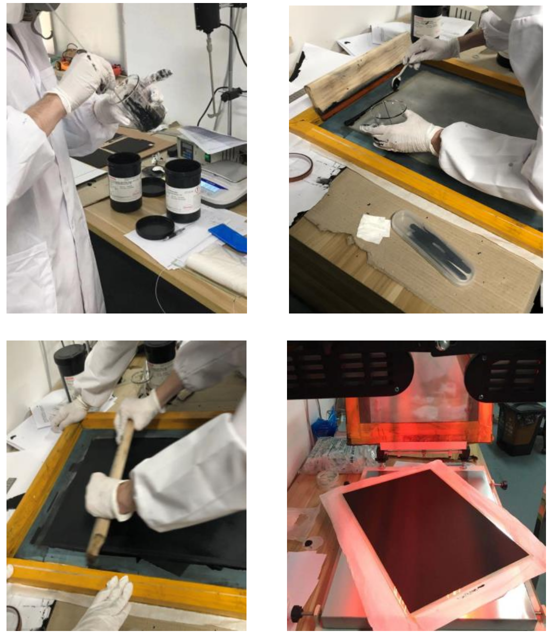
- The gas flow simulation of the RPC detector obtained the **velocity, pressure and vorticity distribution** inside the RPC.
- The **average vorticity of the misplacement** was smaller, that is, the gas flow stability was better.

RPC construction and signal test (by SJTU)

- The laboratory has been able to produce RPCs of the following sizes:
  - **$200 \times 120 \times 1mm^3$、$200 \times 200 \times 1.2mm^3$、$500 \times 350 \times 1.2mm^3$.**
- After graphite coating(Silk Screen Coating), electrode soldering and packaging are completed, the signal is found.

RPC construction

RPC package



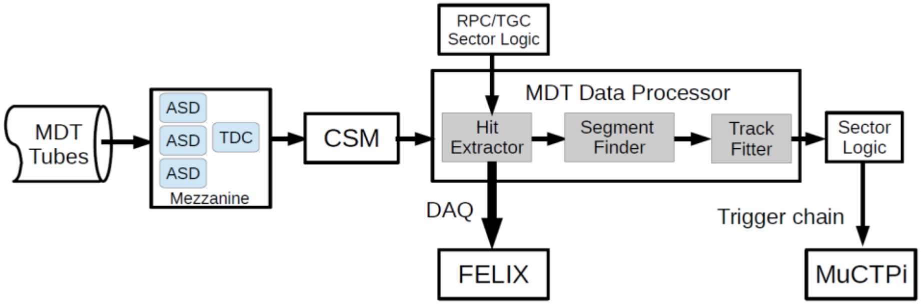
Silk Screen Coating

RPC signal reading

sMDT front electronics upgrade

Introduction: MDT Frontend Electronics Upgrade

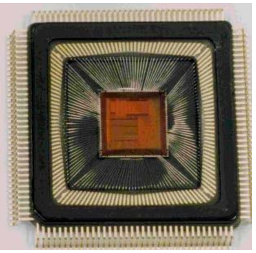
- ➢ Monitored Drift Tube(MDT) in current system is only used for precision readout
- ➢ After Phase II upgrade, MDT information will be used at the first-level trigger to sharpen the trigger turn-on curves
- ➢ MDT electronics needs to cope with new ATLAS TDAQ scheme proposed



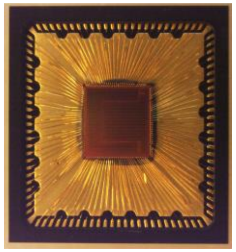
Block diagram of the MDT trigger and readout electronics for HL-LHC runs

Develop a new TDC ASIC for the MDT phase II upgrade:

- Comparable timing performance (Tubes unchanged): 102.4us dynamic range, 0.78ns resolution (~200 ps RMS);
- Time measurement: rising/falling edge/pair;
- No cooling system, need to keep the current power consumption budget: 350mW;
- Higher output data rates: 640Mbps;
- Additional features: Triggerless mode + Triggered mode.

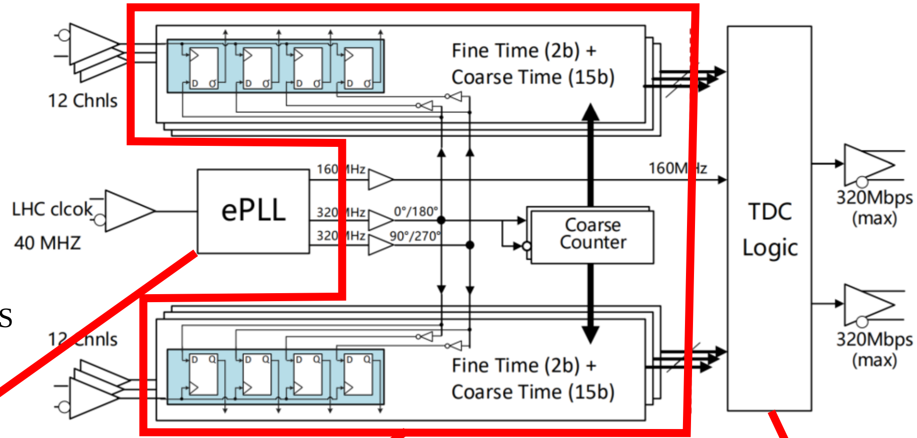


AMT



MDT-TDC UM

ASIC Design



Part 4: Interface
- Serial outputs
- Configuration
- Reference clocks
- TTC

Diff input: SLVS
Diff output: SLVS

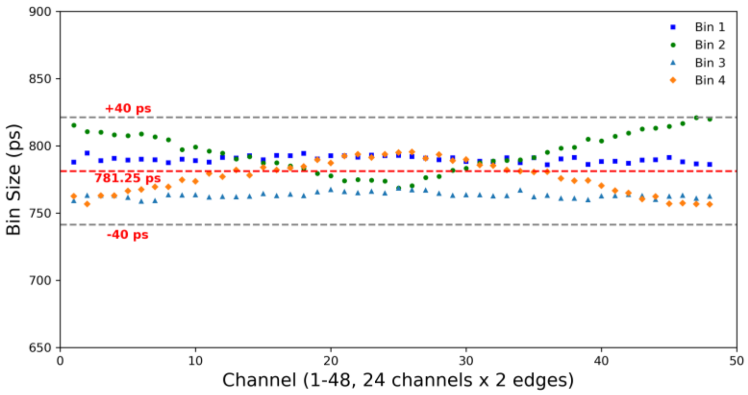
Part 1: ePLL (extended Phase locked loop)
- Migrate from CERN ePLL

Part 2: Timing Circuit: same as TDC v0
- Timing unit: fine time + coarse time
  - 4 clock phase time Interpolator
  - Coarse time(15bit) + fine time(2bit)
  - 0.78 ns bin
- Optimization in power consumption

Part 3: TDC logic:
- Full feature logic
  - Triggerless operation { Pair Mode / Edge Mode
  - Trigger operation { Pair Mode / Edge Mode
  - Output protocol
  - High speed interface
- Optimizations in power consumption

- Responsible for the time-digitization of the discriminated hit signal from ASD
- TSMC 130 nm CMOS technology used
- Triggerless mode used for data taking, triggered mode useful for chamber and test beam studies

Performance of TDC



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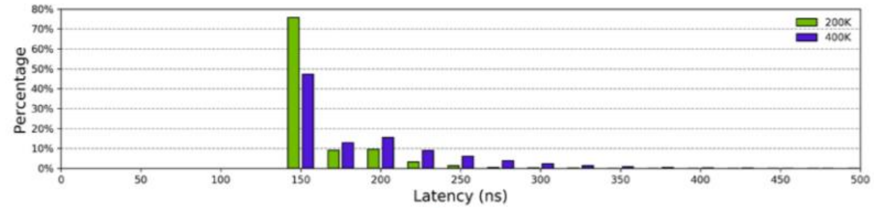
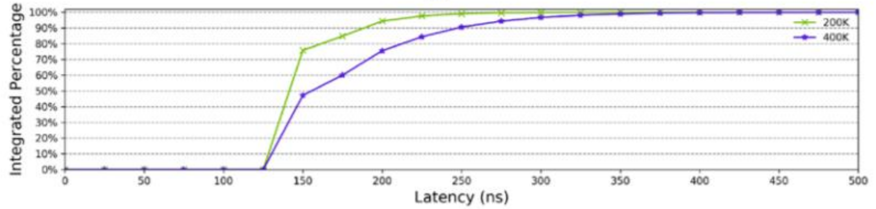
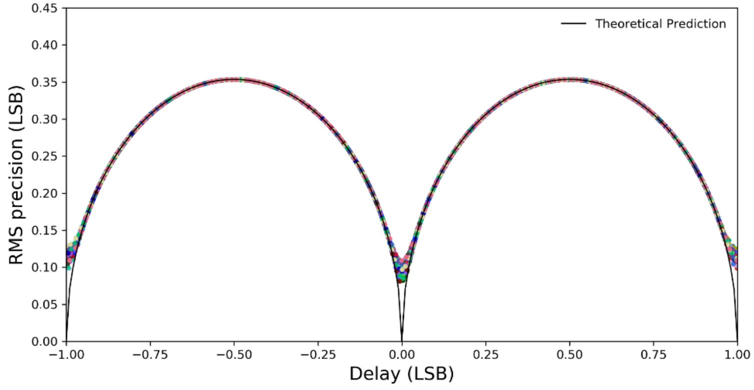


(a)

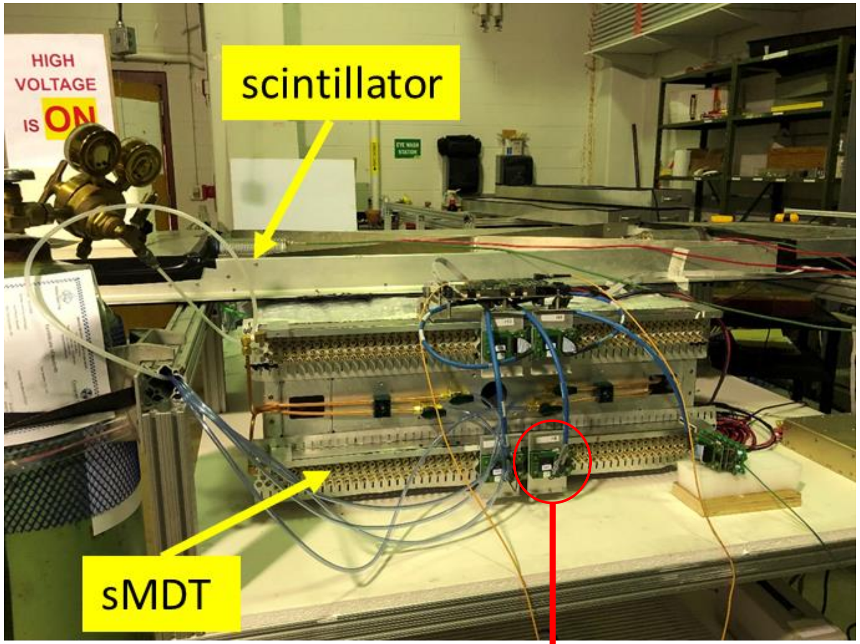


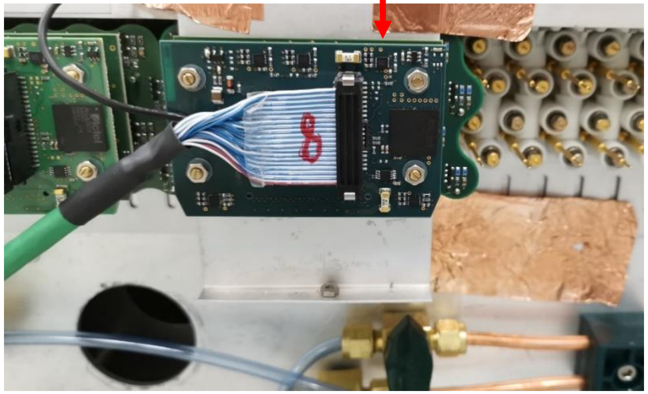
(b)



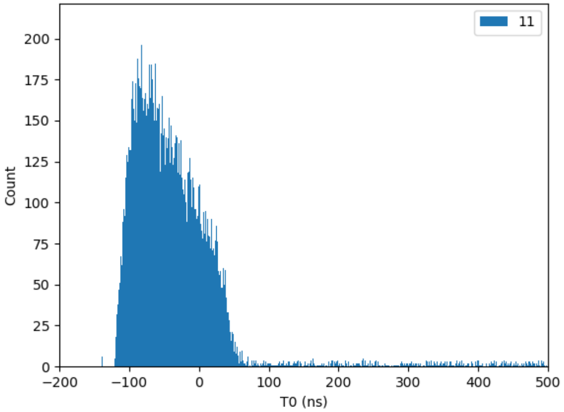
- ❖ **Bin sizes of all 48 channels (leading and trailing) are within (781 ± 40) ps**
- ❖ **timing resolution effect due to the TDC design is ~10% of the LSB (~80 ps)**
- ❖ **Latency is less than 350 ns (99% data read out) for a rate of 400 kHz per tube**
- ❖ **~250 mW power consumption (360 mW from the current AMT)**
- ❖ **No data loss observed for average channel hits at 400 kHz**

On sMDT chamber test





- When configured as legacy mode, the TDC is compatible to the legacy readout system.
- These pictures shows the scene when the TDC is tested on the newly built sMDT chamber at the university of Michigan



- TDC Spectrum of cosmic ray

High-Eta tagger

Introduction: High-Eta tagger

➢ Target of project:

- Complete the prototype of forward muon detector for ATLAS Phase II Upgrade based on multi-gap resistive GEM

➢ Expected performance：

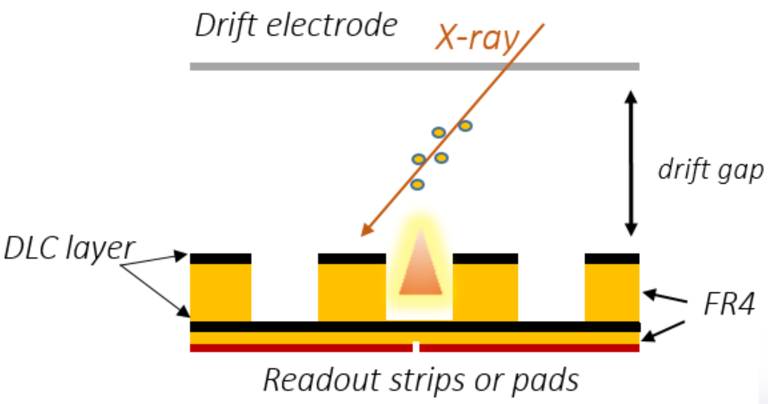
- Counting rate： ～100kHz/cm^2
- Time resolution： < 1ns
- Spatial resolution： $< 150\mu$m
- Efficiency： $> 95\%$

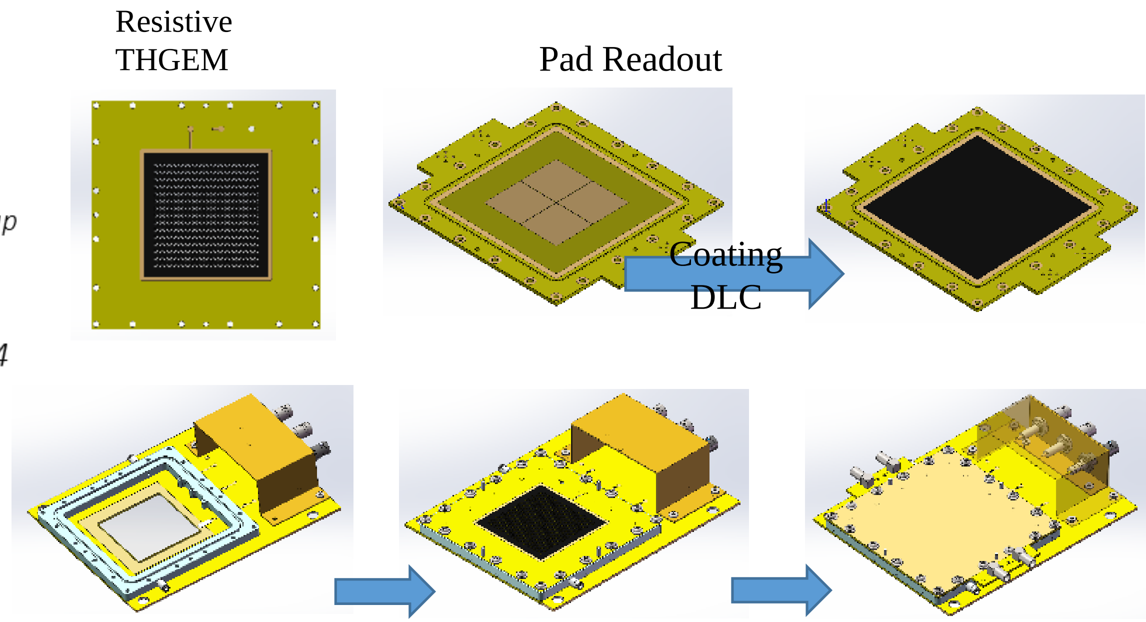
➢ Goal of this year:

- Time resolution of prototype < 1 ns

DLC-THGEM

- New technology of detector is performed: resistive THGEM based on Diamond-like Crystal(DLC)

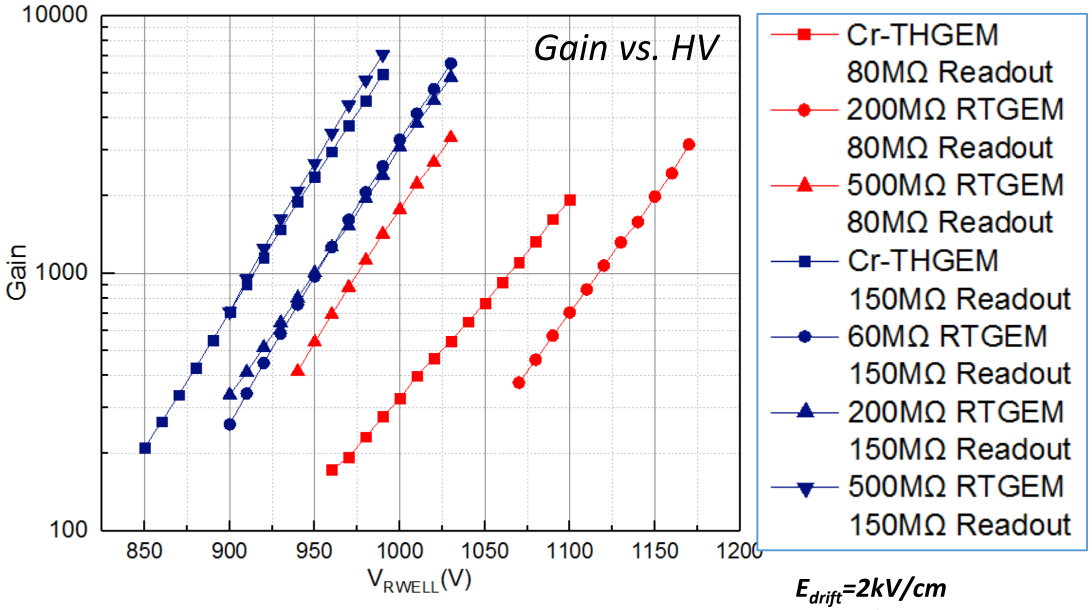




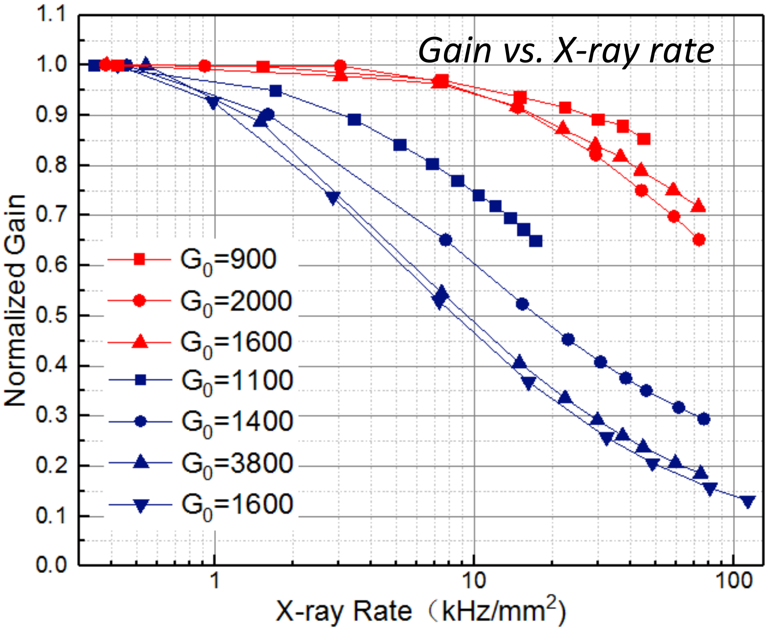
Resistive THGEM： avalanche region in PCB covered by DLC

- Ratio of avalanche region increase, gain increase
- No corrosion of insulating material, independent research and development

Performance test of DLC-THGEM



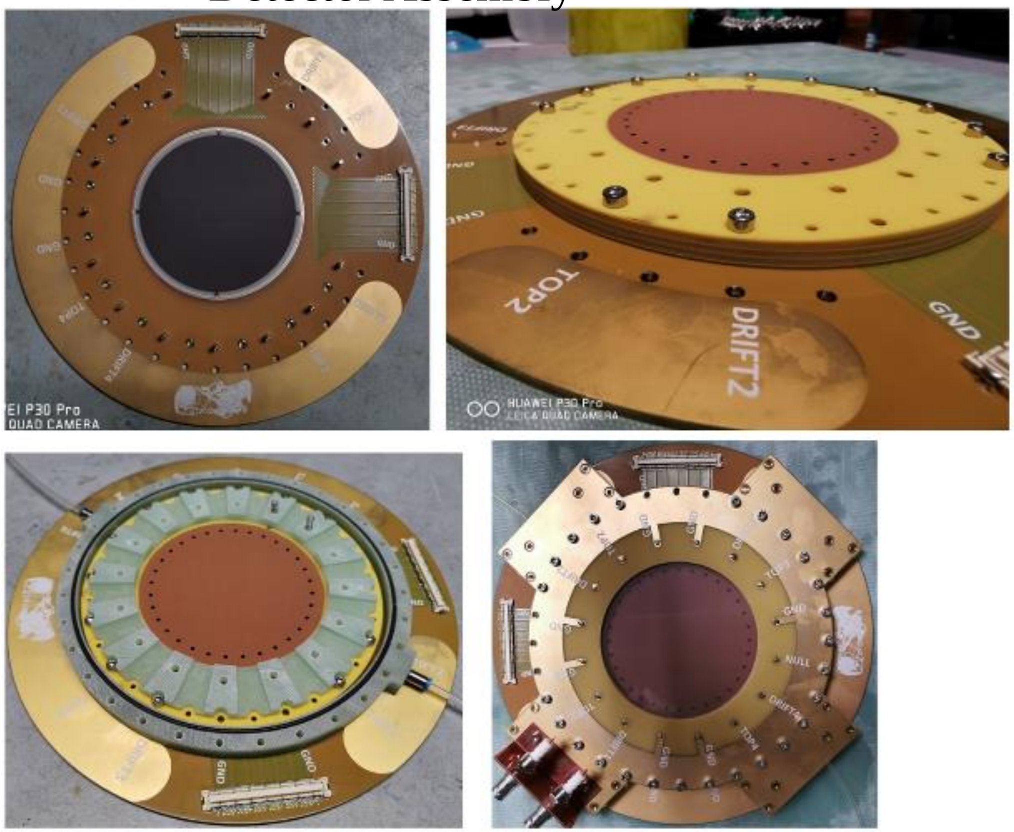
E_{drift}=2kV/cm
100Hz/mm^2 8keV X-ray



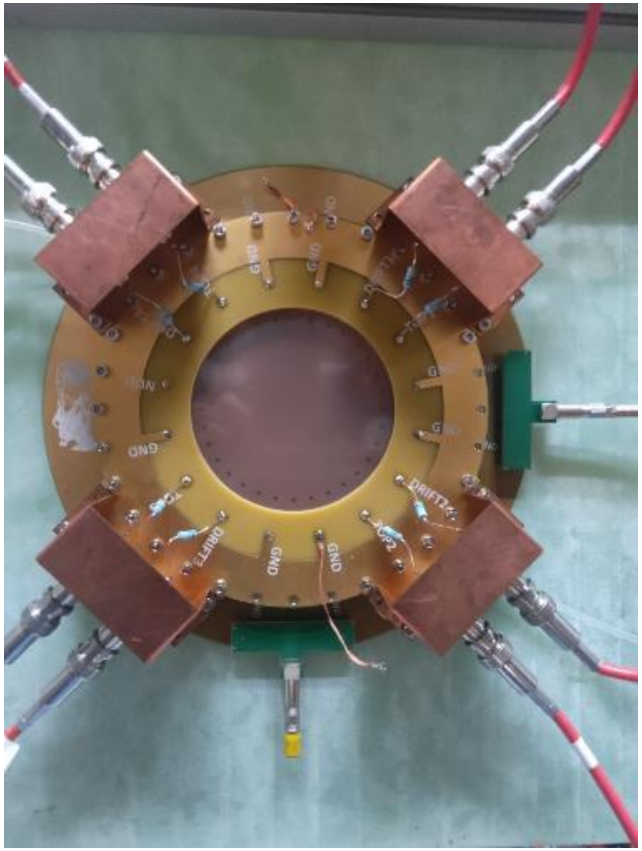
Signal could be found in single layer DLC-THGEM, the gain is ~ 7000

From single layer to 4-layers

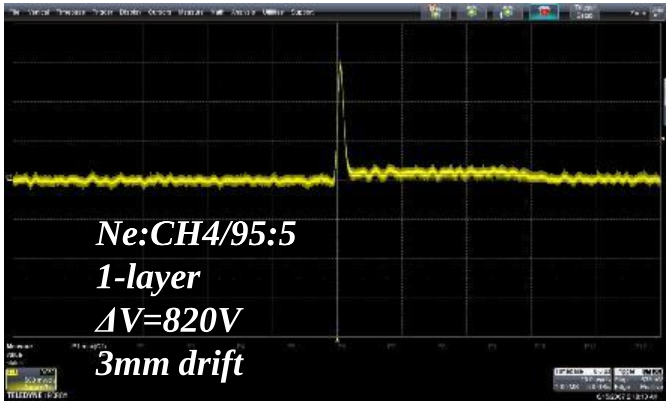
Detector Assembly

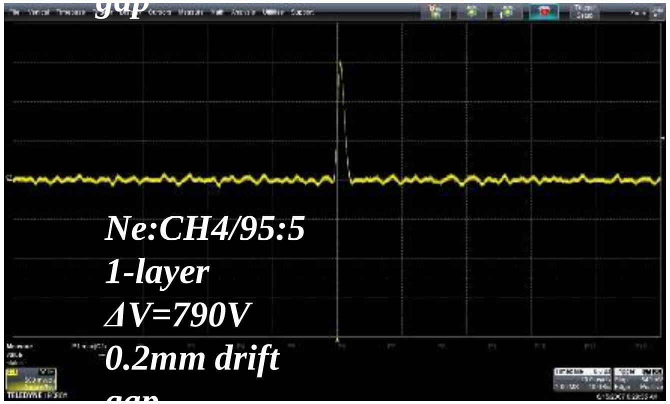


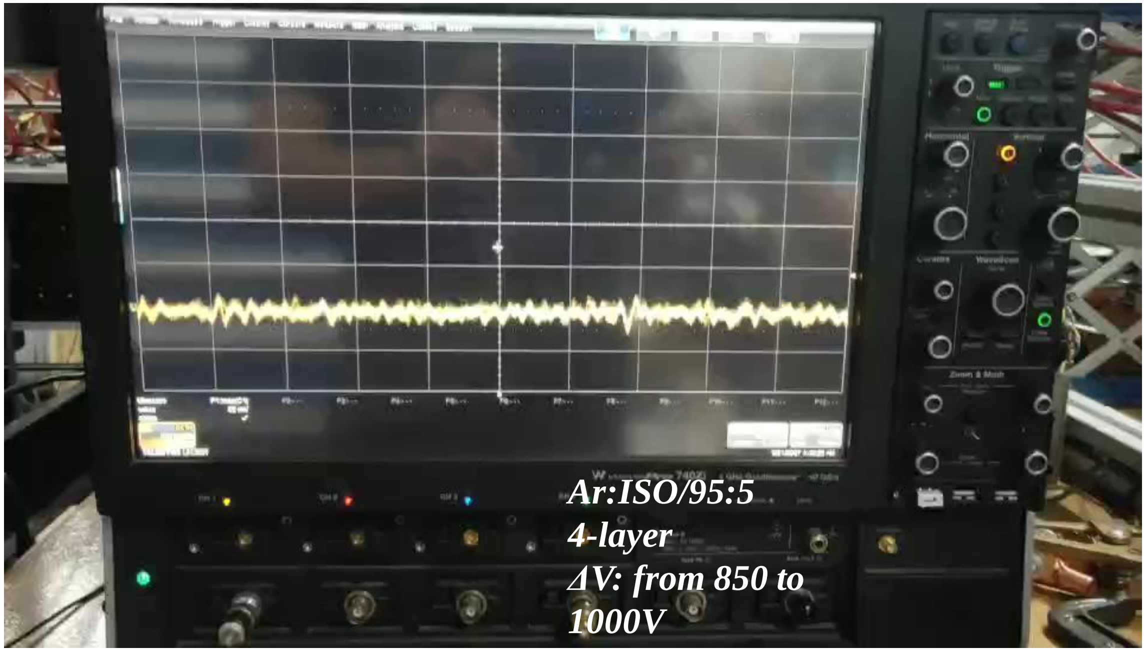
Performance test



Preliminary result







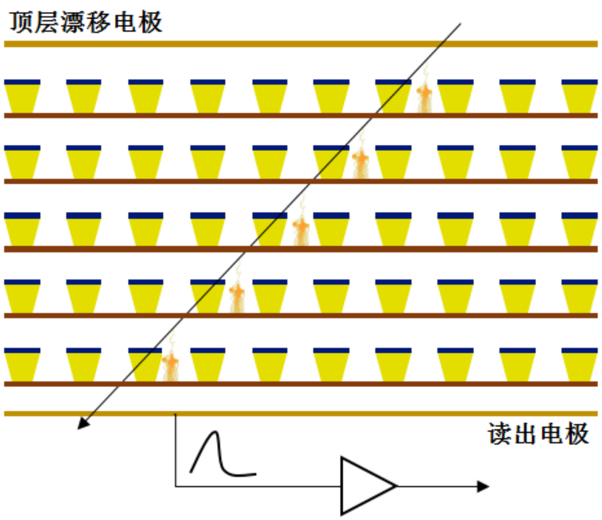
Obvious signal was found in 4-layers DLC-THGEM!

Summary

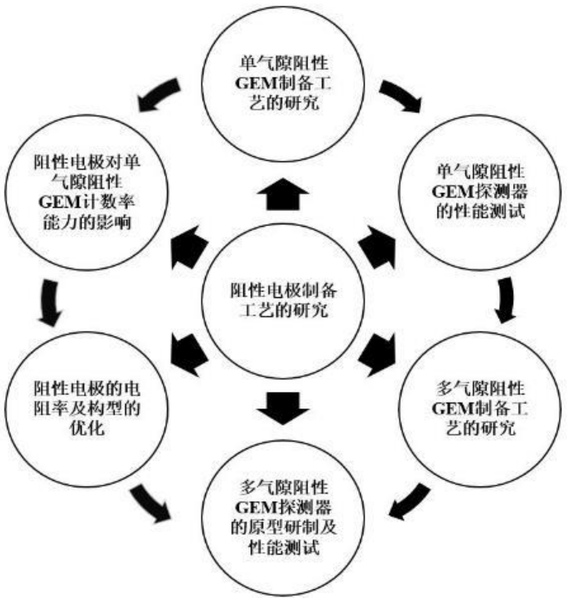
- USTC-SJTU-SDU cluster made great contributions to ATLAS RPC Phase II Upgrade.
  - Platform for RPC performance test and R&D test constructed
  - Improvement study on detector performance and electronics
- USTC participant in the TDC ASIC design and test of sMDT. Required performances achieved.
- New technology(DLC-THGEM) has been introduced in micro-pattern detectors and good timing is expected.

Backup

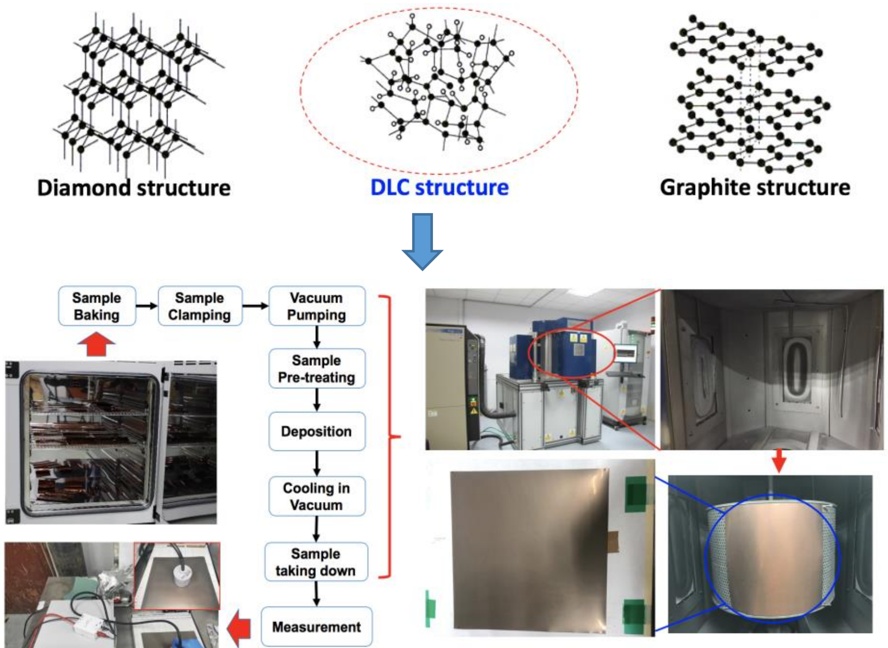
多气隙全阻性GEM结构



全阻性GEM结构的研制路线



阻性电极是核心：DLC薄膜沉积技术



- *Resistive DLC prepared by sputtering the high purity graphite targets*
- *Resistivity controlled by adjusting target power, deposition time, vacuum degree, element doping, and so on.*

与兰州化物所合作

科大牵头CERN RD51研发项目

Title of project: *DLC based electrodes for future resistive MPGDs*

Contact person:
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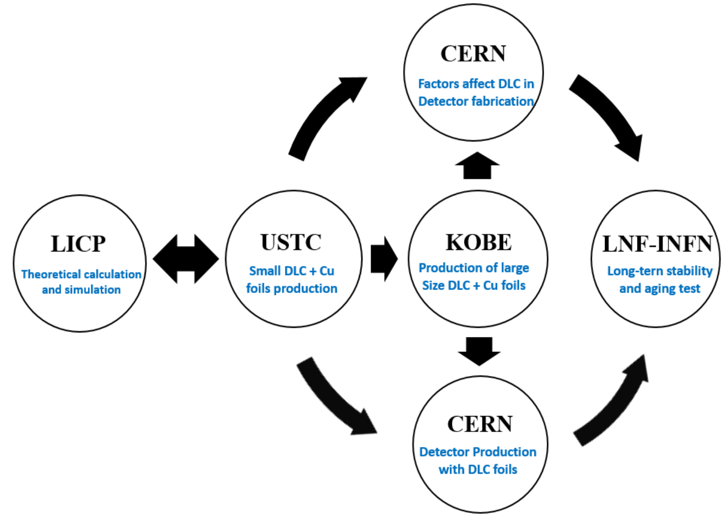
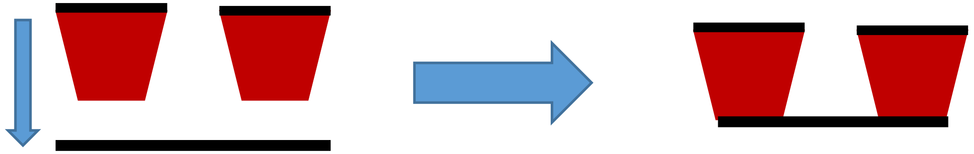
address: Jinzhai Road No.96, Hefei, Anhui, P.R.China, 230026
telephone number: +86-551-63607940
e-mail: zhouyi@mail.ustc.edu.cn



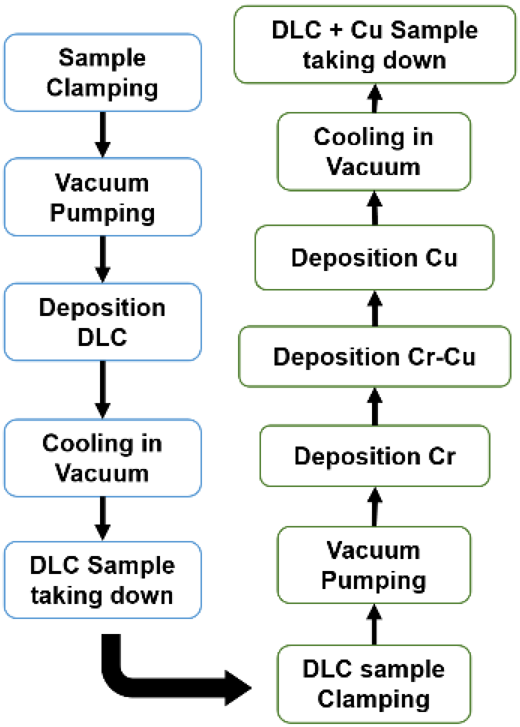
- DLC太薄，无法完全阻止腐蚀液透过，导致孔型结构受损。

- 悬浮式井型结构存在不稳定性，影响探测器的正常运行。

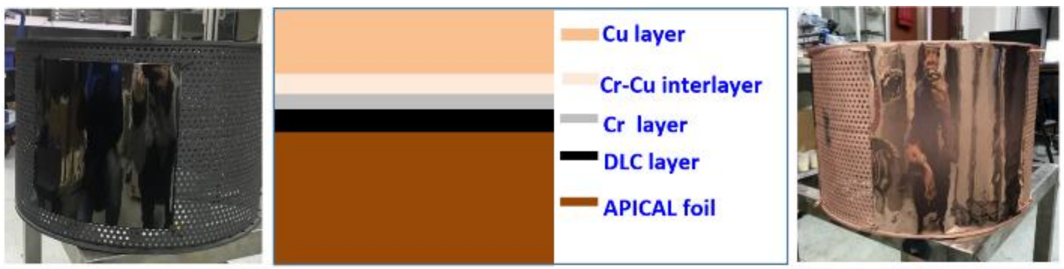


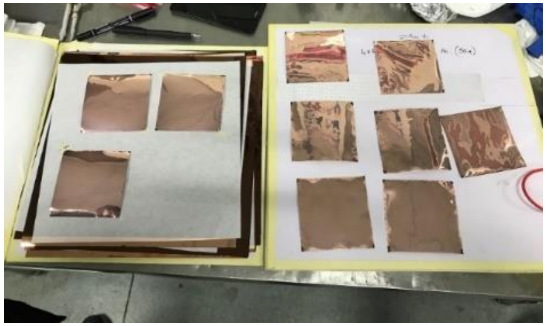
解决方案：镀铜的双面DLC阻性薄膜（复合DLC阻性电极）

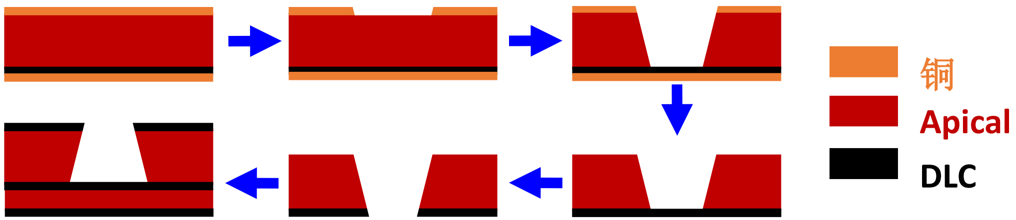
“DLC+Cu”制作流程

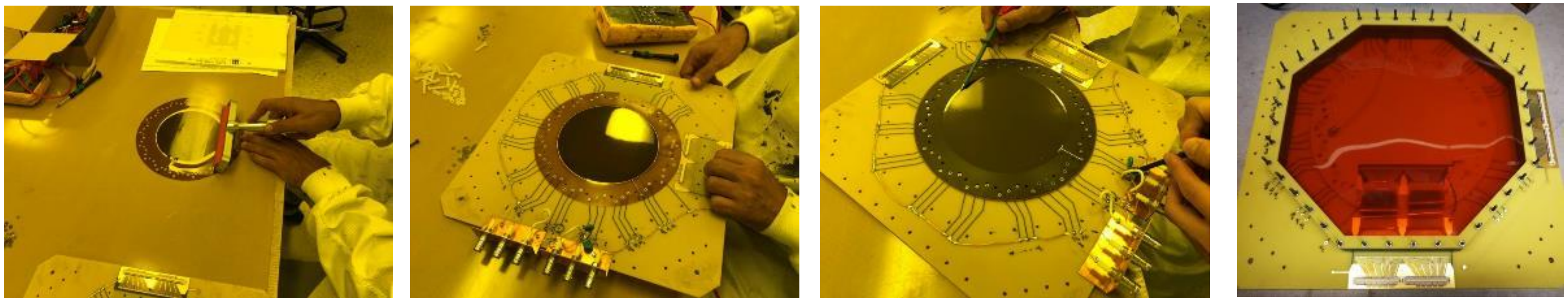


“DLC+Cu” 结构和样品









- 利用X射线测试探测器原型，读出电极有明显的输出电流，但观测不到任何感应信号。
- 原因推断：由于全阻性结构，使得雪崩区域只占权场区域很小一部分，造成感应信号微弱。此外，探测器增益偏低也是一个原因。