ALICE Detector Upgrade

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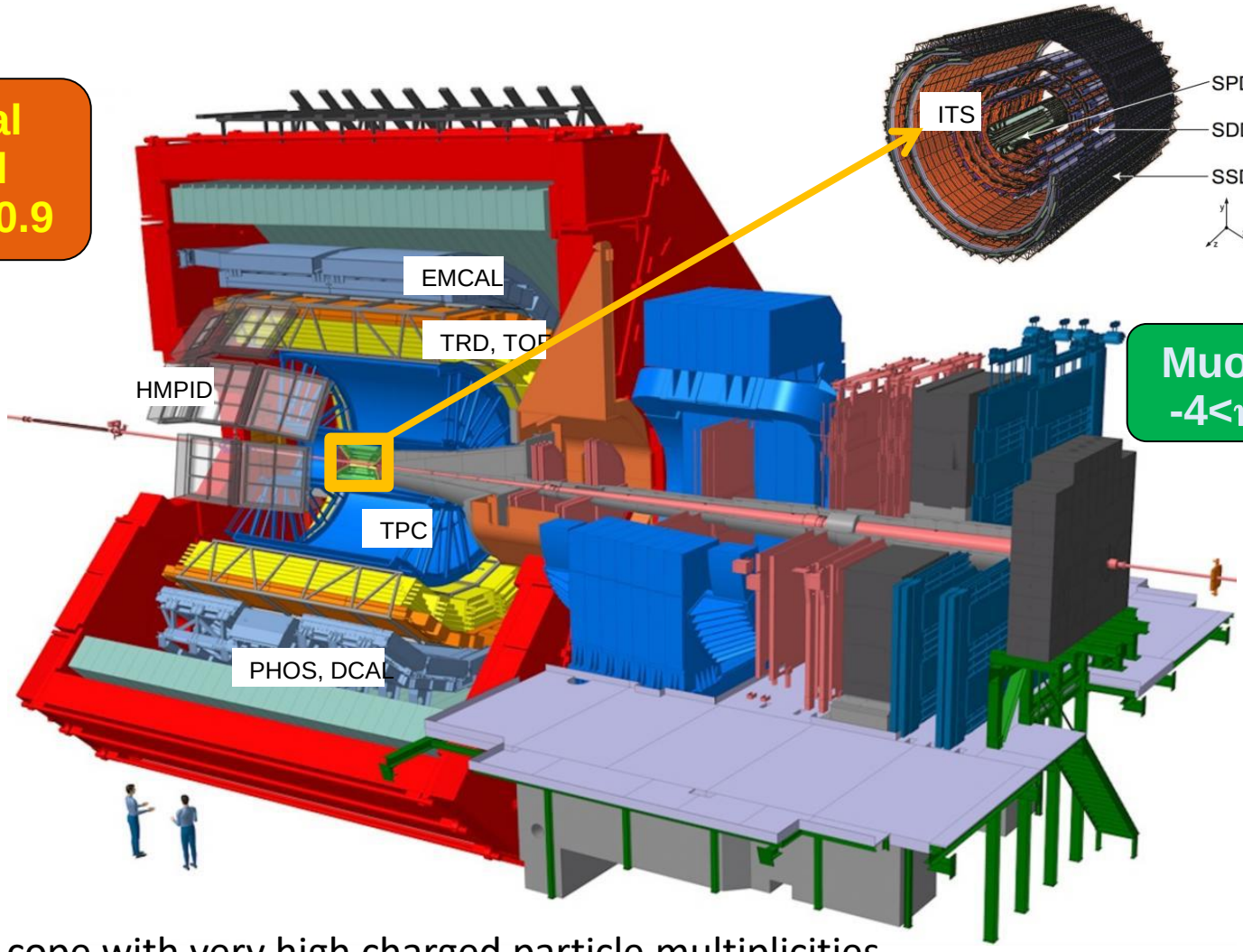
第五届中国LHC物理研讨会(CLHCP2019)，10月14-27日，大连

Outline

- Overview on ALICE detector upgrade programs
- Chinese involvement on ALICE detector upgrade for LS2
- (Possible) involvement on ALICE detector upgrade for LS3
- Summary and outlook

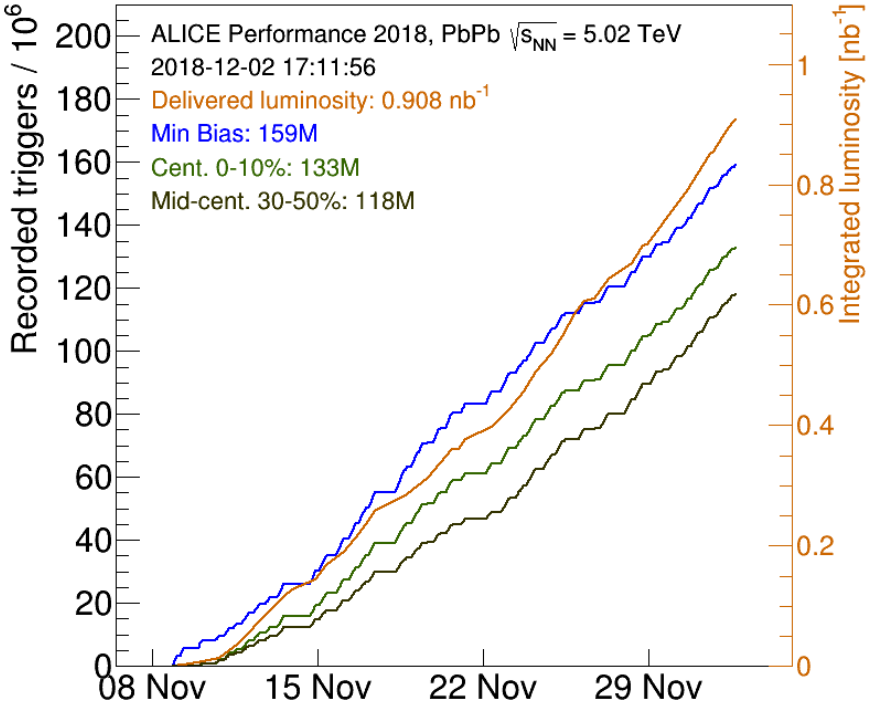
ALICE detector in RUN 1 and 2



- Designed to cope with very high charged particle multiplicities
- Excellent tracking and particle identification of charged particles over wide p_T range

ALICE running status

Colliding System	Year	$\sqrt{s_{NN}}$ (TeV)	Integrated Luminosity
Pb-Pb	2010,2011	2.76	~75 μb^{-1}
	2015	5.02	~250 μb^{-1}
	2018	5.02	~1 nb^{-1}
Xe-Xe	2017	5.44	~0.3 μb^{-1}
p-Pb	2013	5.02	~15 nb^{-1}
	2016	5.02 8.16	~25 nb^{-1} ~3 nb^{-1}
pp	2009-2013	0.9 2.76	~200 μb^{-1}, ~ 100 nb^{-1}
		7 8	~1.5 pb^{-1}, ~2.5 pb^{-1}
	2015,2017	5.02	~1.3 pb^{-1}
	2015-2018	13	~45 pb^{-1}



Pb-Pb 2018 run

– 0-10%: ~ 9 x 2015

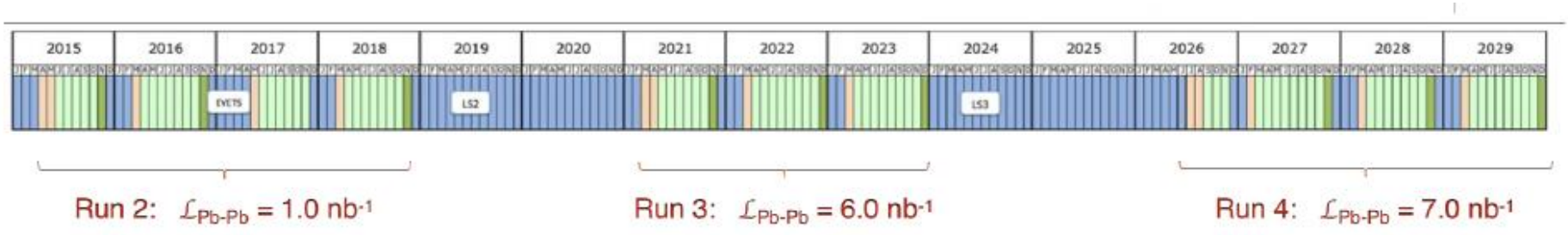
– 30-50%: ~ 4 x 2015

– Minimum Bias: ~ 2015

– delivered lumi. ~ 2 x 2015

Physics reach and limitations

- Measurements on a wide range of observables, from bulk particle production to specific probes, to characterize the de-confined hot and dense medium created in heavy-ion collisions at the LHC.
  - Up to now 244 papers published
- But some probes not fully exploited due to insufficient statistics or large combinatorial background.
  - Heavy flavor, quarkonium, jets, direct photons, dileptons,…

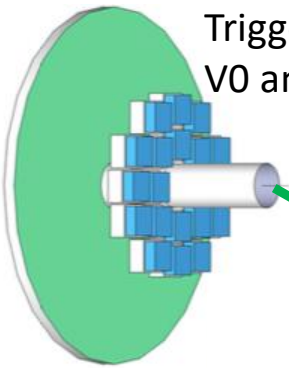


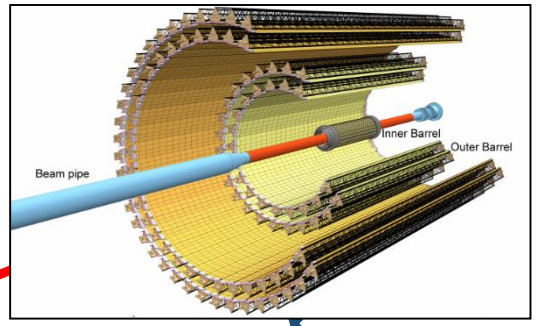
- **A major detector upgrade for the LS2 to fully exploit the higher interaction rate （50 kHz Pb-Pb collisions）.**
- **ITS3 and FoCal are proposed to upgrade the ALICE detector for LS3 to further enhance its physics capabilities.**

Major detector upgrade for LS2

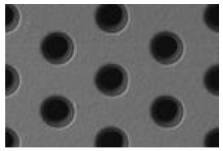
New Inner Tracking System (**ITS2**)

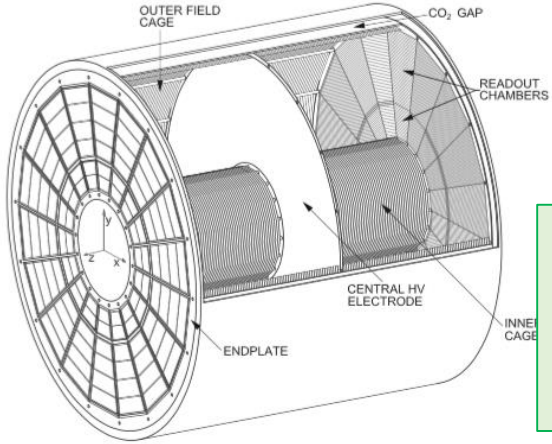
New Forward Interaction Trigger (**FIT**) to replace the V0 and T0 detectors

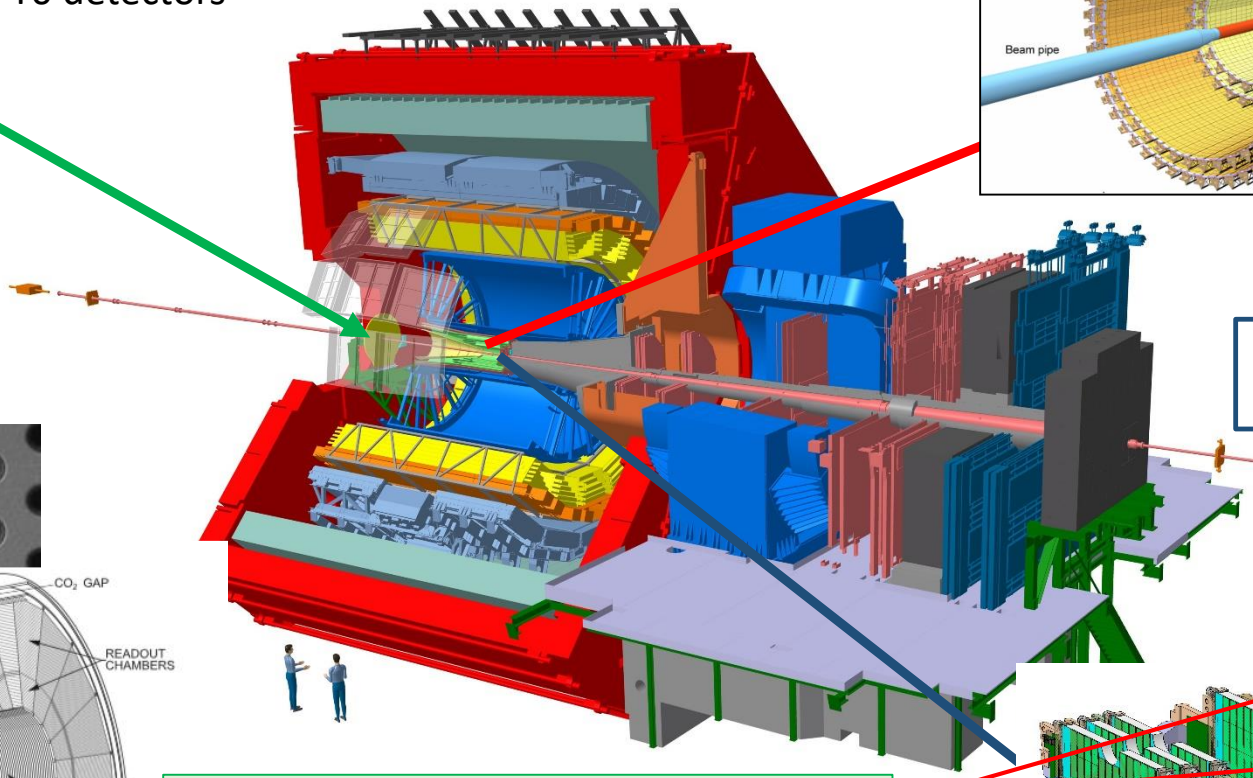




TPC with GEM based readout

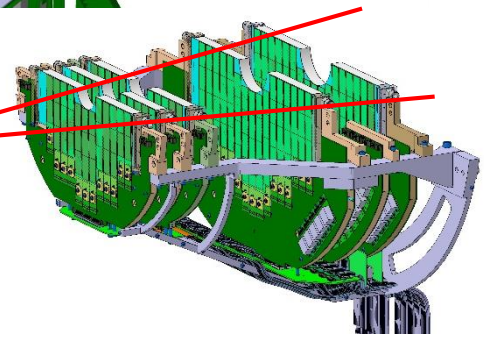






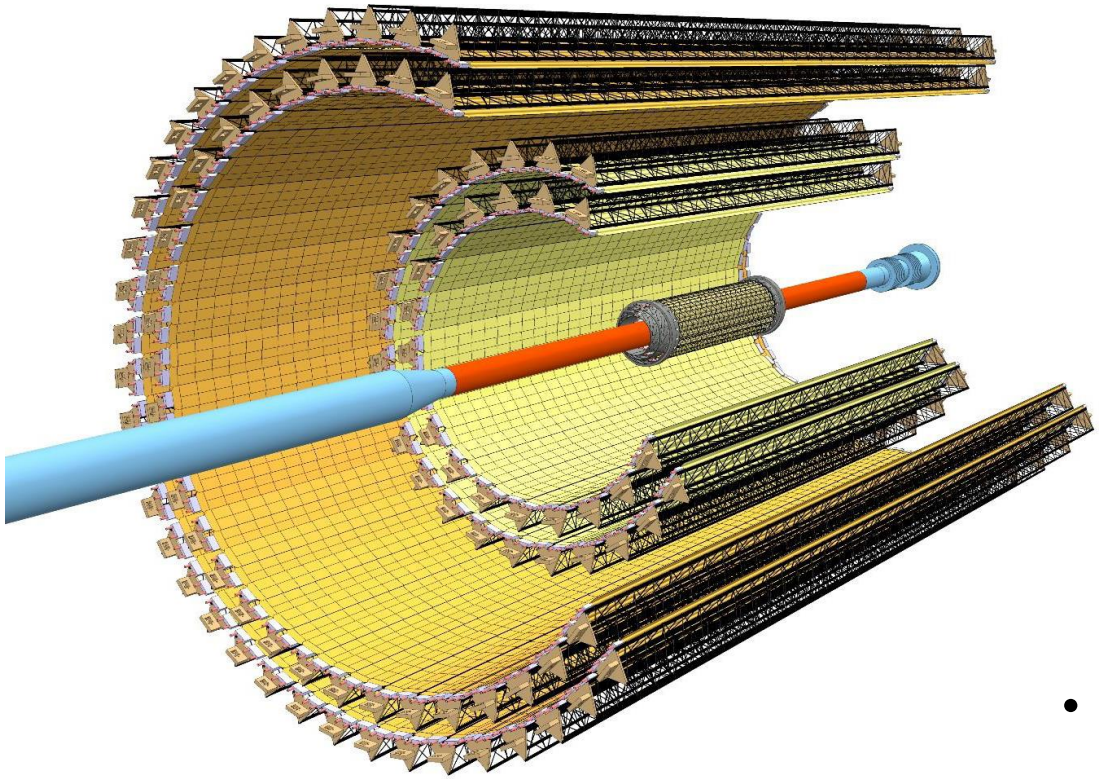
Both based on MAPS

MFT



+ improved readout for TOF, ZDC, TRD, MUON ARM
+ new Central Trigger Processor
+ new DAQ/Offline architecture

ITS upgrade for LS2 (ITS2)



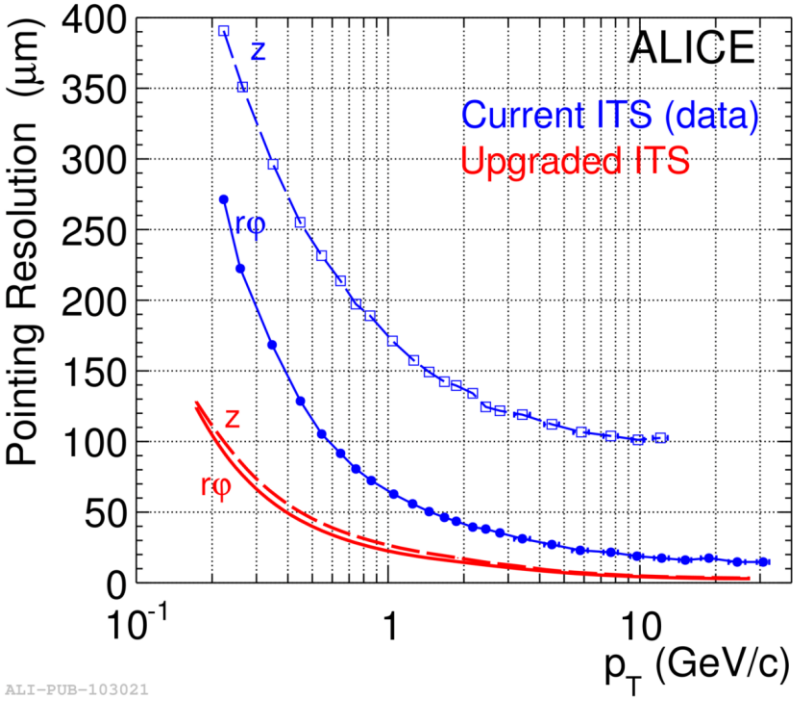
- 7-layer barrel fully equipped with dedicated Monolithic Active Pixel Sensors (**MAPS**): **ALice PIxel DEtector (ALPIDE)**
- Radial coverage: 23 – 400 mm
- η coverage: $|\eta| \leq 1.3$
- Total active area about 10 m^2
- 24,000 pixel chips (12.5G pixels)
- Spatial resolution: 5 μm

- Inner Barrel
  - 3 Inner Layers (48x 9-chip Staves)
  - Material per layer: **~0.35% X_0**

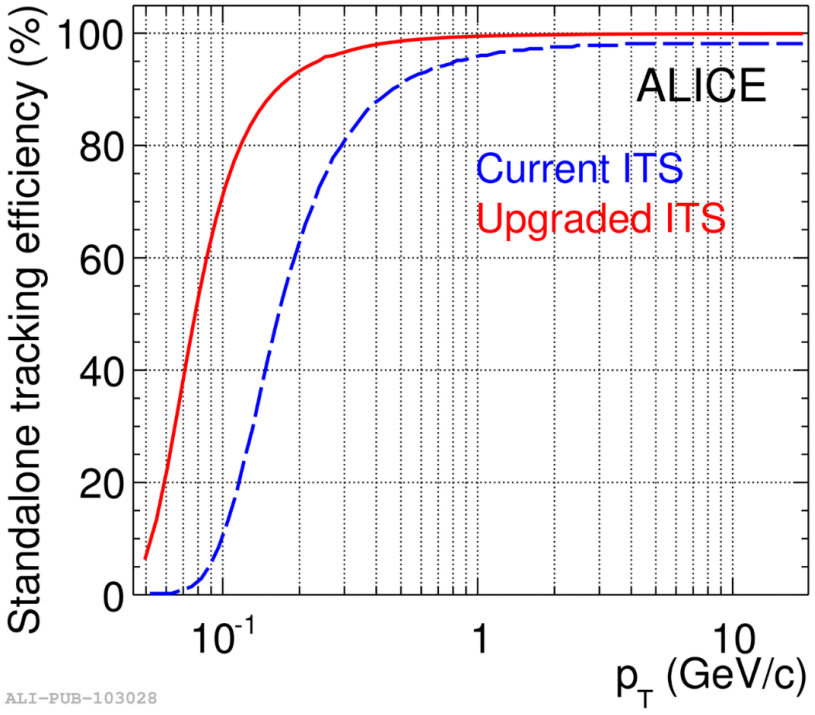
- Outer Barrel
  - 2 Middle Layers (54x 8-module Staves)
  - 2 Outer Layers (90x 14-module Staves)
  - Material/layer: ~ 0.8% X_0

Simulated detector performance

- Pointing resolution improved by a factor of 3 and 5 in rϕ and z direction for 0.5 GeV/*c* π



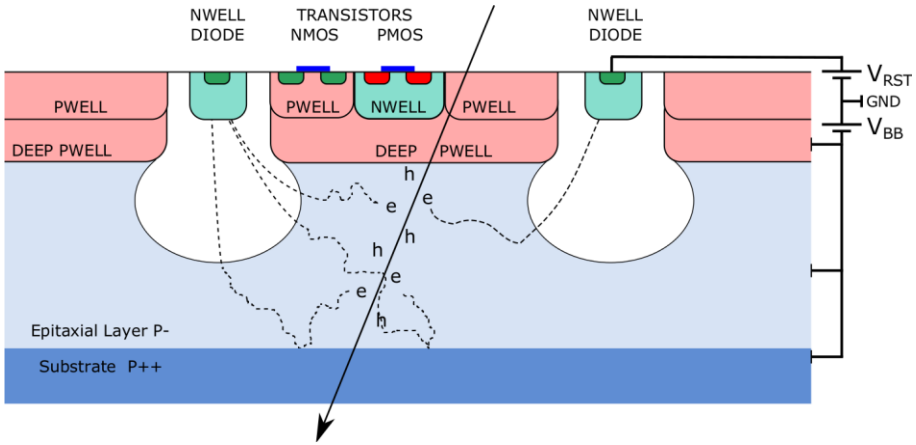
- Standalone tracking efficiency improved significantly at low p_T



- Physics goal: improve heavy-flavor physics studies through low momentum track reconstruction

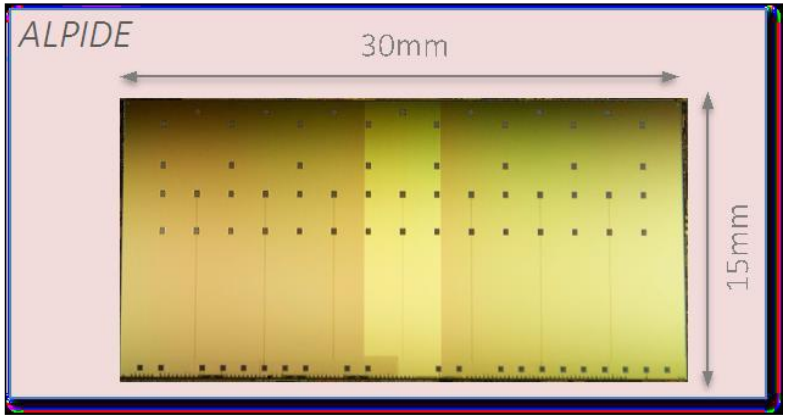
The ALPIDE sensor

Pixel Sensor produced using TowerJazz 0.18µm CMOS Imaging Process



Monolithic Active Sensor Technology

- Deep Pwell allows in-pixel full CMOS
- Low-power read-out
- High granularity, low material budget
- Resistivity (>1 kΩ·cm) p-type epitaxial layer (25 µm)
- Reverse bias to increase the depletion zone around NWELL collection diode

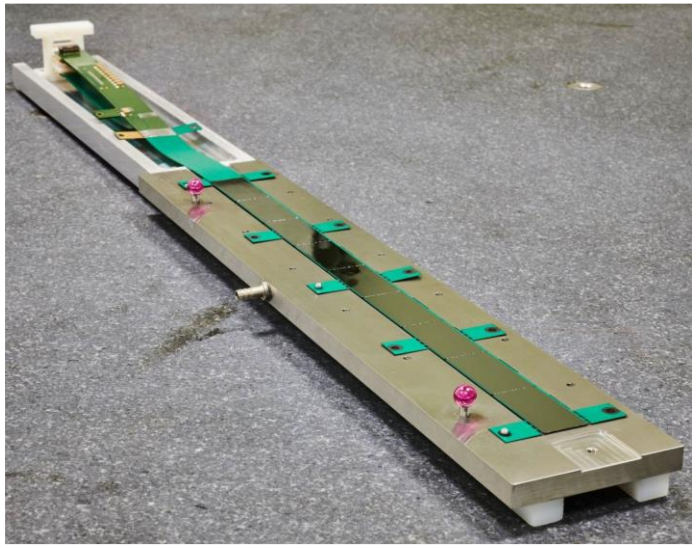


- Pixel Matrix: 1024 cols x 512 rows
- Pixel pitch: 29 µm x 27 µm
- Ultra-low power: ~40 mW/cm^2
- Integration time: < 10 µs
- Trigger rate: 100 kHz Pb-Pb, 1 MHz pp
- Continuous or triggered readout

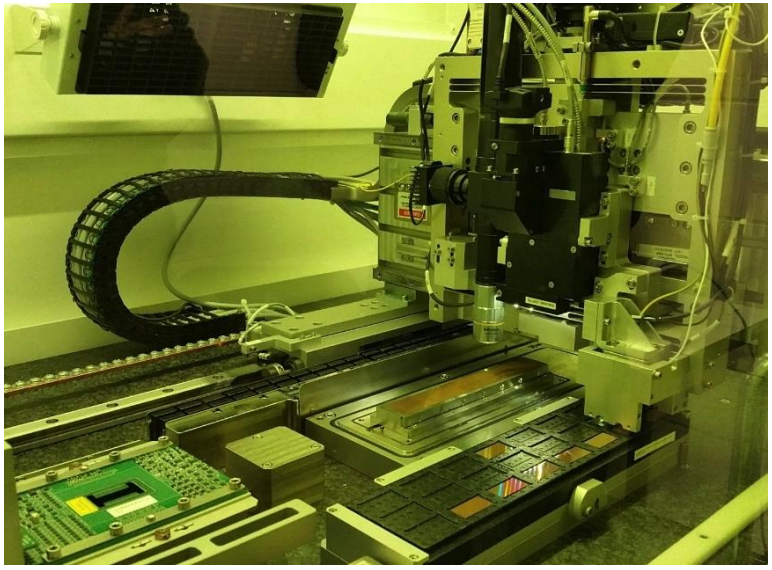
IB: 50 µm thick
OB: 100 µm thick

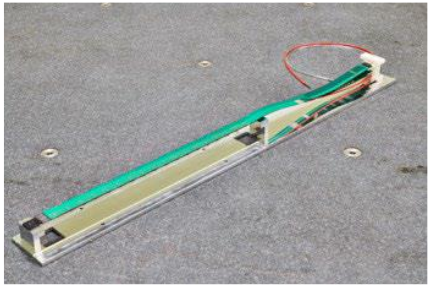
From chips to staves: IB

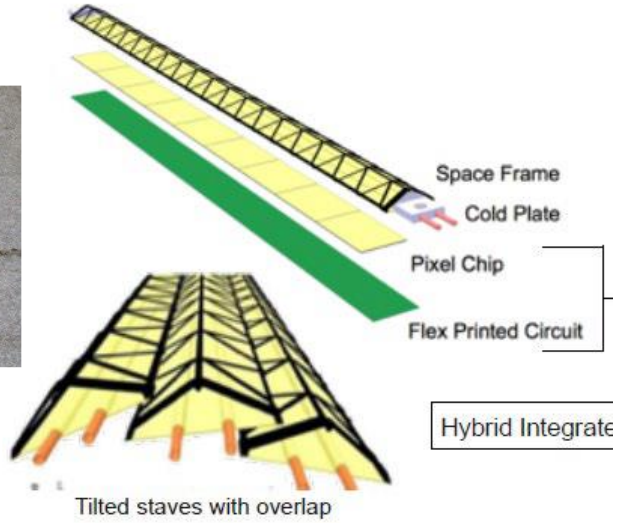
Inner Barrel HIC: 9x 50μm-thick ALPIDE chips wire-bonded to FPC



- Chips read out separately
- Clock, control, data, power lines wire-bonded to aluminum FPC
- Produced at CERN with 73% yield
- 27 cm length stave





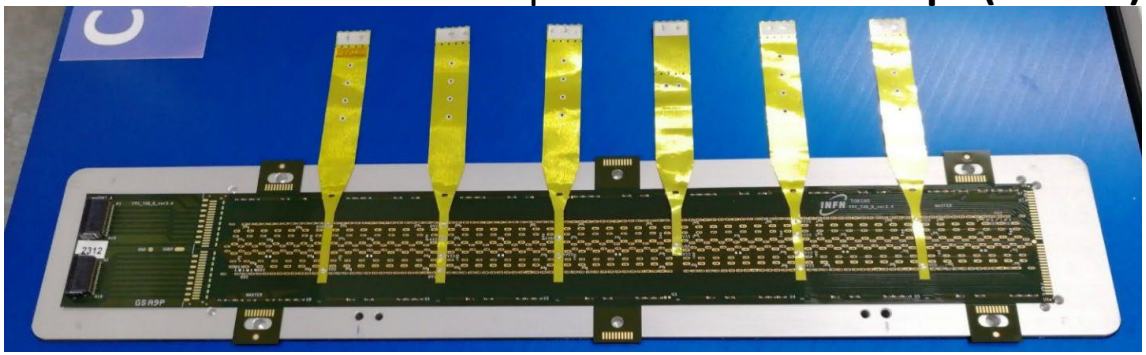


Tilted staves with overlap

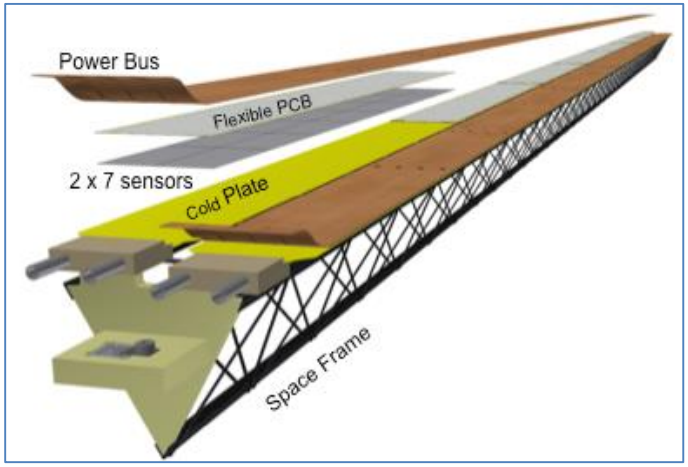
- <radius> (mm): 23, 31, 39
- Nr. staves: 12, 16, 20
- Nr. chips: 432
- Readout speed: 1.2 Gbps

From chips to staves: OB

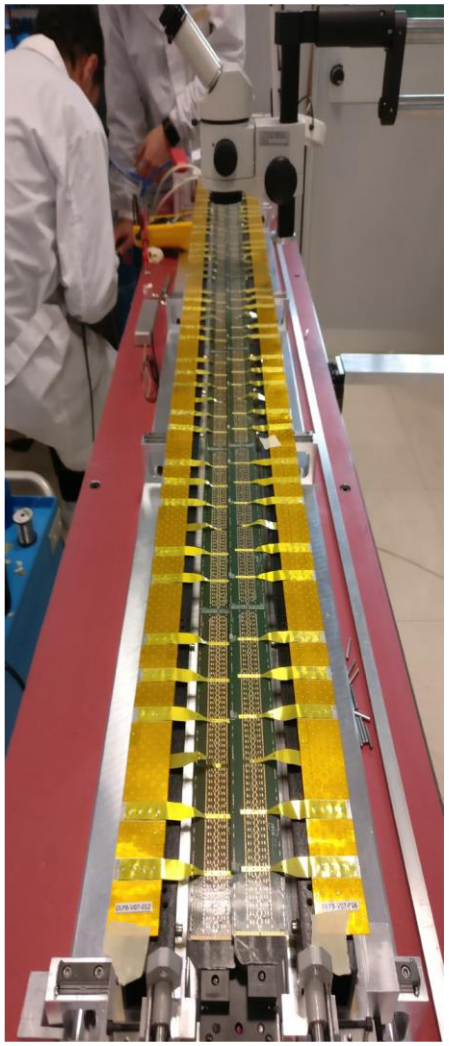
Outer Barrel HIC: 14x 100μm-thick ALPIDE chips (2 rows)



- Data and control transferred through 1 master chip per row
- Chips wire-bonded to copper FPC
- Power delivered via 6 cross-cables soldered to FPC
- Produced at Bari, Liverpool, Pusan/Inha, Strasbourg and **Wuhan**



- HIC alignment on cold plate
- HIC-to-HIC (4 for ML and 7 for OL) interconnection soldering
- Two half staves on space frame
- Power bus installation
- Readout speed for OB: 400 MB/s



Construction installation and commissioning timeline

Dec '17

Detector Construction and Assembly

- HIC production: completed
- Stave production: 90% done
  continues until November 2019 for spare staves
- Electronics production and testing: done

May '19

Jun '19

Aug '19

Sep '19

Commissioning at the surface with final services ongoing (operation 24/7)

Oct '19

Outer-Barrel Layer Assembly: >75% done

June '20

Installation

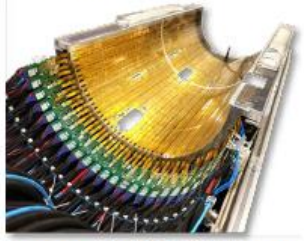
6-month Global Commissioning

Feb '21

Stave

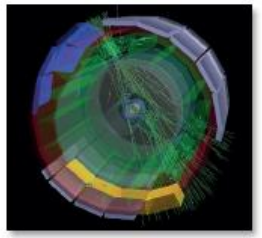
Readout Unit

Inner-Barrel Assembly



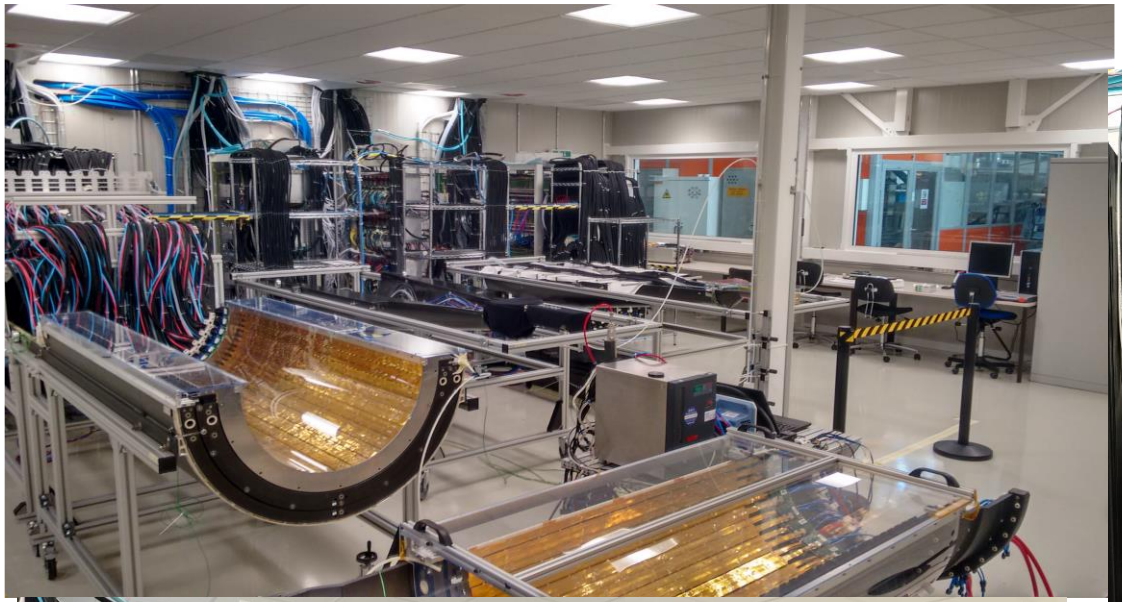
Outer-Barrel Assembly

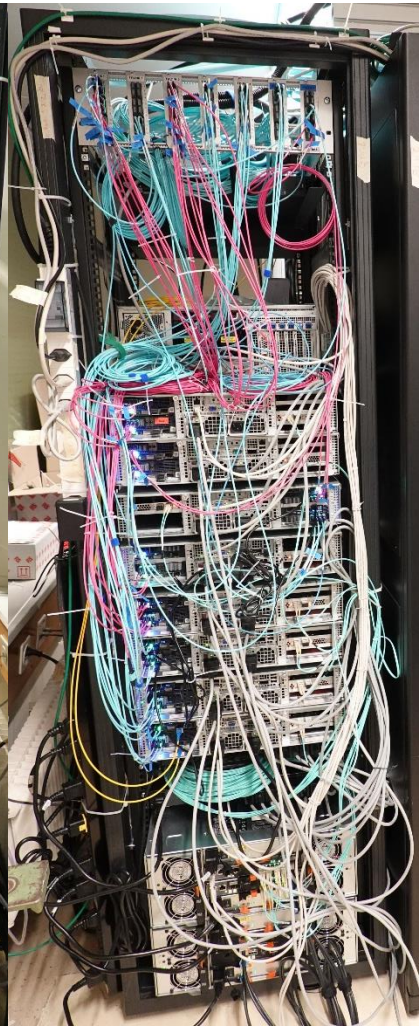
Installation



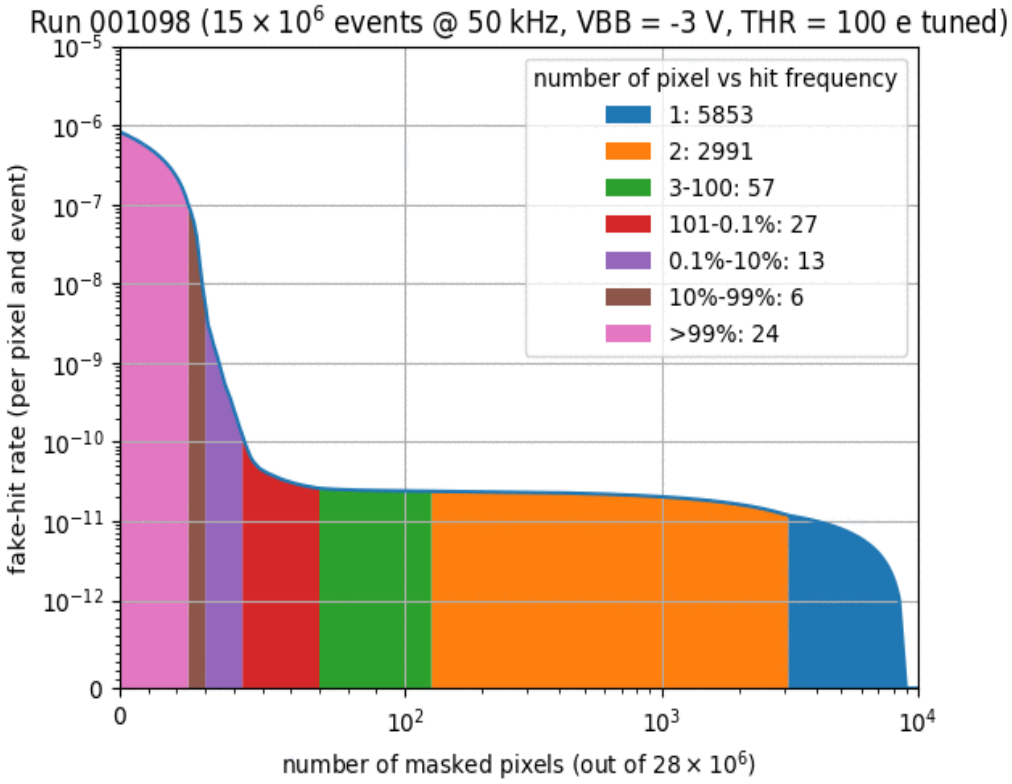
Global commissioning

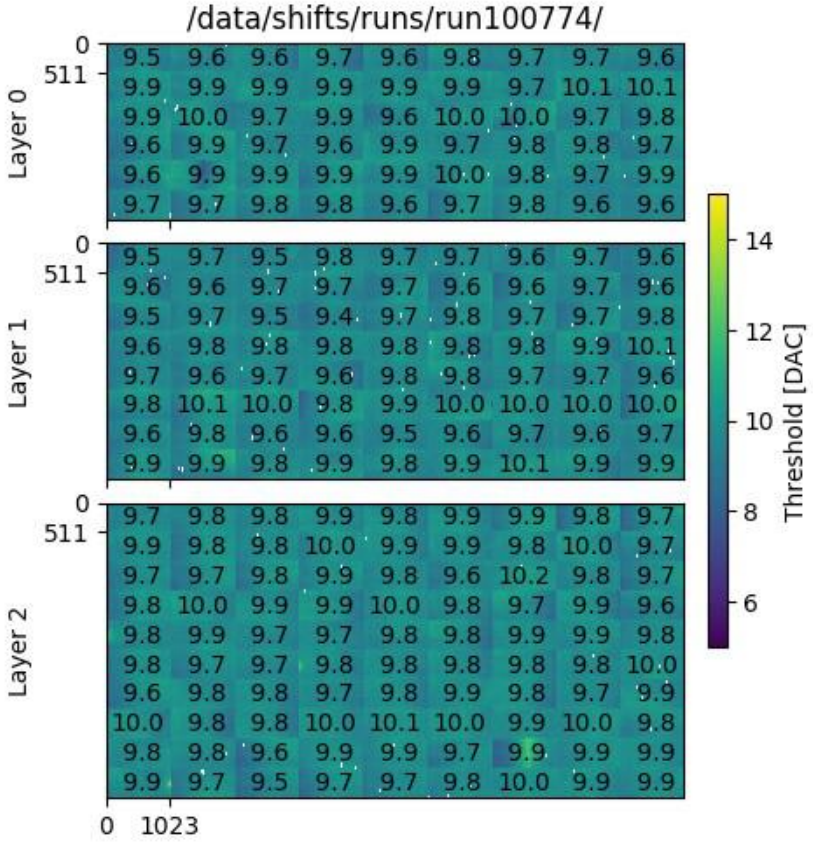
Commissioning on surface





Example results from commissioning



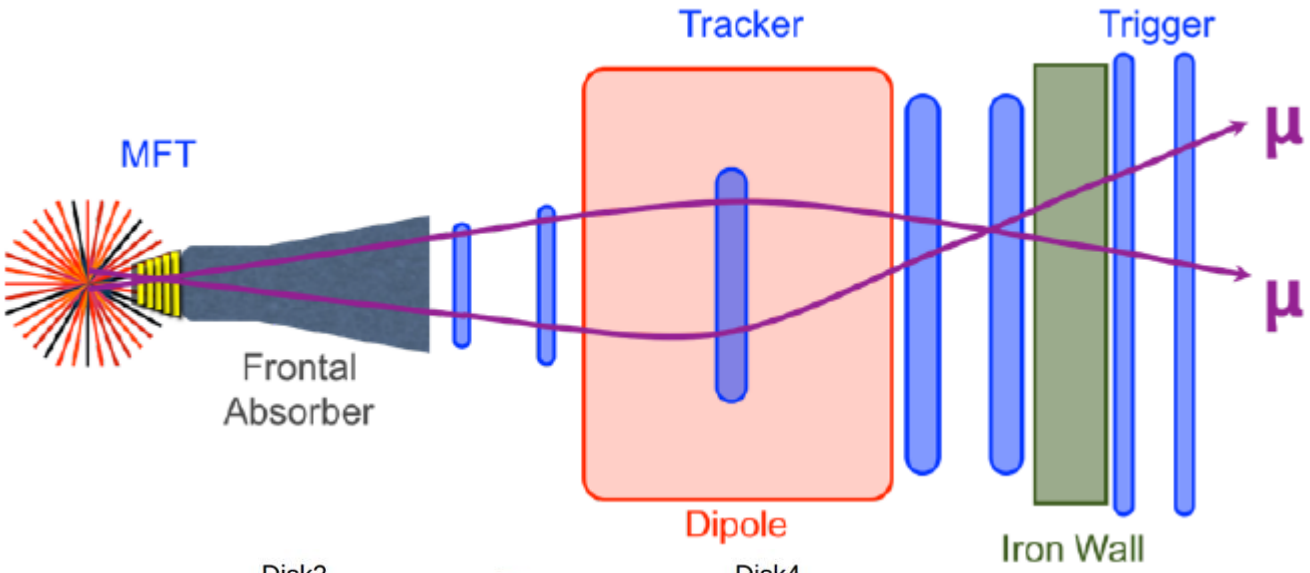


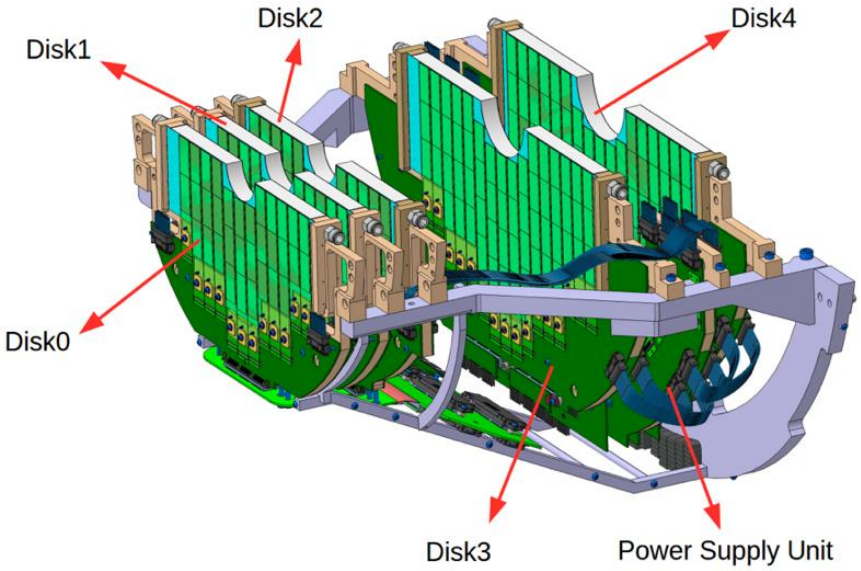
216 chips,
~ 113M pixels

- Very quiet detector
- Fake-hit rate stable over time

- Threshold tuning effective
- Very good uniformity
- Less than 1000 dead pixels

Muon Forward Tracker (MFT)

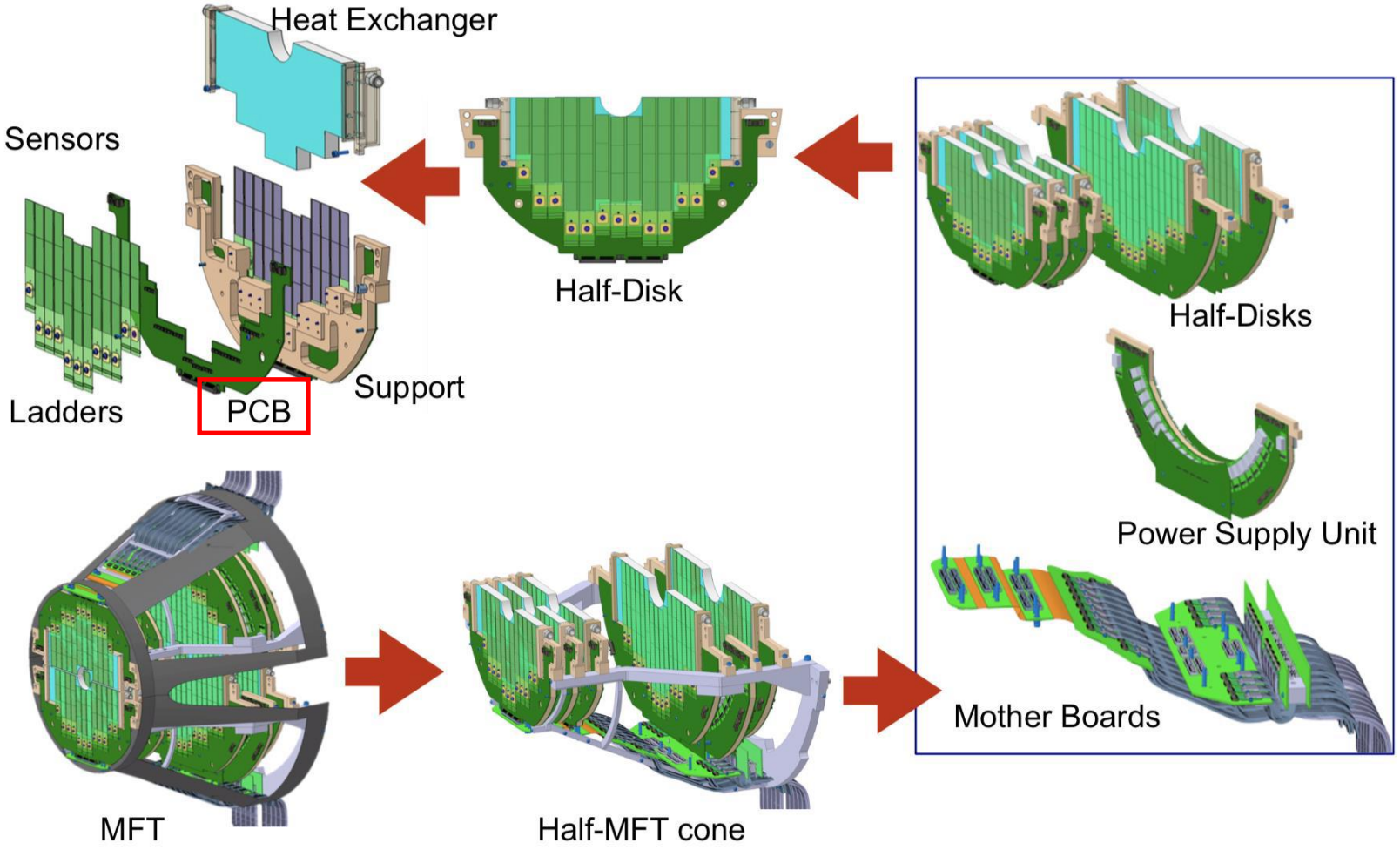




- **Based on same MAPS as ITS upgrade**
- 2212 chips in total
- 5 disks with 2 planes on each disk
- Enables better matching to vertex

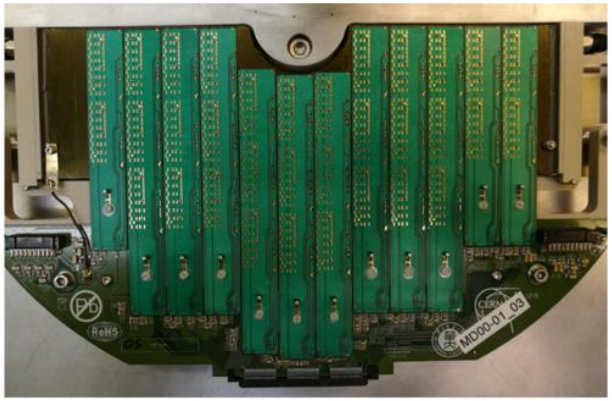
- **Charm/beauty separation possible**
- **Improved mass resolution**

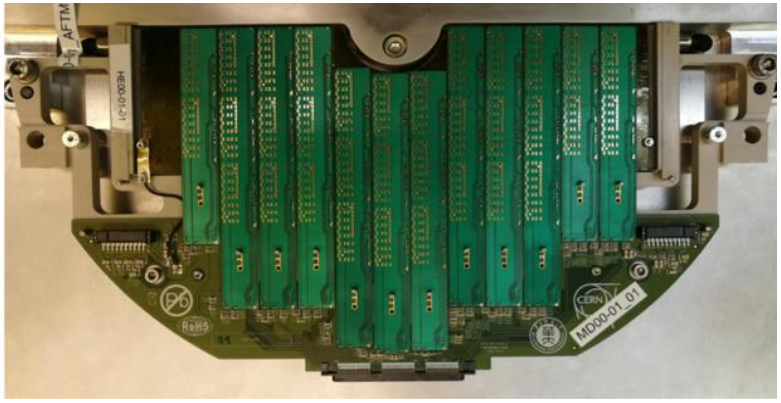
Breakdown of MFT structure



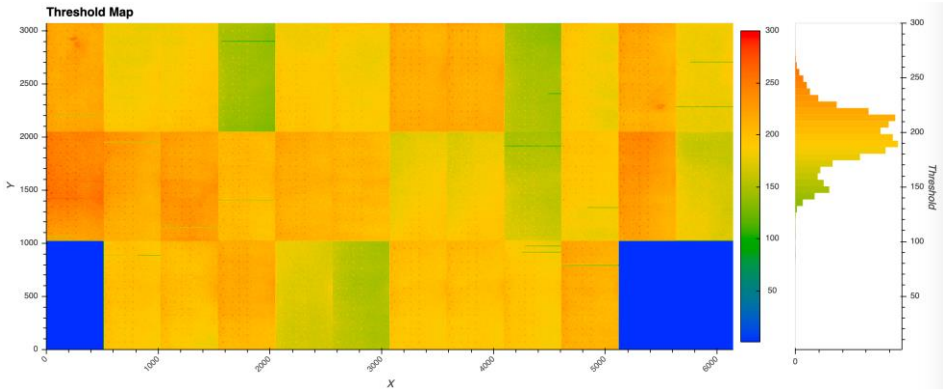
- **CCNU takes charge of PCB design, layout and production**.
- Status: **Completed**

Disk production & Commissioning

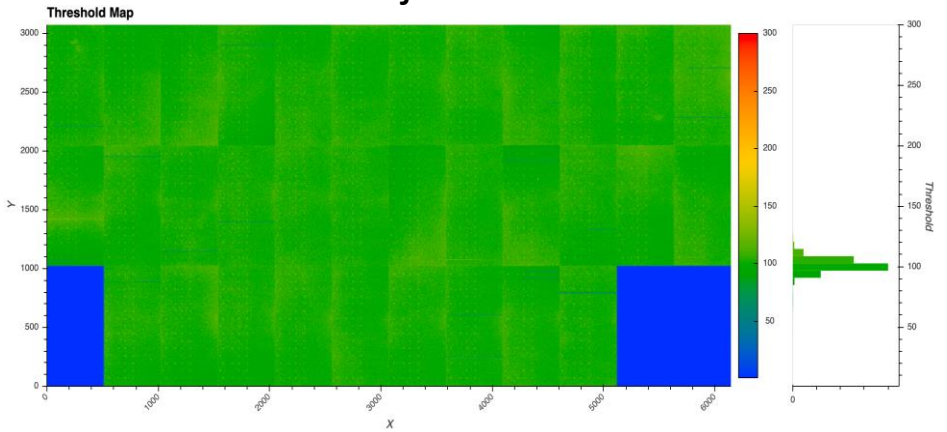




Before threshold adjustment



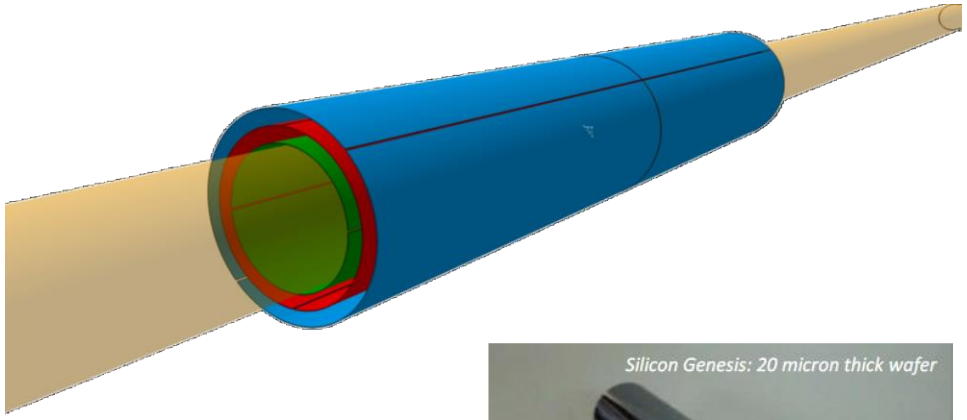
After threshold adjustment

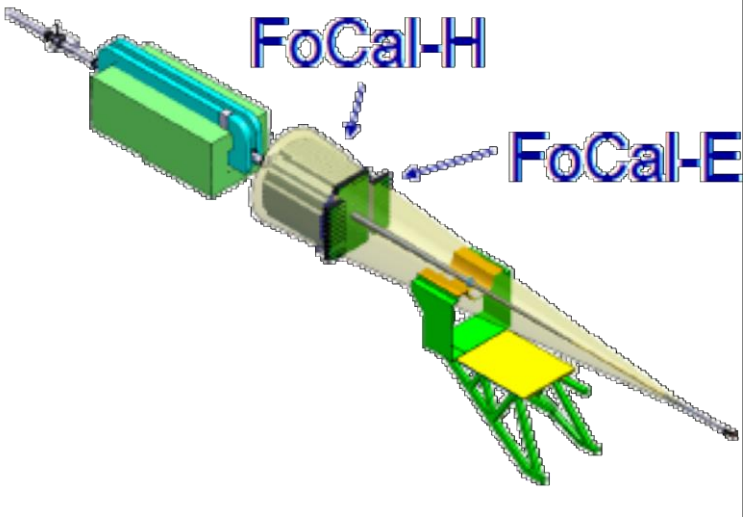


- 2 disks of type 00/01 + 1 disk 02 produced

Possible involvement on ALICE detector upgrade for LS3

- **Proposed upgrade in LS3**

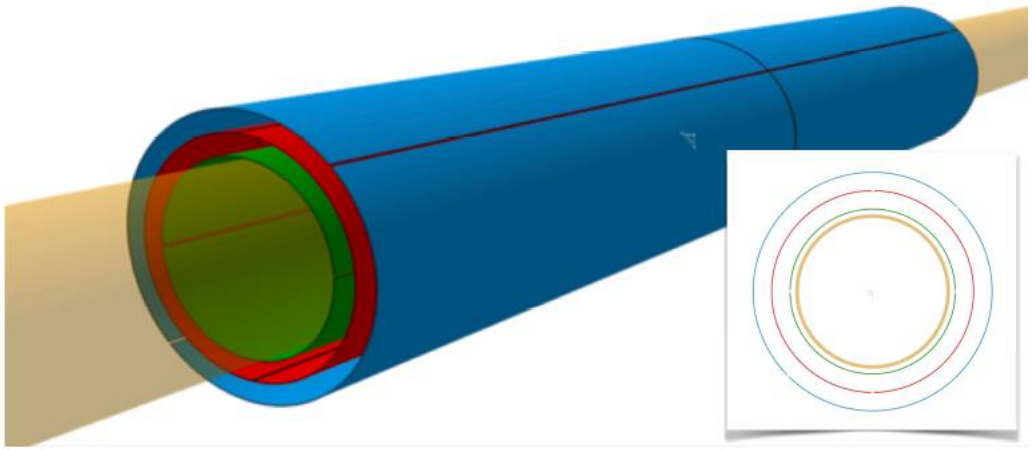




- **ITS3**: Replace the 3 inner layers with three truly cylindrical layers based on **curved** ultra-thin sensors
- Resolution improved further by factor of 2

- Add a forward calorimeter (**FoCal**)

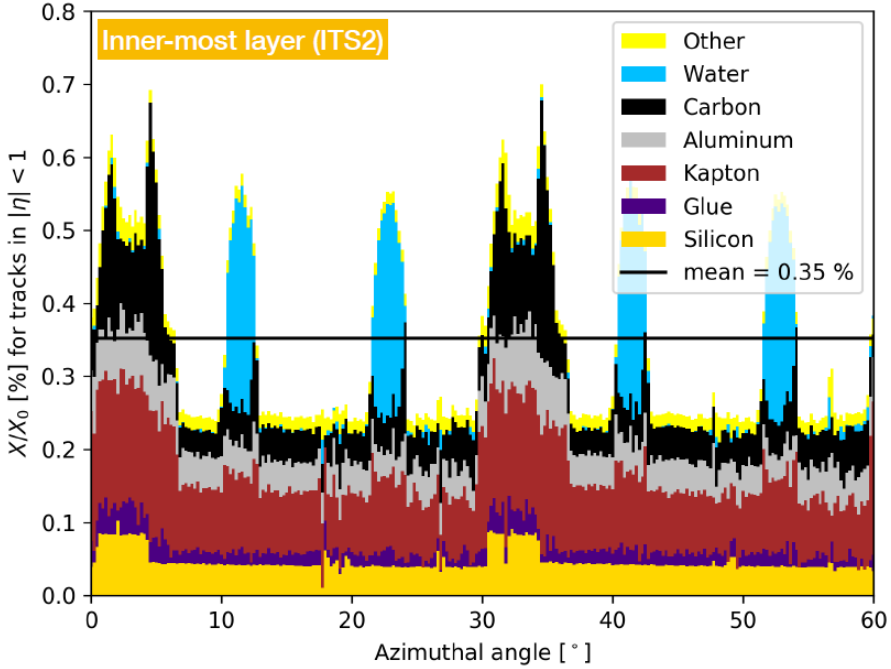
ITS3 layout



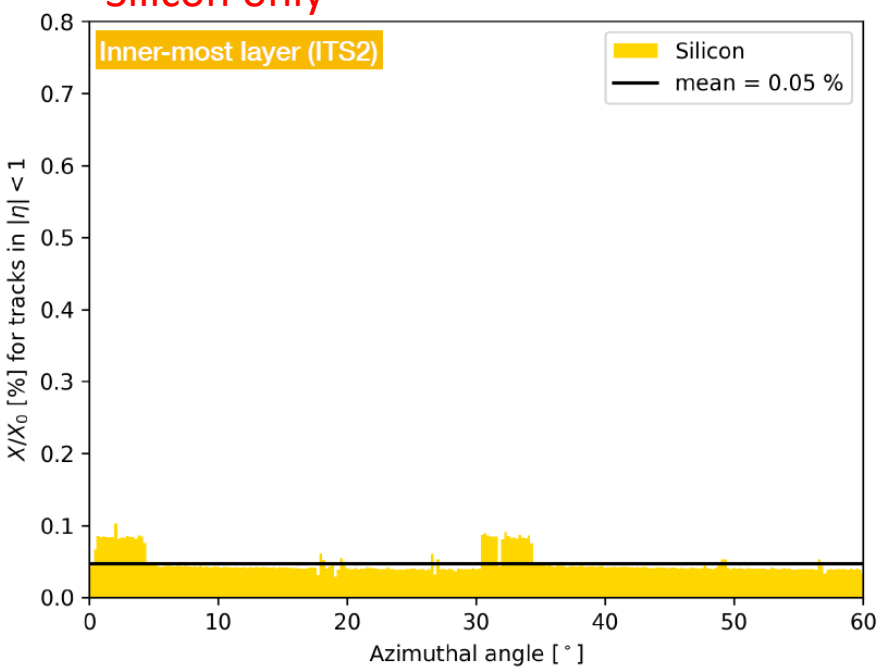
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- New beam pipe:
  - "old" radius/thickness: 18.2/0.8 mm
  - new radius/thickness: 16.0/0.5 mm
- Extremely low material budget:
  - Beam pipe thickness: 500 µm (0.14% X0)
  - Sensor thickness: 20-40 µm (0.02-0.04% X0)
- Material homogeneously distributed:
  - essentially zero systematic error from material distribution

Material budget



Silicon only



- Observations:

– Silicon makes only about **15%** of total material

– I**rregularities** due to support/cooling and overlap

- Removal of water cooling

– **possible** if power consumption stays below 20 mW/cm^2

- Removal circuit board (power+data)

– **possible** if integrated on chip

- Removal of mechanical support

– **benefit** from increased stiffness by rolling Si wafers

Implementation

- **Air cooling**

– Possible below 20 mW/cm^2
– Studied in the context of ITS2
– Achievable *if* periphery outside the fiducial volume

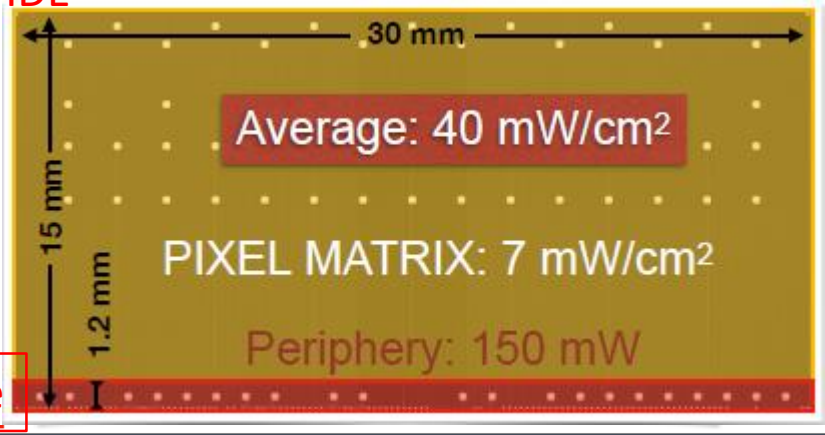
- **Wafer-scale chip**

– Stitching to overcome reticle size limit
– Chip spanning half or full stave length
– Neither support structure nor electrical substrate necessary

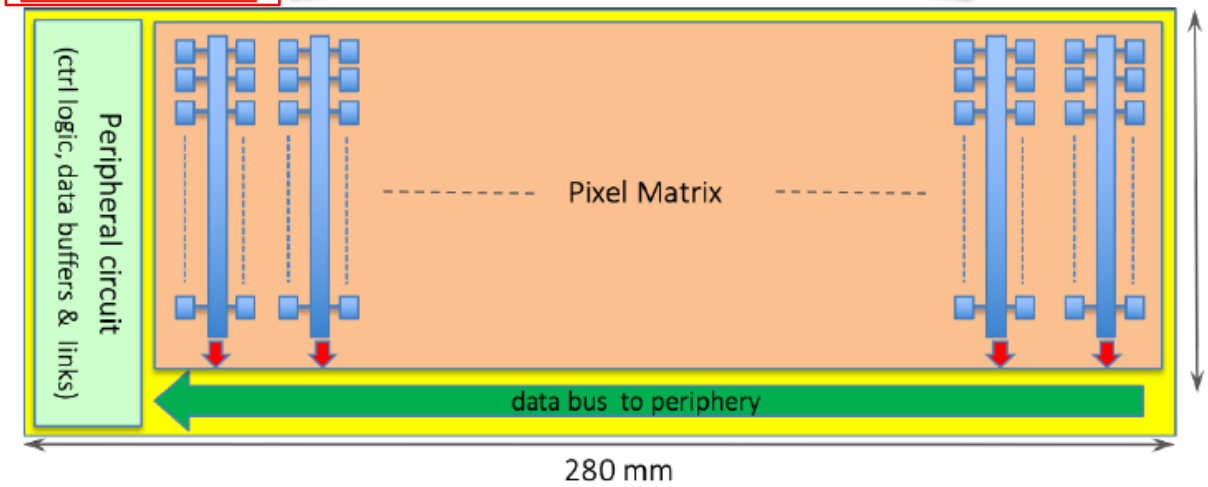
- **Thinning and bending**

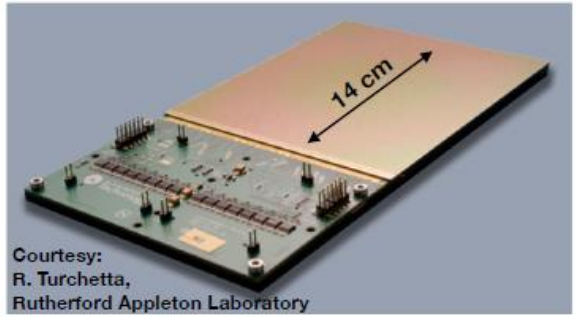
– Currently 50 µm (25 µm active volume)
– Below 50 µm, Si wafers become flexible, “paper-like”

ALPICE

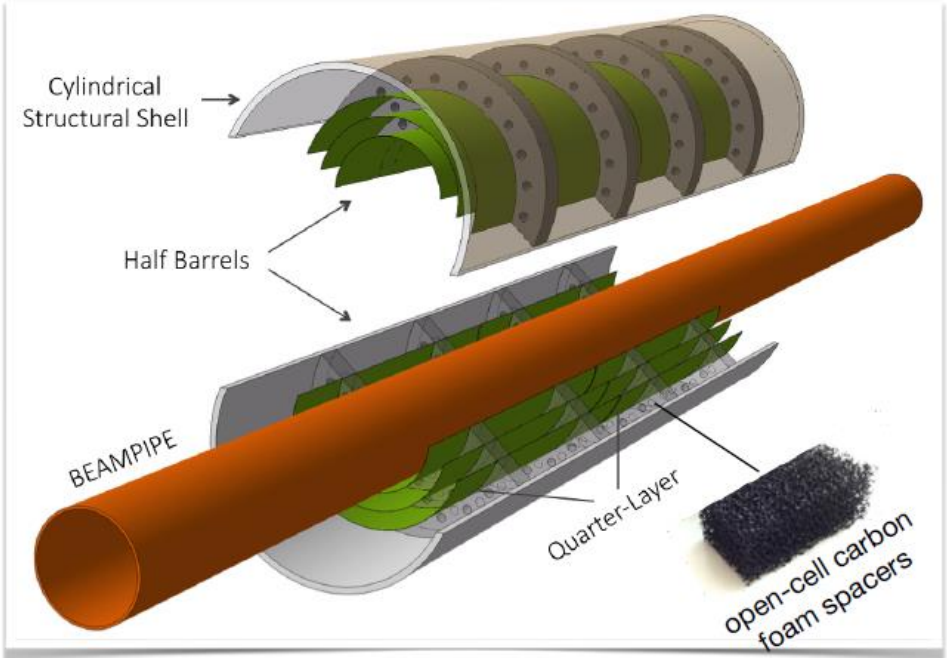


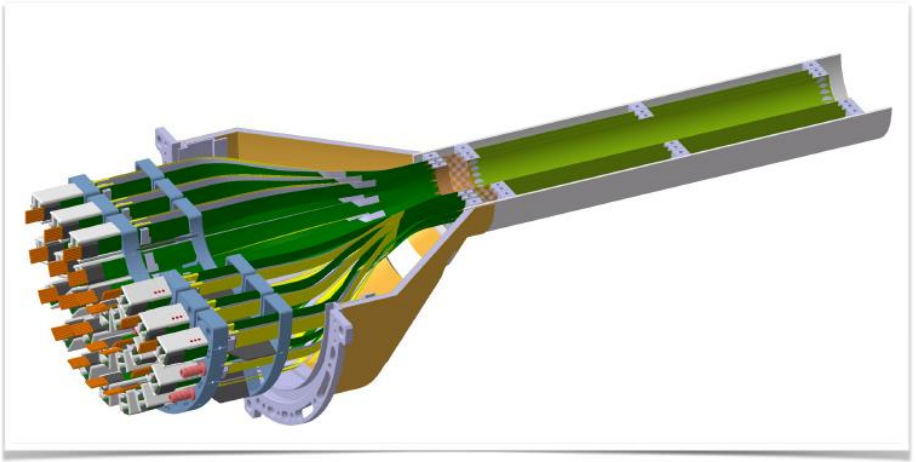
Wafer-Scale





Mechanics layout

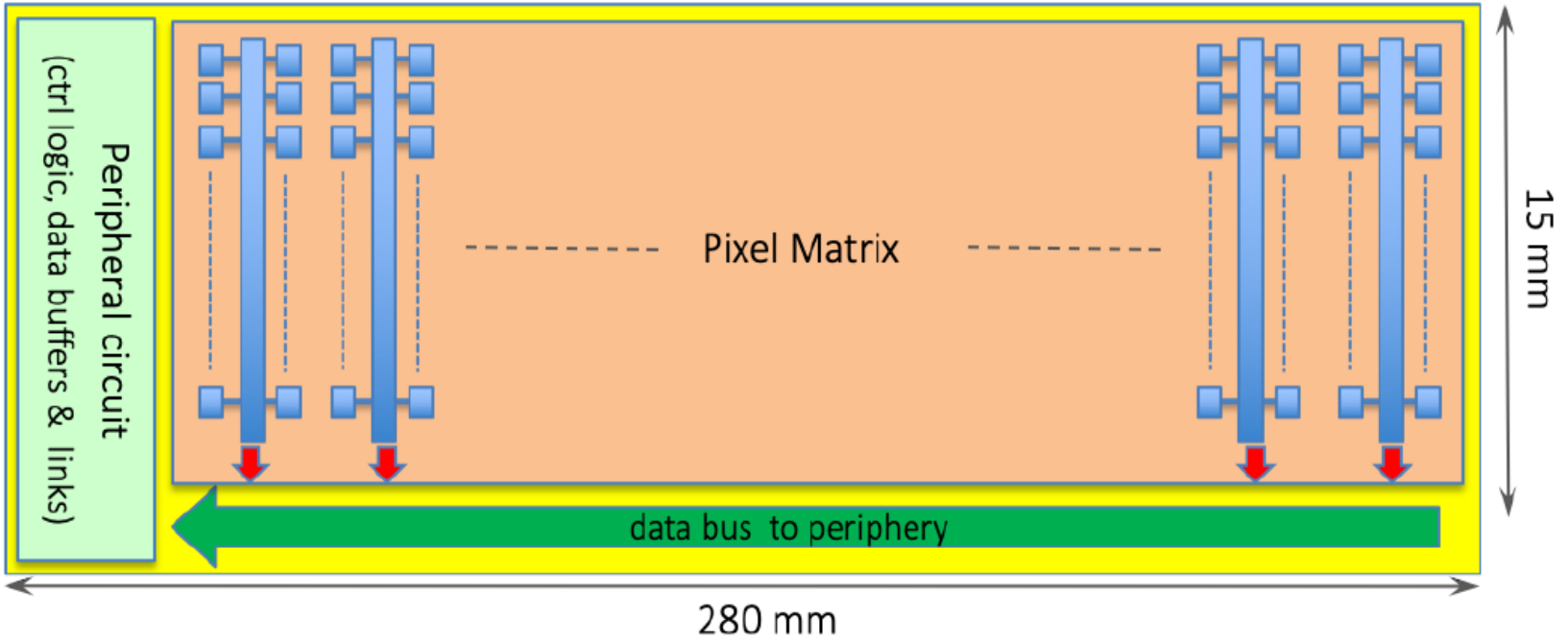




- Possible layout based on air-cooling
- Sensors hold in place with low-density carbon foam

- Fixation into the experiment by surrounding support structure, as well as at both ends
- Cooling at the extremities (chip peripheries)

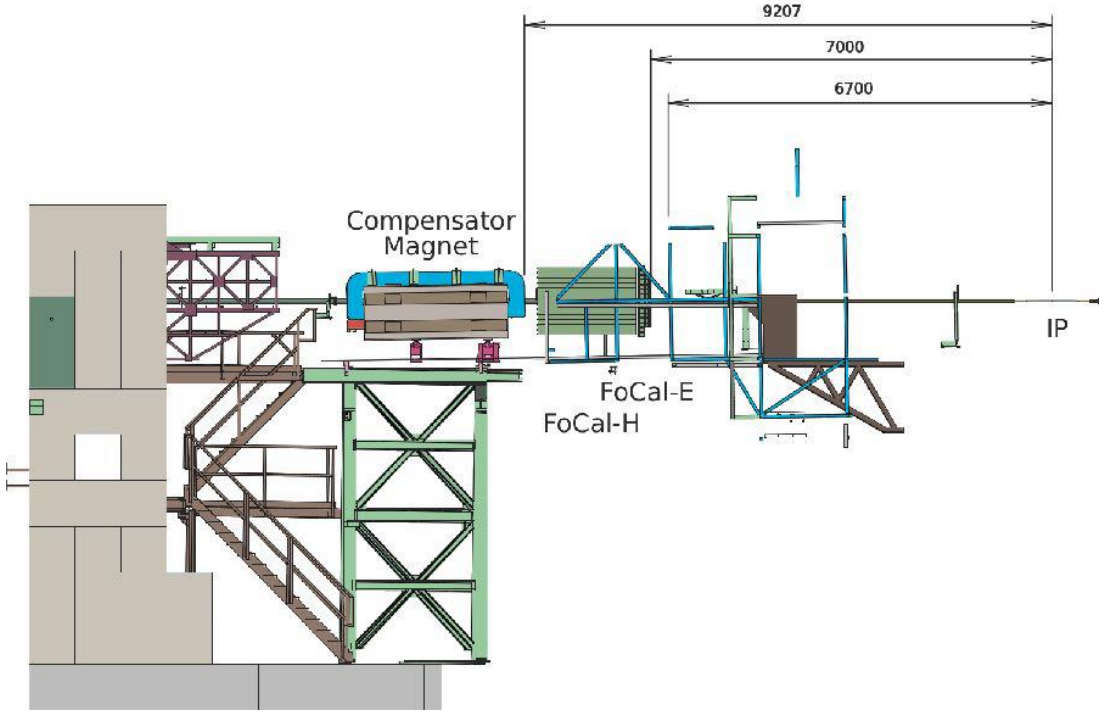
Wafer-scale sensor R&D

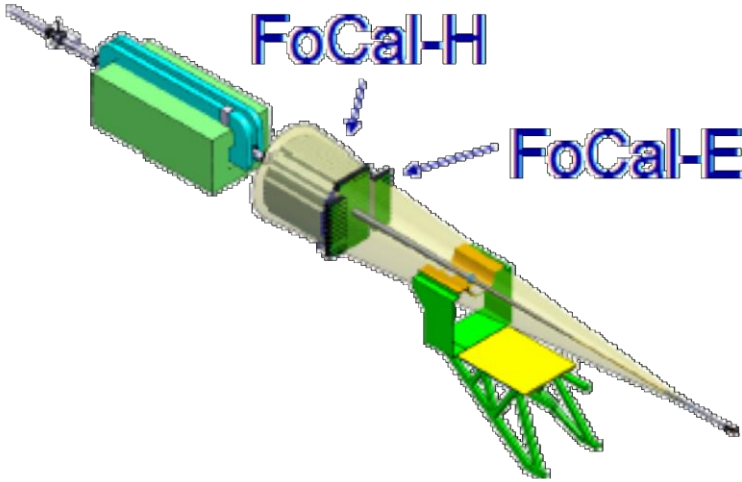


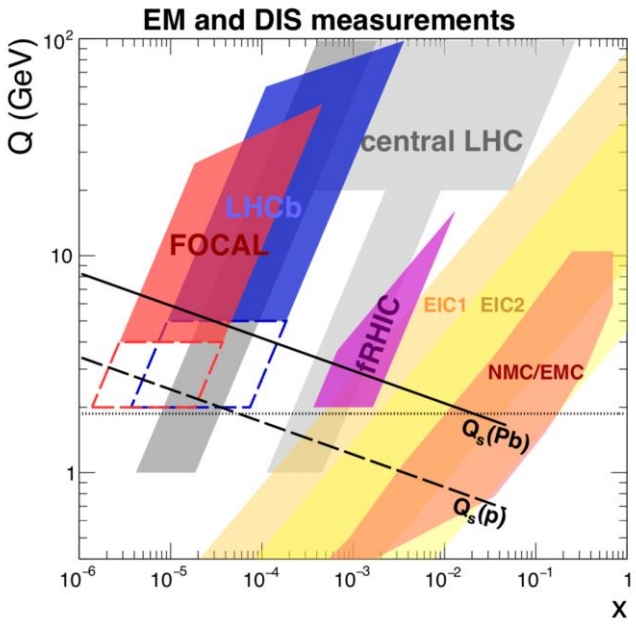
- Starting from ALPIDE architecture
- Porting to 65 nm technology node
  - smaller pixels
  - larger wafers (300 mm instead of 200 mm)
- Basic building block of 15 mm height
  - to be repeated n times in vertical direction to obtain the sizes needed per layer

R&D starts now; TDR is foreseen for 2020.

FoCal for LS3



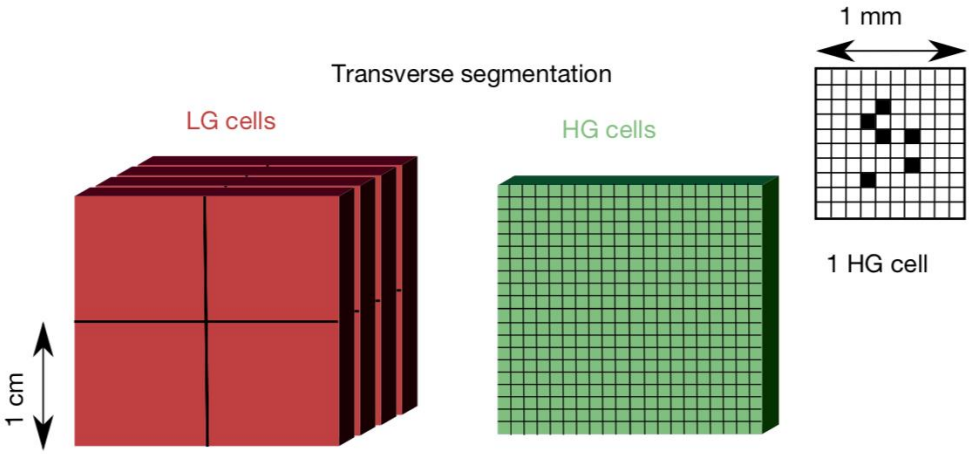


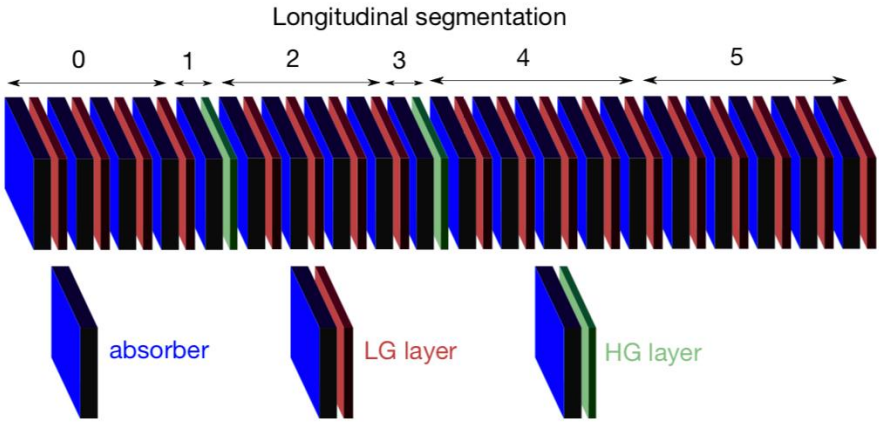


- 7 m away from the nominal IP
- Pseudo-rapidity coverage of 3.2 - 5.8
- To explore small *x* physics

FoCal-E design

high granularity electromagnetic calorimeter for γ and π^0 measurements

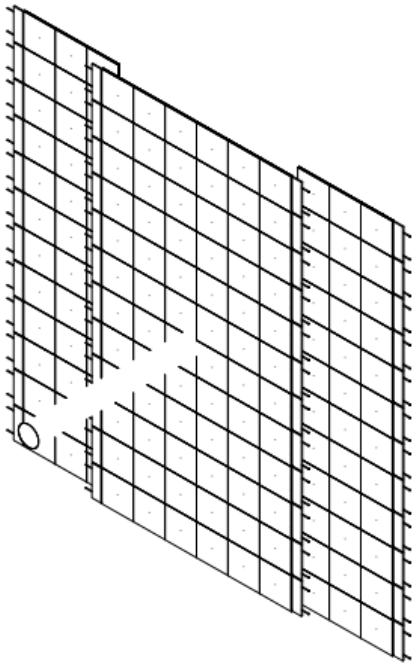




- **Studied in simulations 20 layers: W(3.5 mm ≈ 1X0) + silicon sensors**
- **Two types: Pads (LG) and Pixels (HG)**
  - **Pad layers provide shower profile**
  - **Pixel layers provide position resolution to resolve shower overlaps**

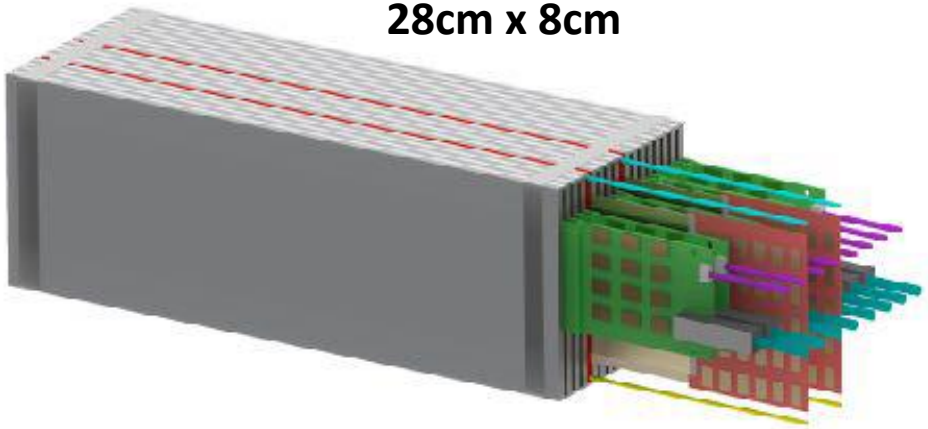
- Main challenge: Separate γ/π^0 at high energy
  - Two photon separation from π^0 decay (p_T = 10 GeV/c, η=4.5) ~2 mm
  - Needs small Molière radius and high granularity readout
  - Si-W calorimeter with effective granularity ≈ 1mm^2

FoCal-E detector Integration



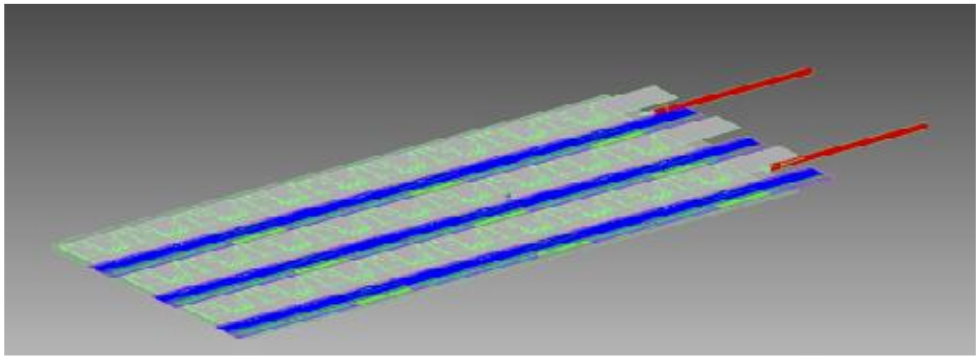
Design of detector module

28cm x 8cm



- module of ≈ 18 pad layer and 2 pixel layers
- sensitive area: 27cm x 8cm
- use edge of detector for services
- designed to be stacked vertically for full detector setup

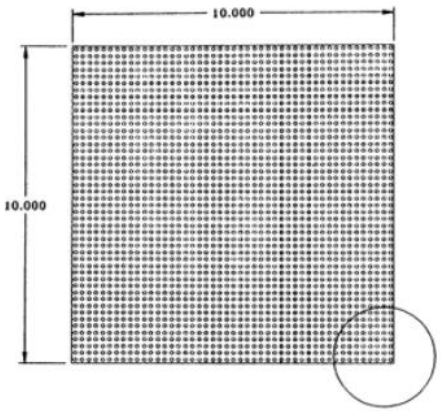
Design of single pixel layer

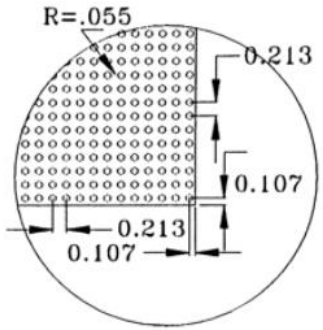


- single metal layer with cooling pipes
- full area coverage with 2 x 3 chains of 9 sensors

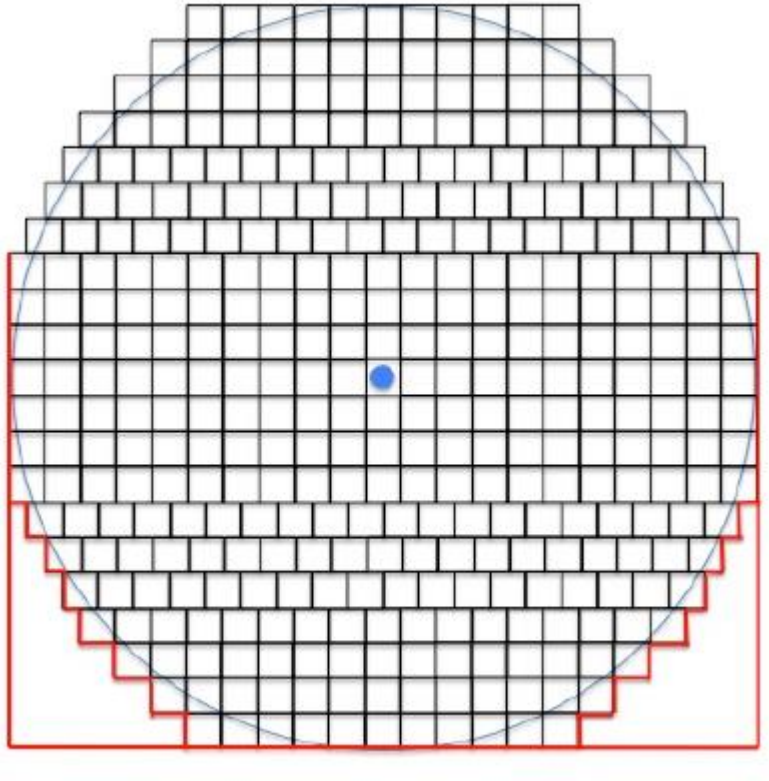
FoCal-H design

Allows to isolate photons in FoCal-E and jet measurements





- Pb/scintillating fiber spaghetti calorimeter module as used in E864
- a lead to fiber ratio of 4.55 : 1 by volume to provide good calorimetric compensation and resolution
- a mass of about 100 kg and an active depth of approximately 8 λ_{had}
- Cu as the passive material is also under consideration to reduce the length and weight



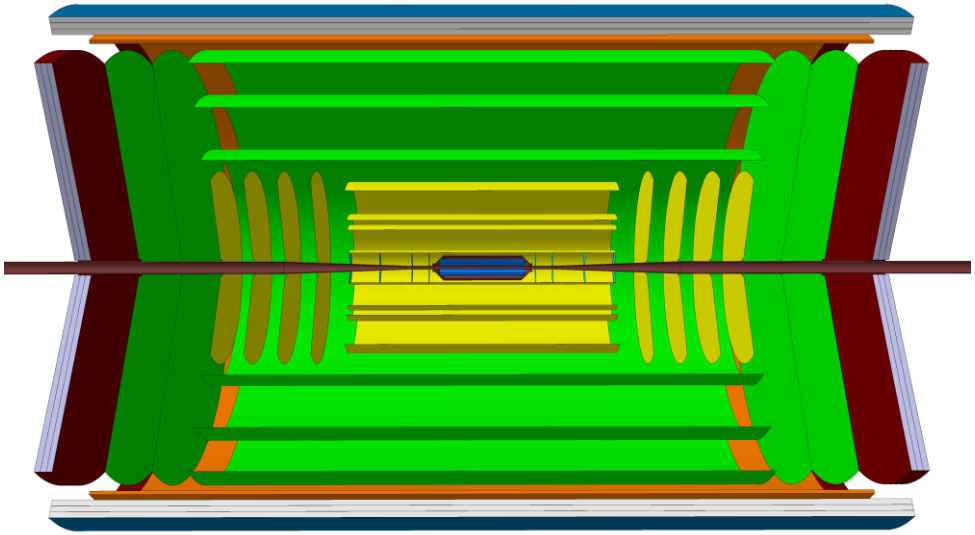
- A nearly circular geometry approximately 1 m in radius
- 372 modules
- 1488 towers of 5cm x 5 cm

FoCal timeline

Year	Activity
2016–2021	**R&D**
2019	Letter of Intent
2020–2021	final design
	Technical Design Report
2022–2026	**Construction and Installation**
2022 - 2024	production, construction and test of detector modules
2024	pre-assembly
	calibration with test beam
2025	installation and commissioning
06/2026	Start of Run 4

Summary and outlook

- **Major upgrade of ALICE detector for LS2 is ongoing.**
  - China involved in ITS2 and MFT
  - OB HIC production completed
  - Commissioning of ITS2 is ongoing
  - MFT PCB production completed
- **ITS3 and FoCal proposed for ALICE detector upgrade during LS3**
  - China involved in R&D of wafer-scale sensor for ITS3
  - Possible contributions (either pixel sensors or readout electronics) to FoCal under discussion
- **Outlook: A nearly pure silicon detector for RUN5 (beyond 2030)**



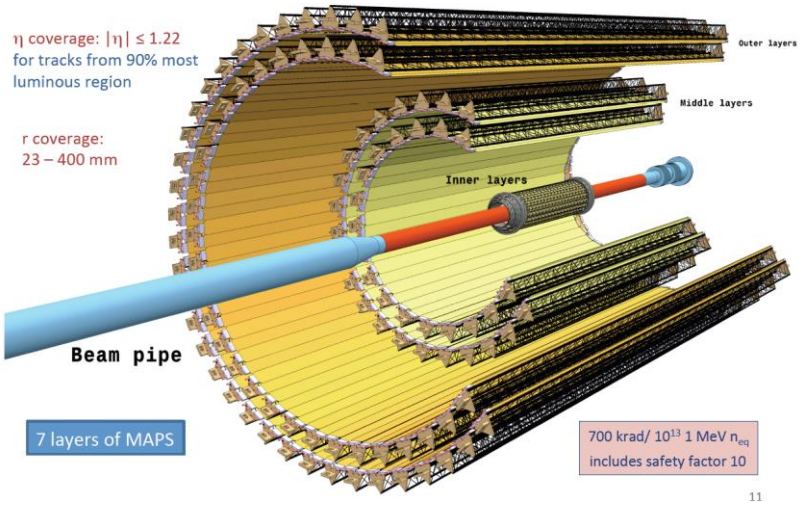
Increase rate capabilities (factor 50 wrt to ALICE RUN4)

– large acceptance, fast tracker based on wafer-scale MAPS
– 0.05% X_0/layer
– PID by TOF in Si layers
– electron and photons: pre-shower detector, converter

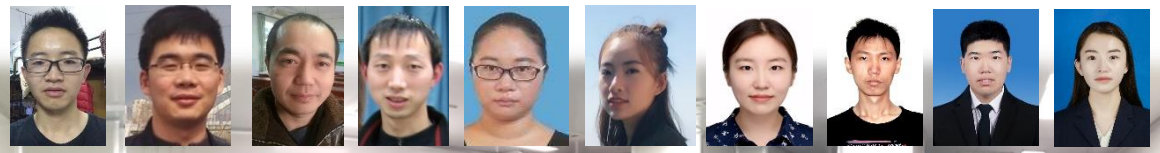
ALICE

Thank you very much for your attention !

参与ALICE升级探测器研制的状况



- 参与ITS硅像素芯片设计：(1) 芯片读出结构; (2) 像素模拟前端电子学改进
- ITS探测器模块建造与测试
  - ✓2017年9月份启动预生产
  - ✓2018年4月份启动正式生产，计划于2019年6月完成（生产率为2 模块/天，共建造500个模块）

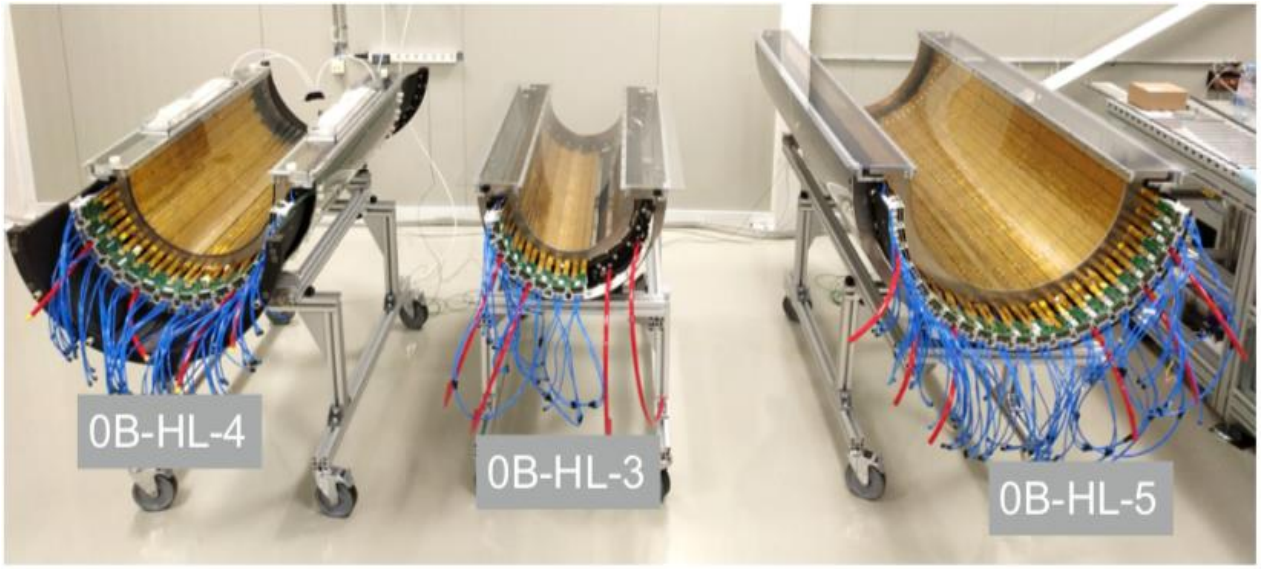


（参与学生与技术员）

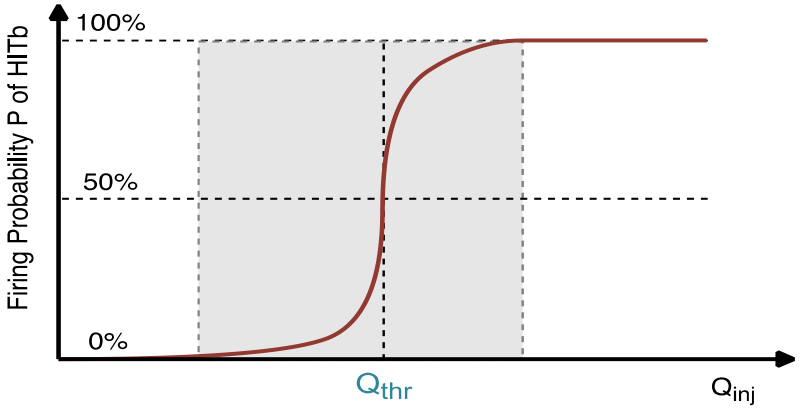
千级洁净室
（温/湿度可控，约100 平方米）

Layer and barrel assembly

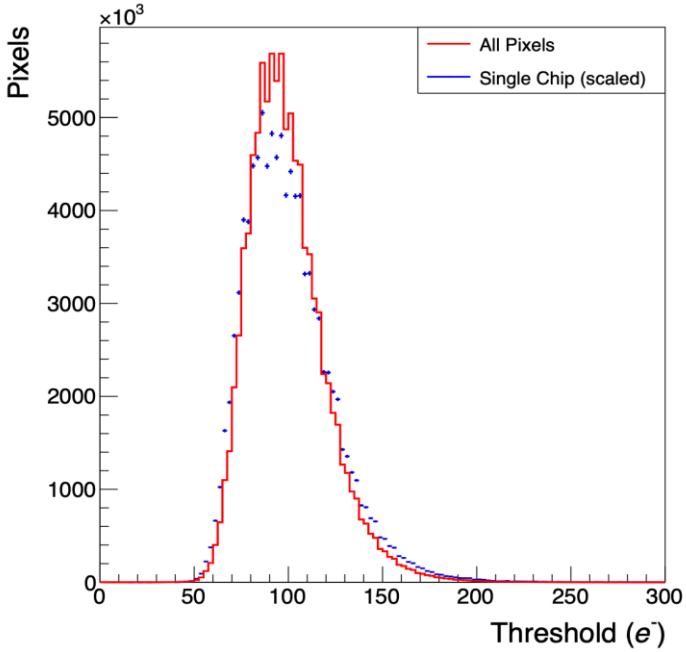
- Inner barrel assembly completed
- Outer barrel layer assembly almost done
- All staves validated after installation
- Inner barrel fully functional
- Outer half-barrels being assembled avoiding overlaps of dead chips
- Maximum accepted dead area per stave is 2%

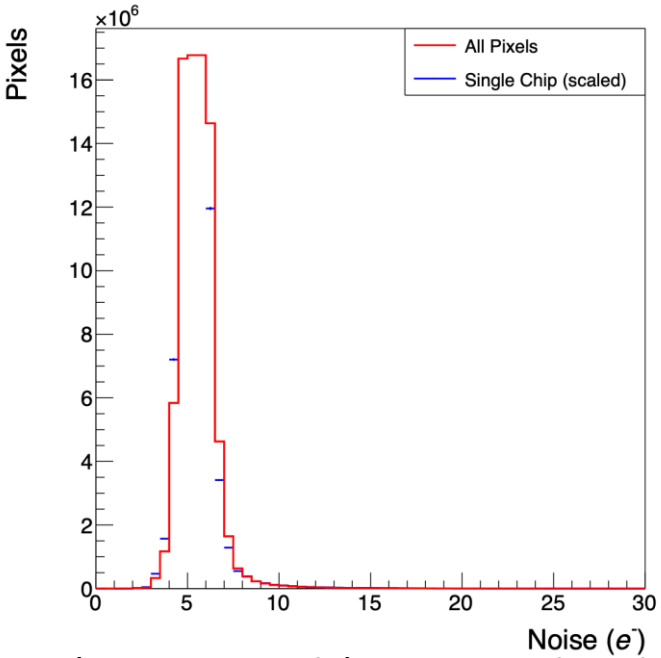


Noise and threshold performance



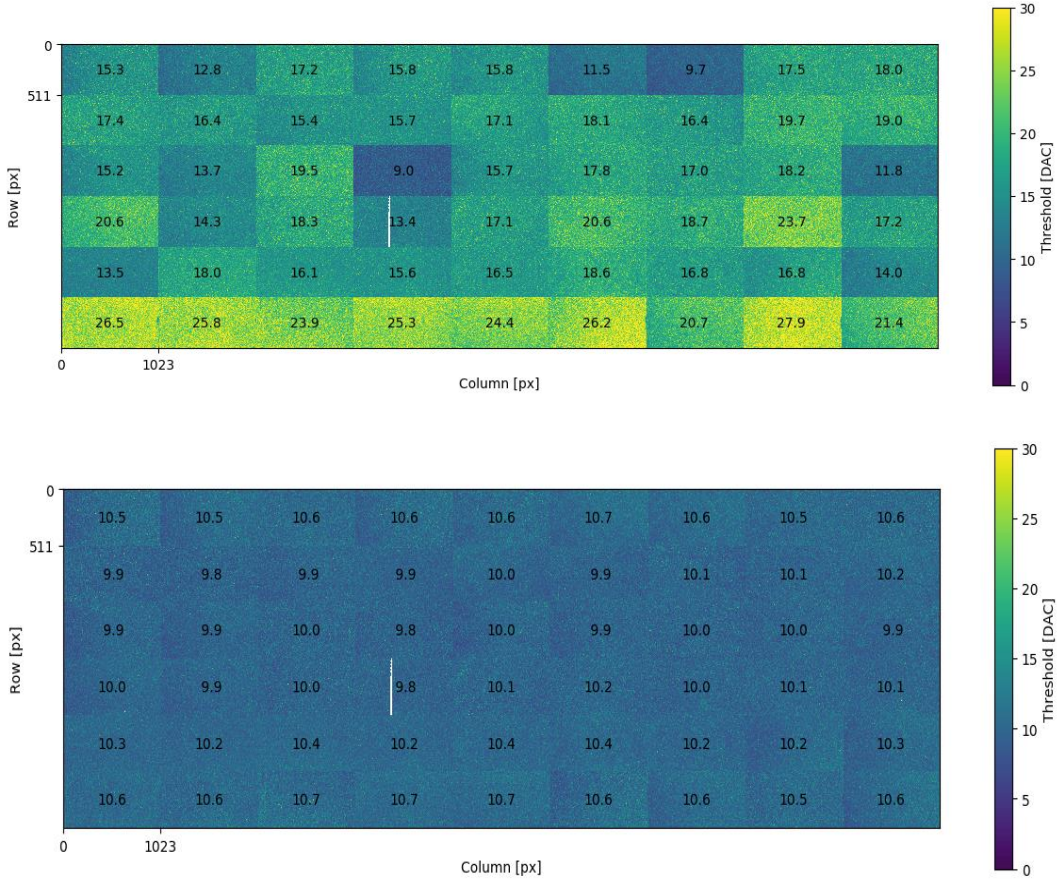
$$P(q) = \frac{1}{2} \cdot \mathrm{Erf}\left[\frac{q - Q_{thr}}{\sqrt{2} \cdot \sigma}\right]$$

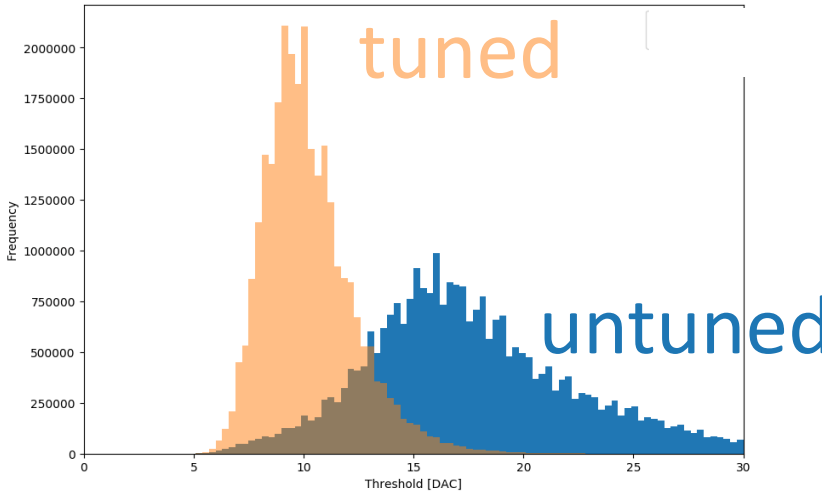




Threshold and noise after tuning for an OL Stave (~100M pixels) compared with a single chip test data

Threshold tuning





- Adjustment front-end parameters to equilibrate the charge threshold of all chips
- Achieving uniform response across the detector, verified on Half-Layer 0