

BESI

TIGER response

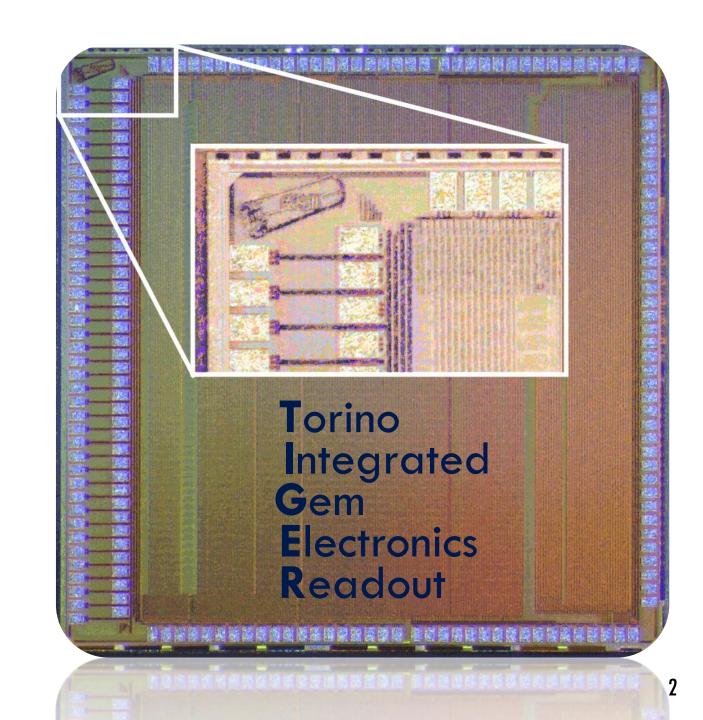
How to model and simulate TIGER response

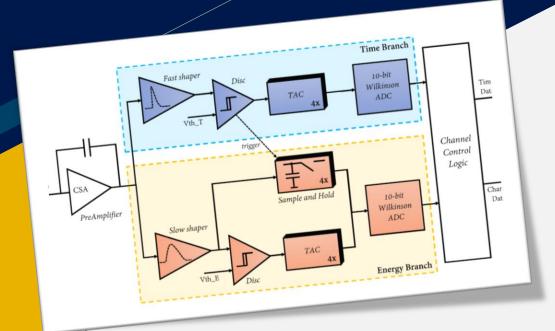
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- Front-End response model
- Charge and Time measurements
- Calibration files (VTH, TDC, QDC)





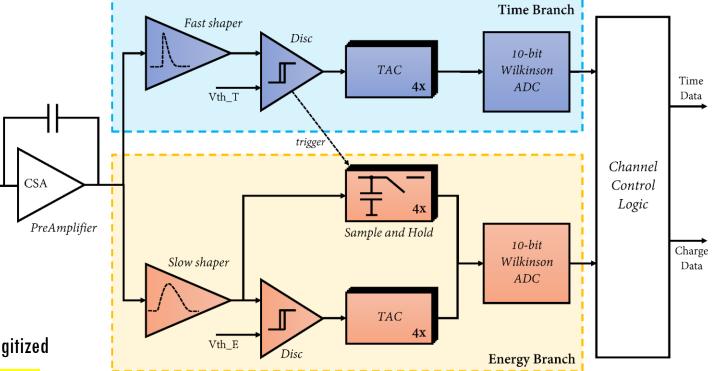
Channel architecture

Main building blocks of one TIGER channel

TIGER channel overview

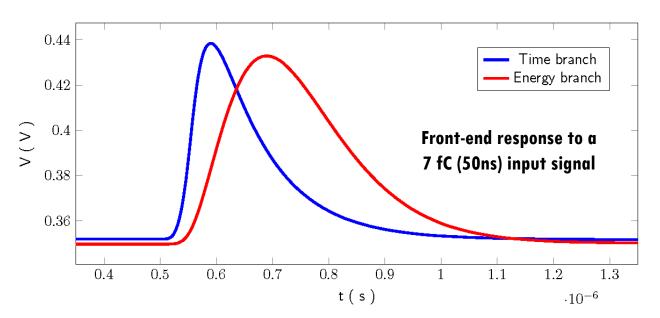
- **Dual-branch** architecture optimized for time and charge measurements
- Two leading-edge **discriminators**:
 - 6-bit DAC for threshold equalization
 - dual-threshold readout mode
- **Timestamp** on rising edge of fast branch using low-power TDCs based on analogue interpolation
- Charge measurement
 - S&H: slow shaper output peak voltage sampled and digitized
 - ToT: timestamp on rising/falling edges of T-branch (BACKUP)
- Charge and time measurements are both encoded using a 10-bit Wilkinson ADC, delivering a **fully-digital** output

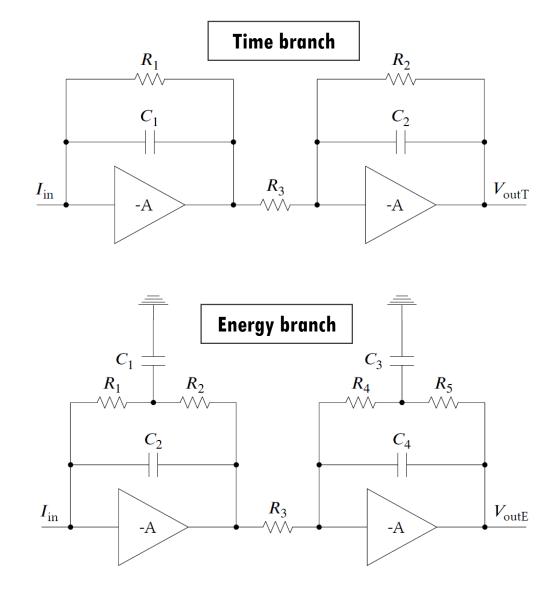
 Q_{in}



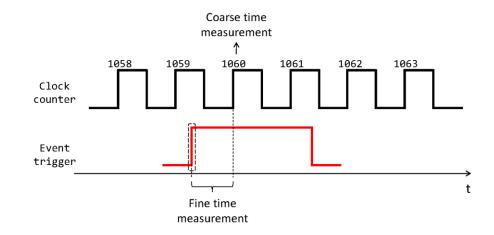
Front-End

- CSA + dual-branch shaper
 - <u>Time branch</u>: 70 ns peaking time shaper for timing measurements (timestamp and *ToT*)
 - Energy branch: 170 ns peaking time shaper for charge measurement in S&H mode



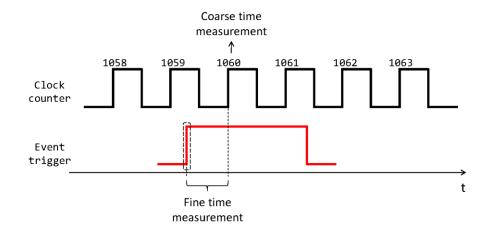


TDC operation

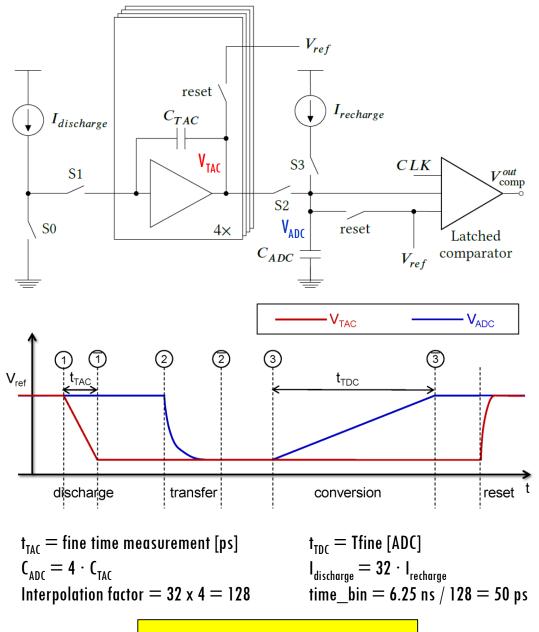


• **Coarse time measurement** from the chip master clock counter (160 MHz)

TDC operation

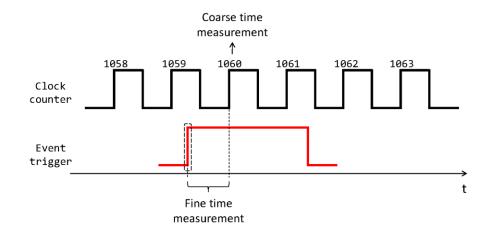


- Coarse time measurement from the chip master clock counter (160 MHz)
- Fine time measurement with low-power analogue TDCs based on time interpolation
 - Each TDC has 4 Time-to-Amplitude Converters (TAC)
 - Calibration is performed for each TAC
 - LUT provides gain-offset correction for each TAC

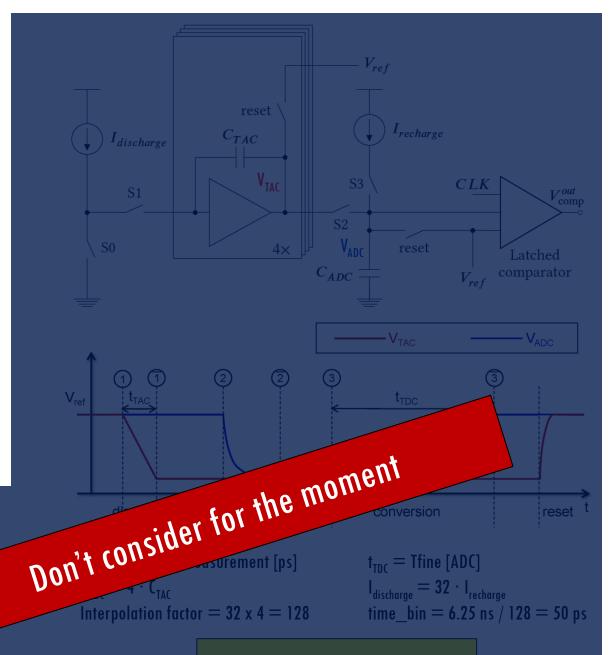


 $t_{TAC} [ps] = 50 ps \cdot t_{TDC} [ADC]$

TDC operation



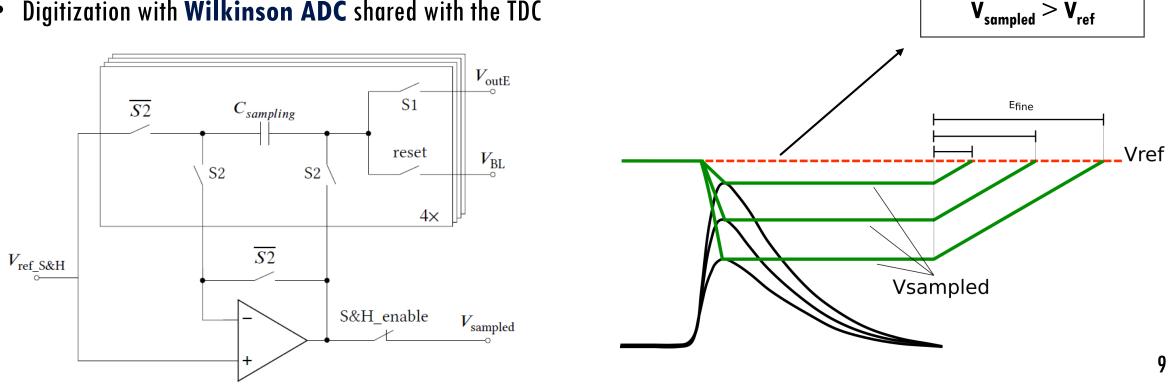
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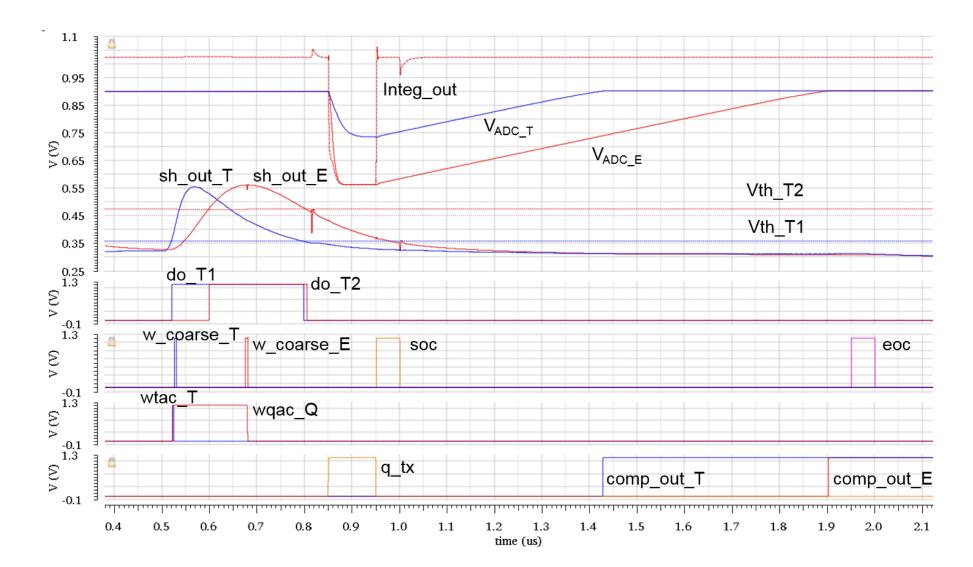
Sample-and-Hold circuit

- **Charge measurement** with S&H circuit sampling the E-branch shaper output
- Programmable sampling time targeting the **signal peak** \bullet
- Digitization with **Wilkinson ADC** shared with the TDC



S&H saturation when

Full channel simulation



10

TIGER output words (64-bit)

• Charge and time measurements are both encoded using a 10-bit Wilkinson ADC, delivering a fully-digital output

K28.1	e ch_id	Tcoarse	Ecoarse	Tfine	Efine	
	6 bits	16 bits	10 bits	10 bits	10 bits	

EVENT WORD

FRAME WORD

K28.1	0x00	reserved	frame count	SEU count	
			16 bits	15 bits	

COUNT WORD

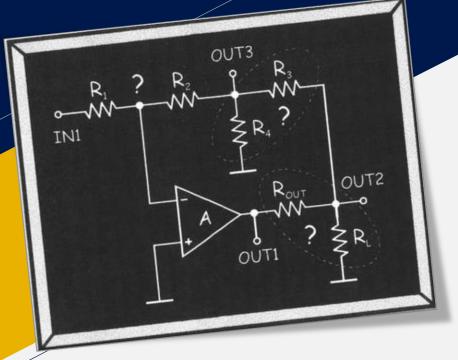
K28.1	0x01	reserved	ch_id	counter value
			6 bits	24 bits

- 1. Event word digitized output of each hit
- 2. Frame word global timing reference

3. Count word read some counters inside TIGER for debug purposes

Event word

Bits	Parameter	Description		
63:56	K28.1	Start of the 64-bit word identifier		
55:54	0b10	Event word identifier		
53:48	Channel_id	Channel identifier		
47:46	TAC_id	TAC index		
45:30	Tcoarse	Leading edge coarse time tag		
29:20	Ecoarse	Falling edge coarse time tag (ToT mode)		
29.20	Ecoarse	Sampling stop time tag (S&H mode)		
19:10	Tfine	T-branch TDC fine time measurement		
9:0	Efine	E-branch TDC fine time measurement (ToT mode)		
7.0		ADC charge value (S&H mode)		



Front-End model

Transfer functions of TIGER analogue very-front-end

TIGER model

- Build a model to simulate the TIGER response in order to be integrated in the CGEM-IT simulation code
- The model must:

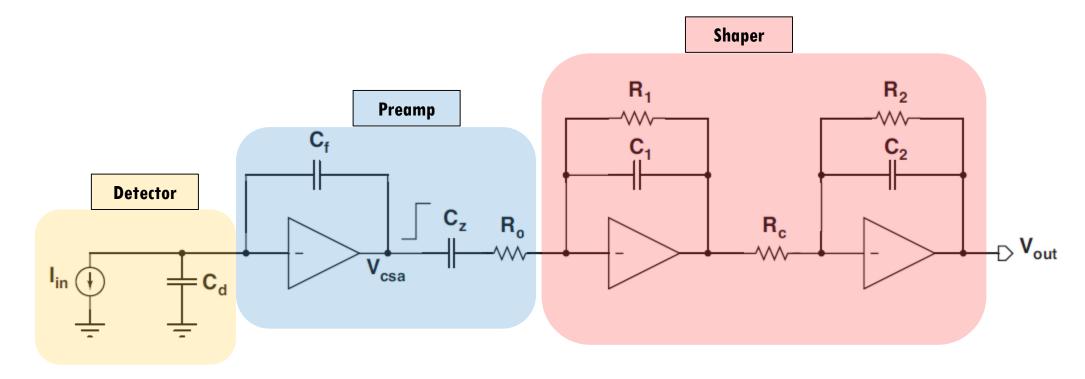
Take into account the different duration and shape of input signals

D show the different responses from T-branch and E-branch

D be faster than computer circuit simulator

anything else?

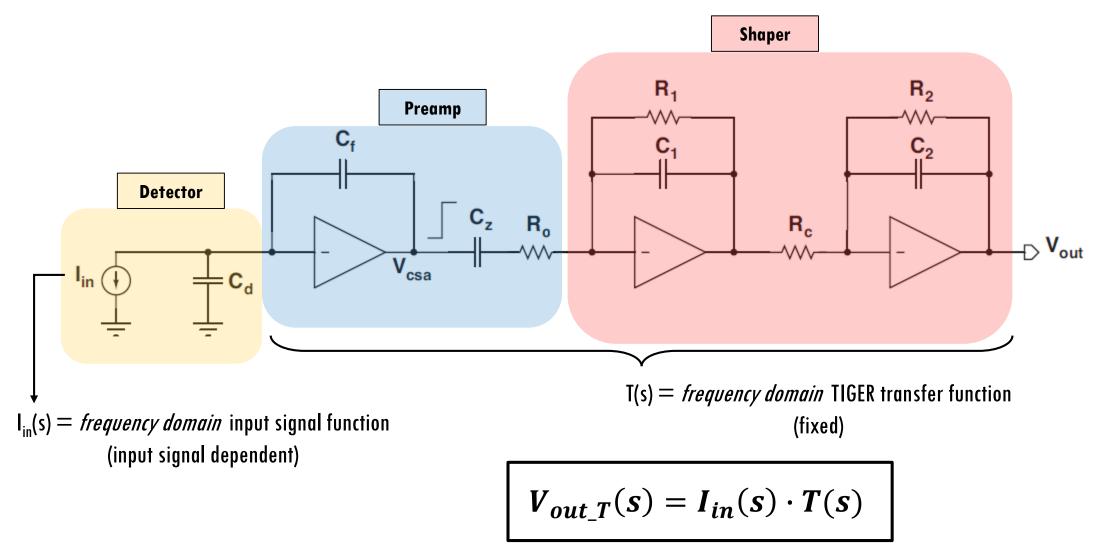
TIGER T-branch



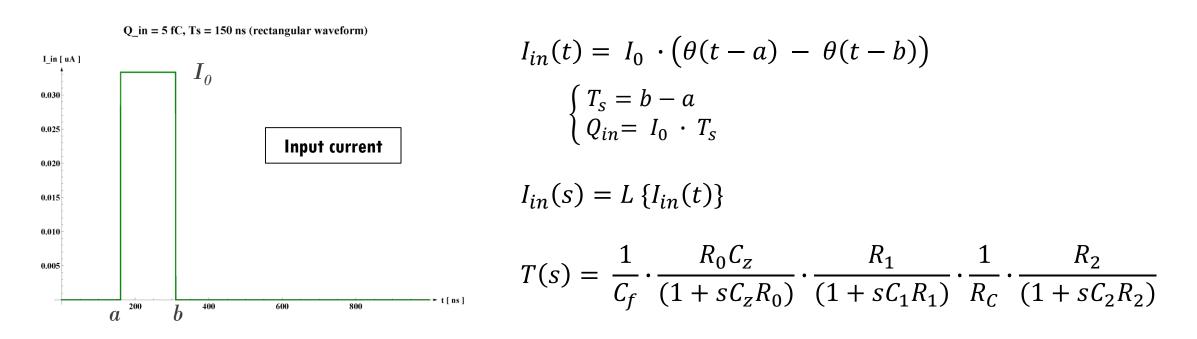
- $C_f = 0.150$
- $C_z = 20 C_f = 3$
- $R_0 = 1$
- $R_1 = 100$
- $C_1 = 1$
- $R_2 = 20$

- $C_2 = 1$
- $R_c = 20$
- $V_{bsln} \approx 350 \text{ mV}$

TIGER model (T-branch)



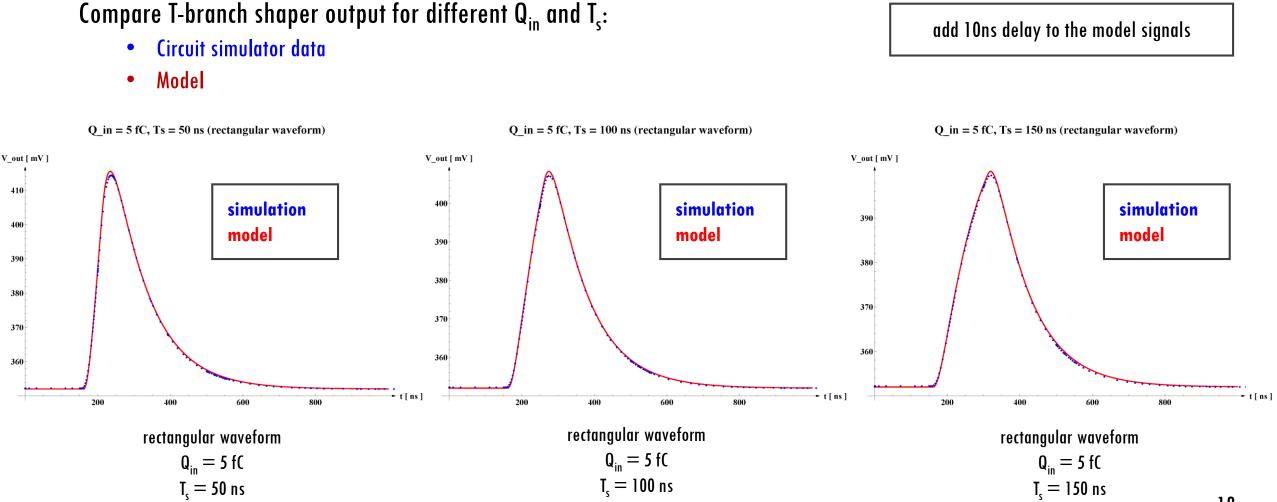
TIGER model (T-branch)



$$V_{out_T}(t) = L^{-1}\{I_{in}(s) \cdot T(s)\} = V_{bs/n} + 2000 \cdot I_0$$

((1-0.00545785e^{0.333333(a-t)}+0.294118e^{0.05(a-t)}-1.28866e^{0.01(a-t)})\theta(-a+t)+ -(1-0.00545785e^{0.333333(b-t)}+0.294118e^{0.05(b-t)}-1.28866e^{0.01(b-t)})\theta(-b+t))

TIGER response (model vs simulation)



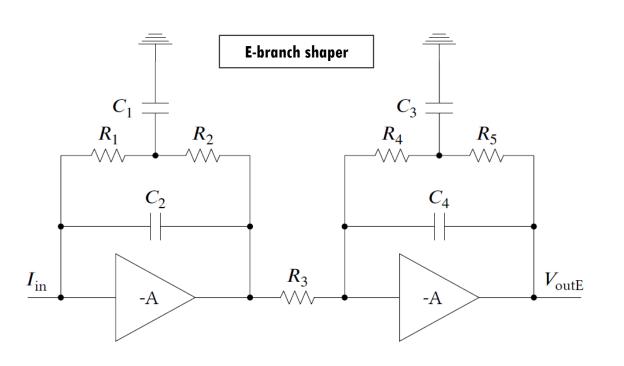
TIGER model (E-branch)

- The E-branch shaper has 2 stages with two complex conjugate poles for each stage
- The transfer function of each stage can be expressed as:

$$T(s) = \frac{G \cdot \omega_0^2}{s^2 + \frac{s \cdot \omega_0}{Q} + \omega_0^2}$$

where:

- G = DC gain
- $\omega_0 =$ natural angular frequency
- Q = quality factor



TIGER model (E-branch)

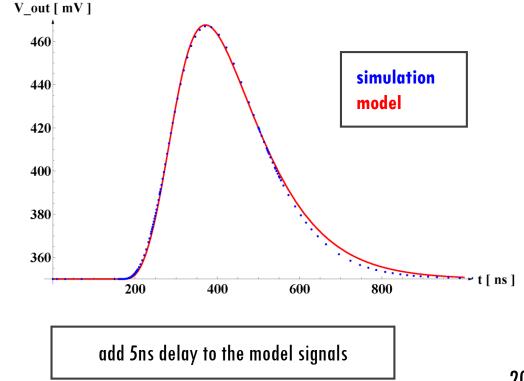
• The overall E-branch transfer function can be approximated as:

$$T(s) = \frac{C_z}{C_f} \cdot \left(\frac{G \cdot \omega_0^2}{s^2 + \frac{S \cdot \omega_0}{Q} + \omega_0^2}\right)^2$$

where:

- G = 12.7
- $\omega_0 = 0.021$
- Q = 0.42
- $C_z = 20 C_f$

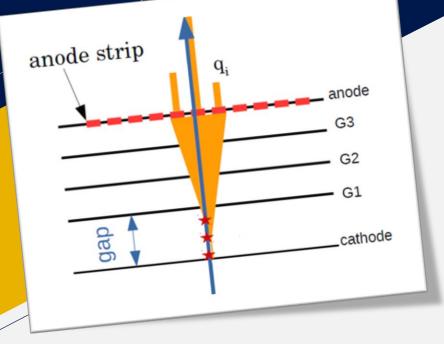
Q_in = 10 fC, Ts = 100 ns (rectangular waveform)



TIGER Front-End model summary

- A first draft of a model to simulate the TIGER response in order to be integrated in the CGEM-IT simulation code has been developed
- The model:
 - \checkmark takes into account the different duration and shape of input signals
 - \checkmark well reproduces the T-branch shaper output
 - \checkmark provides a good approximation for the E-branch shaper output
 - \checkmark validated with "real" CGEM signals
 - ✓ faster than computer circuit simulator (requires *Laplace Transform* evaluation)
- To-Do:

 \Box Take into account the saturation of the front-end (signals > 50 fC will have a different response)



Analogue readout concept

Time and charge measurements principle of operation

Time measurement

3 accuracy levels:

1. Frame-word

- \sim 200 us time resolution
- chip data (frame count, common for the 64 channels)

2. Coarse counter

- 6.25 ns time binning (160 MHz)
- channel data (<mark>Tcoarse</mark>)

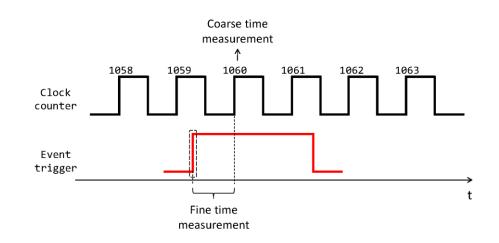
3. Fine counter

- <100 ps time resolution
- channel data (<mark>Tfine</mark>)

						UND		
	K28.1	10	ch_id	AC	Tcoarse	Ecoarse	Tfine	Efine
		qo	6 bits	F	16 bits	10 bits	10 bits	10 bits

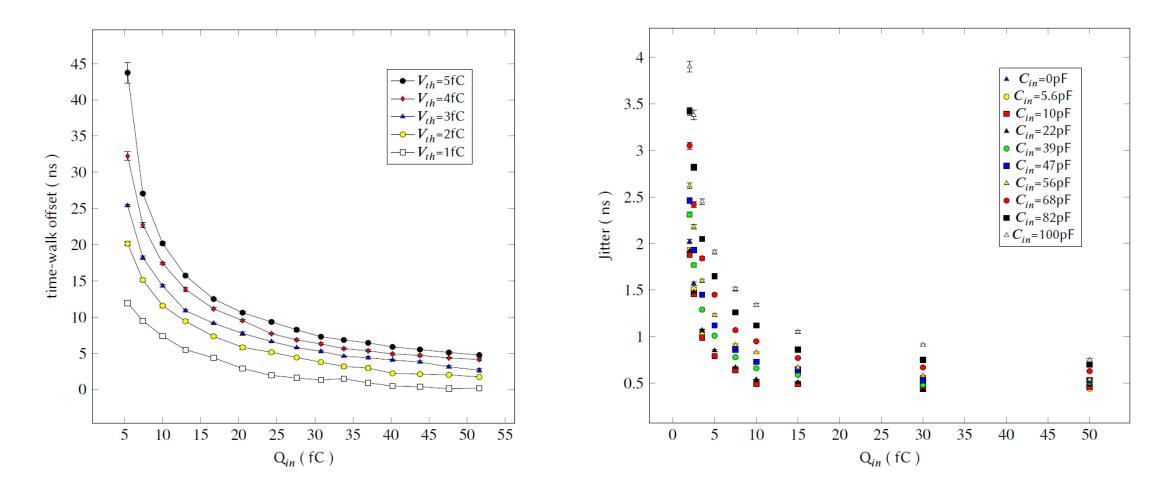
EVENT WORD

FRAME WORDK28.10x00reservedframe count
16 bitsSEU count
15 bits

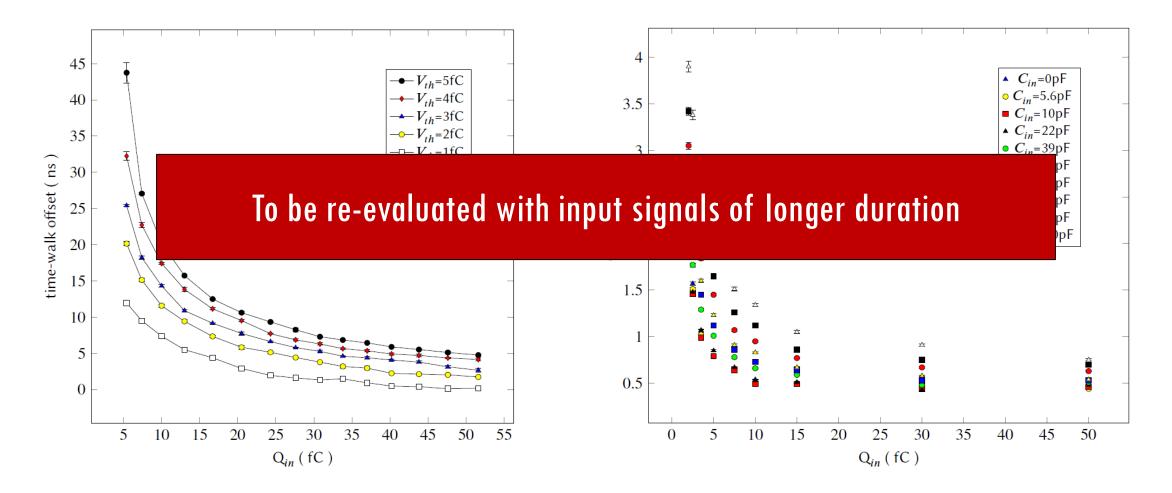


In ToT mode Ecoarse and Efine have the same meaning of Tcoarse and Tfine but for the falling edge

Time-walk and jitter



Time-walk and jitter



Time-walk and jitter

- Use CGEM simulated signals to evaluate TIGER front-end timing performance
 - Time-walk depends only on the applied threshold
 - Jitter can be estimated with the formula:

$$\sigma_t = \frac{\sigma_v}{\frac{dV}{dt}}$$

where:

$$\begin{cases} \sigma_v = \text{noise measured at the T-branch shaper output} \\ \frac{dV}{dt} = \text{T-branch shaper output slew rate around the threshold} \end{cases}$$

Charge measurement

Two mutually exclusive^{*} modes:

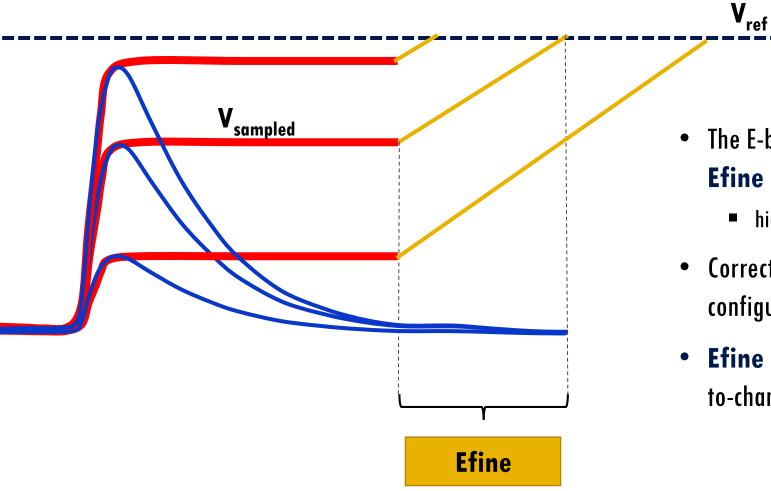
- 1. QDC mode (qdc_mode = 1, integ_en = 1)
- **2. ToT mode** (qdc_mode = 0, integ_en = 0)

ToT is only a backup solution

- To check which charge measurement mode was used in a run, one can check the value of *Ecoarse Tcoarse_10bit*
 - if it is almost constant *QDC mode* was selected
 - otherwise *ToT mode* was selected and this value is the Time-over-Threshold measurement

^{*} The charge measurement mode is set when the chips are configured before running the acquisition

Charge measurement (S&H mode)

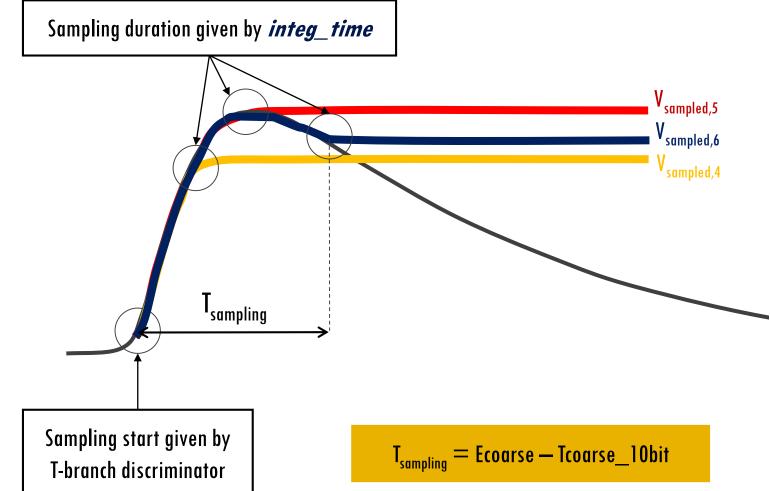


S&H saturation when $\mathbf{V}_{\mathsf{sampled}} > \mathbf{V}_{\mathsf{ref}}$

- The E-branch shaper output is sampled and digitized: Efine provides the information about the charge
 - high Efine means low charge and vice-versa
- Correct peak sampling set by *integ_time* channel configuration register
- Efine calibration curves to compensate channelto-channel and chip-to-chip offsets

Sampling time

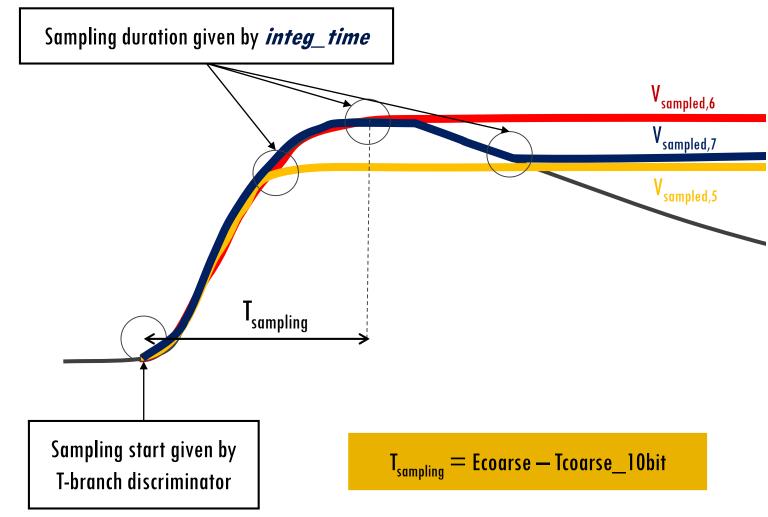
$T_{sampling} = 4 \cdot 6.25ns \cdot (integ_time + 1)$



- S&H peak detector configured and calibrated for a 170 ns peaking time (*integ_time* = 5)
- If signals last longer than the design specification (50 ns) the sampling time (*integ_time*) must be increased → 4 clock cycles steps (= 25 ns)
- Sampling start is given by the T-branch, due to its better timing performance

Sampling time

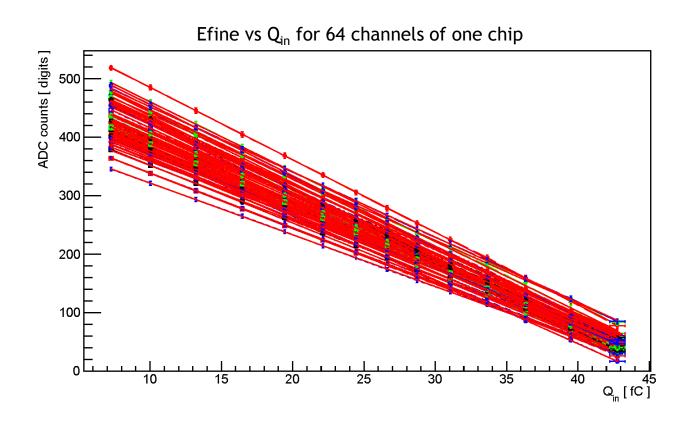
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S&H calibration

Efine calibration curves (linear response) to compensate channel-to-channel and chip-to-chip offsets



Look-Up-Table (LUT)

- FEB_id
- CHIP_id
- CHANNEL_id
- fit SLOPE parameter
- fit CONSTANT parameter

Threshold calibration

- Threshold scans are performed on both branches of all channels to correct channel-by-channel and chip-by-chip offsets and mismatches
- Equalized threshold values are stored in LUT which are used to configure each channel before the acquisition starts
 - Threshold scans allow also to evaluate the noise for each channel (σ = noise)
 - This information is used to set the threshold at a given value (e.g. 3σ) above the baseline in order to equalize the channels noise rate (few kHz)







Backup slides

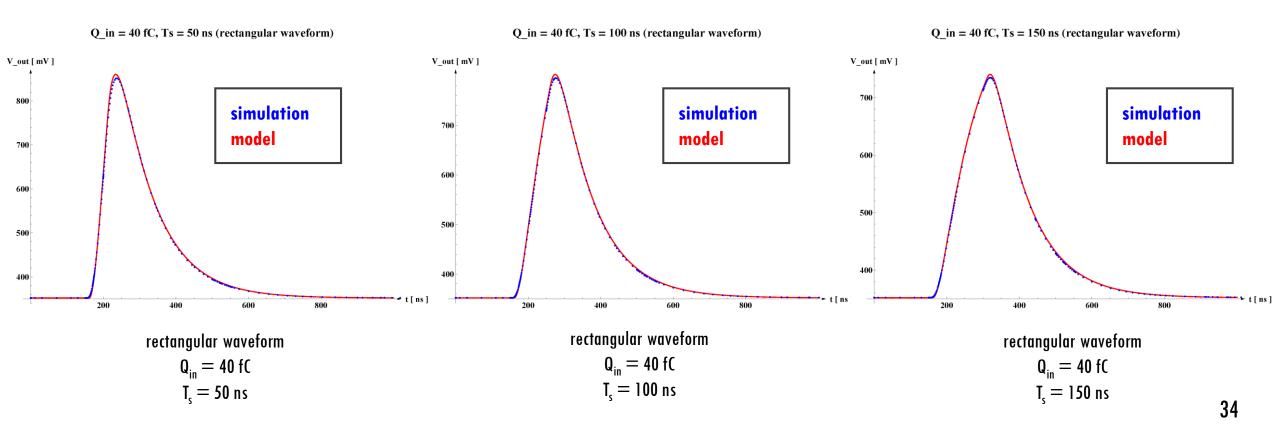


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TIGER response (model vs simulation)

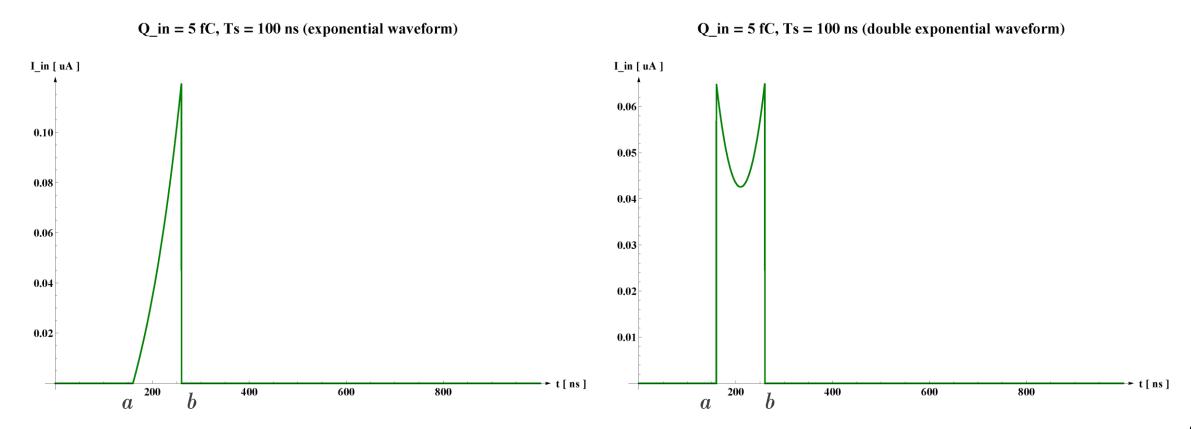
Compare T-branch shaper output for different Q_{in} and T_s:

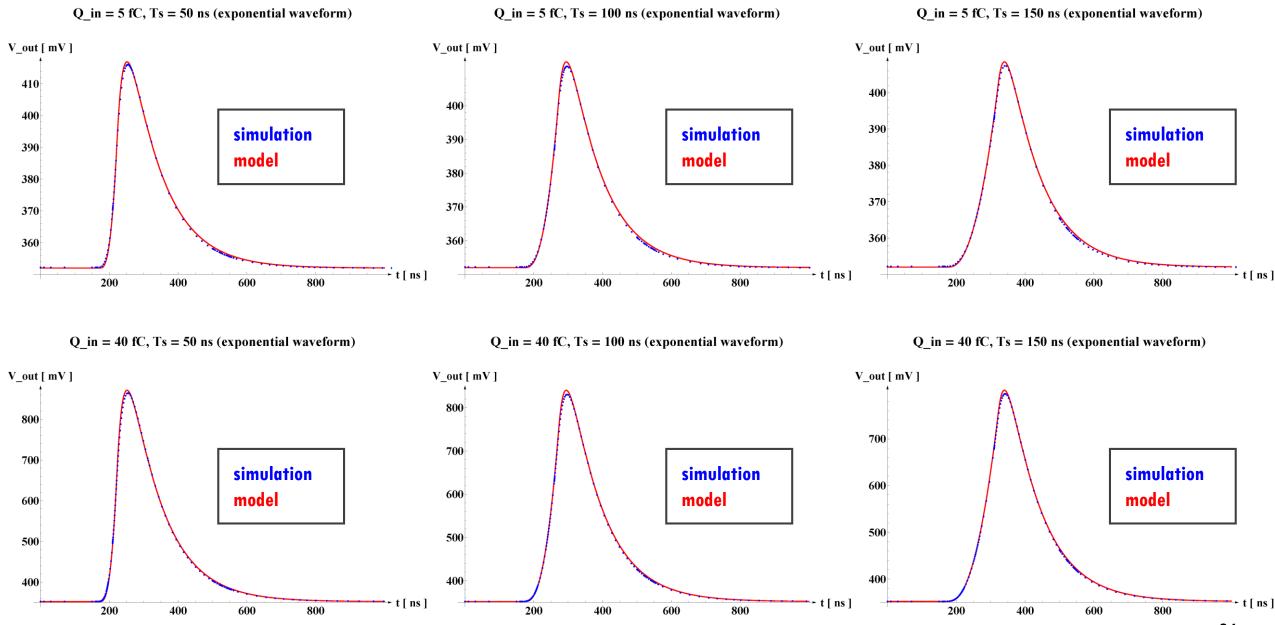
- Circuit simulator data
- Model

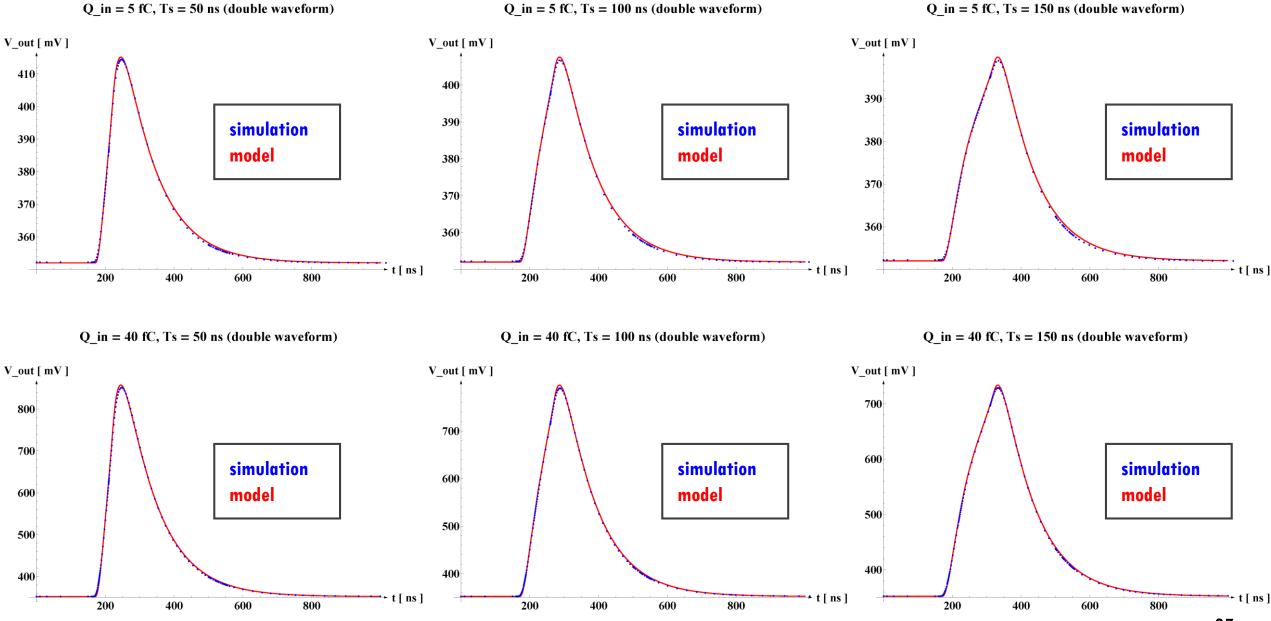


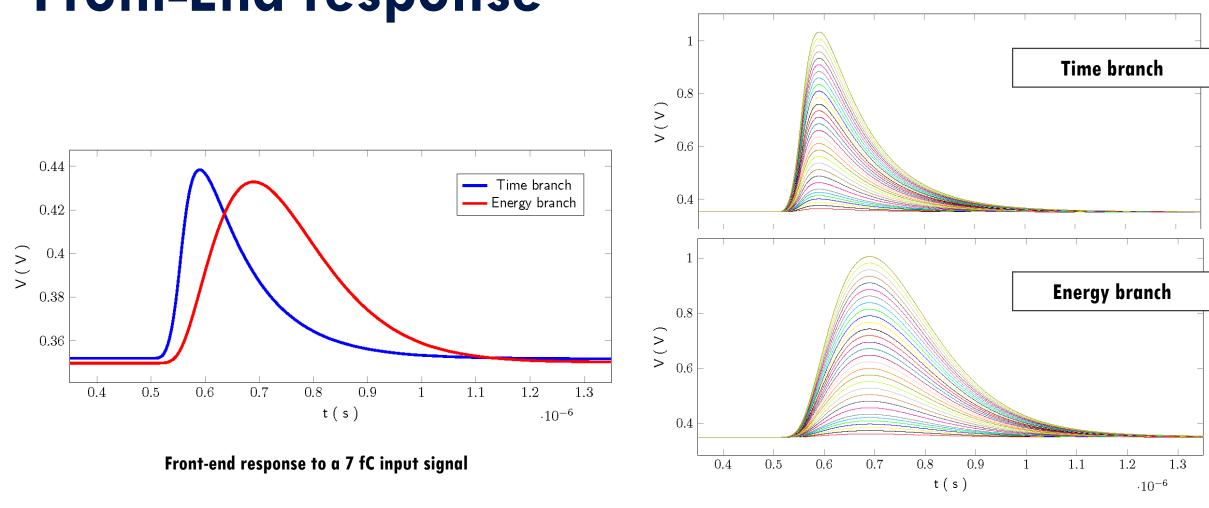
TIGER model (T-branch)

Repeat including also input signals of different shapes









Front-End response

1-50 fC input signal sweep

Time measurement

1. Frame-word

- Used to reconstruct the global timestamp of each event
- Sent off-chip with top-priority (common for the 64 channels)
- 1 frame-word every 2^{15} clock cycles ($2^{15} \times 6.25$ ns = 204.8 us)
- I6-bit counter (roll-over every 13.4217728 s)

2. Coarse counter

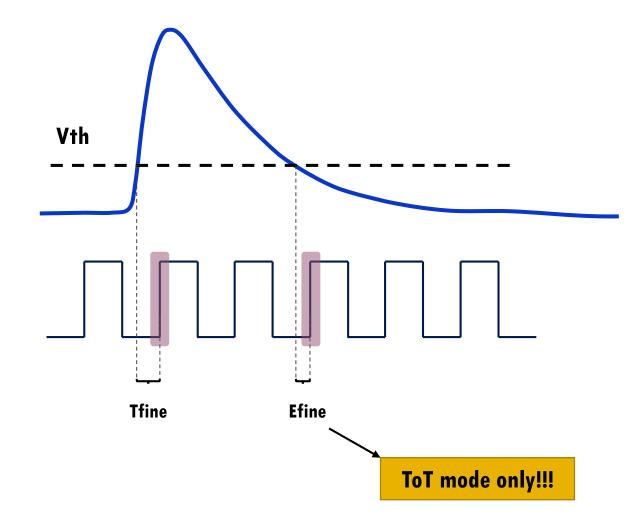
- Combine with frame-word information to reconstruct the global timestamp of each event
- Data related to single channel-event
- I coarse counter = 1 clock cycle (6.25 ns)
- 16-bit counter (roll-over every 6.25 ns x $2^{16} = 409.6$ us)

Time measurement

Frame-word + Coarse counter examples:

- Frame-word = 6546
 → 6546 x 204.8 us = 1340.6208 ms
- Tcoarse = 13465 \rightarrow 13465 x 6.25 ns = 84.15625 us
- Solution State = 1340.6208 ms + 84.15625 us = 1340.70495625 ms
- Frame-word = 6547
 → 6547 x 204.8 us = 1340.8256 ms
- Tcoarse = 43465 \rightarrow (43465 2¹⁵) x 6.25 ns = 66.85625 us
- Solution States States

Fine time correction



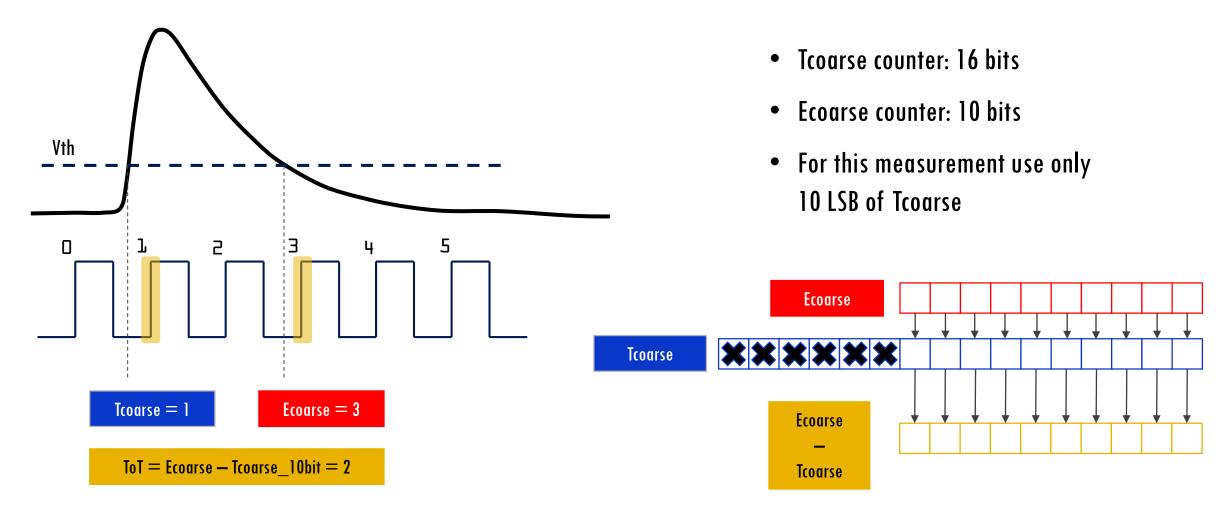
- Tfine counter: 10 bits
- Tfine calibration with a TDC TP phase scan
- This measurement is performed by the 4 TACs (Time-to-Amplitude Converter) of each TDC
- Only in ToT mode apply the same correction also with Efine

Fine time correction

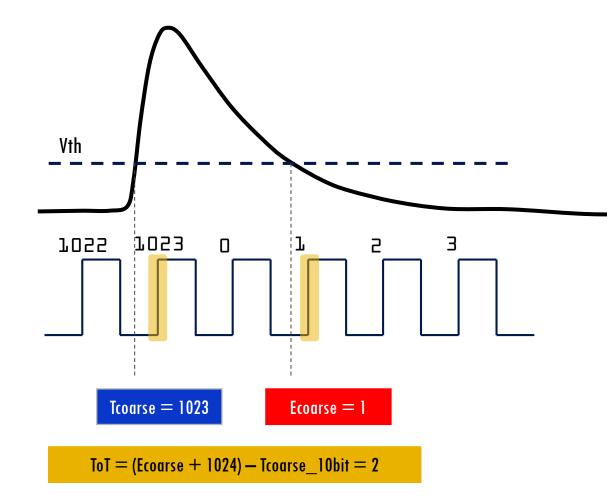
- Timestamp = frame_word + Tcoarse (Tfine offset) · time_bin
- *offset and time_bin* provided by LUT (64 channels x 4 TACs gain-offsets compensation)
 - *offset* = Tfine_{MIN}
 - $time_bin = 6.25 \text{ ns} / (Tfine_{MAX} Tfine_{MIN})$

- The same correction can be applied also to Ecoarse (using Efine) but only when in ToT mode:
- Falling edge trigger time = frame_word + Ecoarse (Efine offset) · time_bin
 - *offset* = Efine_{MIN}
 - time_bin = 6.25 ns / (Efine_{MAX} Efine_{MIN})

Time-over-Threshold measurement



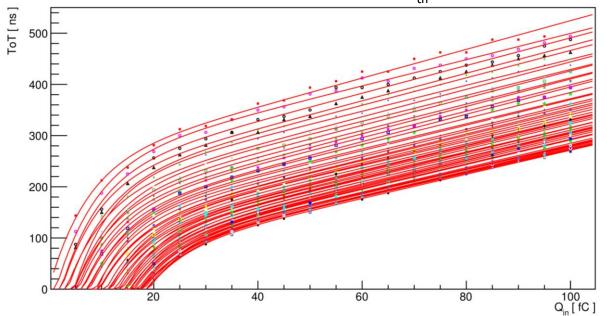
Time-over-Threshold measurement



- Tcoarse counter: 16 bits
- Ecoarse counter: 10 bits
- For this measurement use only 10 LSB of Tcoarse
- Check for counters roll-over (restart from 0 after it reaches 2^10 - 1 = 1023)

Time-over-Threshold calibration

Compensate channel-to-channel offsets due to different thresholds set (depends on acquisition settings) and transistor mismatches (fixed)



ToT curves for different V_{th}

- Response is not linear
- Biggest contribution to channel-to-channel offsets comes from **threshold settings** (not-fixed)
- Fit with the following function:

$$ToT = E \cdot e^{A \cdot Q_{in} + B} + C + D \cdot Q_{in}$$

To be re-evaluated with longer duration input signals