NICA-China

MAPS-based Inner Tracker for NICA/MPD and R&D Plan in China

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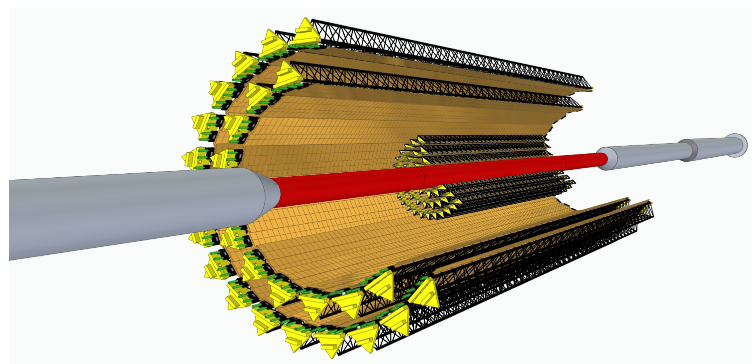
Pixel Laboratory at CCNU
PLAC



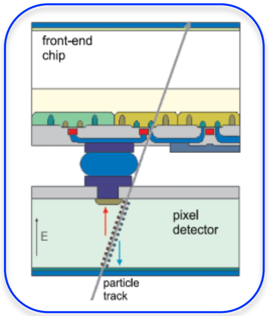
Outline

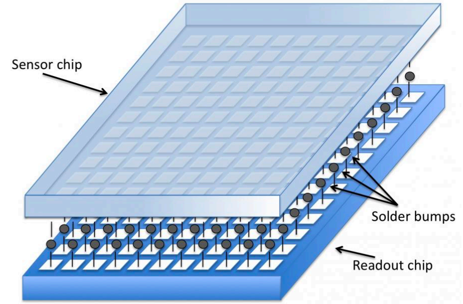
- Introduction
- MAPS-based Inner Tracker (IT) for the NICA/MPD
- R&D Plan in China for the MPD/IT
  - R&D on wafer-scale ultra-thin MAPS chip for Inner Barrel (IB)
  - Detector construction for Outer Barrel (OB)
  - Readout electronics
  - Testing & simulation
  - Organization and plan
- Summary and Outlook

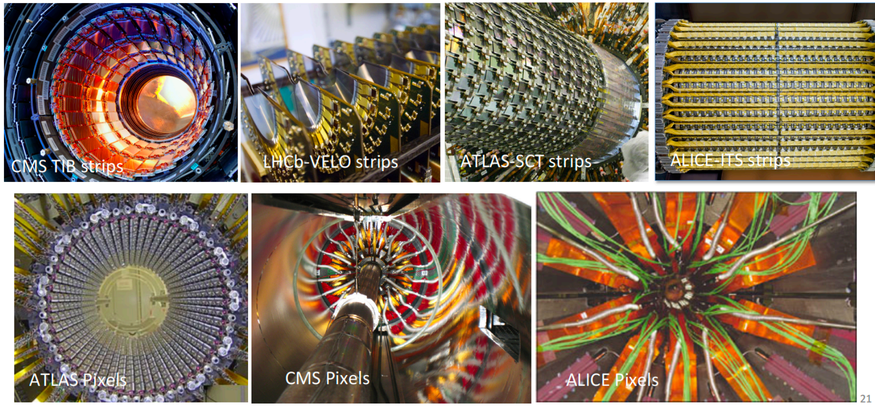
Introduction – Beyond Hybrid Pixel Detector

- First Hybrid Pixel detector installed in WA97 in 1995 (CERN, Omega facility)
- The silicon detectors were installed at the heart of LHC experiments since 2005

Hybrid pixel detector



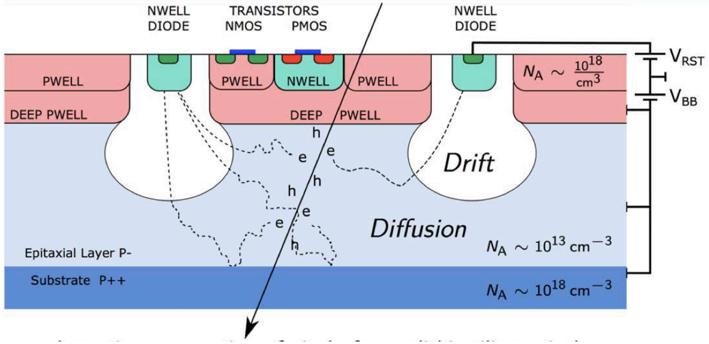




- ➢ Sensor based on silicon junction detectors produced in a planar process
- ➢ Readout chip: ASIC-CMOS sub-micron technology
- ➢ Interconnection technology based on flip-chip bonding
- ➢ Applied in the LHC experiments: ALICE, ATLAS, CMS, PHENIX

- ➢ Charge generation volume integrated into the ASIC
- ➢ Exist in many different flavors: CCDs, CMOS MAPS, DEPFET, …

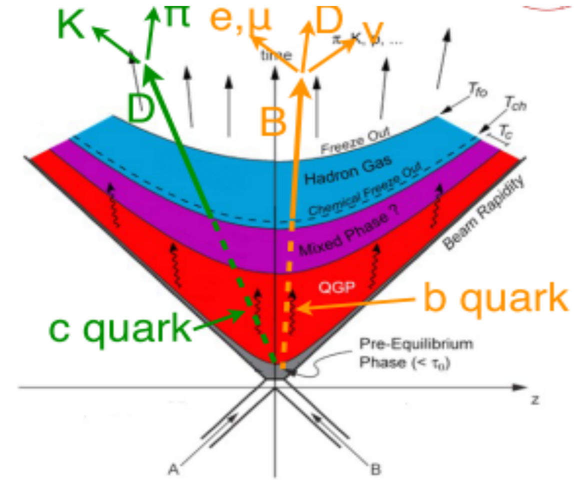
Monolithic Active Pixel Sensors (MAPS)

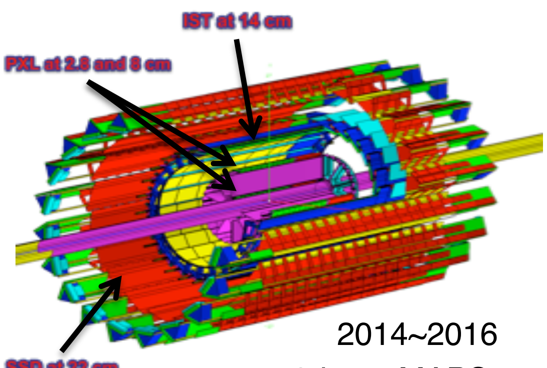


Introduction – MAPS Pixel Detector in HIC Experiments

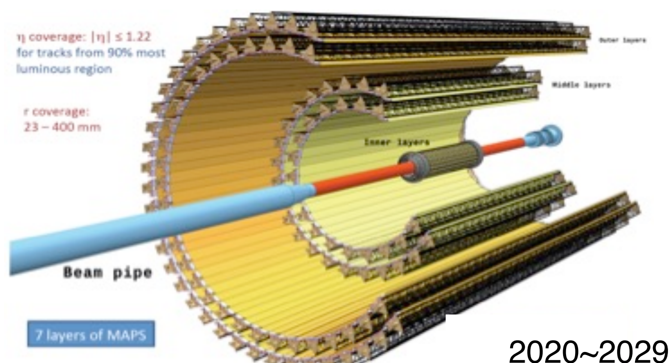
Vertex Detector for HF physics measurements in HIC experiments

- MAPS, hard radiation, low material budget, low power consumption, fast readout, high spatial resolution
- Produced mostly from initial hard partonic scatterings at RHIC energies; exposed to the whole evolution of the Quark-Gluon Plasma (QGP)
- Yield or mass not (significantly) altered within the QGP, sensitive to parton-medium interactions and medium properties

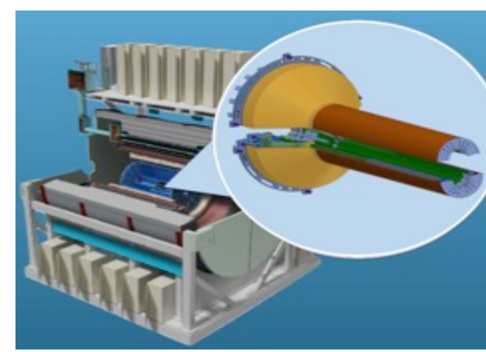




2014~2016
2-layer MAPS,
360M pixels, 20μmx20μm,
inner layer 0.4% X_0

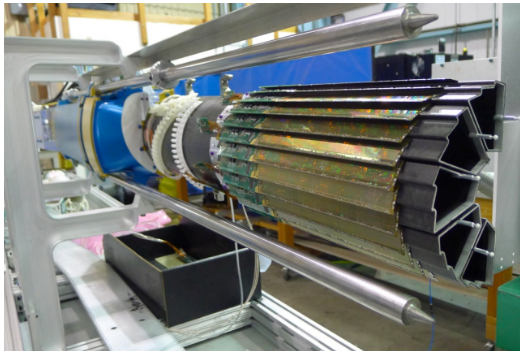


2020~2029
7-layer MAPS, 12.5G pixels,
inner layer 0.3% X_0



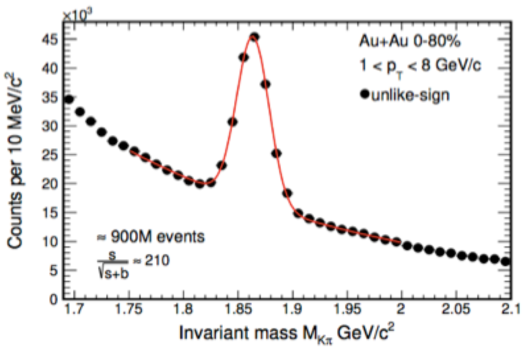
2019~2023@sPHENIX
Replica of ALICE ITS Inner Barrel

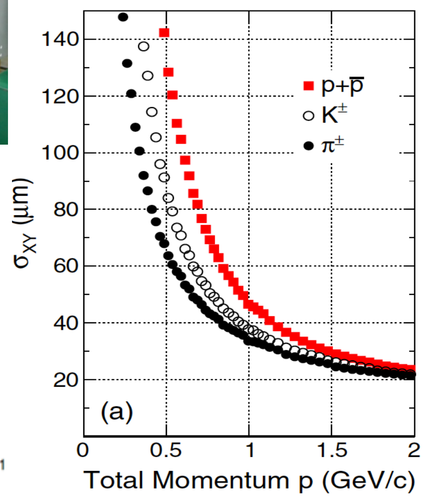
Introduction – MAPS at RHIC/STAR Experiment

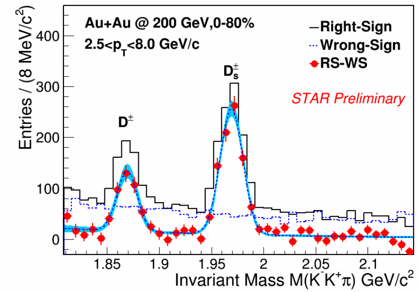


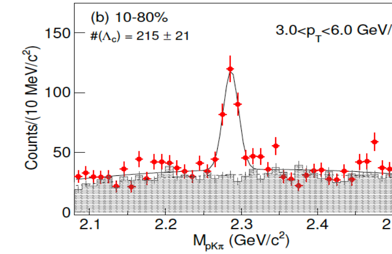
PXL@STAR-HFT

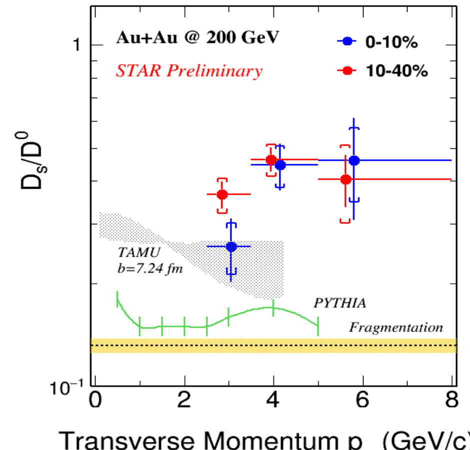
3B minimum-bias Au+Au events at $\sqrt{s_{NN}}$ = 200 GeV with HFT recorded in 2014 and 2016

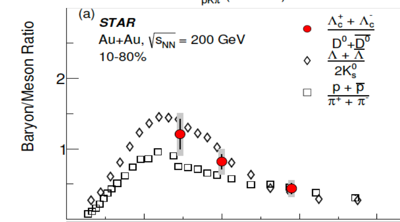


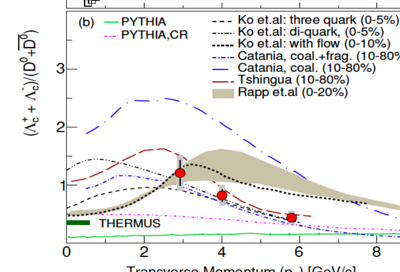


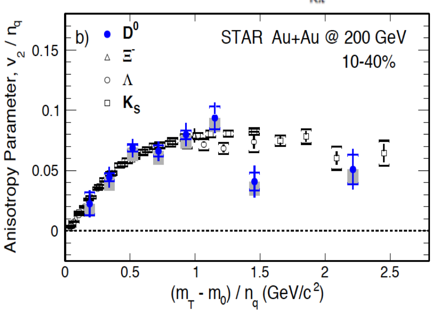


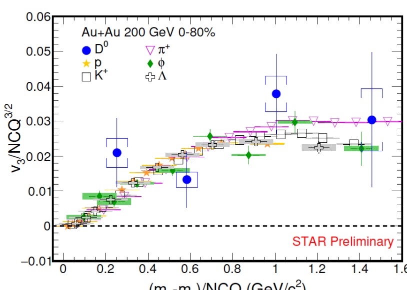






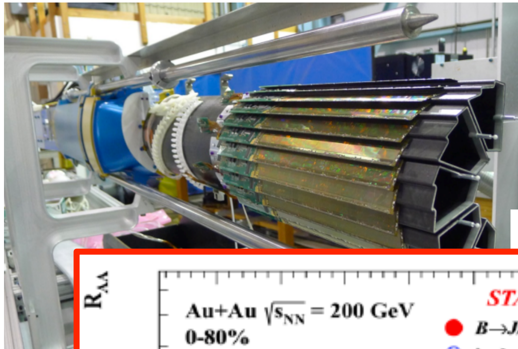






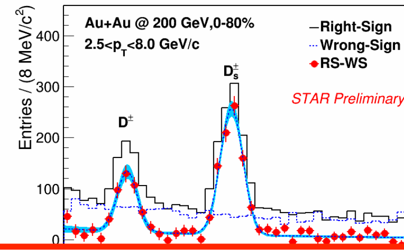
- D^0 v_2 for 10-40% follows mass ordering and NCQ scaling of other hadrons
- First D^0 v_3 measurement, which follows NCQ scales with other hadrons → non-zero at RHIC
- Strong D_s/D^0 enhancement observed over PYTHIA
- First Λ_c reconstruction in A+A collisions

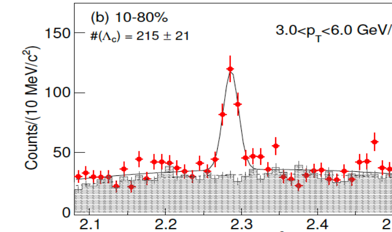
Introduction – MAPS at RHIC/STAR Experiment

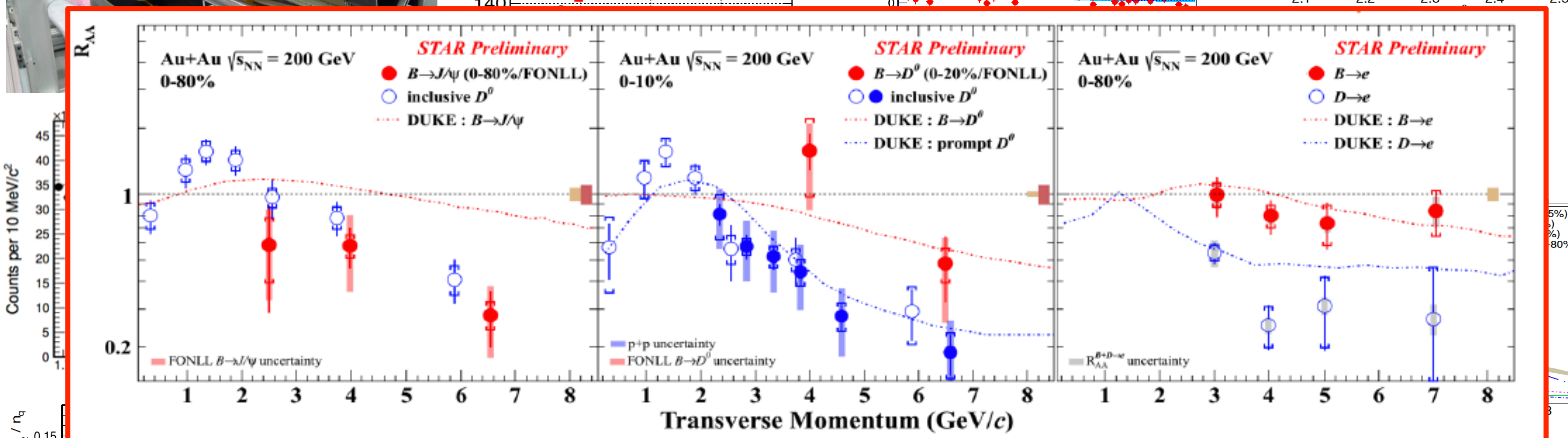


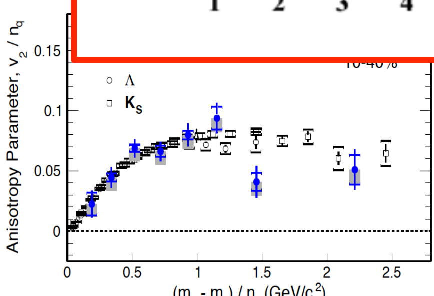
PXL@STAR-HFT

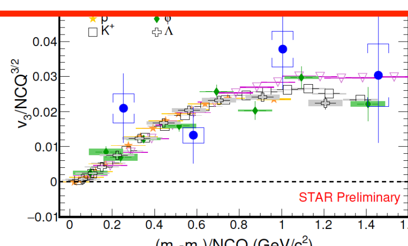
3B minimum-bias Au+Au events at $\sqrt{s_{NN}}$ = 200 GeV with HFT recorded in 2014 and 2016





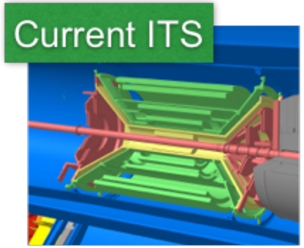


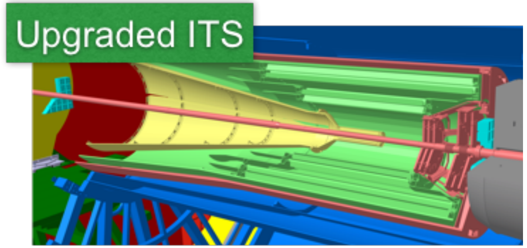




- D^0 v_2 for 10-40% follows mass ordering and NCQ scaling of other hadrons
- First D^0 v_3 measurement, which follows NCQ scales with other hadrons → non-zero at RHIC
- Strong D_s/D^0 enhancement observed over PYTHIA
- First Λ_c reconstruction in A+A collisions
- Open-bottom measurements via non-prompt J/ψ, D^0 and NPE channels

Introduction – MAPS at LHC/ALICE Experiment



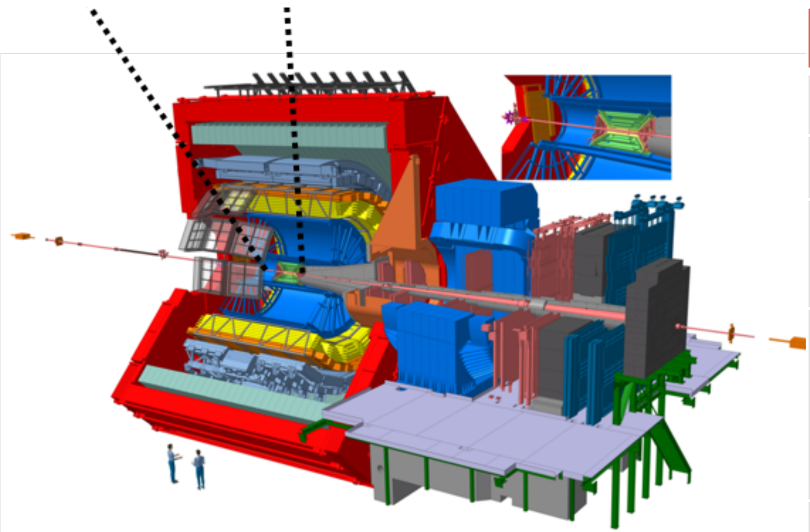


6 layers (<u>39mm</u> < r < 440mm)
$-1 \le h \le 1$

7 layers (<u>22mm</u> < r < 400mm)
$-1.5 \le h \le 1.5$

Motivations and goals

- Improved vertex and tracking precision
  - ➢ closer to IP, smaller pixels, less material
- Faster readout

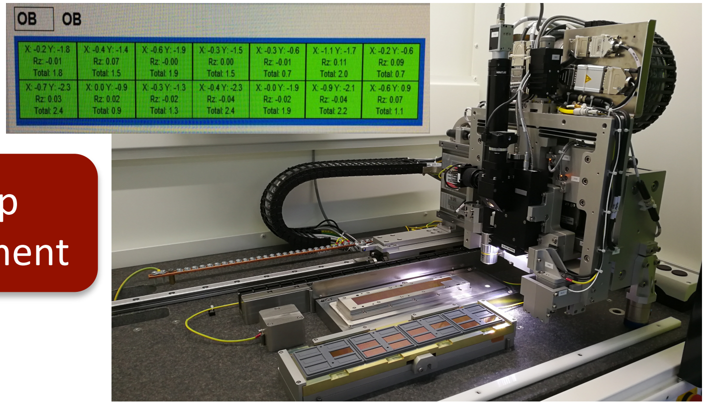


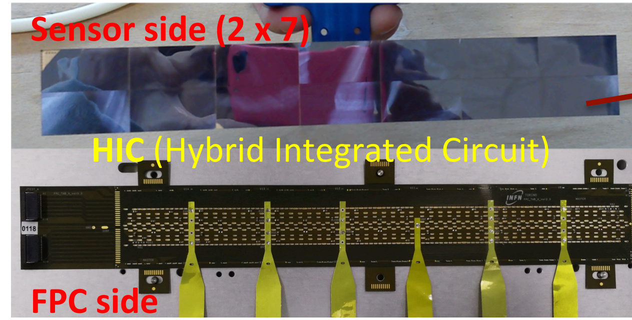
Parameter	Current ITS	ITS Upgrade
N Layers	6 (pxl/drift/strip)	**7 (MAPS)**
Inner Radius	3.9 cm	**2.3 cm**
Layer material (innermost layers)	1.14% X_0	**0.35% X_0**
Spatial resolution	12 x 100 μm^2 35 x 20 μm^2 20 x 830 μm^2	**5 x 5 μm^2**
Max readout rate	1 kHz	**100 kHz (Pb-Pb) 1MHz (pp)**

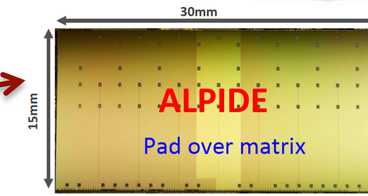
ITS Upgrade in LS2 (ITS2)

Introduction – MAPS at LHC/ALICE Experiment

Chip Alignment





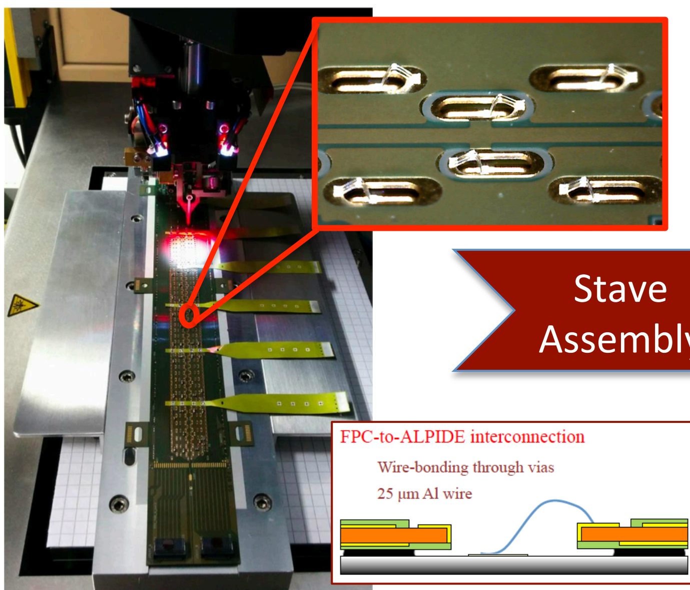


130,000 pixels / cm^2 27x29x25 μm^3

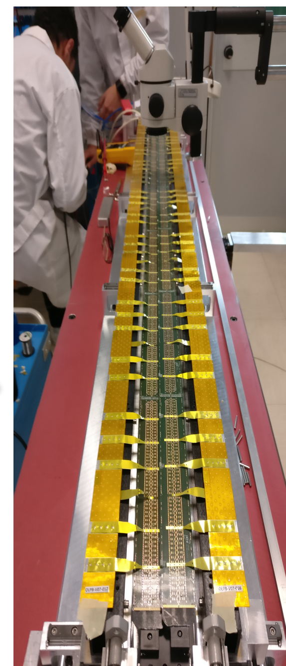
charge collection time <30ns (V_{bb} = -3V)

Max particle rate: 100 MHz/cm^2

Wire Bonding



Stave Assembly

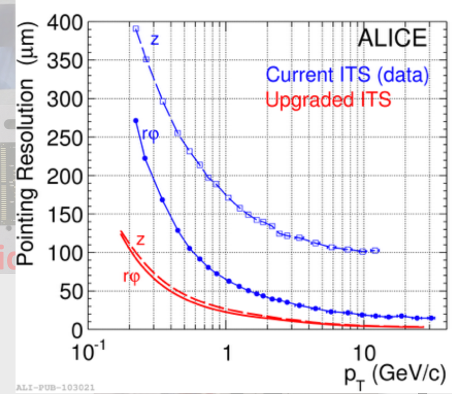


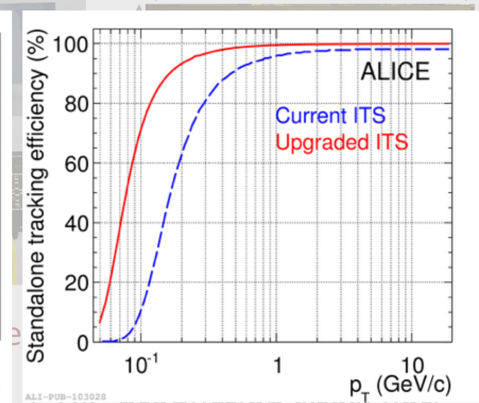
Outer Barrel HIC/Stave Production:

- 5 HIC production sites: Bari, Liverpool, Strasbourg, Wuhan (CCNU), Pusan/Inha
- HIC Production ended in June 2019, and cumulative yield ~ 85% (2580 HICs)
- 5 stave production sites: Berkeley, Daresbury, Frascati, Nikhef, Torino
- Stave Production will end in August 2019, and cumulative yield ~ 90%

Introduction – MAPS at LHC/ALICE Experiment

Last HIC shipment to Europe, CCNU clean room, June 2019





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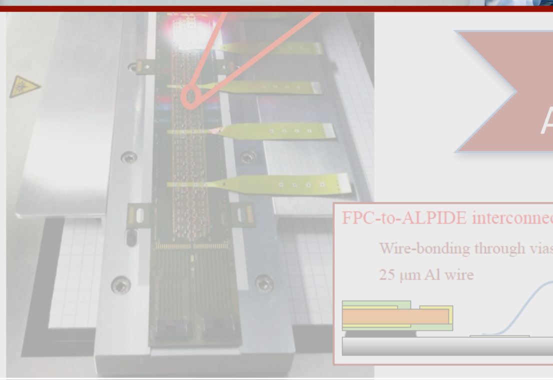
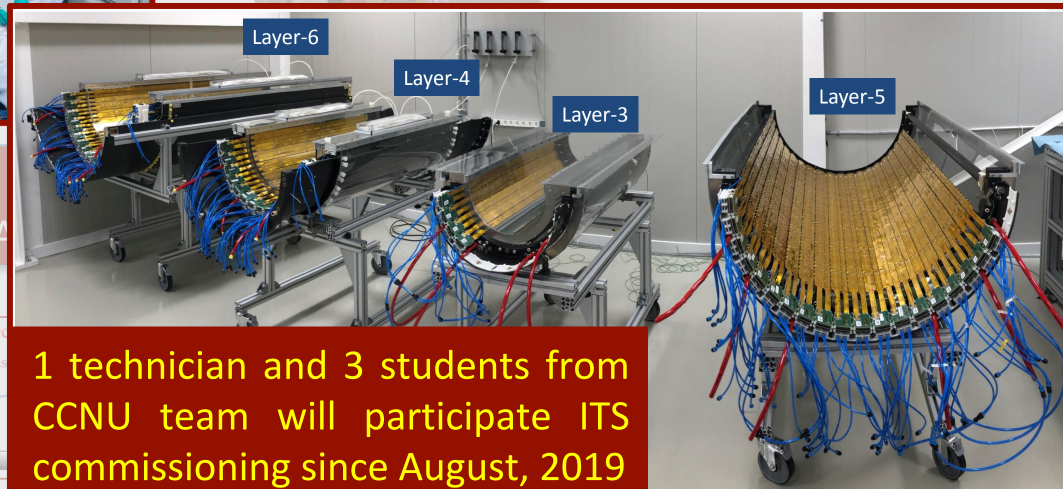
Wire Bonding



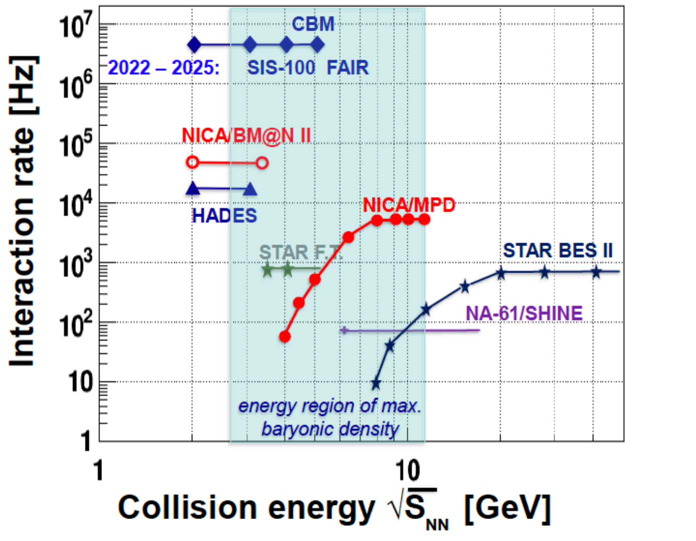


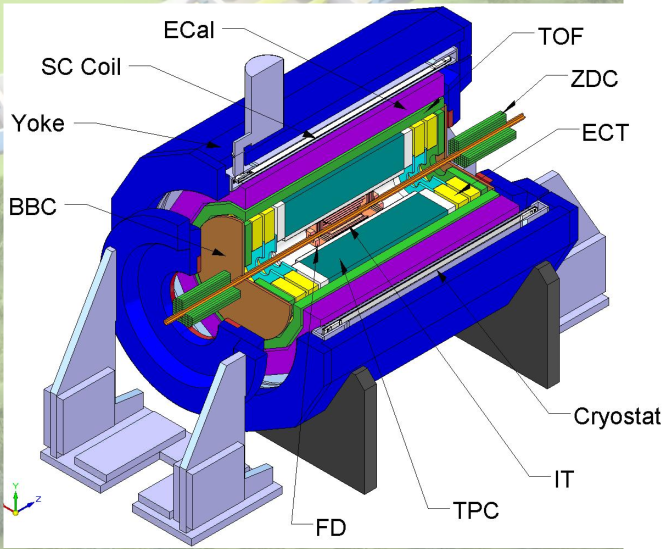
1 technician and 3 students from CCNU team will participate ITS commissioning since August, 2019

Introduction – NICA/MPD

Main targets:

- ***study of hot and dense baryonic matter at the energy range of max net baryonic density***
- ***construction of collider to collide***
  - ✓ ***relativistic ions from p to Au at energy range $\sqrt{S_{NN}}$= 4 - 11 GeV***
  - ✓ ***polarized p and d at energy up to $\sqrt{S}$ =27 GeV (p)***





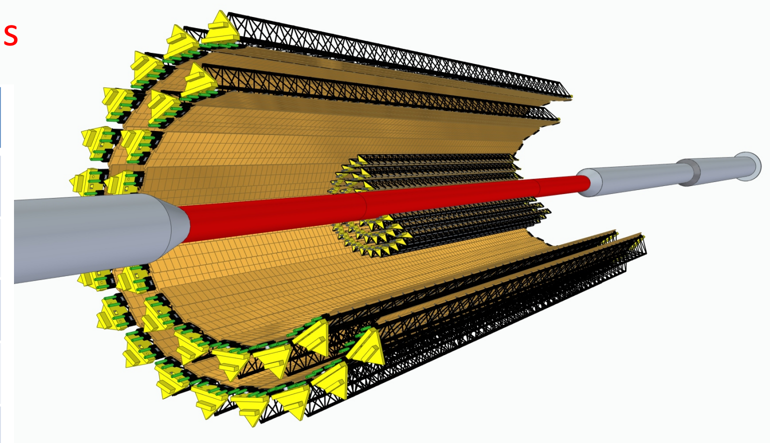
MAPS-based Inner Tracker (IT) for the NICA/MPD

The MAPS-based IT detector will enable charm-hadron measurement and isolate collision vertex at high luminosity environment for the MPD experiments:

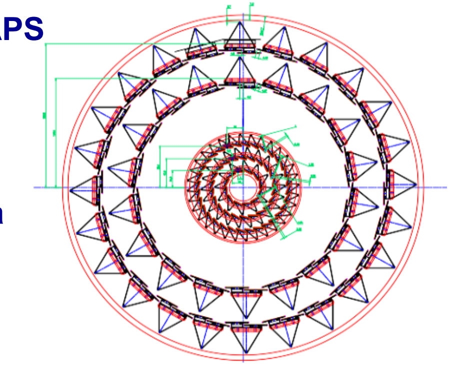
- ✓ Charm production in heavy ion collisions at the NICA energies
- ✓ Clean measurement of (multi-)strange hadron productions

	Inner Barrel[a]			Outer Barrel	
	Layer0	Layer1	Layer2	Layer3	Layer4
R_{min} (mm)	22.4	40.7	59.8	145.8	194.4
R_{max} (mm)	26.7	45.9	65.1	147.9	197.6
Length (mm)	542[a]	542[a]	542[a]	1468	1468
Pseudo-rapidity	±3.1	±2.5	±2.2	±2.3	±2.0
Nr. Of pixel chips (chips per stave x stave)	18 x 12	18 x 22	18 x 32	196 x 18	196 x 24
Active area (cm^2) (2mm dead area in r-phi)	842	1546	2246	13758	18345

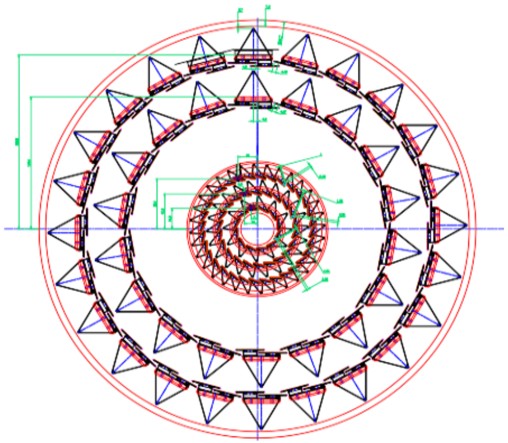
a) ALPIDE-based IB layers will depend on the beam pipe upgrade from 64 mm to 38 mm in diameter after 2023.

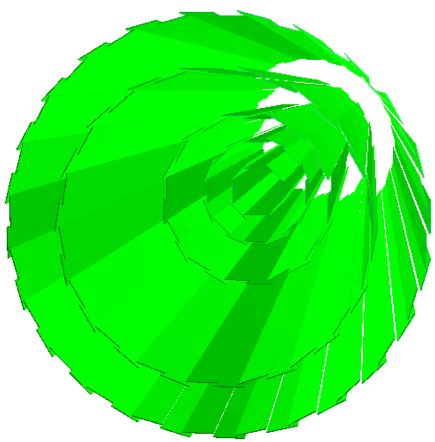


- **9420 ALPIDE MAPS**
- **5** cylinder layers
- **2** barrels (IB, OB)
- 4.9 x 10^9 pixels,
- 3.6 m^2 active area
- $|\eta| \leq 2.0$

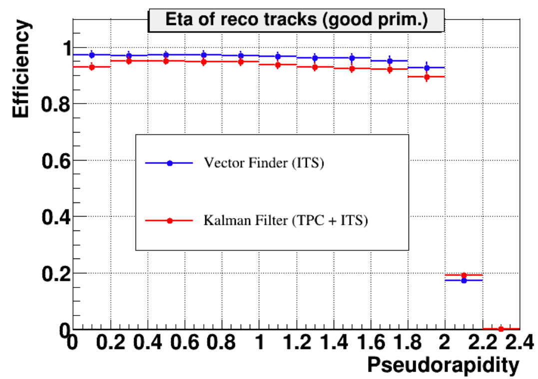


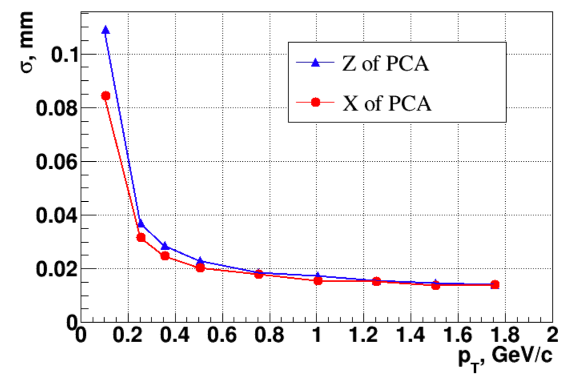
MAPS-based Inner Tracker (IT) for the NICA/MPD

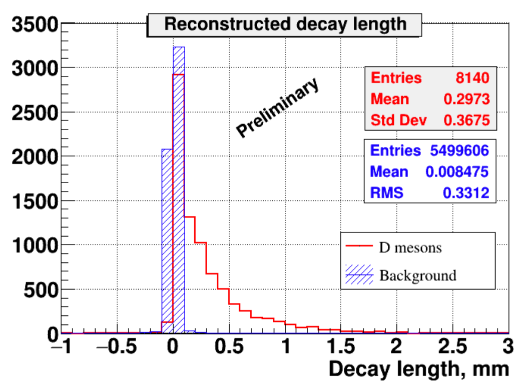


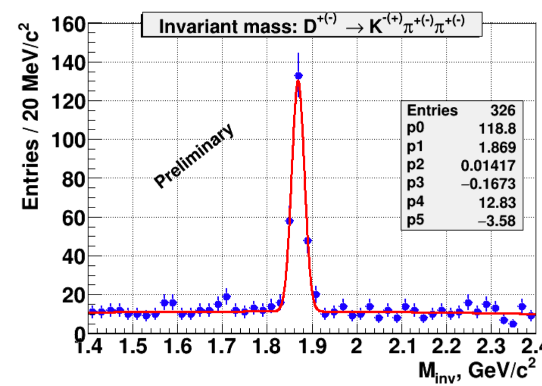


✧ Possible geometry of the MPD/IT from Y. Murin (LHEP JINR) and V. Kondrat'ev (SPbU).









Reference: A.Zinchenko, "*Event reconstruction at MPD: current status*", MPD collaboration meeting, 16 April 2019

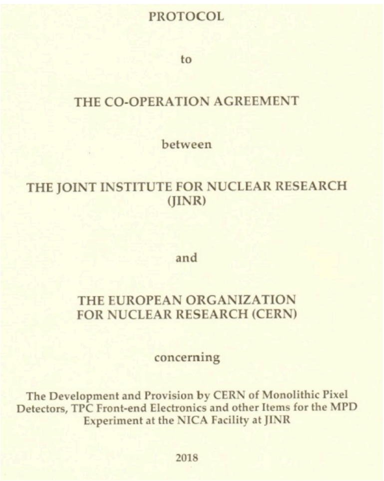
MAPS-based Inner Tracker (IT) for the NICA/MPD

MPD-ITS (OB) is now recognized at Stage I

Stage I: **TPC, TOF, ECAL, ZDC, FFD + ITS (OB)**

Stage II : **ITS (IB) + EndCap (CPC, Straw, TOF, ECAL)**

✓ Transfer of High Tech Instrumentation Know-How from CERN to NICA-MPD



PROTOCOL

to

THE CO-OPERATION AGREEMENT

between

THE JOINT INSTITUTE FOR NUCLEAR RESEARCH
(JINR)

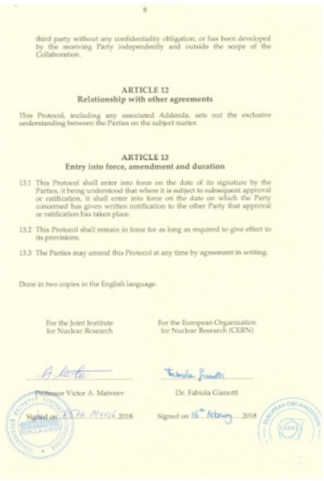
and

THE EUROPEAN ORGANIZATION
FOR NUCLEAR RESEARCH (CERN)

concerning

The Development and Provision by CERN of Monolithic Pixel Detectors, TPC Front-end Electronics and other Items for the MPD Experiment at the NICA Facility at JINR

2018



8

third party without any confidentiality obligation; or has been developed by the receiving Party independently and outside the scope of the Collaboration.

ARTICLE 12
Relationship with other agreements

This Protocol, including any associated Addenda, sets out the exclusive understanding between the Parties on the subject matter.

ARTICLE 13
Entry into force, amendment and duration

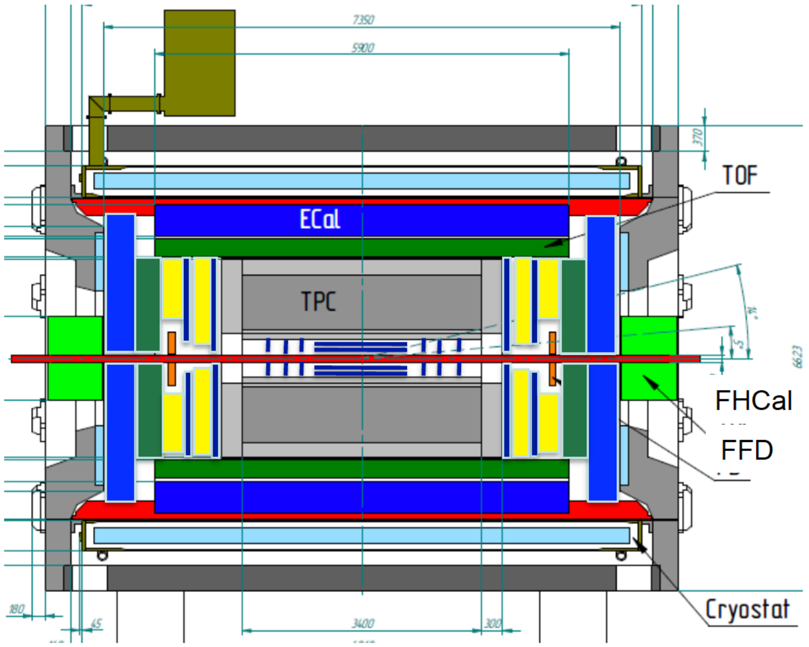
13.1 This Protocol shall enter into force on the date of its signature by the Parties, it being understood that where it is subject to subsequent approval or ratification, it shall enter into force on the date on which the Party concerned has given written notification to the other Party that approval or ratification has taken place.

13.2 This Protocol shall remain in force for as long as required to give effect to its provisions.

13.3 The Parties may amend this Protocol at any time by agreement in writing.

Done in two copies in the English language.

For the Joint Institute for Nuclear Research	For the European Organization for Nuclear Research (CERN)
Professor Victor A. Matveev	Dr. Fabiola Gianotti
Signed on 15th March 2018	Signed on 16th February 2018



Stage I: overall commissioning starts in 2022

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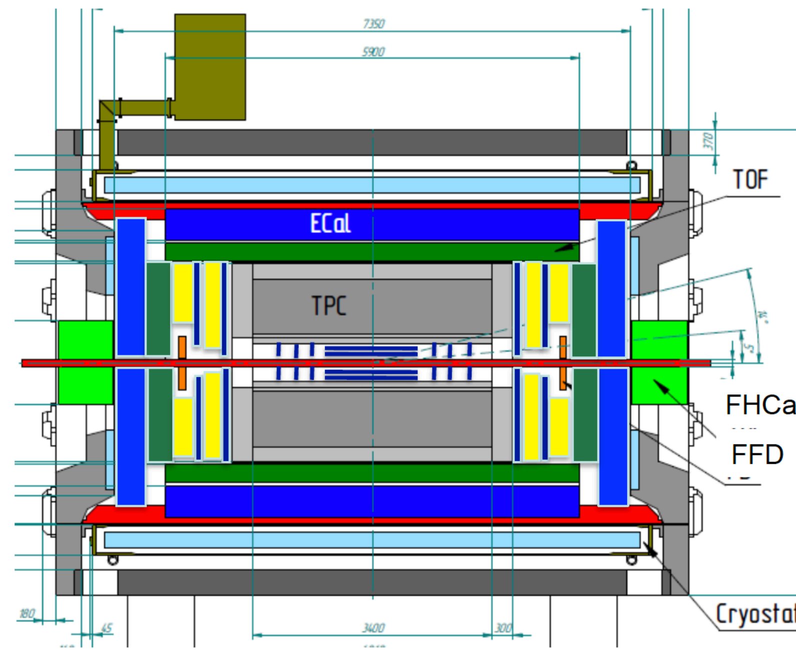
Stage II : **ITS (IB) + EndCap (CPC, Straw, TOF, ECAL)**

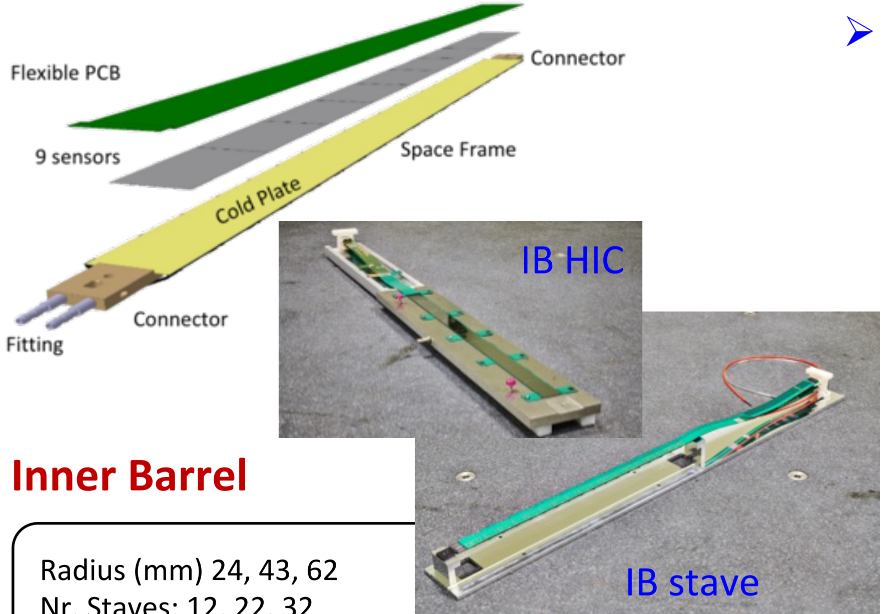
✓ Transfer of High Tech Instrumentation Know-How from CERN to NICA-MPD

- 19'000 MAPS ALPIDE for the MPD ITS
- 4'500 SAMPA electronic circuits for the TPC readout
- 5'000 FEAST DC/DC converters for the ECAL MPD
- Jigs and fixtures for module and supermodule assembly for the MPD ITS
- Training of personal for assembly and QA certification modules and supermodules of the MPD ITS
- Provision of complete technical and commercial information on parts of the new ALICE Inner Tracking System, including drawings, internal technical reports, quotes, etc.



Stage I: overall commissioning starts in 2022

R&D for the Inner Barrel



Inner Barrel

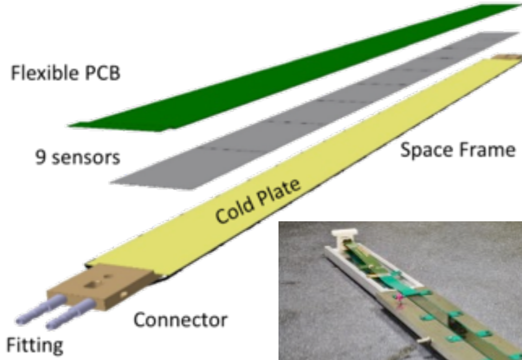
Radius (mm) 24, 43, 62
Nr. Staves: 12, 22, 32
Nr. Chips/ layer: 216, 396, 576

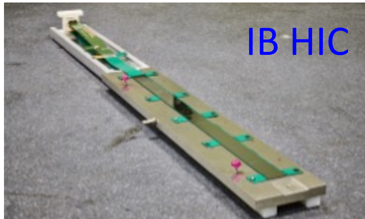
Length in z (mm): 542 mm
Nr. chips/ Stave: 18
Material thickness: ~0.3% X_0

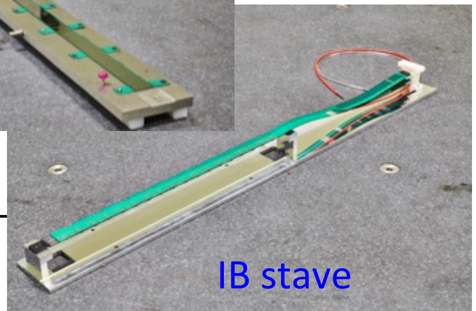
Coolant Single-phase H_2O leak-less
Pixel operational temperature < 30°C
Pixel max temperature non-uniformity < 5°C
Chip Power dissipation < 50mW/cm^2

- **IB HIC/Stave Option A (ALPIDE-based)**
  - 132 working HICs needed to assemble the IB barrel (double length of the IB staves of the ALICE ITS2)
  - 181 assembled HICs assuming a total yield of 73%
  - 200 assembled HICs with 10% spare
  - Target rate: 1 HIC per day per site in average

R&D for the Inner Barrel







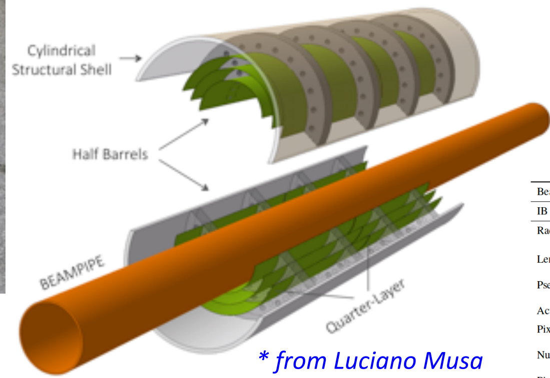
Inner Barrel

Radius (mm) 24, 43, 62
Nr. Staves: 12, 22, 32
Nr. Chips/ layer: 216, 396, 576

Length in z (mm): 542 mm
Nr. chips/ Stave: 18
Material thickness: ~0.3% X_0

Coolant Single-phase H_2O leak-less
Pixel operational temperature < 30°C
Pixel max temperature non-uniformity < 5°C
Chip Power dissipation < 50mW/cm²

- **IB HIC/Stave Option A (ALPIDE-based)**
  - 132 working HICs needed to assemble the IB barrel (double length of the IB staves of the ALICE ITS2)
  - 181 assembled HICs assuming a total yield of 73%
  - 200 assembled HICs with 10% spare
  - Target rate: 1 HIC per day per site in average



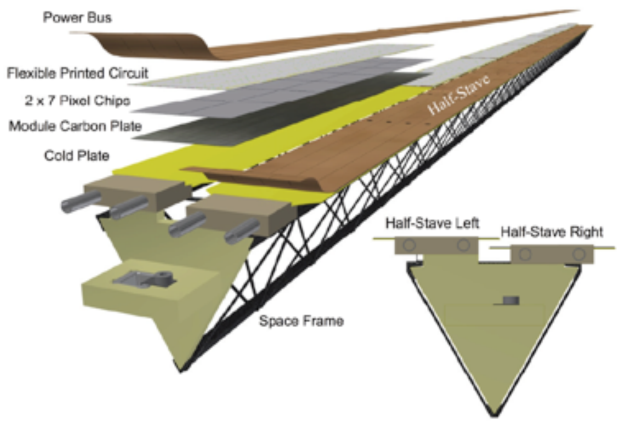
** from Luciano Musa*

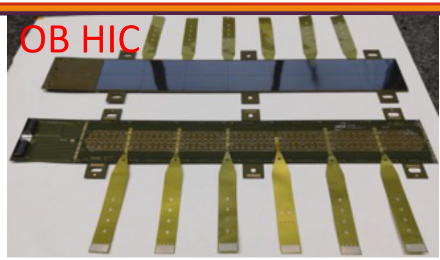
Table 1: Geometrical parameters of the upgraded ITS.

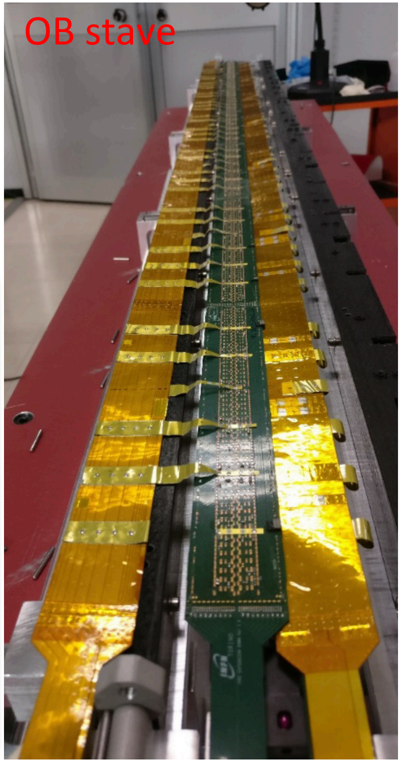
Beam pipe inner/outer radius (mm)	16.0/16.5		
IB Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	270	270	270
Pseudo-rapidity coverage[a]	±2.5	±2.3	±2.0
Active area (cm²)	305	408	508
Pixel sensors dimensions (mm²)	140 × 56.5	140 × 75.5	140 × 94
Number of pixel sensors / layer	4		
Pixel size (μm²)	$O(30 \times 30)$		

- **IB HIC/Stave Option B (ALICE ITS3 upgrade plan)**
  - Wafer-scale ultra-thin pixel sensor with spatial resolution better than 3 μm and a time resolution of the order of 200 ns
  - Assembly strategy not defined yet
  - R & D plan and technical parameters will be introduced in Xiangming's talk.

The Outer Barrel Construction







Outer Barrel

Radius (mm) 147, 196
Nr. Staves: 18, 24
Nr. Chips/ HIC module: 2x7

Length in z (mm): 1468
Nr. HIC module/ Stave: 7
Material thickness: ~0.8% X_0

Coolant Single-phase H_2O leak-less
Pixel operational temperature < 30°C
Pixel max temperature non-uniformity < 5°C
Chip Power dissipation < 40 mW/cm^2

- **OB HIC Production**
  - 588 working HICs needed to assemble the OB barrel
  - 784 assembled HICs assuming a total yield of 75%
  - 980 assembled HICs with 20% spare
  - Target production rate: 2~3 HICs per day per site in average

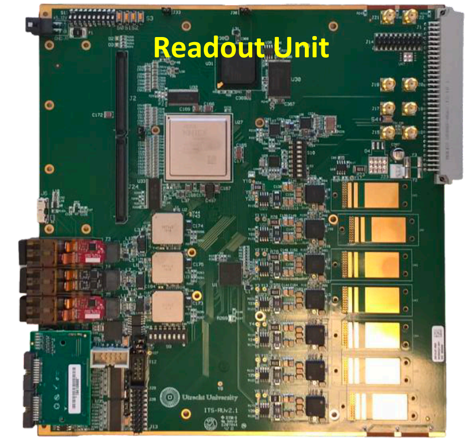
  ~1 year needed for HIC mass production by 2 construction sites

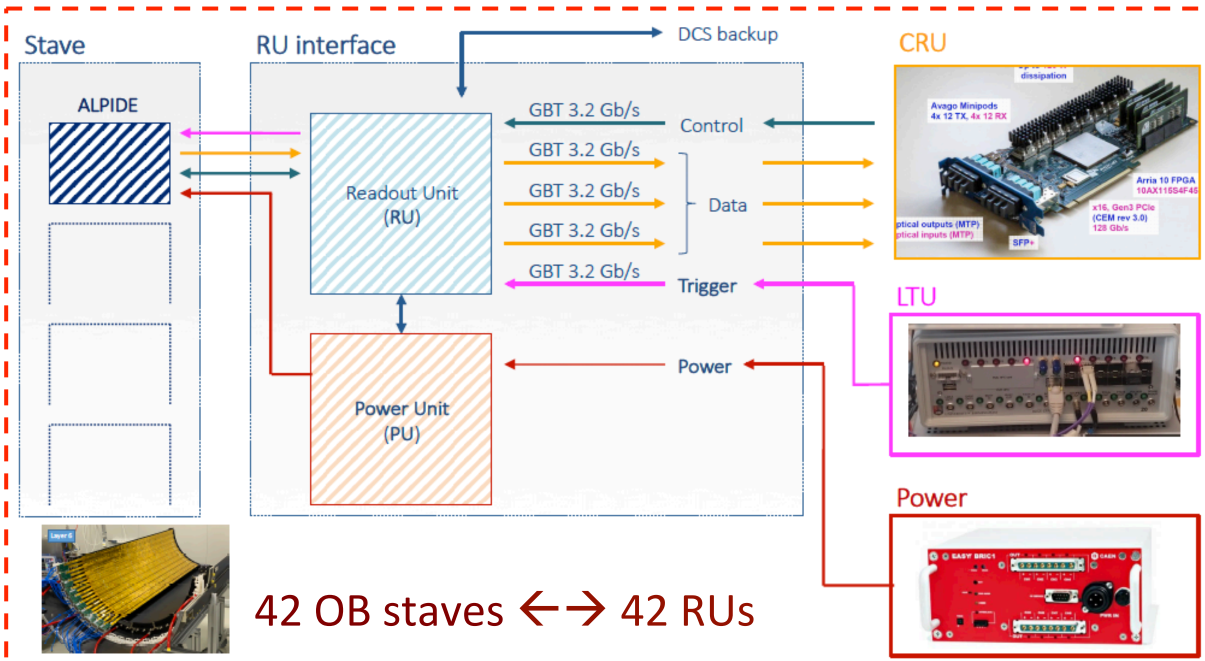
- **OB Stave Production**
  - 84 working half staves (HS) needed to assemble OB barrel
  - 100 assembled HSs (take into account spare and stave yield)
  - Target rate: 1 HS per week per site in average

  ~1.5 year needed for stave mass production by 2 construction sites

Readout Electronics

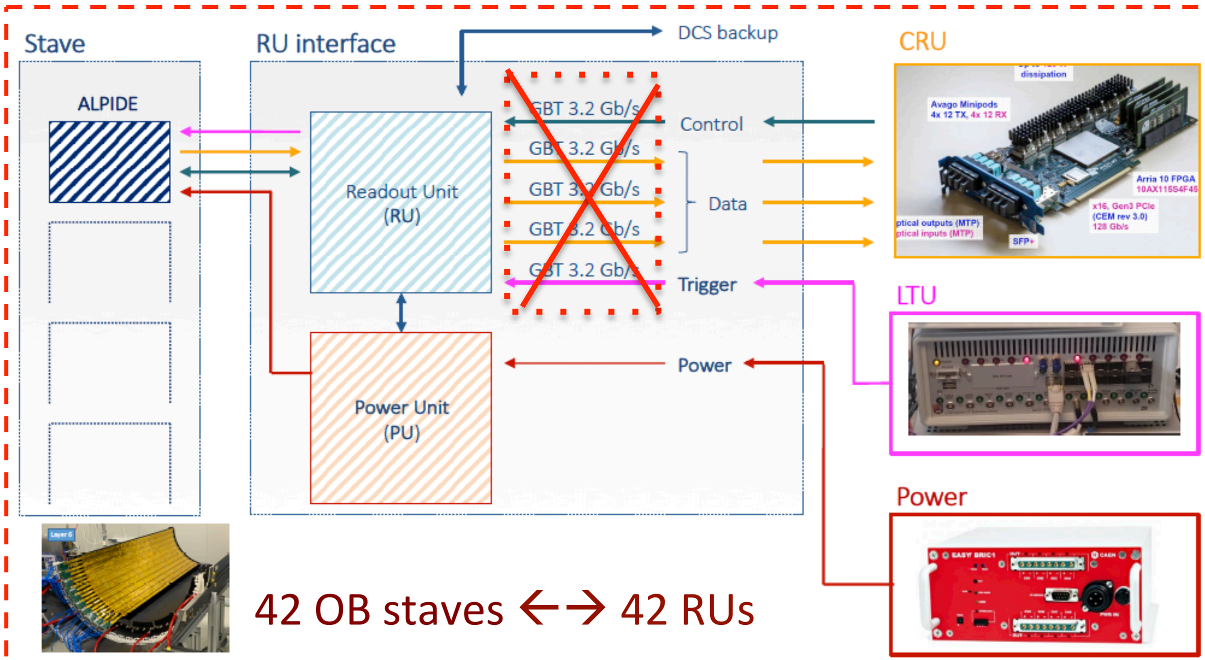
- Readout electronics divided into modular Readout Units (RU), identical for each layer
- Each RU controls an entire stave, including the distribution of power to the sensors
- The CRU interfaces with the RU only, which in turn manages the trigger and the power for the stave.

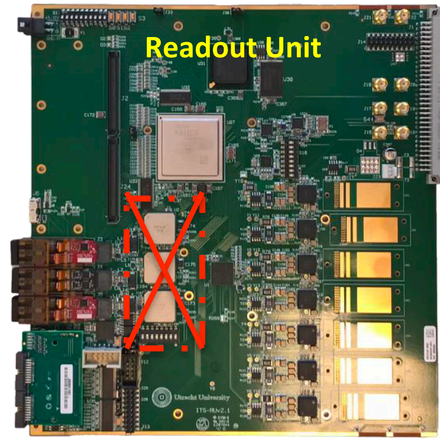


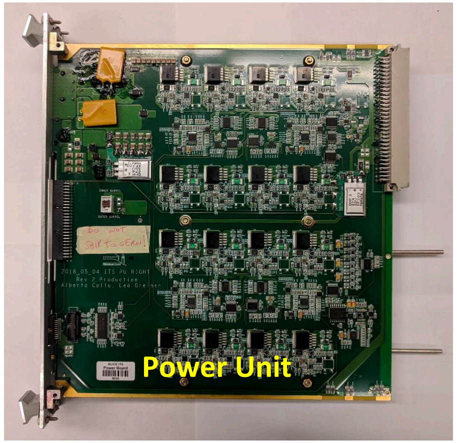


Readout Electronics

- Readout electronics divided into modular Readout Units (RU), identical for each layer
- Each RU controls an entire stave, including the distribution of power to the sensors
- The CRU interfaces with the RU only, which in turn manages the trigger and the power for the stave.
- All the RU modifications to avoid GBTx chips, produced by ourselves
- The Power Units can be purchase from LBNL directly. Again an alternative, Luciano Musa confirmed that they can provide all executive manufacturing drawings to China and the production is done in China.







Testing and Simulation

- Chip testing for wafer-scale MAPS chips
- Qualification and endurance testing software maintenance for HICs and staves
- Database maintenance and management for shipment, assembly and test (CERN or Dubna?)
- Commissioning and offline/online software

- Detector performance simulation with IT geometries for TDR preparation, which has been started by Russian team within MPDROOT framework, but more detailed work need to do:
  - ✓ 2 ALPIDE-based OB layer
  - ✓ 2 ALPIDE-based OB layer + 3 ALPIDE-based IB layer
  - ✓ 2 ALPIDE-based OB layer + 3 wafer-scale pixel chip IB layer
- Physics performance simulation with IT and TPC on charm & strangeness production
- …

Organization and Plan

Involved Institutions:

China side:

- Central China Normal University (CCNU)
- China Three Gorges University (CTGU)
- Institute of Modern Physics (IMP/CAS)
- University of Chinese Academy Sciences (UCAS)
- University of Science and Technology of China (USTC)

Russian side:

- Joint Institute of Nuclear Research (JINR)
- Moscow State University (MSU)
- Saint-Petersburg State University (SPbU)

Technical goals:

1) master techniques for design & production of the state-of-the-art MAPS technology
2) master techniques for constructing the high-tech vertex detector within China
3) master the necessary techniques for operation of the vertex detector including calibration, daily running and maintenance

Organization and Plan

经费预算及依据：

此项目由中国和俄罗斯合作，等额出资 (~8M USD)。

中方承担的主要任务列明如下：

- ✓ 内三层基于MAPS技术的新型大尺寸超低物质量超低功耗高速硅像素芯片研发及其探测器原型样机；
- ✓ 基于ALPIDE硅像素芯片的外两层探测器建造与测试、集成与试运行、物理模拟研究与实验研究等；
- ✓ 高速稳定数据传输和处理的系统读出电子学研发、生产与测试等；

Summary and Outlook

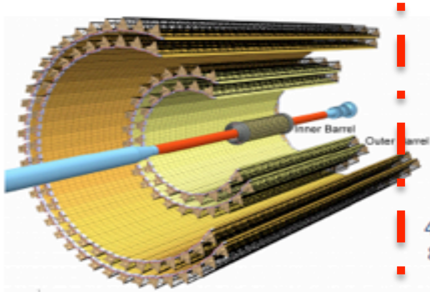
- MAPS-based Inner Tracker has been proposed to be constructed for the NICA/MPD, and it's scheduled to install 2 outer-layers in Stage 1 (before 2023).
- R&D on wafer-scale MAPS chip will be started for the IB layers of MPD/IT.
- Technician training with the support of ALICE ITS upgrade project have been discussed:
  - ✓ Luciano Musa confirmed to provide training sessions (trainers from European side) on the stave assembly for China teams
- Facilities of CCNU team are ready to transfer to MPD/IT project (the HIC production has been done in June for the ALICE ITS upgrade); And the infrastructure for IT assembly/testing at IMP/CAS is under preparation.
- Detector & physics performance simulation will be started with Russian team for the IT TDR preparation.

NICA/MPD
(Au+Au @ 11 GeV)

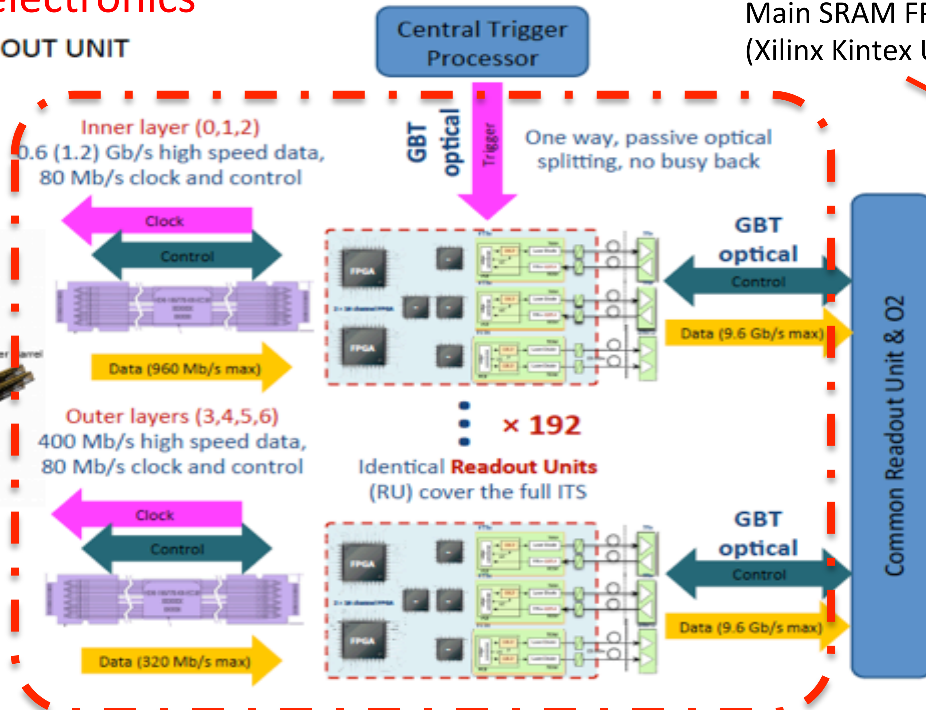
Thanks for your attention!

ALICE ITS2 Readout electronics

Detector Readout → 192 READOUT UNIT

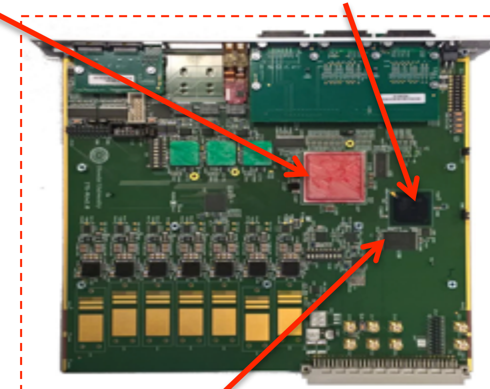


Each Readout Unit is connected to one stave both for Inner and Outer Barrels

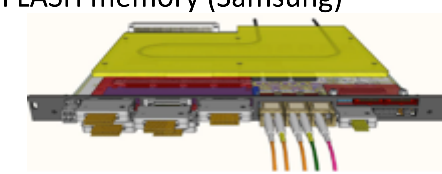


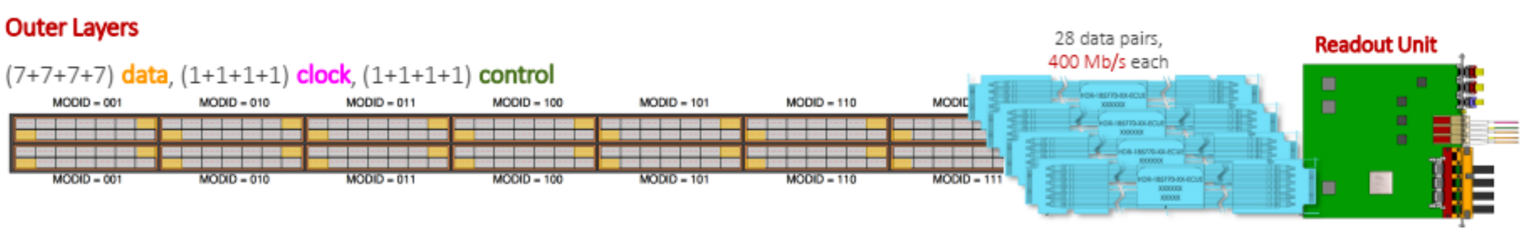
Main SRAM FPGA (Xilinx Kintex Ultrascale)

Secondary FPGA (Microsemi Proasic3)



FLASH memory (Samsung)





HIC Assembly Procedure