Digital design and readout architecture for CEPC Vertex pixel chip

Tianya Wu

On behalf of MOST2 chip design group

twu@ifae.es

15-04-2019

Institut de Física d'Altes Energies

EXCELENCIA SEVERO OCHOA

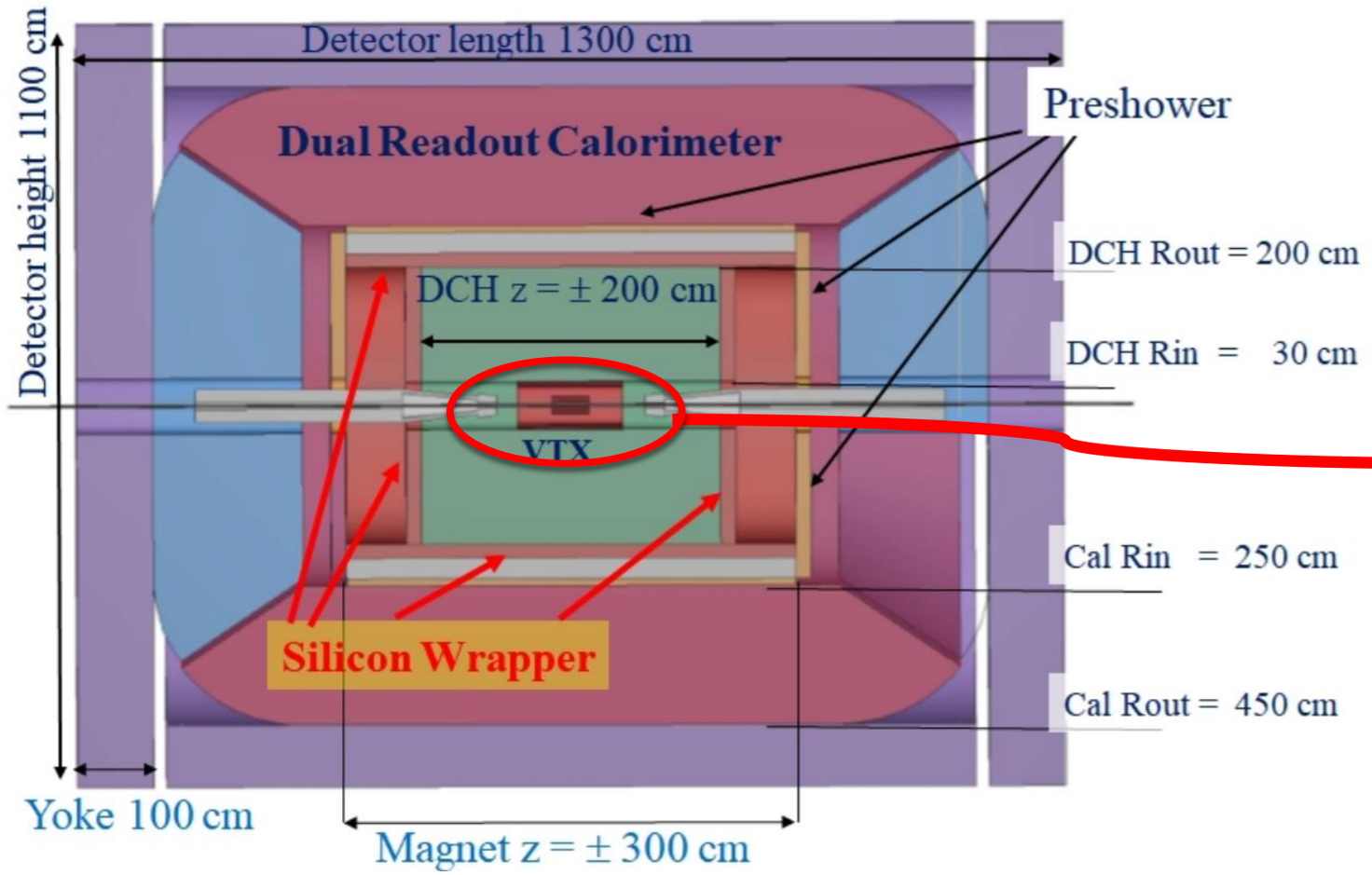
BIST Barcelona Institute of Science and Technology

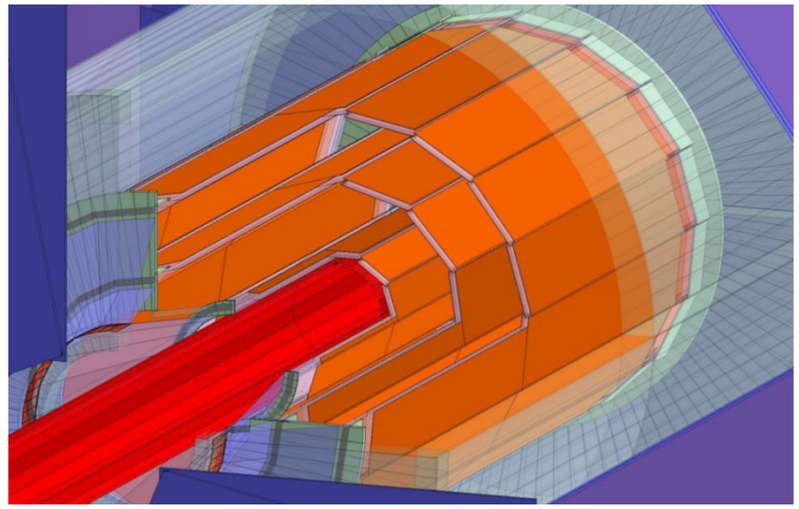
CENTRAL CHINA NORMAL UNIVERSITY

OUTLINE

- Introduction on CEPC Vertex detector
- MOST2 Chip structure
- Analog front end pixel
- Digital pixel logic
- Status of pixel design
- Peripheral readout Architecture
- Summary and Outlook

CEPC vertex detector concept





CEPC VTX Geometry

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ (μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

- Three ladders with double-sided pixels
- Innermost layer σ=2.8 μm

CEPC Vertex detector requirements

First prototype we aim for :

- Ultimate spatial resolution near the interaction point ***3~5 μm***

  --> Prototype with small ***pixel size （25μm x 25μm）***

- Material budget < 0.15% X_0/layer

  --> ***monolithic pixel sensors***

  -->***low power consumption（<50mW/cm2 if air cooling)***

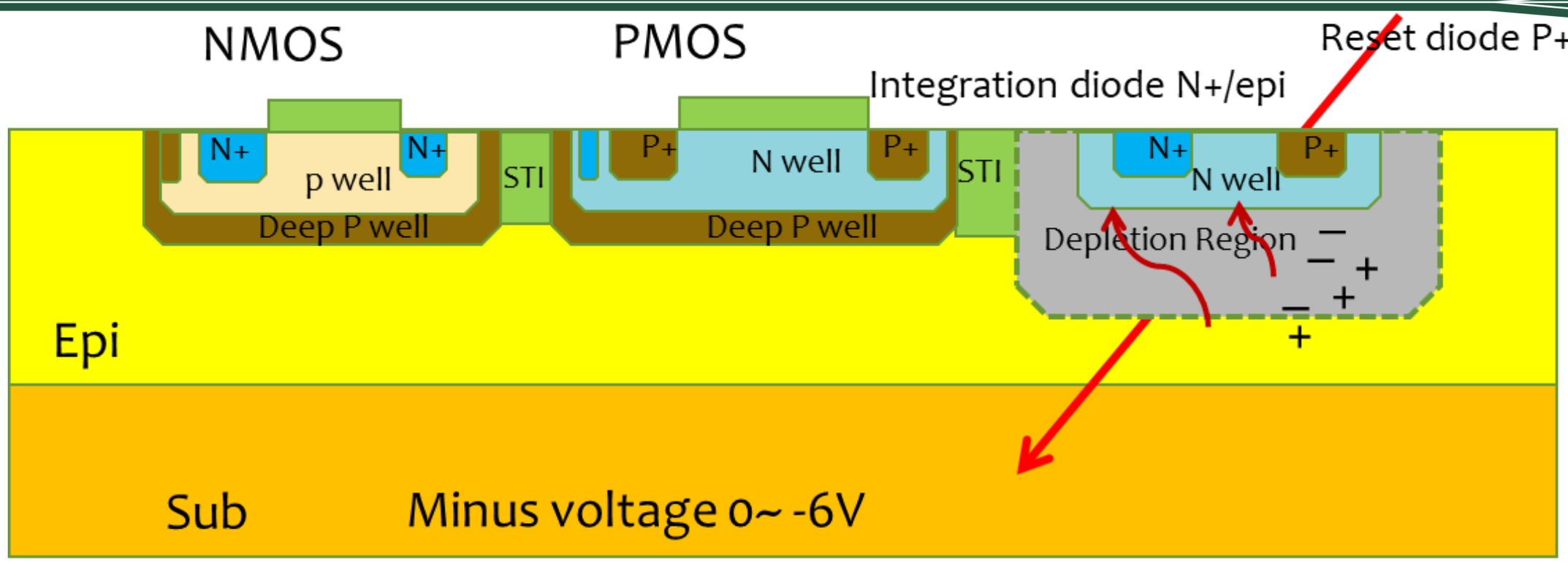
- Bunch spacing： Higgs: 680ns; W: 210ns; Z: 25ns

  --> Edge detection within 25ns

- Radiation tolerance(Pre.) : Total Ionizing dose ~ 1MRad/yr

  Non-ionization energy loss ~ $2x10^{12}$ neq/cm^2/yr

CMOS pixel sensor

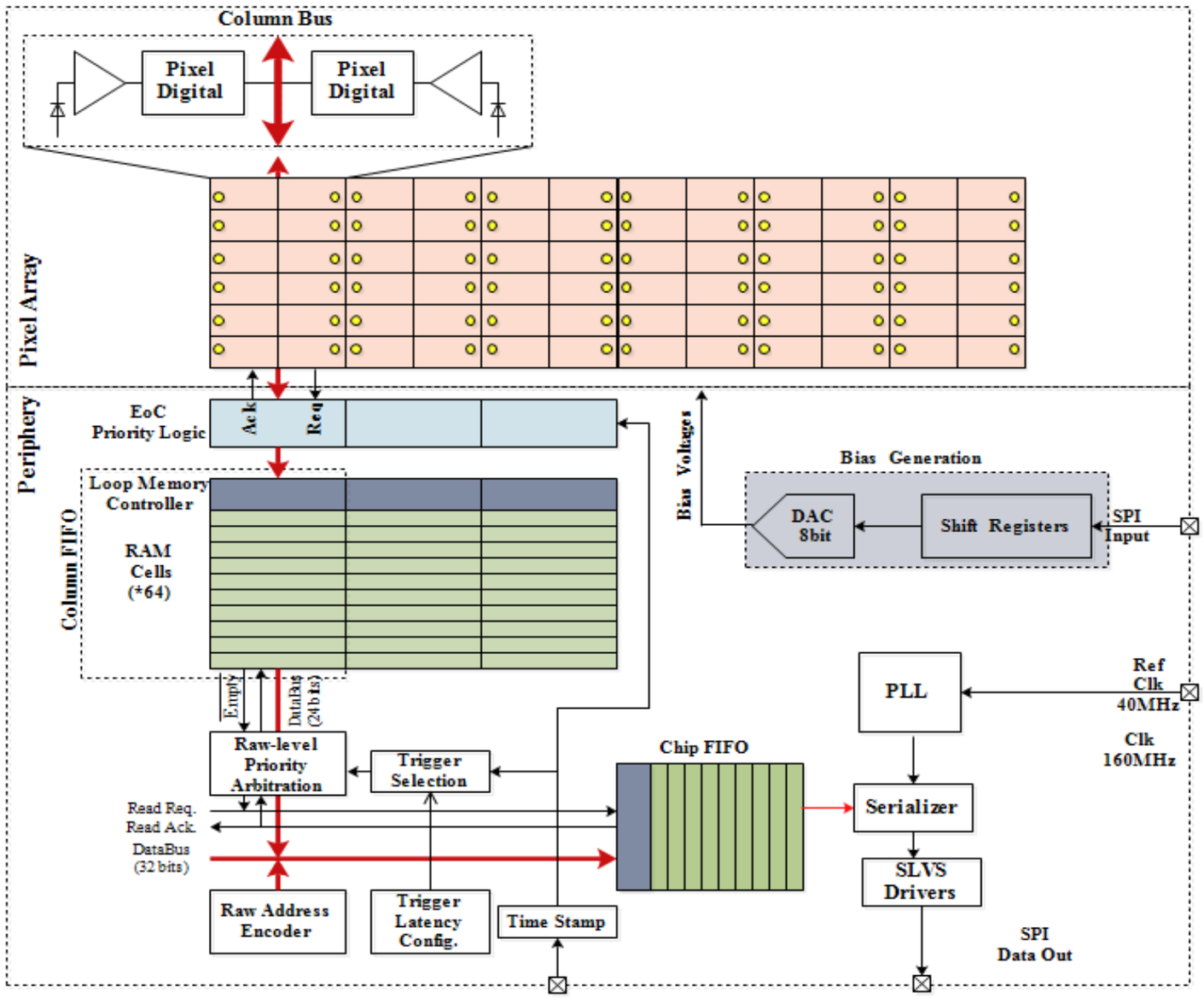


P.Yang et al.
JINST 10 C03030,2015

- Integrated sensor and readout electronics on the same silicon bulk with "standard" CMOS process : low material budget, low power consumption, low cost …
  eg. Ultimate (Mimosa 28) installed for STAR PXL, ALPIDE for ALICE ITS Upgrade

- Selected TowerJazz 0.18 µm CIS technology for CEPC R&D, featuring:
  - Quadruple well process: deep PWELL shields NWELL of PMOS
  - Thick (18-40 µm) and high resistivity (≥1 kΩ•cm) epitaxial layer
  - Thin gate oxide (< 4 nm): robust to total ionizing dose
  - 6 metal layers: increase the area utilization ratio

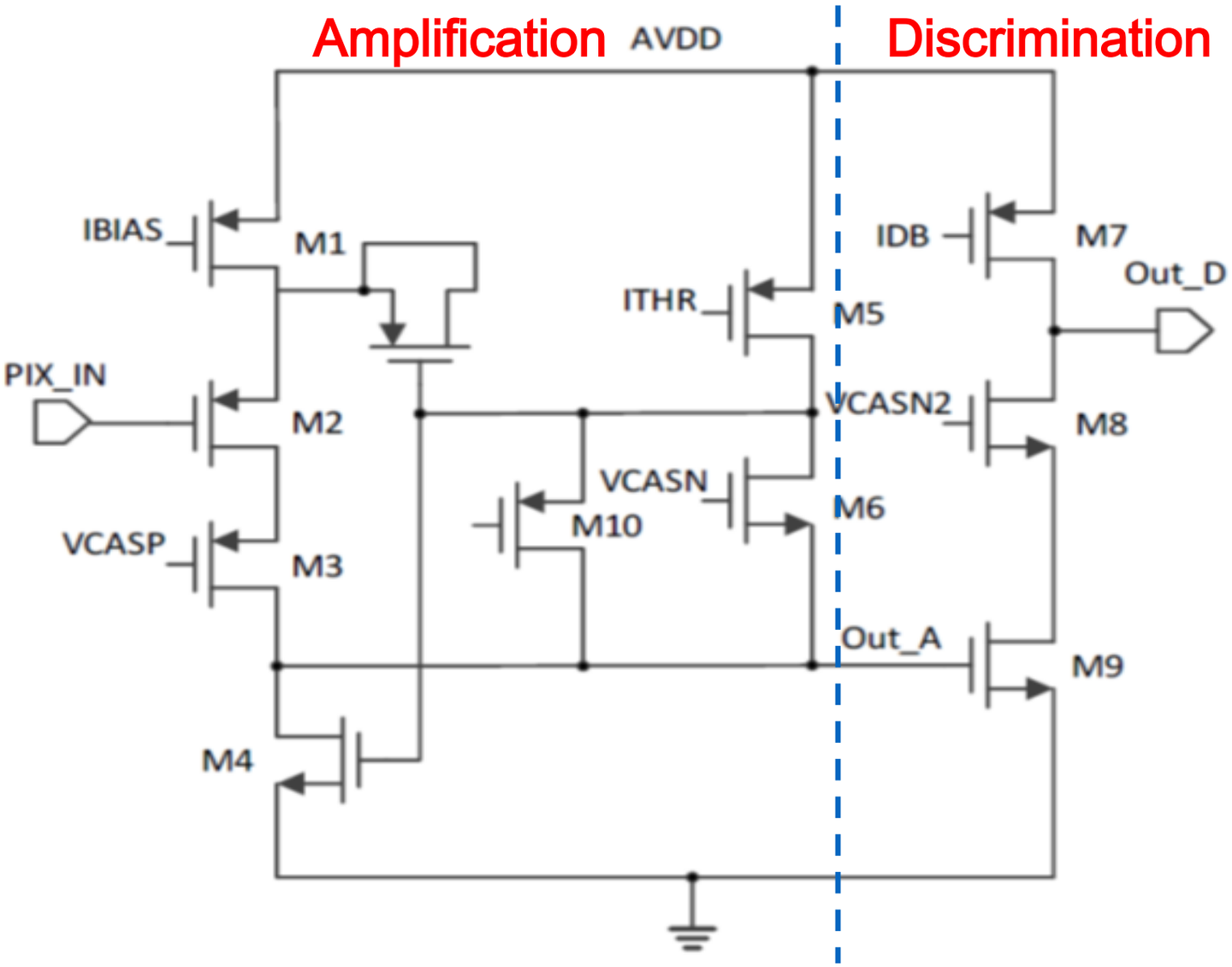
Block diagram of MOST2 chip

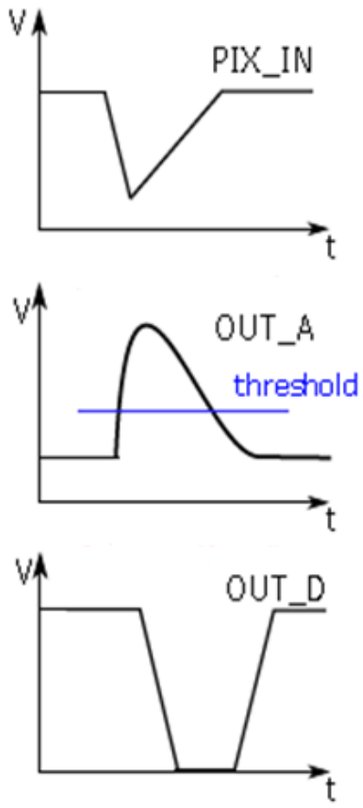


- Similar to the ATLAS pixel readout
- Column-drain readout with priority data
- Time stamp is added at EOC
- Asynchronous data-driven readout prototype
- Dead time is 2 clk for each pixel
- 2-level FIFO architecture

From W. Wei for the group meeting

Analog Front-end



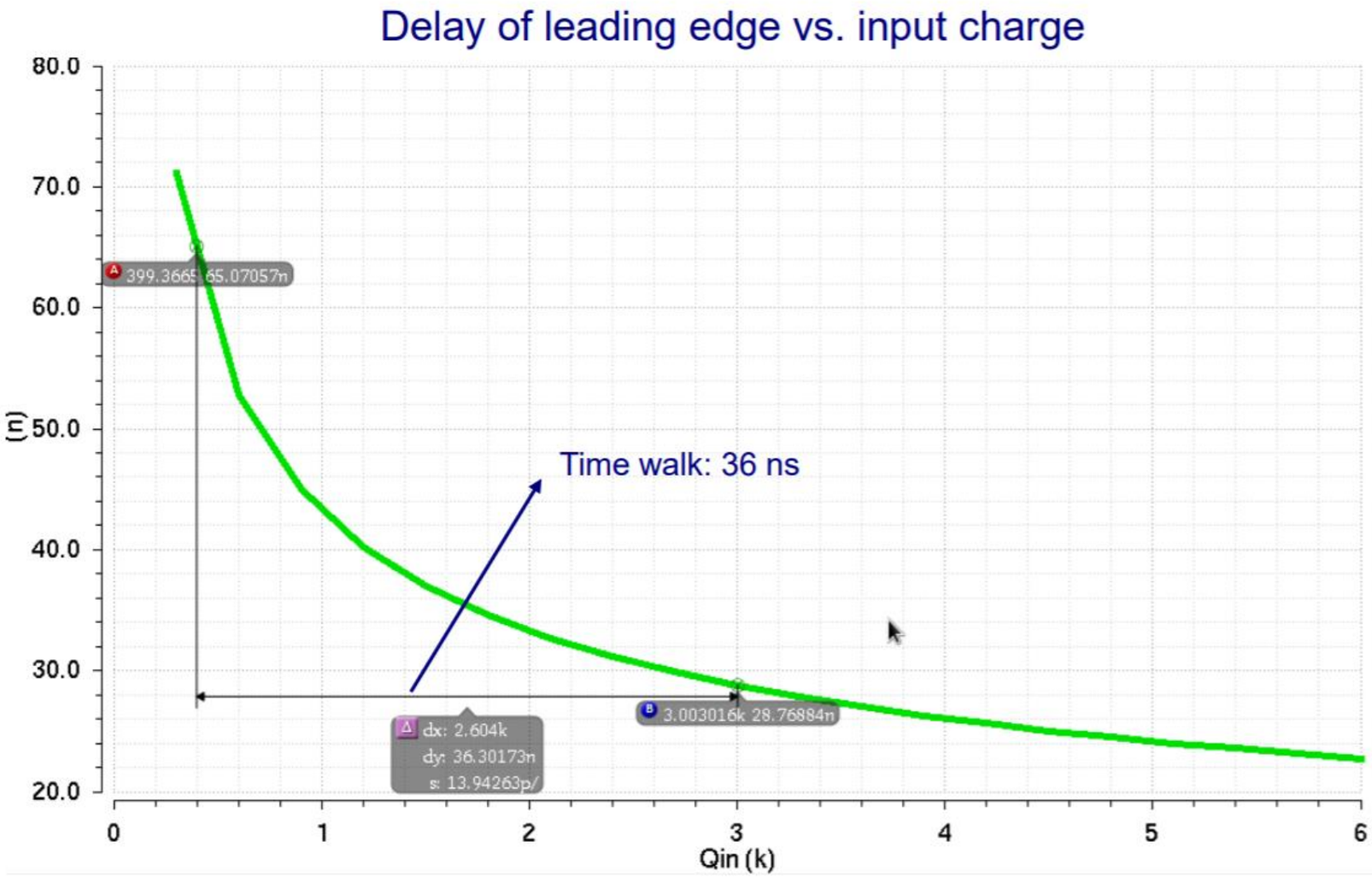


- Peaking time< ?ns
- Duration < ?µs
- Itotal: ? nA
- ENC< ?

- Operating principle derived from ALPIDE front end *D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042*
- M1 acts as a source follower and M2 is a cascode transistor to increase the gain on the output node
- Signal charge creates negative voltage step at input node(PIX_IN)

Front-end simulation

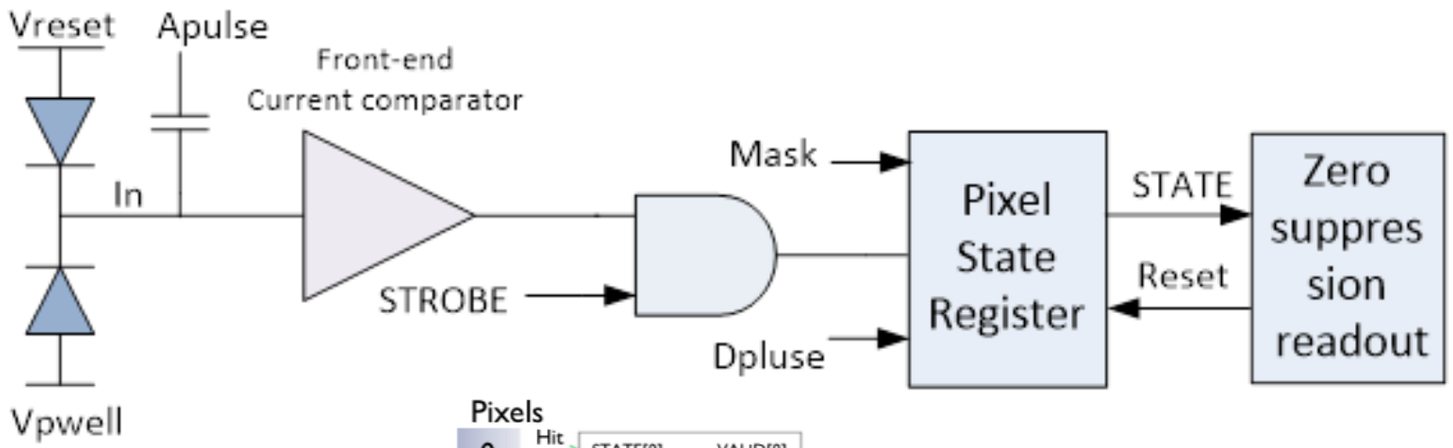
Simulation condition: Cd = 2.5 fF, IBIAS = 440 nA

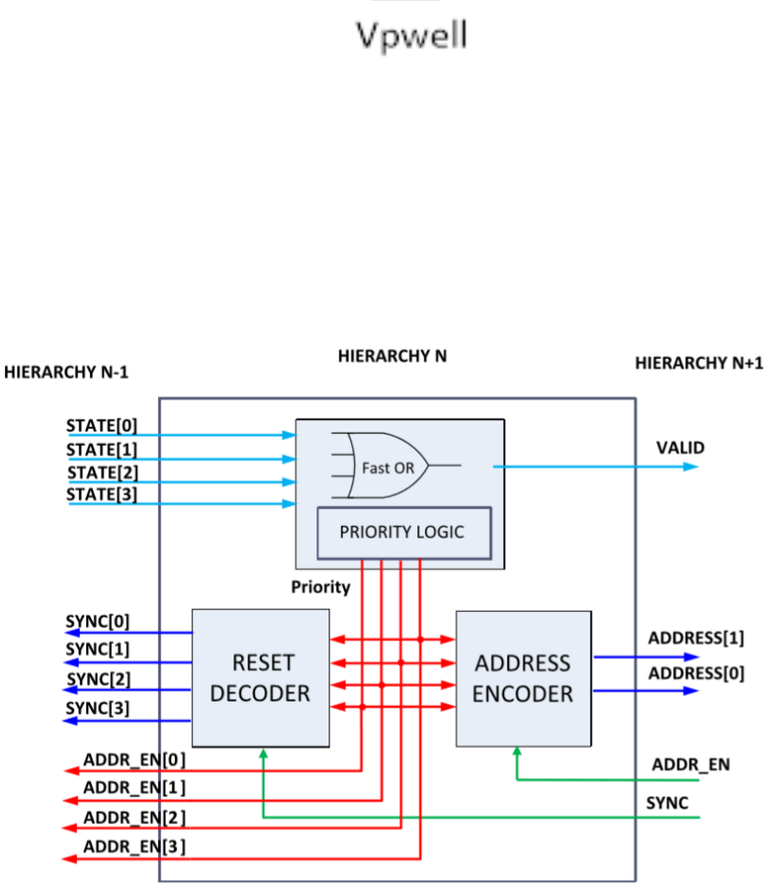


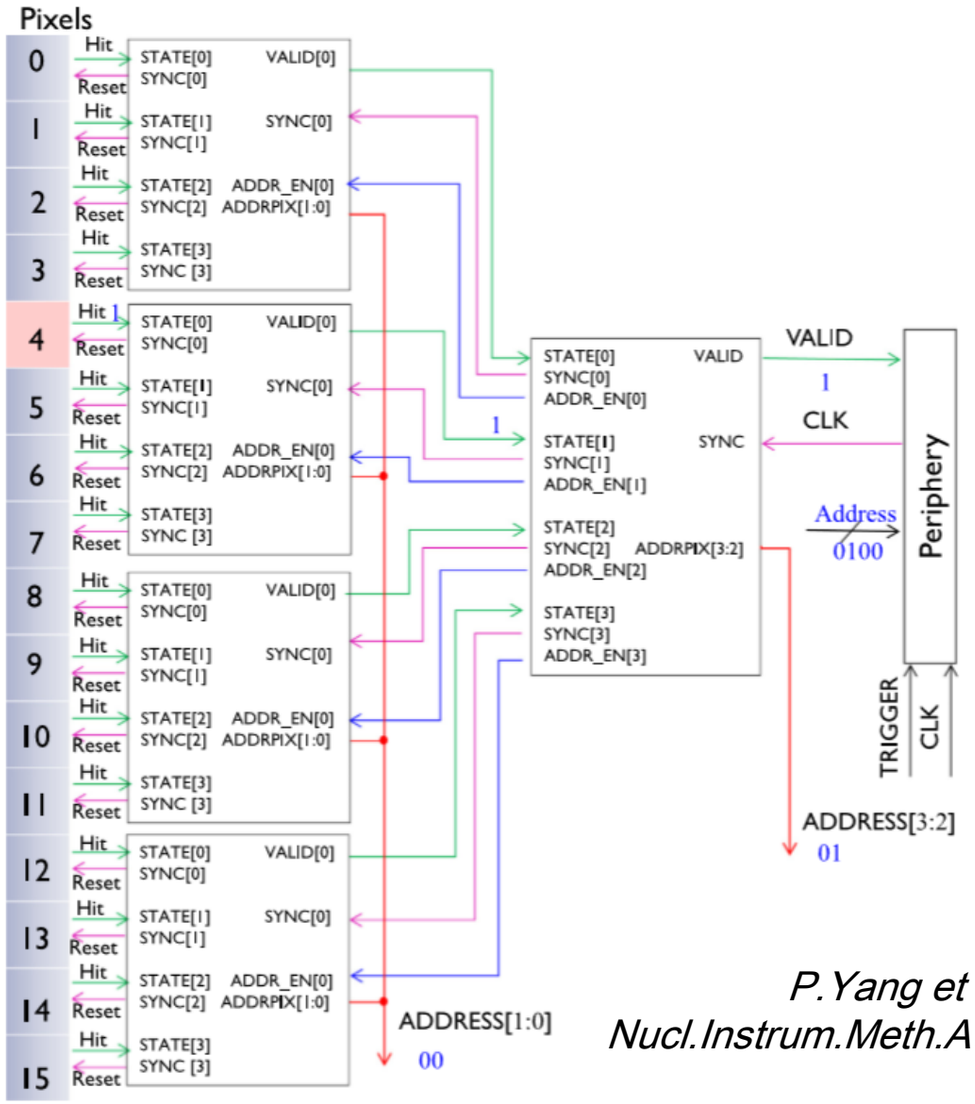
- Simulation: Time walk of 36 ns corresponds to 2600 e-
- Biasing current has to be increased, in order to achieve a peaking time of ~25ns
- Power dissipation increased: bias@440nA with peaking time 29ns, but 138mW/cm^2 for analog

From Y. Zhang for the group meeting

Pixel logic based on ALPIDE



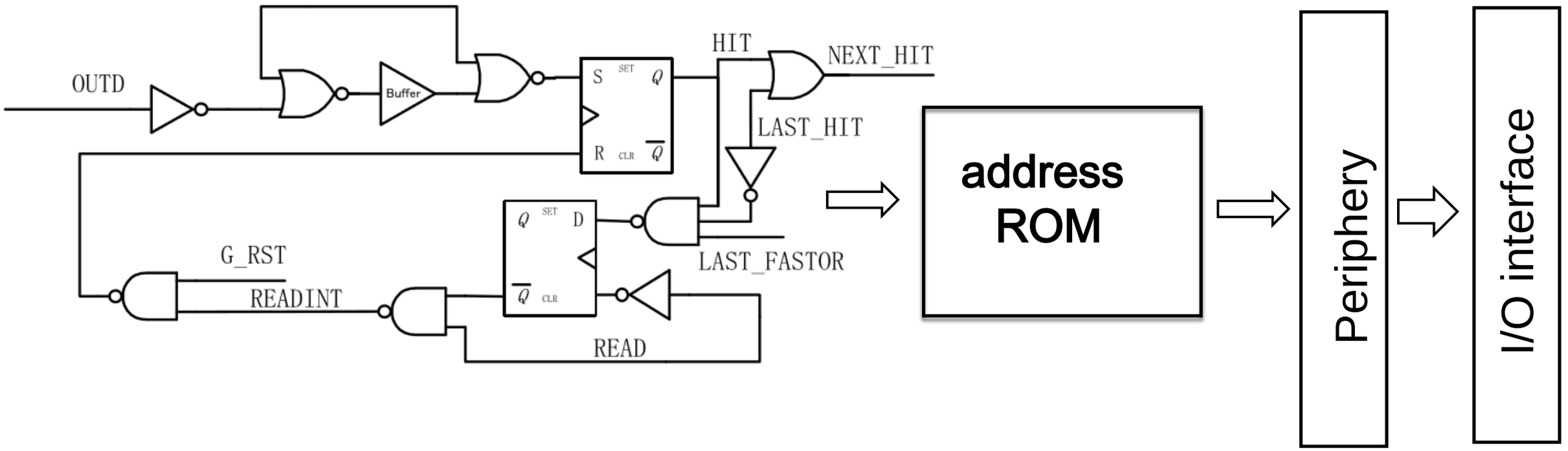




- Boosting speed to run at 40MHz
- Low power consumption

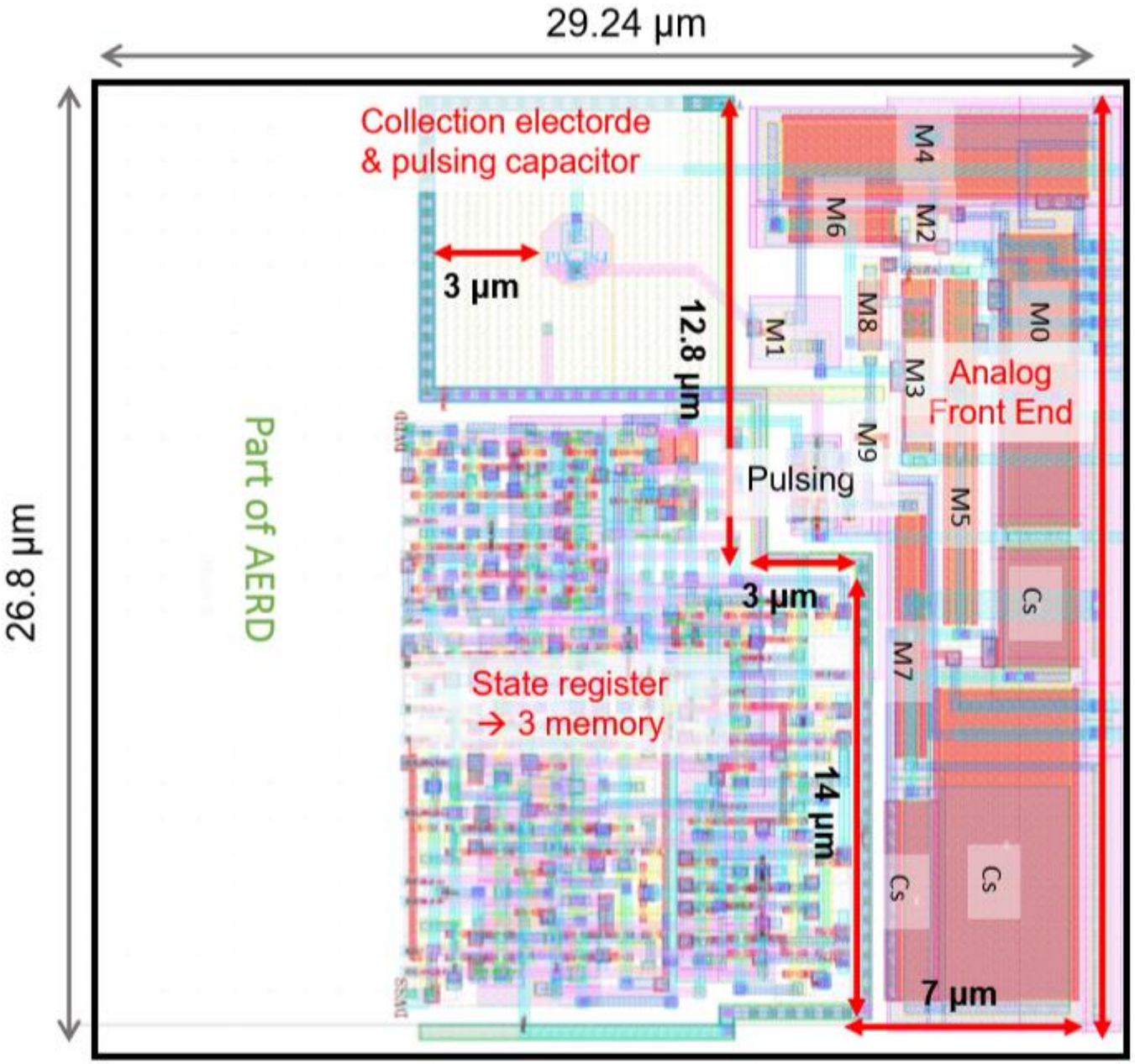
P.Yang et al.
Nucl.Instrum.Meth.A785(2015)61

Pixel logic based on FE-I3



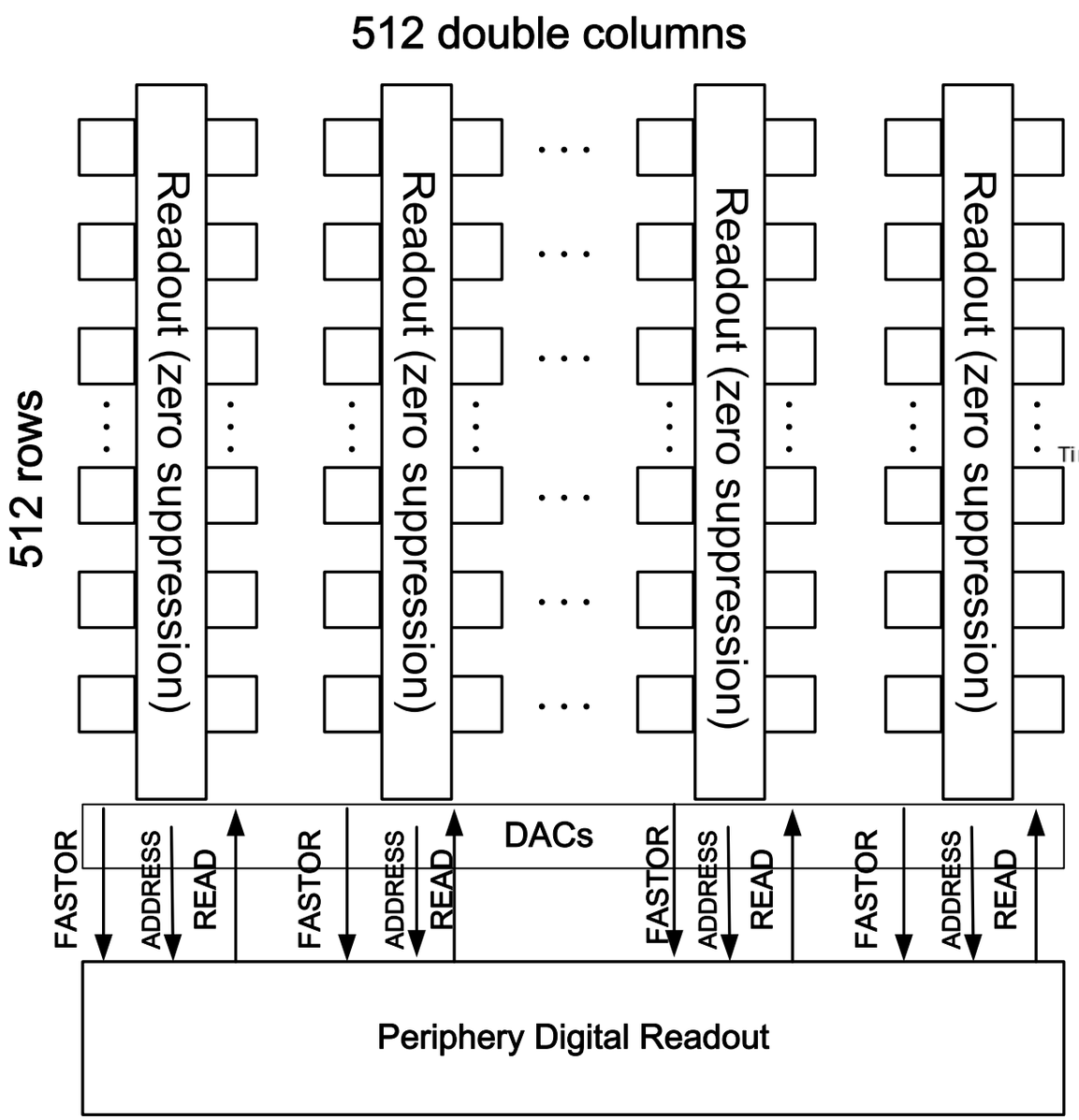
- Column average hit period: 8.3us; cluster size: 3 pixels; clk :40MHz
- More or less FE-I3 like, but simplified
- Priority mask and arbitrary by the busy-bus (fastor)
- Request for 2 latches, One to latch the HIT, one to latch the priority token

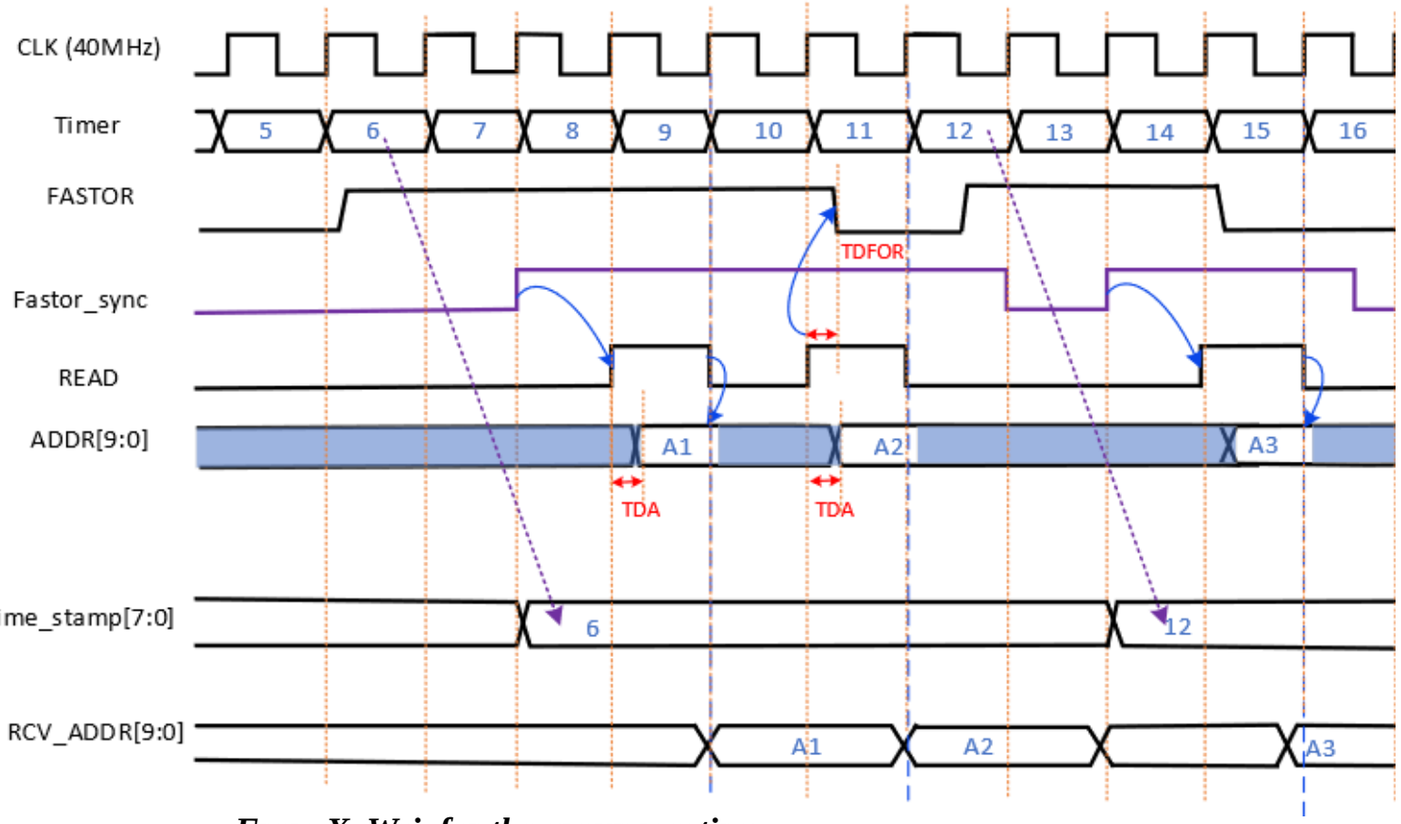
Status of pixel design



- 25x25um2 pixel pitch
- The area of Analog pixel : ?
- The area of digital logic : ?
- The area of address encoder: ?

Peripheral readout architecture





From X. Wei for the group meeting

- Receive a busy signal(fastor) from the EOC
- Generate read signal to read the hitting pixel
- Read out the address of the hitting pixel
- Match the data with the timestamp

Summary and Outlook

Summary

- **Time stamp added at the EOC ,and trigger coincidence will use the time stamp for arbitration.**

- **Ultimate readout design satisfies every 25ns bunch crossing.**

- **Pixel analog modified for faster peaking time and satisfy the requirement.**

Outlook

- **CEPC aims for 2.8 μm spatial resolution (pixel size < 16μm *16μm), therefore, based on the previous design and study, we may choose other smaller technology and for further design in the future.**

Thanks for your attention.