REVIEW OF THE MONOLITHIC CMOS SENSOR TECHNOLOGY AND APPROACH FOR HIGH LUMINOSITY LHC

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IHEP - EPD seminar

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Abstract

The LHC upgrade and other future colliders will lead to a significant **increase in luminosity.**

The context of the ATLAS program focusing on the future tracker upgrade is a good start to show the benefits in **the design of a new approach tracker**, especially at a nominal leveled instantaneous luminosity of 5×10^{34} $cm^{-2}.s^{-1}$

These future tracker detectors require enhanced granularity, reduced material budget and increased radiation hardness to all components.

I will introduce the benefit of **monolithic depleted CMOS sensor (DMAPS)**, which may be able to replace the diode sensor and electronics of a hybrid module.

This new technology proposes thinner module with less material, finer pixel granularity, lower price on any used technology and much simpler production model.

In addition, enough **radiation hardness** for at least 1.5 10^{15} neq $/cm^{-2}$.

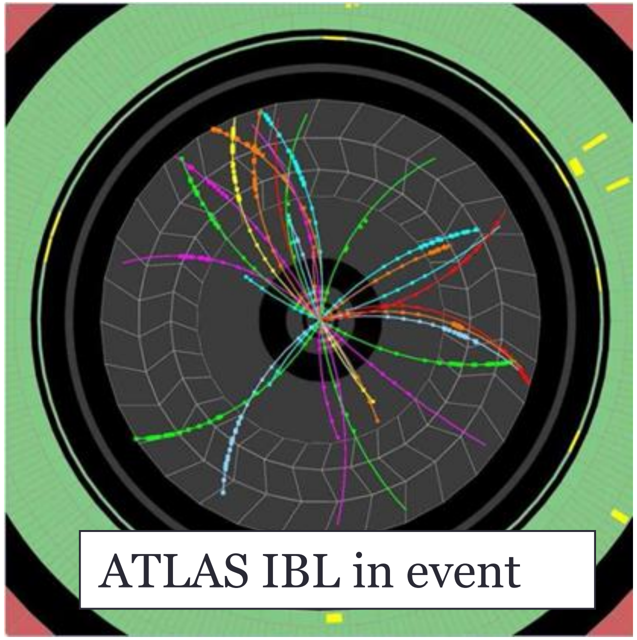
Content

- Silicon Sensor : A quick overview
- Why Depleted CMOS sensor
- New electronics development for the pixel detector of the ATLAS ITk
  - New Read-Out Chip for ATLAS and CMS phase II pixel detectors.
  - CMOS pixel sensors in the ITk.
- Conclusion and Perspectives.

SILICON SENSOR : A QUICK OVERVIEW

Tracking detector for particle detection

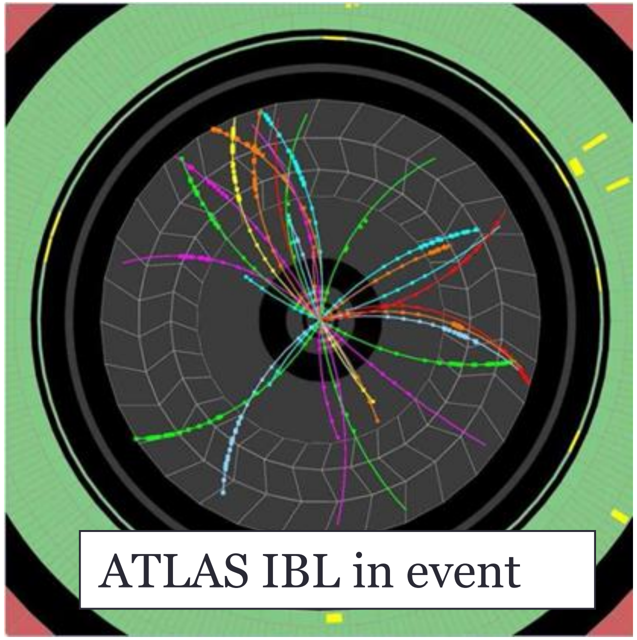
- Understanding an event
  - Individual tracks ~ particles
  - Measures their proprieties
  - LHC : ~1000 particles per 25ns "events"



Tracking detector for particle detection

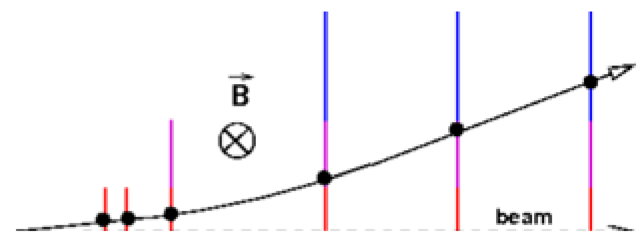
- Understanding an event
  - Individual tracks ~ particles
  - Measures their proprieties
  - LHC : ~1000 particles per 25ns "events"

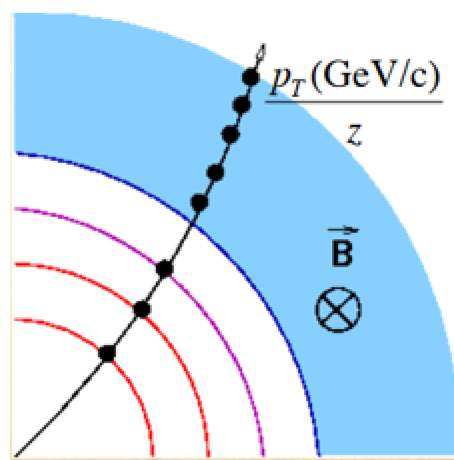
- Track properties
  - Momentum
    - Reconstruction invariant masses
  - Energy
  - Mass ⇔ identification
  - Origin ⇔ vertexing (track merging)
    - Identify decays
    - Measures flight distance



Tracking detector for particle detection

- Magnetic field curves trajectories $\frac{\overrightarrow{dp}}{dt} = \mathrm{q}\vec{\mathrm{v}} \times \vec{\mathrm{B}}$
  - Rewritten with position (x) and path length (l) = basic equation $\frac{\overrightarrow{d^2r}}{d^2l} \propto \frac{\mathrm{q}\vec{\mathrm{B}}(\vec{x})}{\overrightarrow{\|p\|}} \times \frac{\overrightarrow{dr}}{dl}$
  - In B=4T a 1 GeV/c particle will get a sagitta of 1.5mm





$$\frac{p_T(\mathrm{GeV/c})}{z} = 0.3.B(T).R(m)$$

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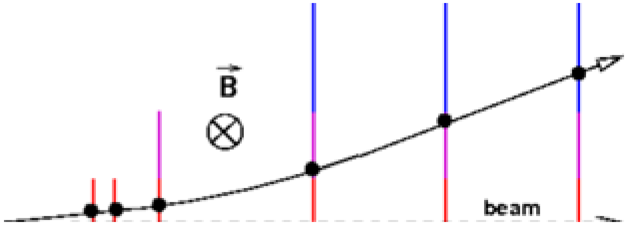
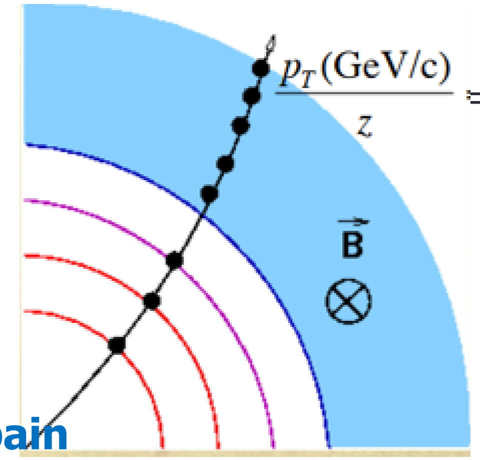


- Fixed-target experiments
  - Dipole magnet
  - Measurement of deflection (angle variation)
- Collider experiment
  - Barrel-type with axial B
  - Measurement of curvature (sagitta)
- Other arrangements
  - Toroidal B .. Not covered
- Two consequences
  - **Position sensitive detectors needed**
  - **Any perturbation effects on trajectories is a pain**



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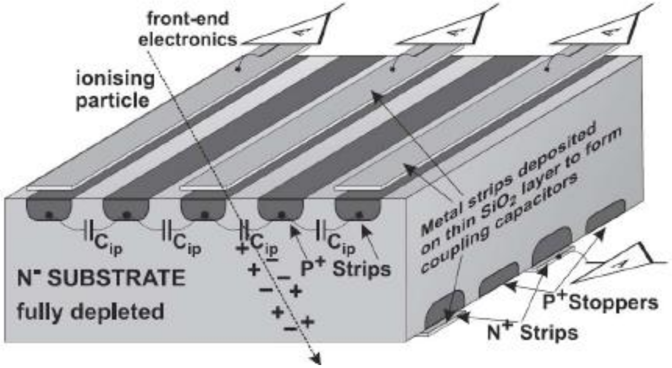
Silicon sensors : strips

- Basic sensitive element
  - e-h pairs are generated by ionization in silicon
    - 3.6 eV needed
    - 300 µm thick Si generates ~22k charges for MIP BUT beware of Landau fluctuation
  - Collection: P-N junction = diode
    - Full depletion (10V to 0.5 kV) generates a drift field (104 V/cm)
    - Collect time ~ 15 ps/µm



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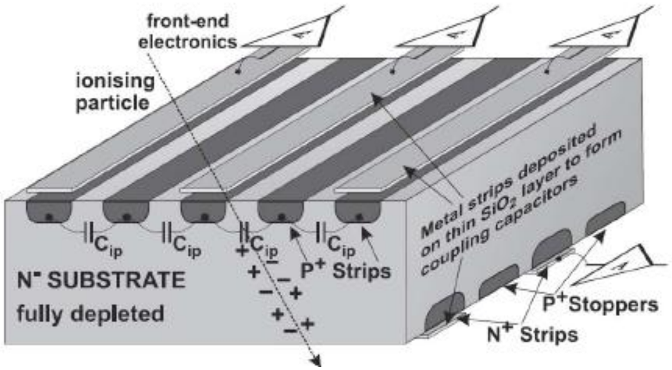

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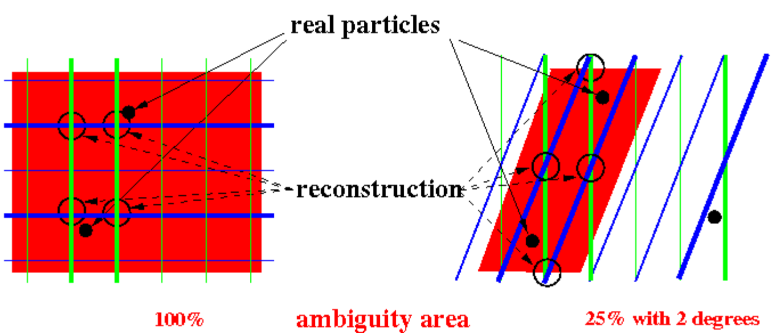
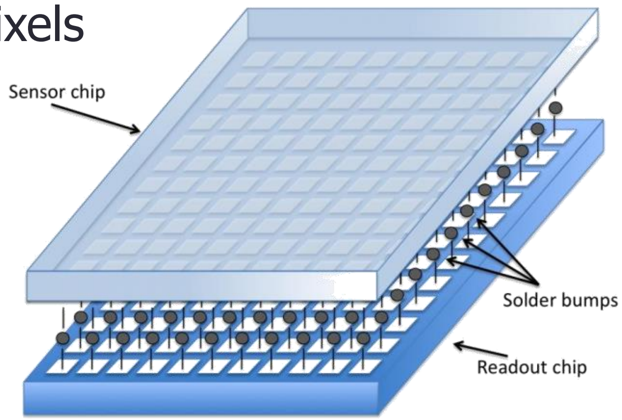
- Silicon strip detectors
  - Sensor "easily" manufactured with pitch down to ~25 µm
  - 1D if single sided
  - **Pseudo-2D** if double-sided
    - Stereo-angle useful against ambiguities
  - Difficult to go **below 100 µm** thickness
  - Speed and radiation hardness: LHC-grade



Silicon sensors: hybrid-pixels

- Concept
  - Strips → pixels on sensor
  - One to one connection from electronic channels to pixels
- Performances
  - **Real 2D detector** & keep performances of strips
    - Can cope with LHC rate (speed & radiation)
    - non-ionizing rad. tolerance ~ 10^{16} neq(1MeV)/cm^2



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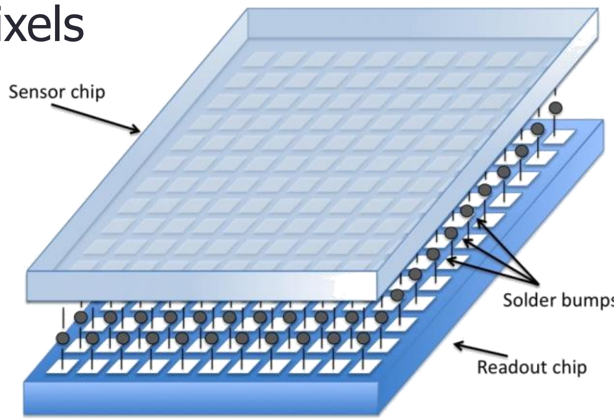
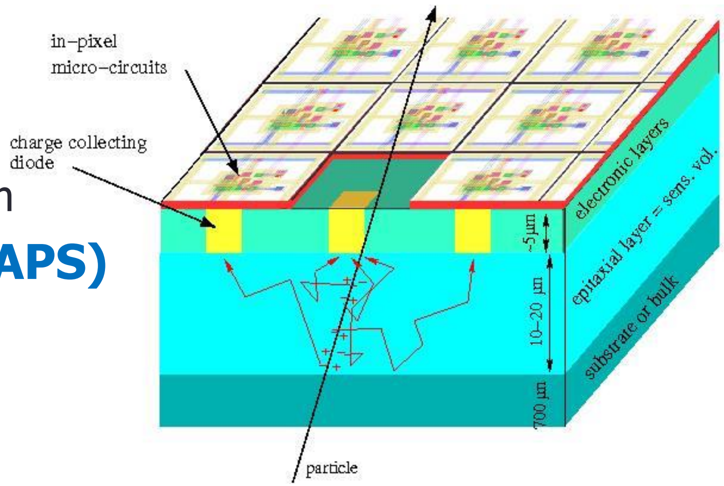


- Performances
  - **Real 2D detector** & keep performances of strips
    - Can cope with LHC rate (speed & radiation)
    - non-ionizing rad. tolerance ~ 10^{16} neq(1MeV)/cm^2
  - **Pitch size limited** by physical connection and number of transistors for treatment
    - minimal (today): 50x50 µm2
      typical: 100x150/400 µm2
    - spatial resolution about 10 µm
  - Material budget
    - Minimal(today): **100 µm(sensor)+100 µm(electronic)**
    - Power budget: **10 µW/pixel**

Silicon sensors: CMOS Pixel Sensor

- Concept
  - Use industrial CMOS process
    - Implement an array of sensing diode
    - Amplify the signal with transistors near the diode
  - Benefit to
    - granularity: pixel pitch down to ~10 μm
    - material: sensitive layer thickness as low as 10-20 μm
  - Known as **Monolithic Active Pixel Sensors (MAPS)**



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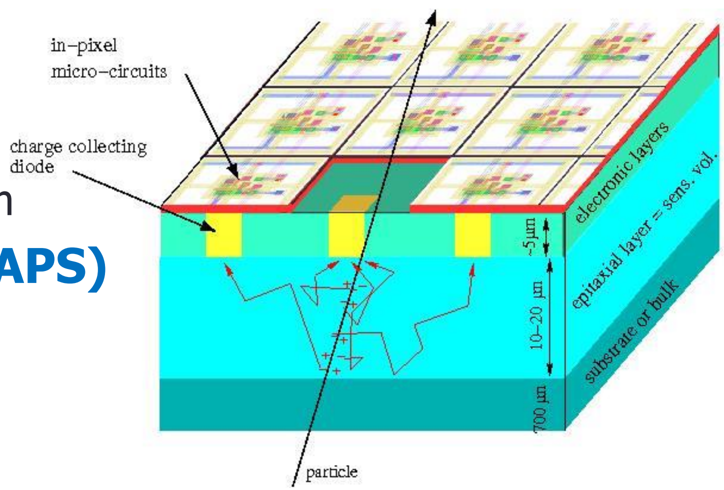
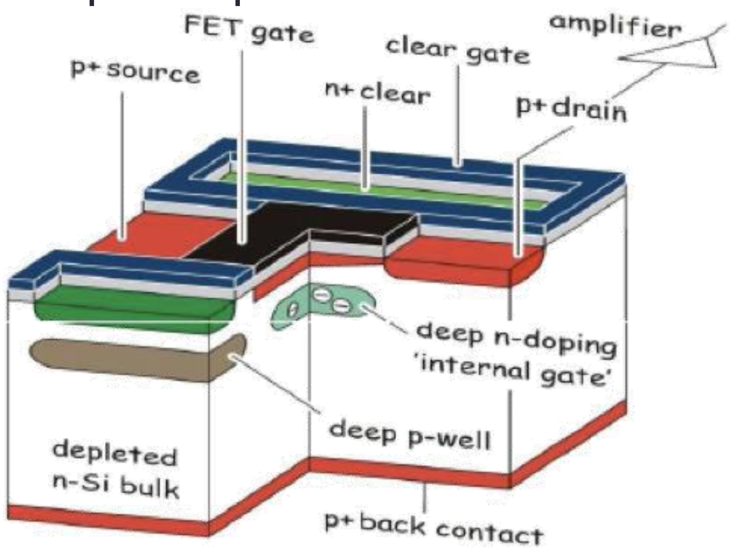


- Performances **(Sensitive undepleted layer)**
  - Slow (100 ns) thermal drift of charges (diffusion)
  - non-ionizing rad. tolerance $\lesssim 10^{13}$ neq(1MeV)/cm^2
  - Spatial resolution 1-10 µm (in 2 dimensions)

  - Material budget
    - Material budget: $\lesssim$ **50 µm**
    - Power budget: < **µW/pixel**

Others Silicon sensors

- DEPFET
  - Depleted p-channel FET



  - **Fully depleted** sensitive layer
  - Large sensor amplification
  - Still require some read-out circuits
    - **Not fully monolithic**
    - Possibly limited in read-out speed

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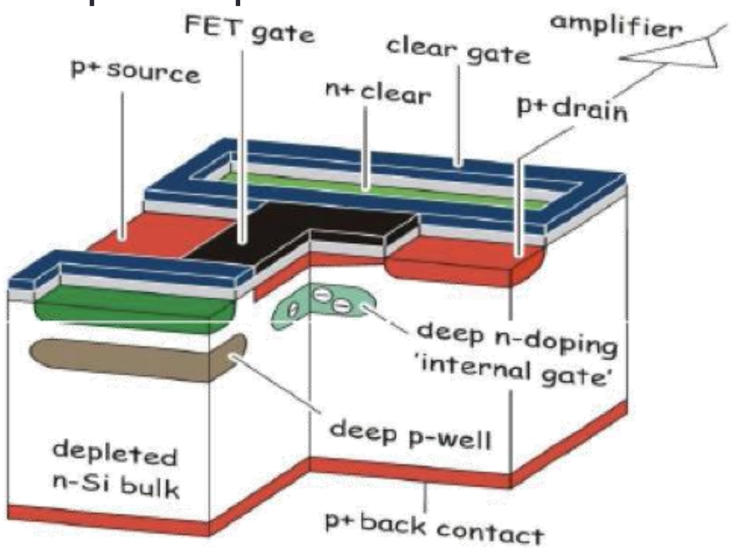
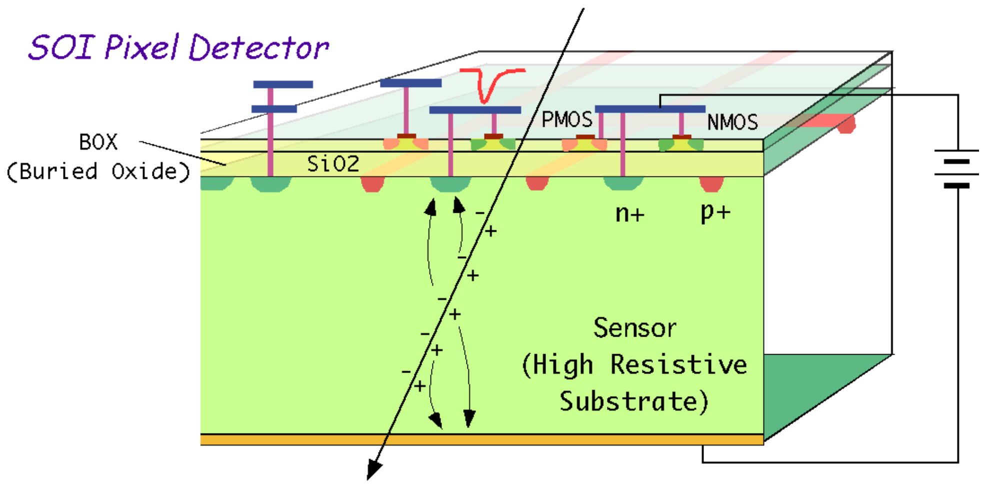


- Silicon On Insulator (SOI)



- **Fully depleted** sensitive layer
- Large sensor amplification
- Still require some read-out circuits
  - **Not fully monolithic**
  - Possibly limited in read-out speed

- **Partially depleted** sensitive layer
- **Fully monolithic**
- Electronics similar to MAPS
- But **Backgate effect**
  -> limitation of the depletion area.

WHY DEPLETED CMOS SENSOR

Why CMOS sensor

Why using commercial CMOS technology for monolithic pixel detectors is interesting . Some features/advantages ... using CMOS process lines

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Usage of a **matured commercial process** technology

huge production capabilities (> 30 000 wafers/month)

cost per wafer low (interesting for large area)

turn around time ~ 3 months (fast supply / reaction times)

Much **less elaborate module assembly** process (e.g. no hybridization)

Lower module **cost** (factor **3-4** compared to hybrid pixel modules)

Thin monolithic modules (100 µm)

Pixel size of 50 x 50 µm² (same as hybrid) or smaller possible

Why depleted CMOS sensor (DMAPS)

Why using commercial CMOS technology for depleted monolithic pixel detectors is interesting . Some features/advantages ... using CMOS process lines

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Why using commercial CMOS technology for depleted monolithic pixel detectors is interesting . Some features/advantages … using CMOS process lines

Depleted CMOS sensor combines the compactness of CMOS sensor with the performance of hybrid planar silicon sensors

By using **high-voltage** compliant CMOS processes/design rules.

Electronics shielded from bias voltage

By using an **isolated deep well** that collects charge **and** includes both analogue and digital circuits **->** **monolithic pixel**

The isolated deep well is biased up to 400 V giving a depletion depth of 200 µm in the bulk.

large signal and fast charge collection,

Radiation tolerant

Sensors can be thinned **to 50 µm without signal loss**.

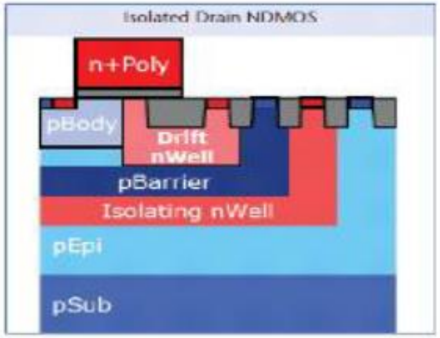
Sensors can operate in a high rate environment (< 25 ns)

What is needed to realize DMAPS?

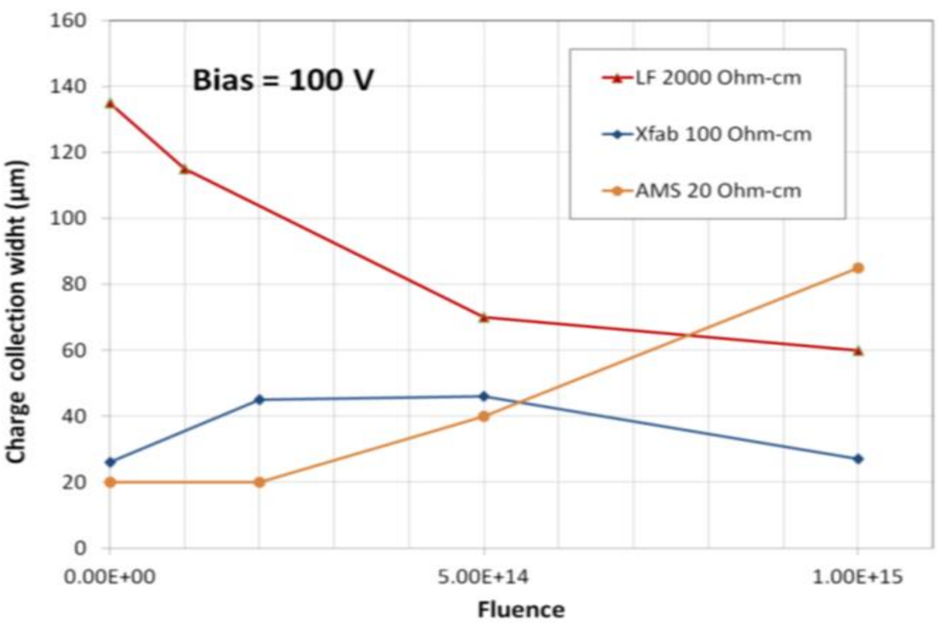
"High" Resistivity Substrate (or epi layer) Wafers (100 Ω.cm – kΩ.cm)

"High" Voltage add-ons to apply 50 – 200 V bias

Multiple (4) nested wells
(for full CMOS and for shielding)



from: www.xfab.com



I. Mandić et al.

Backside Processing
(for thinning and back bias contact application
=> thin modules with high field)

DMAPS concepts

High-radiation environment
=> fast charge collection => **depleted** sensitive layer => $d \sim \sqrt{\rho \cdot V}$

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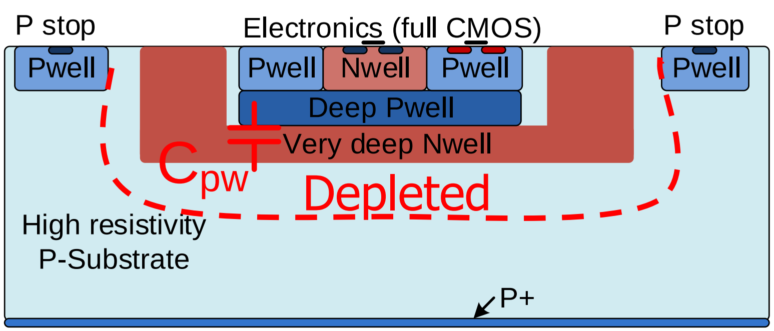
Large fill factor



Radiation hardness

- uniform field, short drift distance

Large sensor capacitance (200 - 400fF)

- non-negligible C_{pw}
- noise & speed (power) penalties
- cross-talk: dedicated pixel design needed

DMAPS concepts

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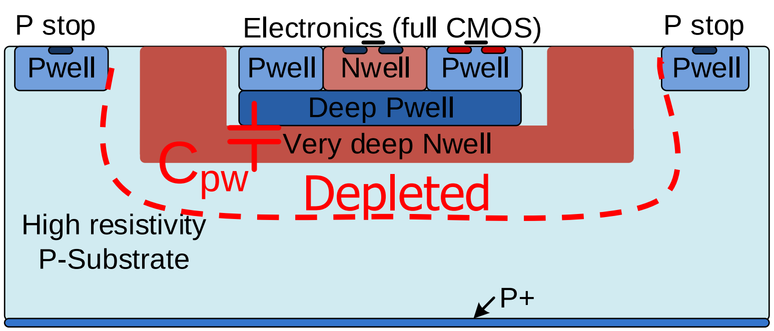
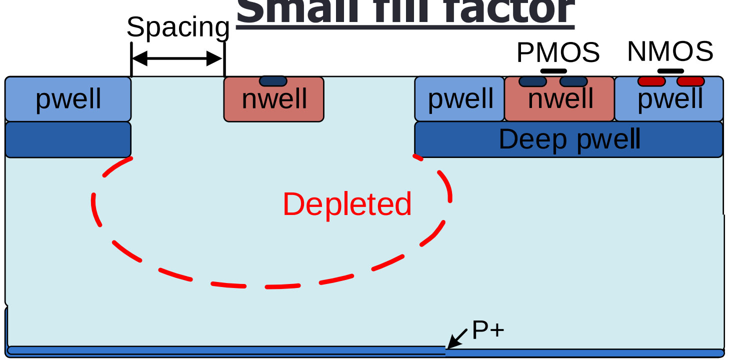


Small fill factor



☺ Radiation hardness
- uniform field, short drift distance

☹ Large sensor capacitance (200 - 400fF)
- non-negligible C_{pw}
- noise & speed (power) penalties
- cross-talk: dedicated pixel design needed

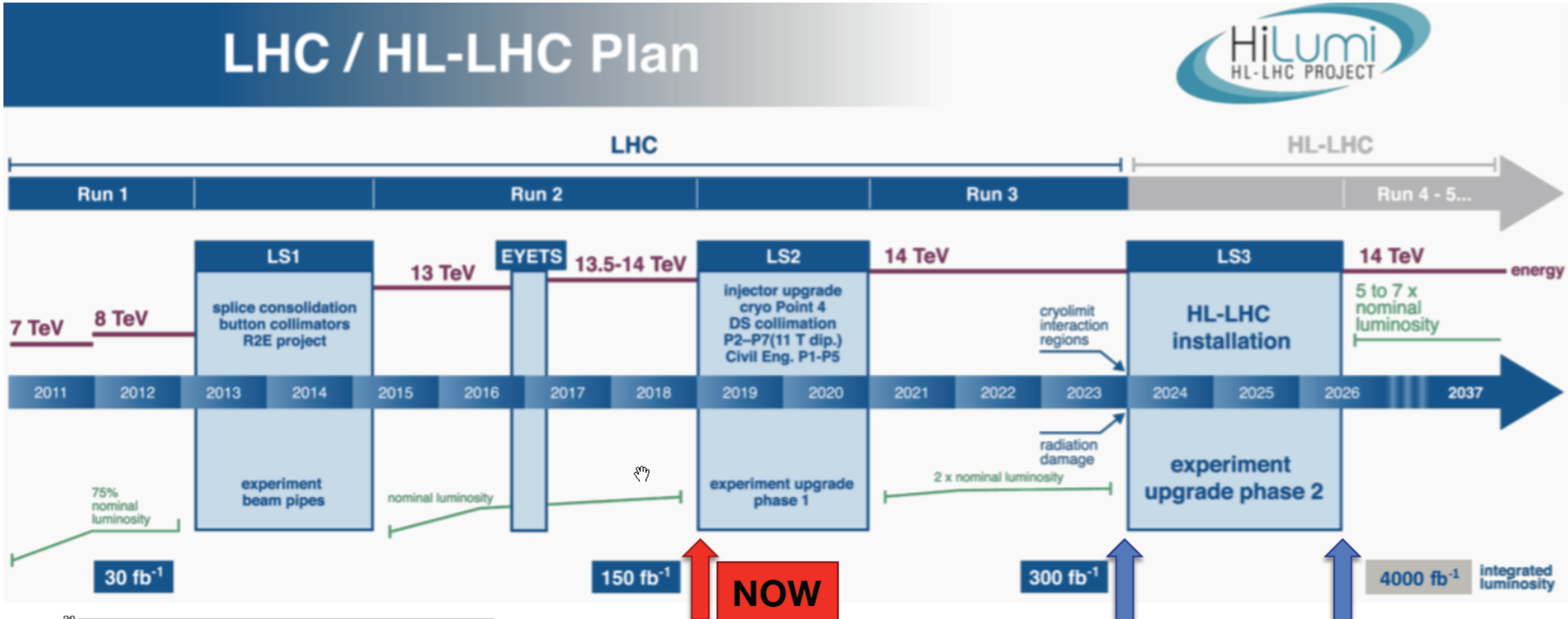
☺ Very small sensor capacitance (< 10fF)
- low noise & power

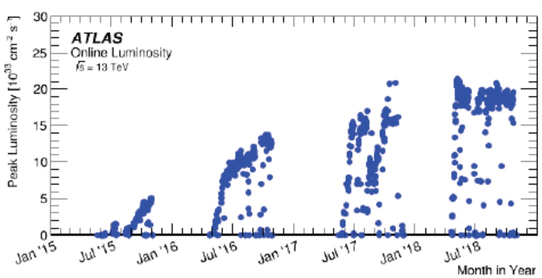
☹ Limited depletion, long sig. travel path
- dedicated efforts to enhance depletion

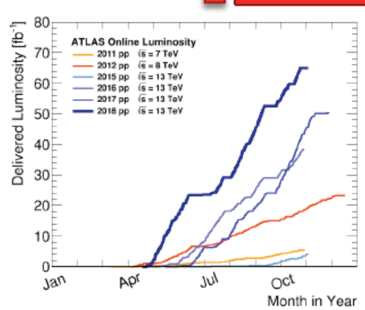
NEW ELECTRONICS DEVELOPMENT FOR THE PIXEL DETECTOR OF THE ATLAS ITK

RD53 : New Read-Out Chip for
ATLAS and CMS phase II pixel detectors.

Upgrade of the LHC





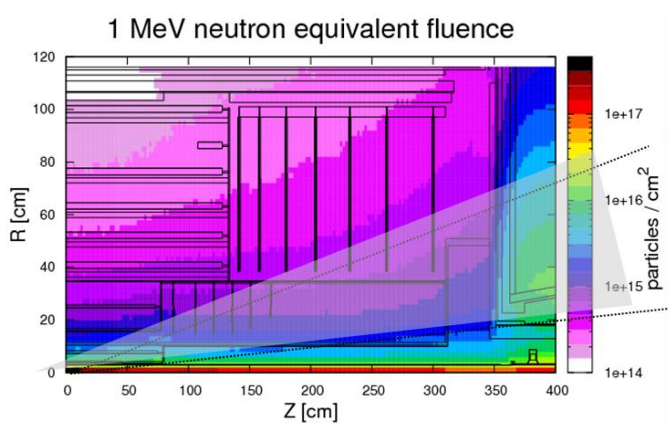


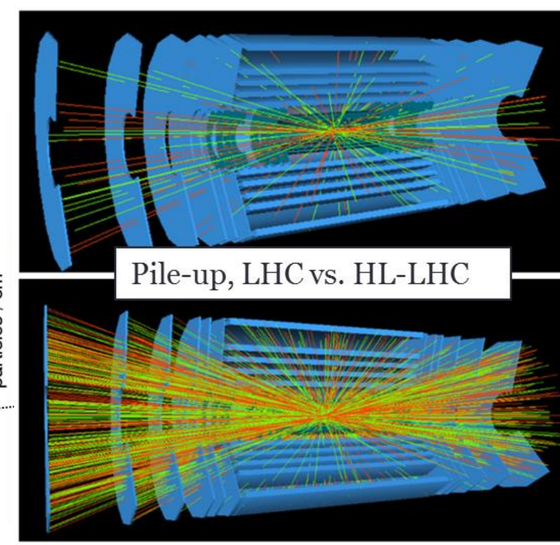
Current pixel detector
$L = 2\times10^{34}\ cm^{-2}s^{-1}$
$\int L = 300\ fb^{-1}$

ITk pixel detector
$L = 7\times10^{34}\ cm^{-2}s^{-1}$
$\int L = 4000\ fb^{-1}$

ATLAS ITK : Why a new tracker?

- A huge pile-up: **200 interactions** per beam crossing!
  - ATLAS designed for 25 interactions
  - The new detector will allow to keep current performances in terms of tracking and vertexing, b-tagging…
- More difficult radiation environment:
  - Central layers should cope over lifetime with **> 2.10^{16} n$_{eq}$/cm^{-2} > 1 Grad**
  - vs. 100-200 Mrad design for current inner layers
- Better η coverage:
  - **η = 2.5 → 4.0**
  - higher lepton acceptance
  - better pile-up rejection



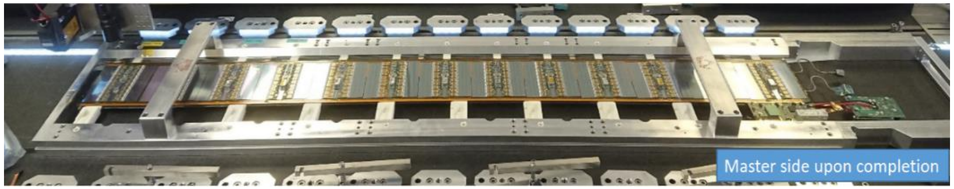


The Inner Tracker Upgrade (ITK)

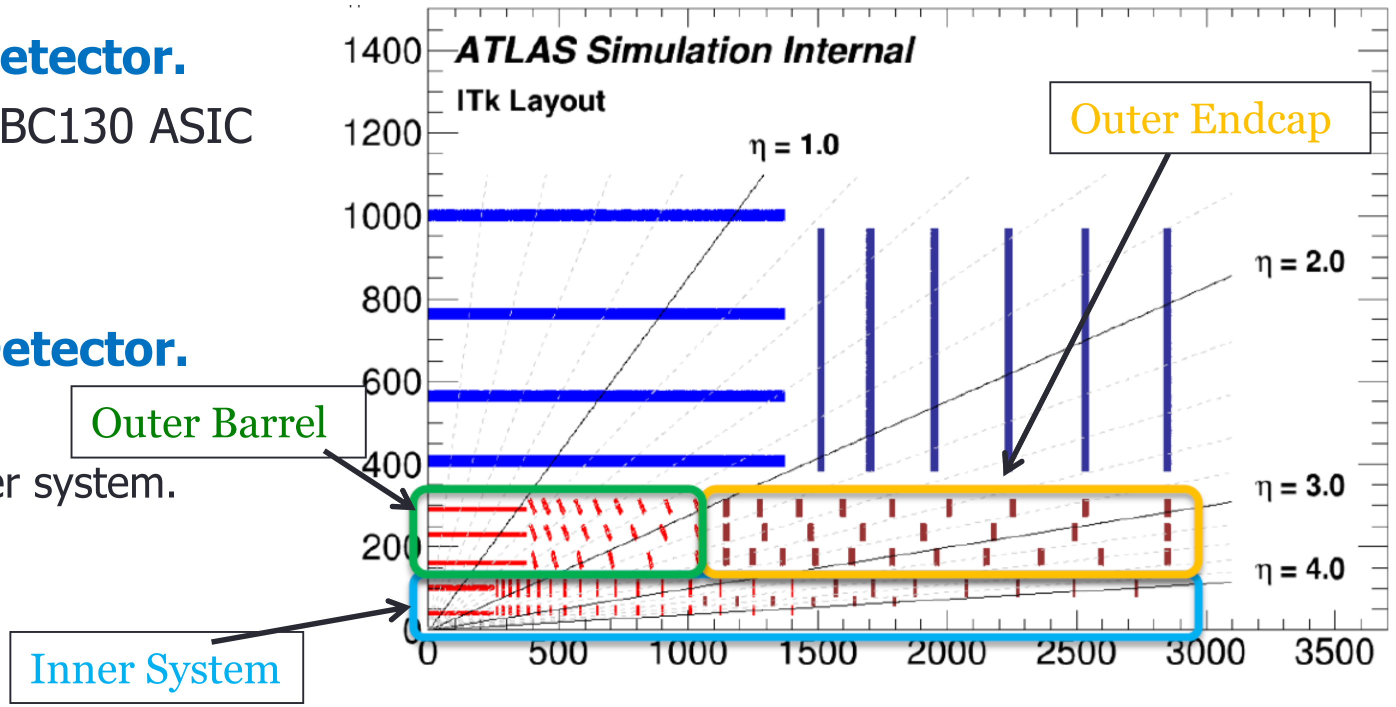
ATLAS biggest upgrade project

- An all silicon tracker, covering up to radius approx. 1m and extended tracking coverage η = 4.
- Reduced material (<1 X_0 up to η ~ 3)

Prototype double sided strip stave

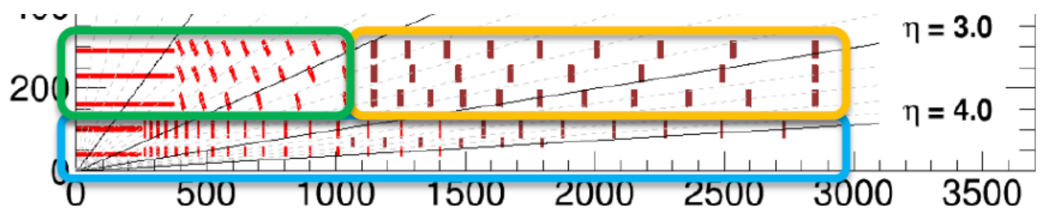


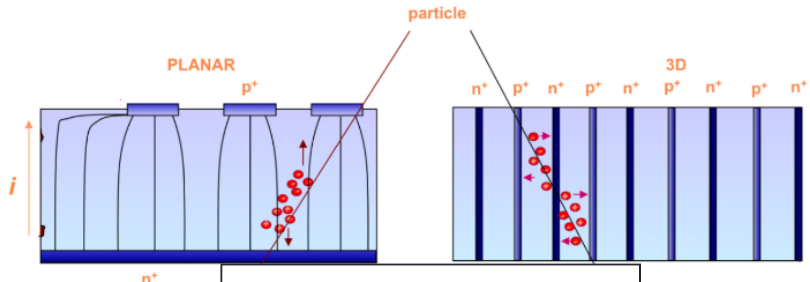
- Silicon strip
  - **4 layers Strip Detector.**
  - n^+-in-p FZ and ABC130 ASIC
- Pixel detector:
  - **5 layers Pixel Detector.**
  - Features:
    - Replaceable inner system.
    - Serial Powering.



ATLAS-ITK : Sensors / Read-Out-Chip

- Various sensors options depending on location
  - Inner system:
    - L0 and R0: 3D sensors
    - L1 and R1: 100 µm thin planar
  - Outer barrel and endcaps:
    - L2-4 and R2-4: 150 µm thick planar
    - In L4: Option of using **Depleted monolithic CMOS sensor (DMAPS)**





Planar vs. 3D Si sensor

- The sensor technology is chosen wrt several criteria:
  - **Radiation hardness**
  - **Cost**
  - **Production capability**

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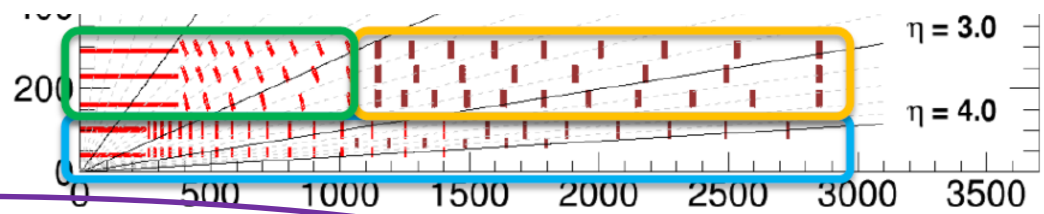

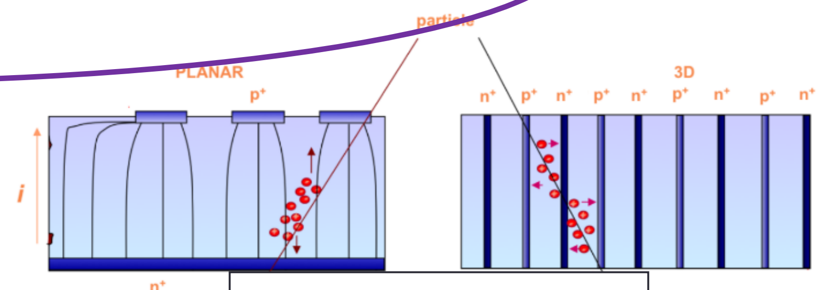

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Hybrid FE / RD53 collaboration

- RD53 project : Design and develop pixel chips for **ATLAS/CMS phase 2 upgrades**, started in 2013

- Baseline technology : TSMC **65nm** CMOS

~100 people from 20 institutes :

- Bonn University
- CERN
- Fermilab
- INFN : Bari - Bergamo-Pavia – Milano - Padova – Perugia – Pisa - Torino
- IN2P3 : CPPM – LAPP – LAL - LPNHE
- LBNL
- New Mexico
- NIKHEF
- Prague IP/FNSPE-CTU
- RAL
- Sevilla University

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Hybrid FE / RD53 collaboration

- RD53 project : Design and develop pixel chips for **ATLAS/CMS phase 2 upgrades**, started in 2013

- Extremely challenging requirements for HL-LHC
  - **Hit rates: 3 GHz/cm²** (200 MHz/cm² in the current system) / **~220 hits/IC/bx**
  - Small pixels: **50 x 50 µm²** - Low power - Low mass
  - Radiation : **500 Mrad - 10^{16} n_{eq}/cm² over 5 years**
    - Inner layer to be changed after 5 years
  - Local memory for 500 bx

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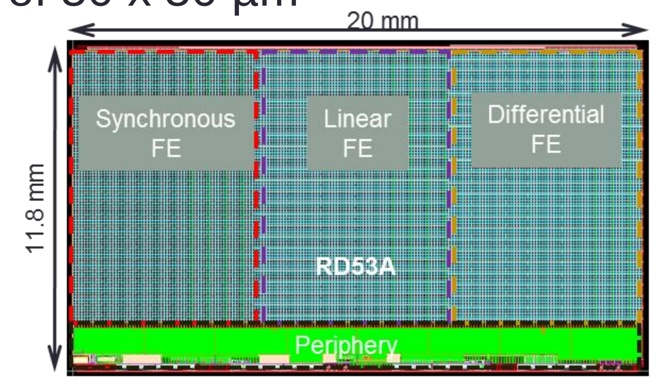
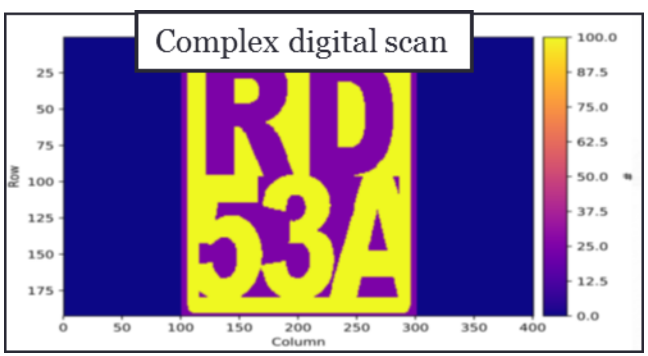
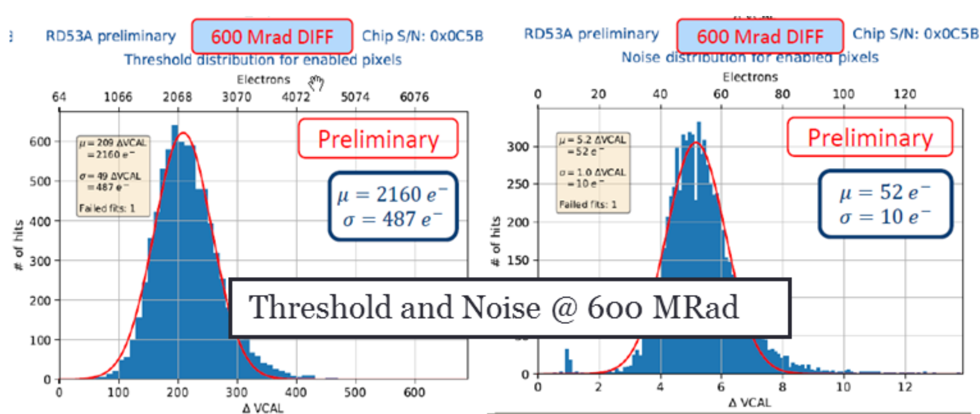
RD53 : Final production IC development

- **RD53A** chip **half size prototype**
  Sensitive area : 2 cm x 1.18 cm → 400 x 192 pixels of 50 x 50 µm²
  3 different Analog Front End flavors :
  Synchronous, Linear, Differential
  Submission August 2017
  First chip tested December 2017
  First **bump-bonded chip tested April 2018**







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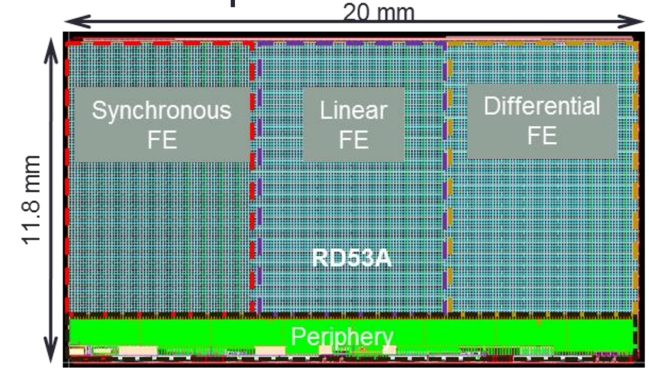
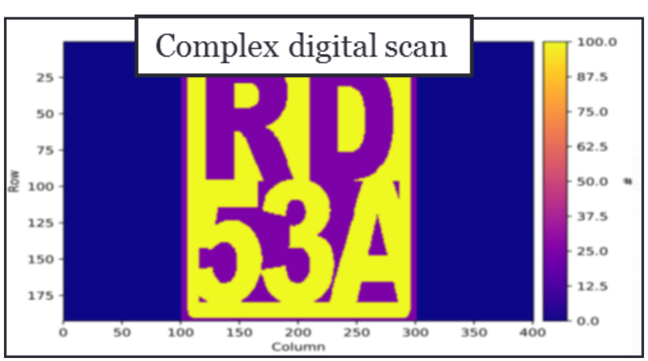
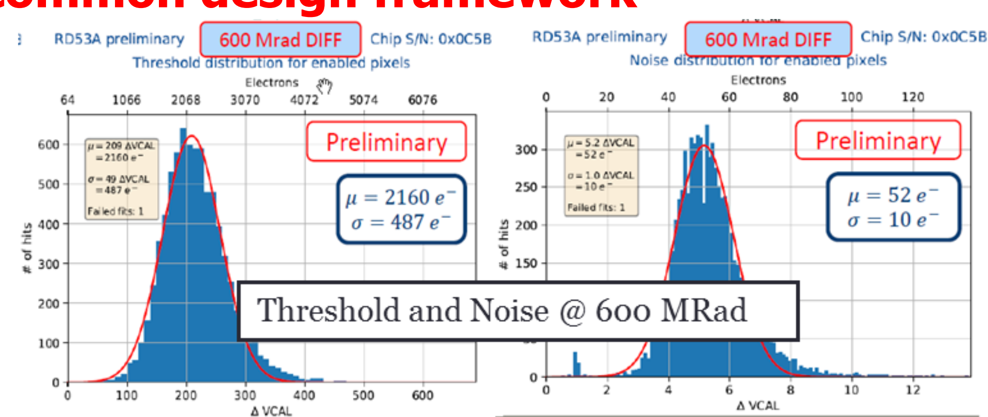


- **Development of the final production chips is ongoing (minor modifications)**
  - **ATLAS chip submission target July 2019** (20 mm × 21 mm)
  - **CMS chip submission December 2019** (21.7 mm × 18 mm)
  - Both chips are **synthesized from a common design framework**





NEW ELECTRONICS DEVELOPMENT FOR THE PIXEL DETECTOR OF THE ATLAS ITK

Monolithic Depleted CMOS sensor (DMAPS) in the ITk

DMAPS collaboration

Developing detectors for HL-LHC environment is actually **paving the road** for a general use of this technology

- Generating a collaborative effort of **~25 ATLAS ITK institutes**
- Capable of attracting also non-ATLAS institutes and resources

AIDA 2020 **WP6: Novel high voltage and resistive CMOS sensors**

STREAM, Smart Sensor Technologies and Training for Radiation Enhanced Applications and Measurement
Innovative Training Network (ITN)
under the Marie Skłodowska-Curie Actions
https://stream.web.cern.ch/

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Exploring **different solutions is paramount**:

- Every solution has pros and cons
  → avoid missing opportunities or delays by technical difficulties of one specific solution

- **Close collaboration** with foundries is critical
  → risk mitigation against industrial policies

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Task force and working group

GOALS

Could provide an **advantageous replacement for hybrid pixels.**

Show that CMOS pixel sensors can be designed **radiation-hard** to at least 10^{15}neq/cm² and 100 Mrad.

Choose suitable **technology** (and suitable vendor)

Optimize cell for fast and complete charge collection and simultaneous radiation tolerance

Design **monolithic full rad-hard** R/O architecture devices
(complete (depleted) CMOS pixel detectors)

- HV/HR technologies
  - HV CMOS
    - AMS 350 nm
    - **AMS 180 nm**
  - HR CMOS
    - **LFoundry 150 nm**
    - Global Foundry 130 nm
    - ESPROS 150 nm
    - Toshiba 130 nm
    - **TowerJazz 180 nm**
    - IBM T3 130 nm
    - STM 180 nm
    - ON Semiconductor 180 nm
- SOI – CMOS Pixel
    - XFAB 180 nm

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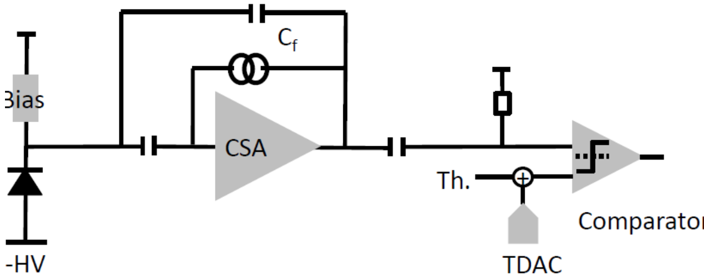
The Matrix (Pixel Level)

- All of present CMOS sensor designs include for Each pixel = **CSA + discriminator + Hit Memory**
  - Including analog test pulse
  - Including pixel mask
  - Diode or PMOS reset
  - Discriminator with edge output injected to double column pixel logic
  - Hit memory in active matrix
  - Control of bias current (individual or on chip level)

CMOS chip	Fill Factor	Pitch [um x um]
AMS AtlasPix3	Large	50x150
TJ Malta	Small	36x36
TJ Monopix1	Small	36x40
LF Monopix1	Large	50x250



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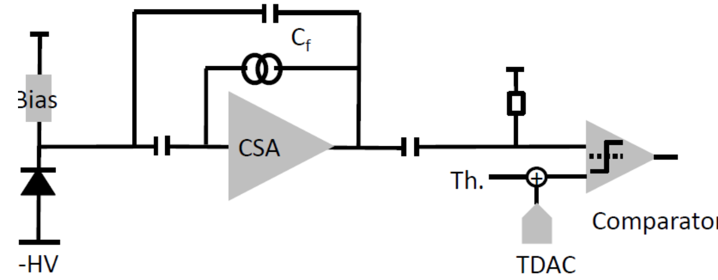

- Full matrix needs = 512x512 pixels
  - Cover active area ~18 x 20 mm^2 (assuming RD53 like coverage)
  - **Coarse** analog measurement
  - All pixel addresses with hits are (a)synchronously transmitted over **high-speed bus** to End-of-Column logic

CMOS RO	Architecture
AMS AtlasPix3	Synchronous (column drain)
TJ Malta	Asynchronous (Novel)
TJ Monopix1	Synchronous (FEI-3)
LF Monopix1	Synchronous (FE-I3)

Why AMS/TSI, LF and TJ foundries

- **AMS/TSI 180nm**
  - 3 (+1 option) wells (deepN/P) available for partial **(full) CMOS** implementation in matrix
  - Free choice of **HR substrate** and repeatedly achieved very high substrate voltages without breakdown (>100V)
  - **Access** to foundry simple
  - Well **established process** and readily available engineering runs in already qualified process

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- **LFoundry 150nm**
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- **TowerJazz 180nm**
  - DeepPwell available, **unrestricted CMOS** implementation in matrix
  - Customer or TJ supplied **HR wafers** for depleted sensors
  - Best established MAPS producer in HEP with >1000 wafers delivered to experiments, hence **minimal risks for future production availability**

DMAPS sensor development lines

Monolithic sensors with electronics all in one!

2 lines of development followed : (a) large electrode design / (b) small electrode design

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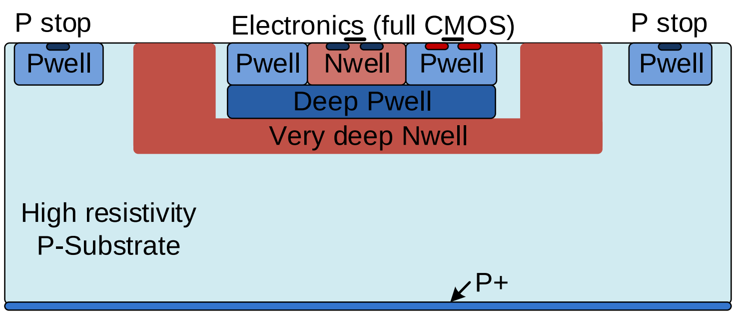

LF or AMS/TSI processes

- Pros:
  - Full CMOS
  - Uniform field, short drift distance → radiation hardness (TID & NIEL), 2.10^{15} $n_{eq}.cm^{-2}$ proven
  - HV reverse. bias > 300V possible (LF)
  - Back Side thinning and processing possible
- Cons:
  - Deep nwell Q collection → big Capacitance (>200 fF) → noise, power & crosstalk

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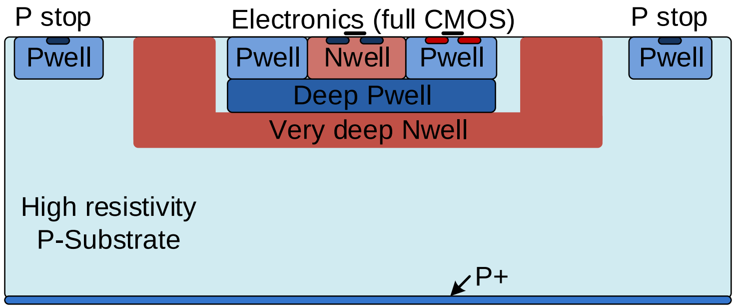

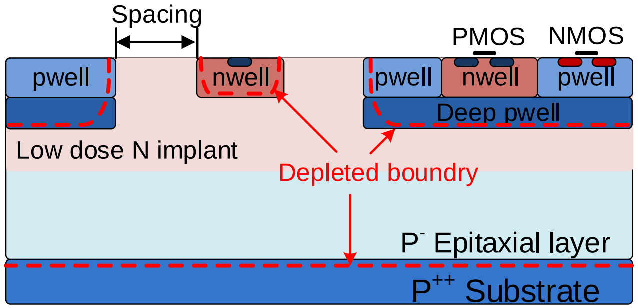

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  - Deep nwell Q collection → big Capacitance (>200 fF) → noise, power & crosstalk

Modified TJ process

(W. Snoeys et al., NIM A871 (2017) 90–96)

- Pros:
  - Full CMOS
  - Small capacitance (<10fF) → low noise & low power.
  - Vendor established at CERN
  - Thin detector possible.
- Cons:
  - Limited depletion, long drift distance → radiation hardness (need process modification)

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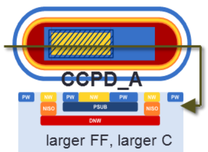
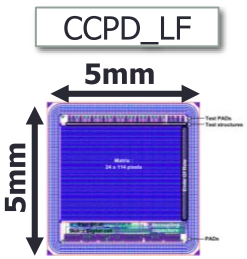
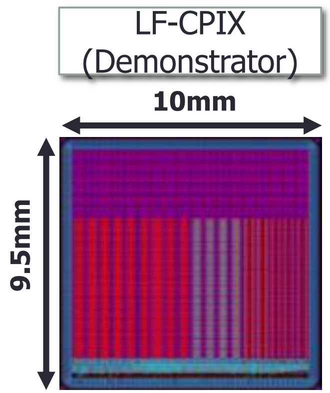
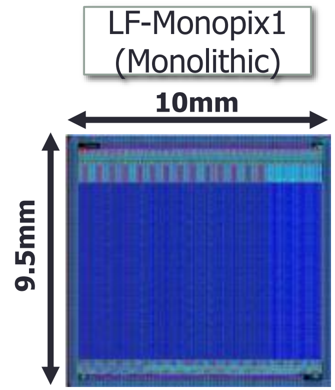
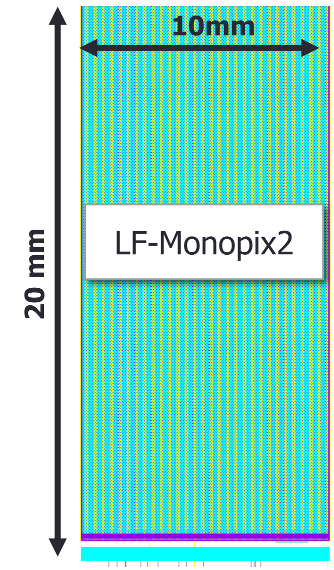
LFoundry DMAPS prototyping line











CCPD_LF

- *Subm. in **Sep. 2014***
- *33 x 125 µm² pixels*
- *Fast R/O coupled to FE-I4*
- *Standalone R/O for test*
- *Bonn/CPPM/KIT*

LF-CPIX (DEMO)

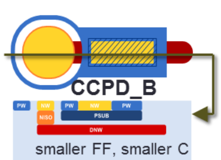
- *Subm. in **Mar. 2016***
- *50 x 250 µm² pixels*
- *Fast R/O coupled to FE-I4*
- *New Sensor Guard-Ring*
- *Standalone R/O for test*
- *Bonn/CPPM/IRFU*

LF-Monopix1

- *Subm. in **Aug. 2016***
- *50 x 250 µm² pixels*
- *Fast column drain R/O*
- *Bonn/CPPM/IRFU*

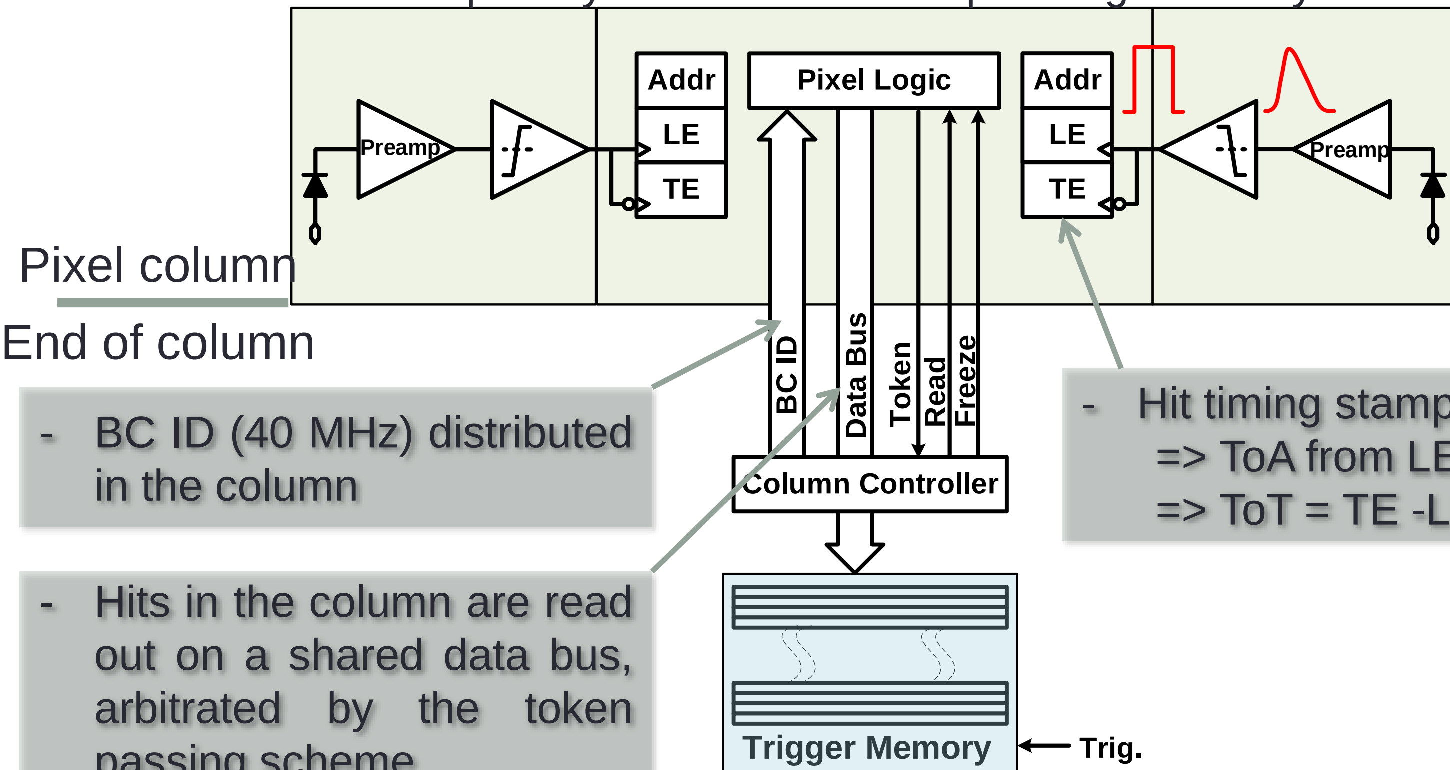
LF-Monopix2

- *Being designed*
- *50 x 150 µm² pixels*
- *Full height matrix*
- *Fast column drain R/O*
- *Bonn/CERN/CPPM/IRFU*



LF-MONOPIX1 Column drain readout architecture

- Similar to the current ATLAS pixel readout chip **“FE-I3”**
  - Sufficient rate capability with affordable in-pixel logic density for CMOS pixels

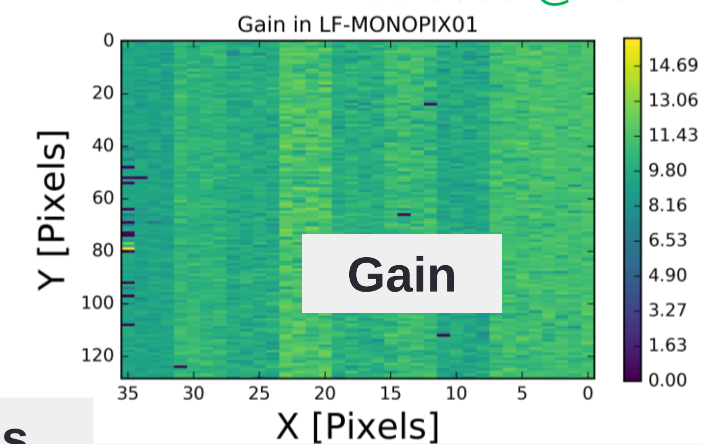


- BC ID (40 MHz) distributed in the column
- Hits in the column are read out on a shared data bus, arbitrated by the token passing scheme
- Hit timing stamped in pixel
  => ToA from LE time stamp
  => ToT = TE -LE

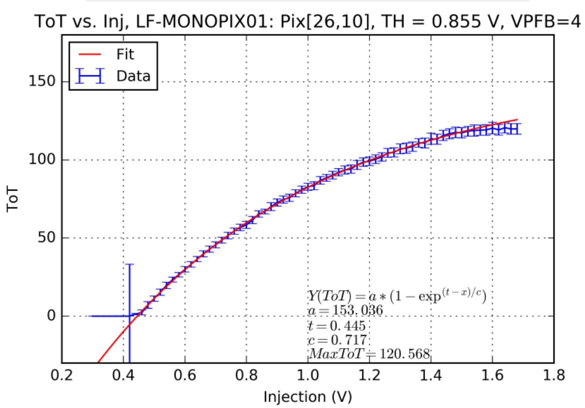
LF-MONOPIX1 : Laboratory results

- Breakdown @ **-280 V** => up to ~ 300 µm depletion
- ToT calibrated with sources: ^{241}Am, terbium
- Gain **10 -12 µV/e⁻**
- Typical ENC ~ **200 e⁻**
- Tunable threshold down to **1400 e⁻**
  - dispersion ~ **100e⁻** after tuning

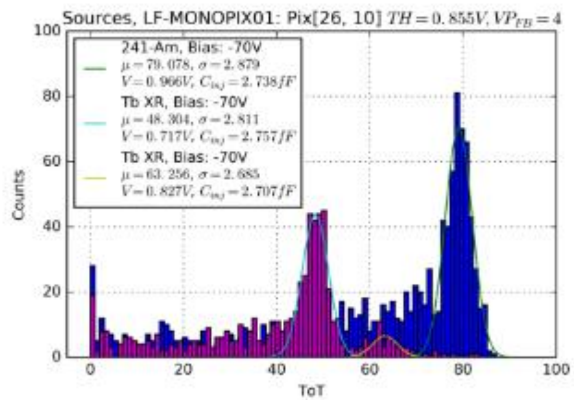
I. Caicedo @Bonn

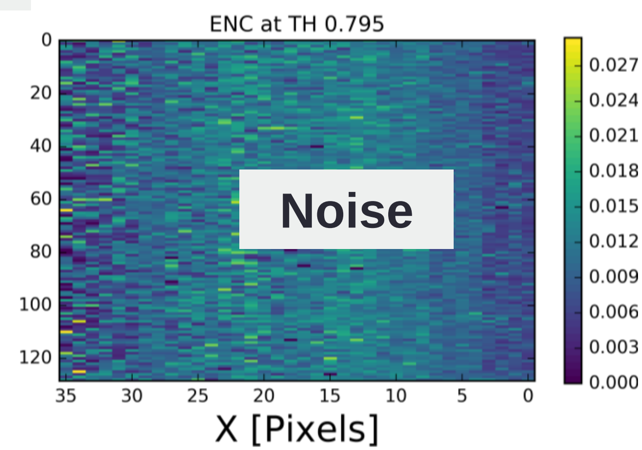


ToT vs. Injection



Response to sources



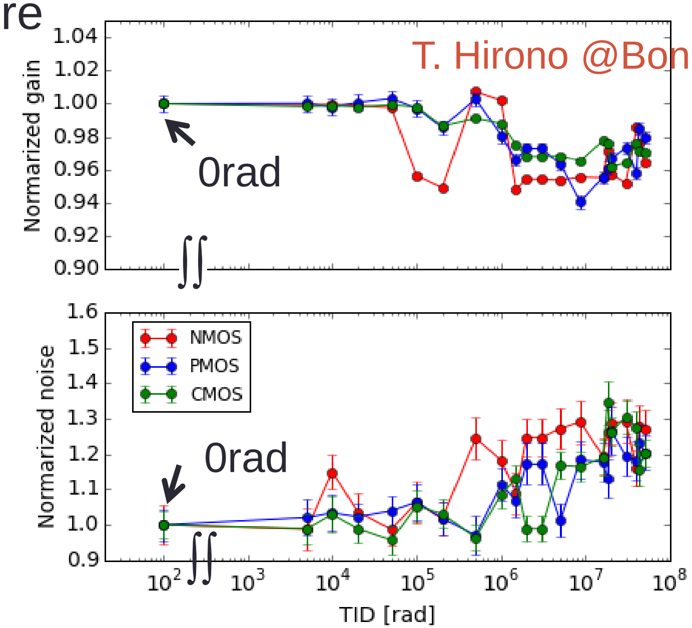


LF-MONOPIX1 : TID, NIEL performance

- X-ray irradiation up to **50Mrad**
  - Irradiated and measured in room temperature
  - Gain degradation **<5%**
  - Noise increase **~25%**

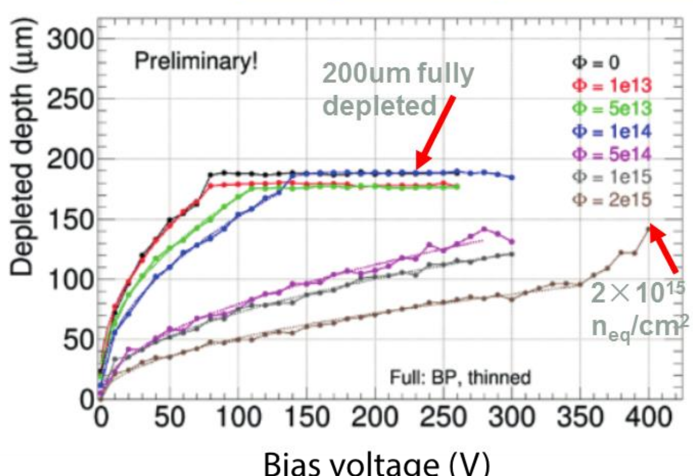
    => higher leakage current after irradiation.
  - No significant difference between the CSA

Normalized gain and ENC (LF-CPIX)



- Neutron irradiation

  I.Mandić, et al., doi.org/10.1016/j.nima.2018.06.062



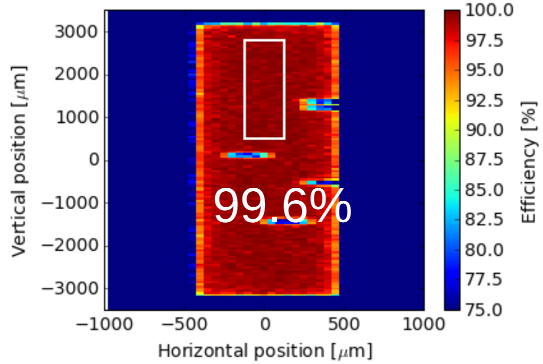
*Depletion depth ~ **140 µm** after **2×10^{15} n_{eq}/cm^2***

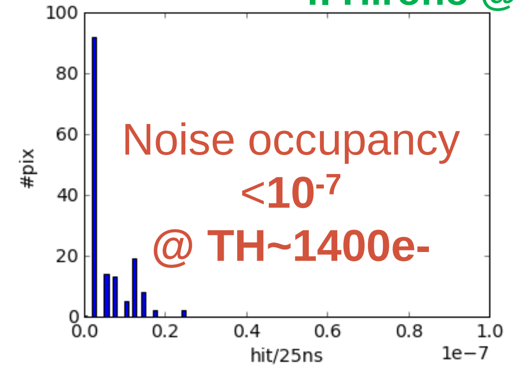
LF-MONOPIX1 : Telescope test beam

T. Hirono @Bonn

- Non-irradiated

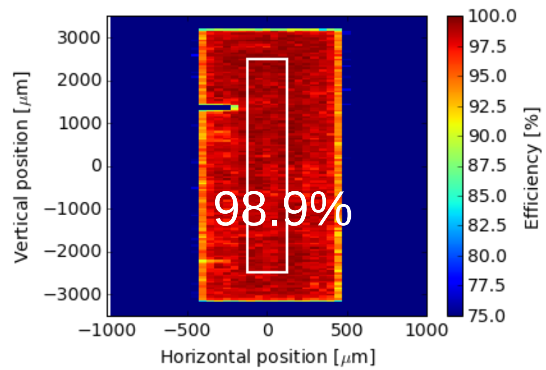
TH tuned by noise
Columns: 16-20
HV: -200V
Temp: dry ice

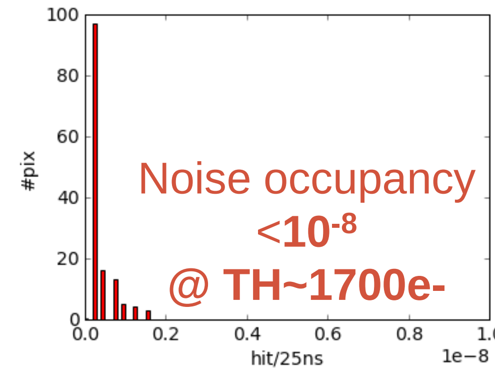




- 1 x $10^{15}n_{eq}/cm^2$

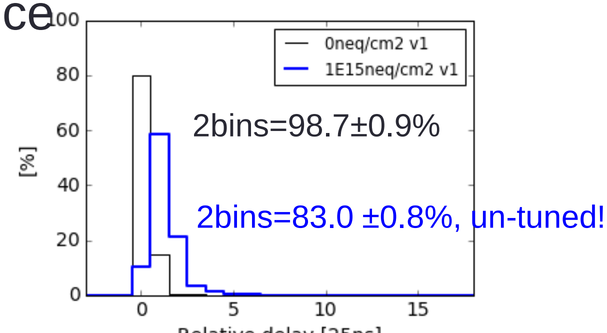
TH tuned by noise
Columns: 16-20
HV: -130V
Temp: dry ice





- Timing performance

TH tuned by noise
Columns: 16-20
HV: -200V
Temp: dry ice



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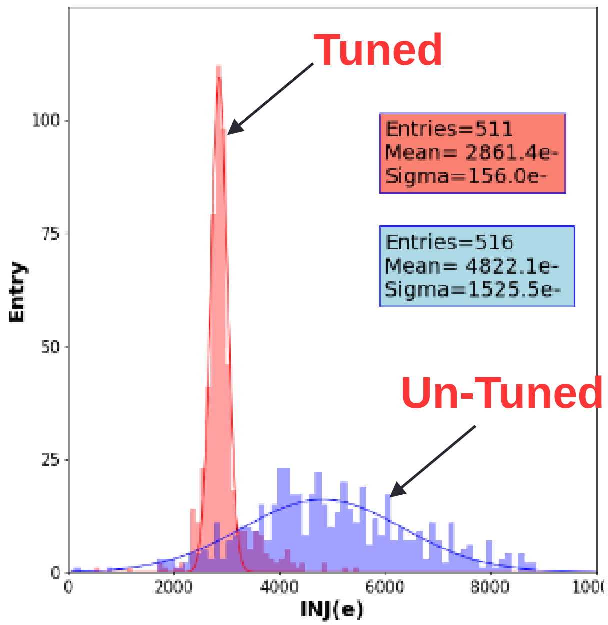
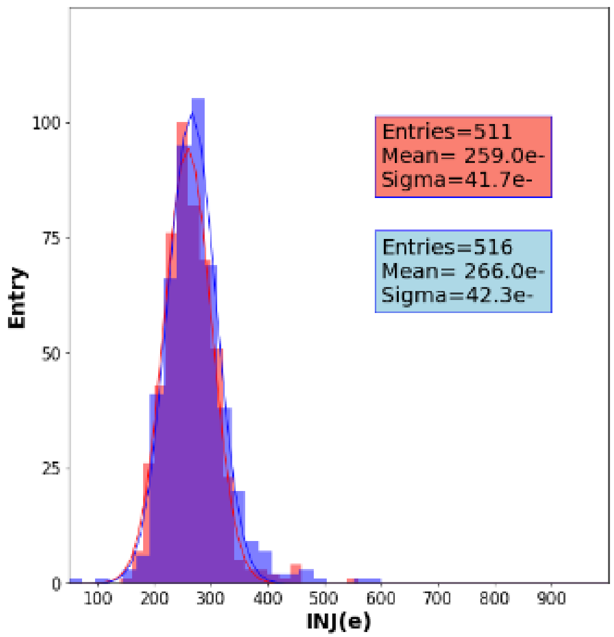
LF-MONOPIX1 : Proton irradiation

- Chip irradiated to **160 Mrad**, 80 days room temperature annealing
- Measured at -12 ℃, HV = -40 V
- NMOS pre-amplifier + Discriminator V2
  - Noise ~ **250 e-**
  - The threshold dispersion can be tuned to ~ **150e-**

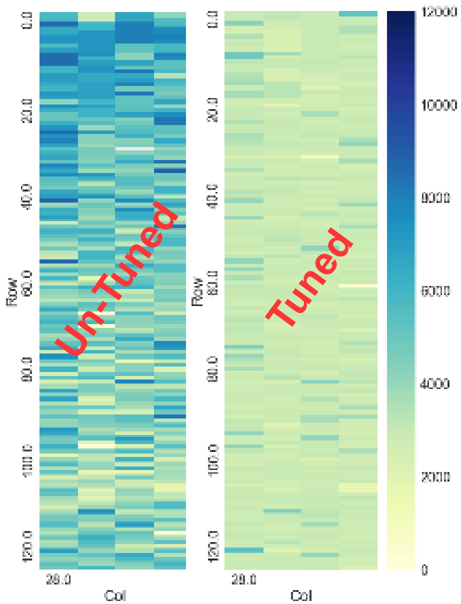


Threshold



ENC

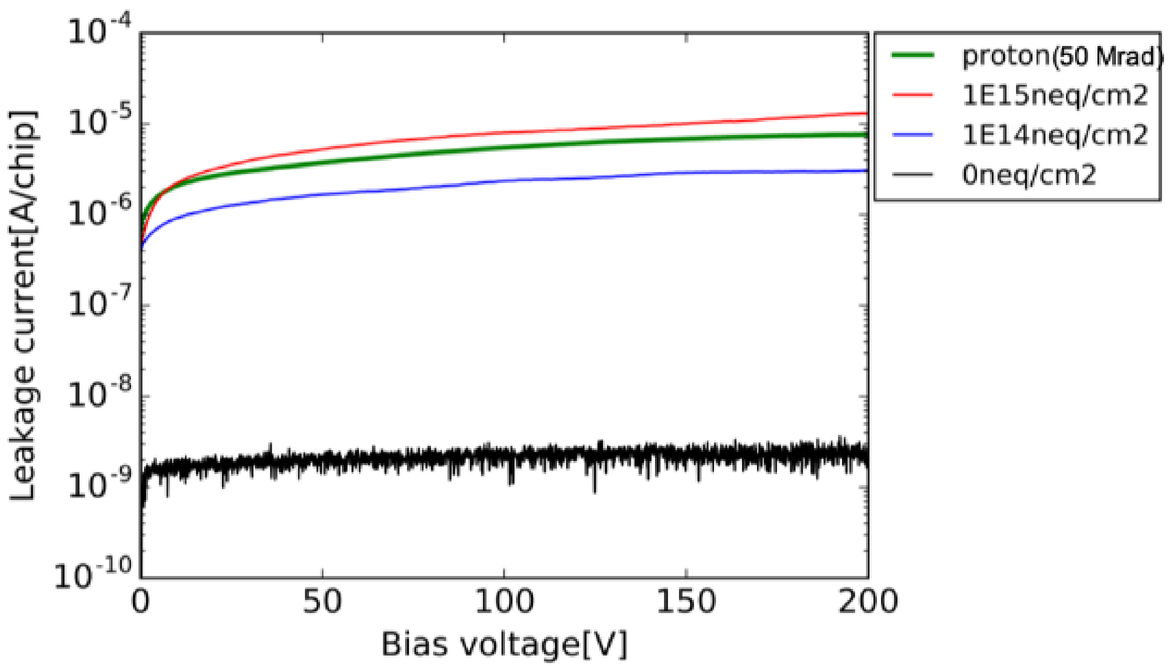
Z. Chen @CPPM



Threshold mapping

LF-MONOPIX1 : I-V curves

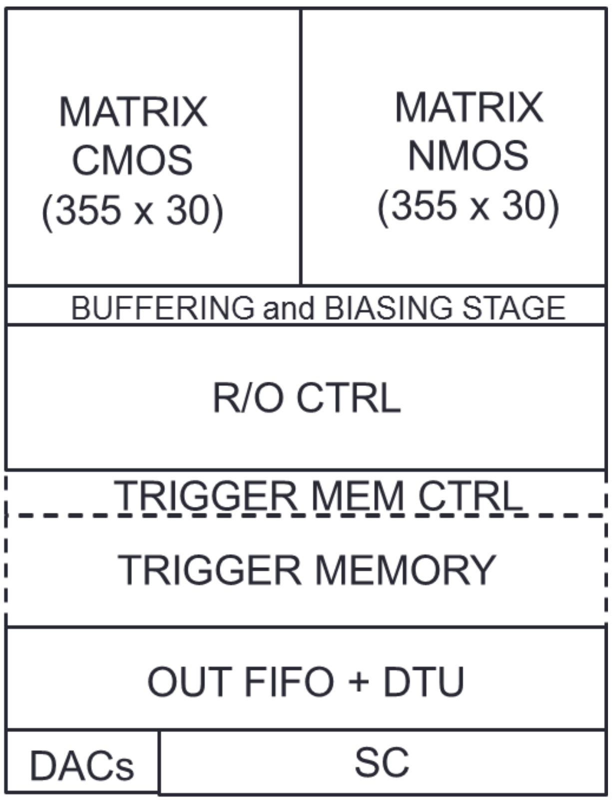
- High breakdown voltage > 200 V (low T°)
  - *Not influenced by* ***backside thinning and processing***
- **Acceptable leakage** increase after irradiation



Design towards LF-MONOPIX2

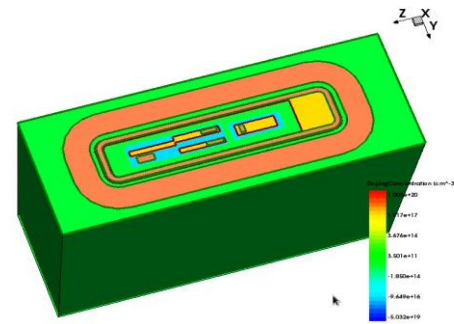
LF-MONOPIX2 circuit optimization

- Time walk
- Efficiency for thinned devices
- Sensor pixel size (smaller) and leakage current
- Electronic devices crosstalk
- Yield studies



<u>Design goals:</u>

- Matrix
  - Pixel size : **150µm x 50µm**
  - Fast and low power AFE
  - **Enhanced ToT** extraction
  - Full height approaching 2 cm
- Matrix RO control - same LF-Monopix1
  - **Enhanced BCID** distribution scheme
- Trigger memory
  - Same strategy as TJ-Monopix2
- Out FIFO and fast IO link (LVDS etc)
- Slow control – same as LF-Monopix1
- Develop digital chip assembly flow & chip verification flow
- Submission before end of **2019**



M. Zhao @IHEP

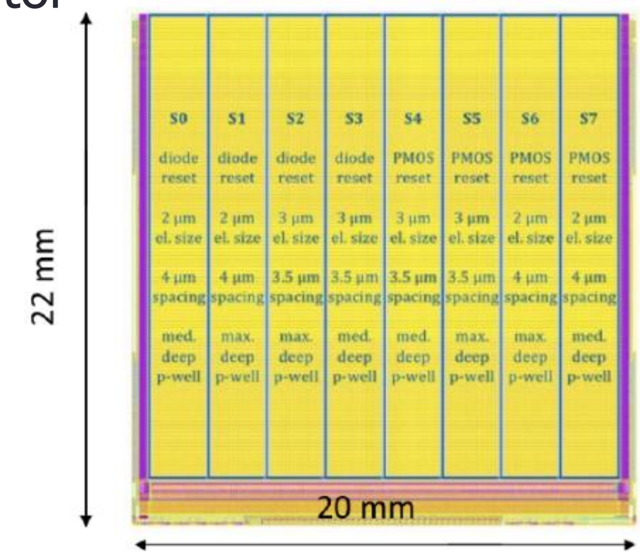
TJ DMAPS
Design of large-scale demonstrators

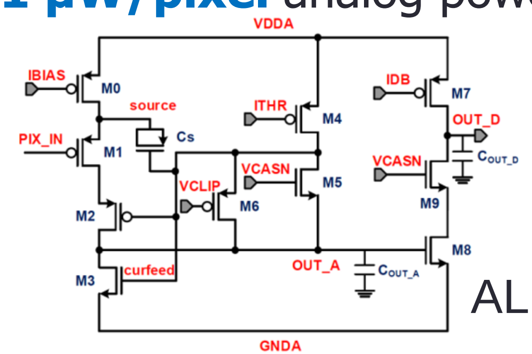
TJ strategy : Design of two full-scale demonstrators to match ATLAS specifications for outer pixel layers

- The “MALTA” chip
  - Analog front-end based on a previous design (ALPIDE) for the ALICE experiment
  - Novel asynchronous readout architecture to reduce digital power consumption and increase hit rate capability
- The “TJ-Monopix” chip
  - Front-end similar to the “MALTA” chip
  - Uses the well-established column drain readout architecture (experience from “FEI-3” LF-Monopix design)

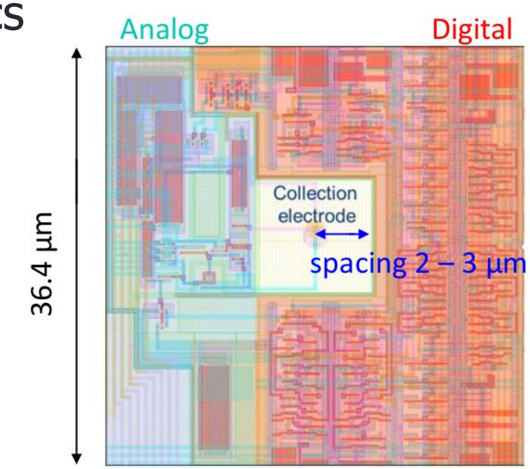
TJ MALTA : asynchronous architecture

- The TJ Malta is a 22 x 20 mm² full size demonstrator
  - 8 sectors with different pixel flavors
  - **Fully clock-less** matrix architecture
    - → low power
  - Charge information from time-walk
  - Pixel size 36.4 x 36.4 um²
  - **2-3 µm collection electrode**
  - → small input capacitance
  - 3.4 – 4 um separation between electrode and electronics → low cross-talk
  - **1 µW/pixel** analog power (75 mW/cm²)



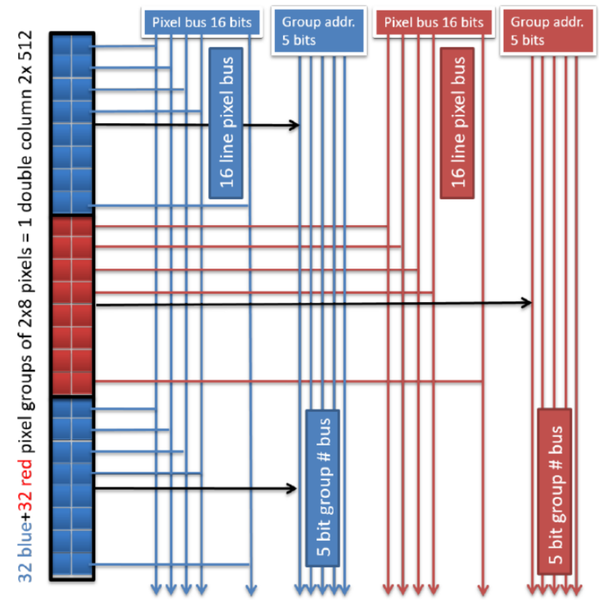


ALPIDE Front-End

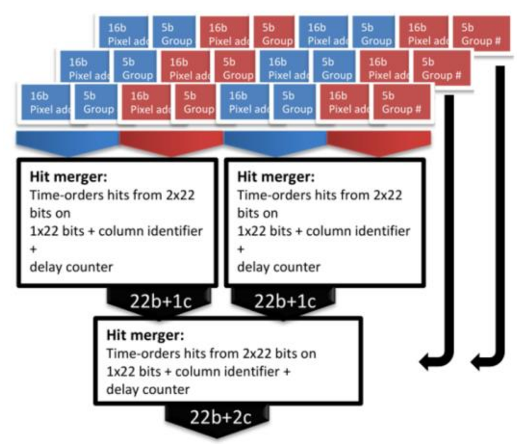


TJ MALTA : asynchronous architecture

- The TJ Malta is groups of 2x8 pixels with pattern assignment to reduce data size from clusters
  - Front-end discriminator output is processed by a double-column digital logic
  - Pulse width adjustable **between 0.5 ns and 2 ns**
  - Data are transmitted **asynchronously** over high speed us to the end of column
  - At the periphery, an arbitration and merging logic resolves timing conflicts of simultaneous signals
  - Timing information is kept by dedicated bits
  - Each hit is represented by a 40 bit word



*I. Berdalovic et al 2018 JINST **13** C01023*



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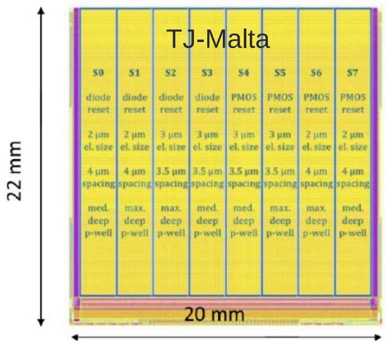
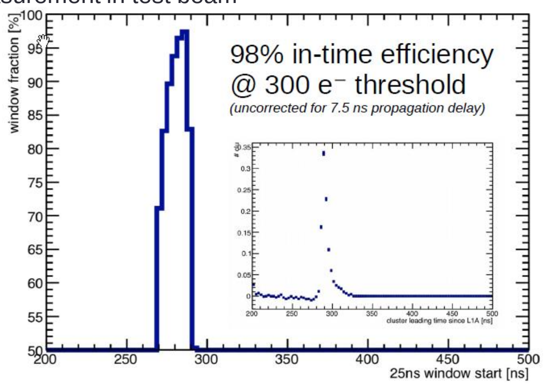
TJ MALTA and TJ MONOPIX : results

- Weakness understood: weak E field under electronics.
- Modification with (reactive!) founder → summer 2018 submission

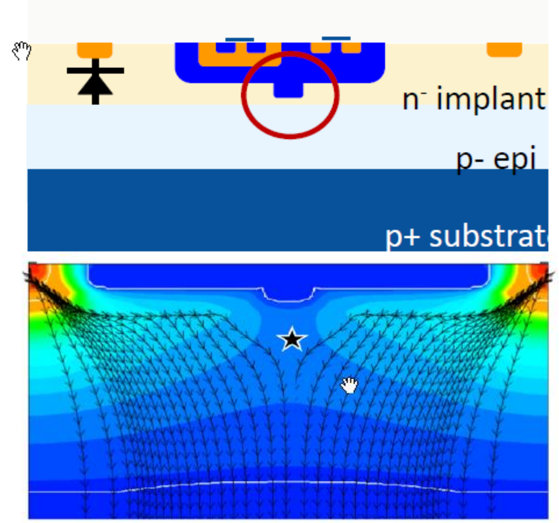


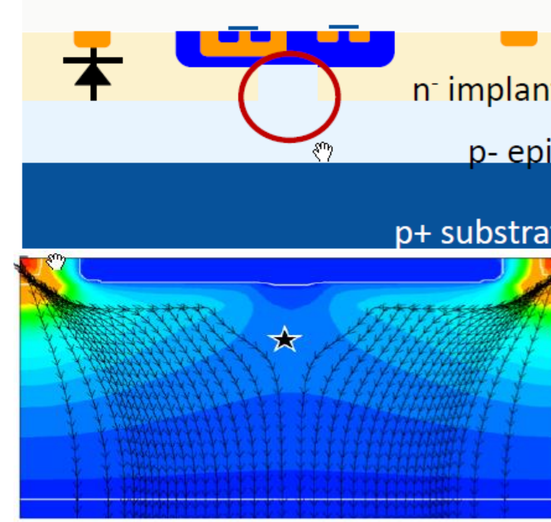
E.J. Schioppa, digital measurement in test beam



Modification1: Additional PWELL

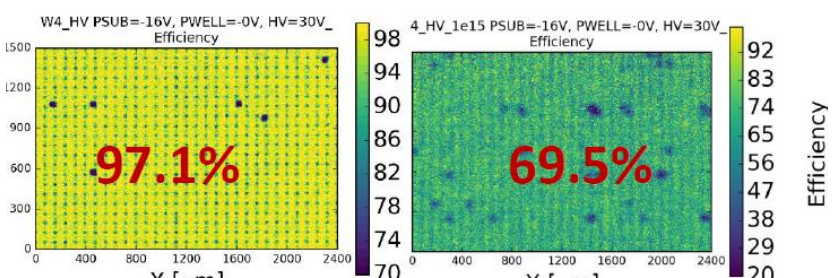
Modification2: Gap in n⁻implant



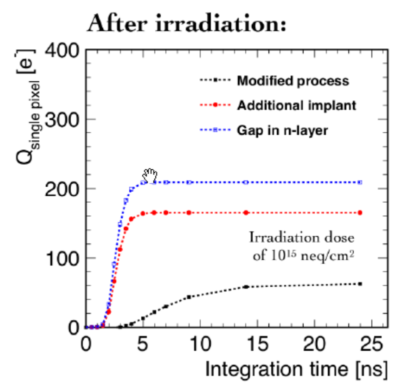


3D TCAD by M. Munker, CERN

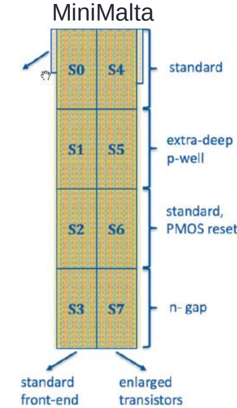
Un-irradiated Neutron irradiated



I. Caicedo, Bonn, summer 2018



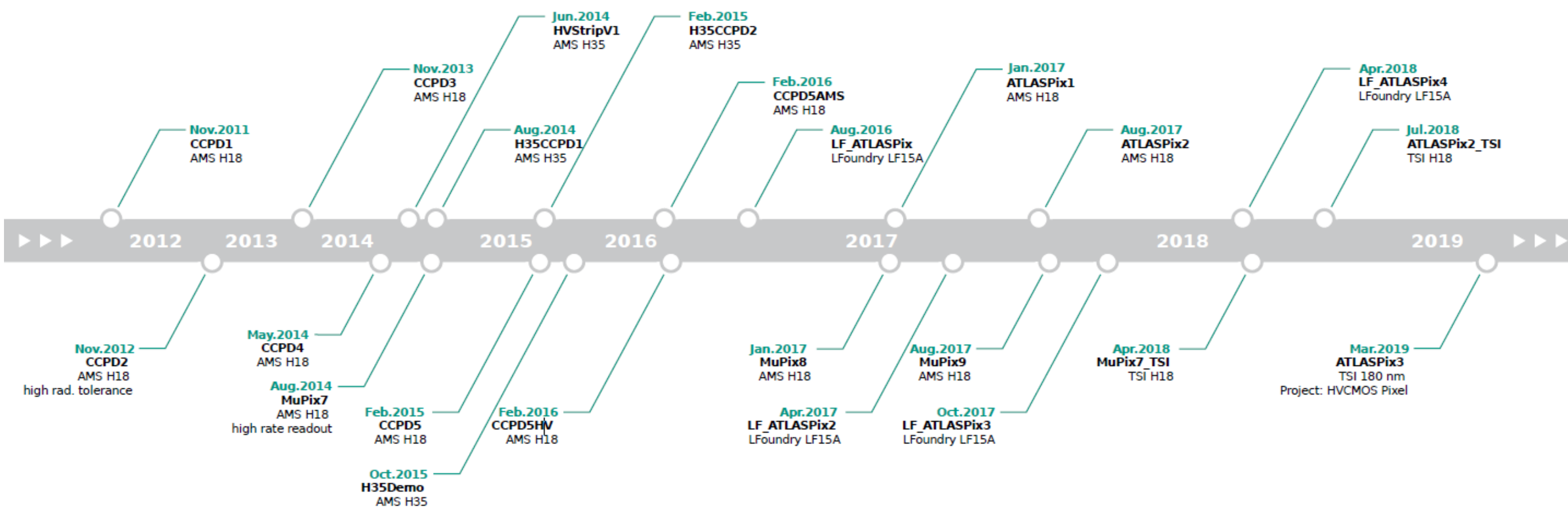
MiniMalta



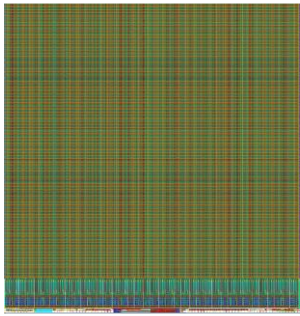
MiniMalta beam test ongoing, first indication very encouraging, more results soon

AMS/TSI DMAPS prototyping line

- Many prototypes since 2011. AMS 180nm processes no longer accessible. Development moved to **TSI 180nm**. TSI is very similar to AMS 180 nm.



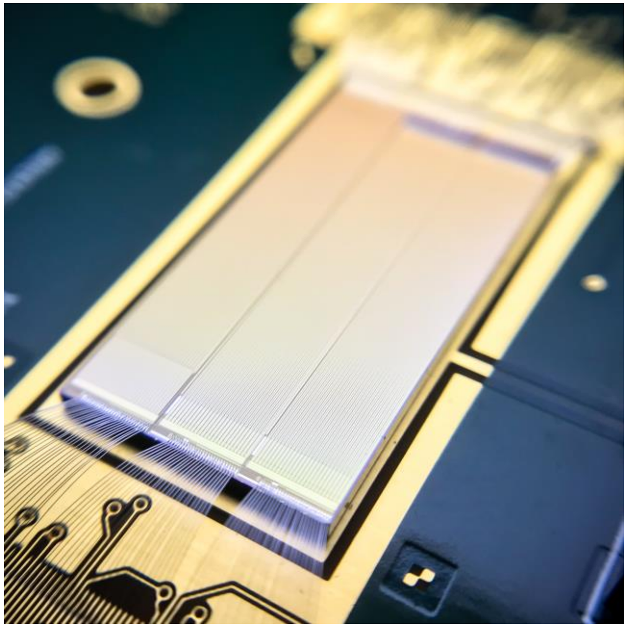
- The last version is the ATLASPix3, a **20.2mm x 21mm chip size** submitted in April 2019
  - Synchronous Column drain architecture
  - Pixel size : 150µm x 50µm
  - Matrix size : 132 x 372



AMS/TSI DMAPS : ATLASPix1 results

- **Results (no radiations)** **Requirements:**

- material budget:
  → 100 µm (50 µm possible) < 200 µm
- spatial resolution:
  → in y: RMS = 11.3 µm < 7 µm
  pixel size = 130 µm x 40µm
- timing resolution:
  → 6.8 ns at ~480e thres < 10 ns
- efficiency:
  → above 99.7% > 99.7-99.9%
  → no dead/masked pixels



Conclusion

- After 10 years of R&D, the Monolithic depleted CMOS sensor technology is entering a state of becoming a true contender with hybrid pixels
- The actual low cost technologies are showing good results and performances on large signal and fast charge collection by using rad-hard small pixel, and reduced material cost.
- The DMAPS offers a cost effective solution for large area coverage

Conclusion

- After 10 years of R&D, the Monolithic depleted CMOS sensor technology is entering a state of becoming a true contender with hybrid pixels
- The actual low cost technologies are showing good results and performances on large signal and fast charge collection by using rad-hard small pixel, and reduced material cost.
- The DMAPS offers a cost effective solution for large area coverage **BUT** option to use **DMAPS in ATLAS ITk L4 recently dropped out.**
- The high level of development and the closeness to specifications was recognized, but concern is that depleted CMOS diverts attention from main hybrid-like solution at a time when schedule is tight and several challenges still lay ahead for the standard solution.

Perspectives

- The **value of this technology for future applications makes no doubt**
  - Work continues with other targets:
    - Future application in ATLAS?
    - CepC, FCC-ee, Belle experiment, future hadron circular collider?
    - Timing layers, imaging applications (Synchrotron radiation imaging, Medical imaging during proton therapy …)
  - All contexts in which radiation hardness, high hit rate, speed is required.

- **Strong collaboration with our partners in various framework**

  (ACC, Bonn/CPPM/CERN/CEA-IRFU collaboration, CERN RD50…)