Design and performance of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS Semiconductor Tracker

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Abstract

The ABCD design is a single chip implementation of the binary readout architecture for silicon strip detectors in the ATLAS Semiconductor Tracker. The prototype chip has been manufactured successfully in the DMILL process. In the paper we present the design of the chip and the measurement results. The basic analogue performance of the ABCD design has been evaluated using a prototype SCT module equipped with the ABCD chips. The digital performance has been evaluated using a general purpose IC tester. The measurements confirmed that all blocks of the ABCD design are fully functional and the chips meet all basic requirements of the SCT.

Wafer screening has been performed using a customised wafer tester. The set-up allows measurements of all analogue and digital parameters at the nominal clock frequency of 40 MHz as well as evaluation of speed margins for the digital blocks.

The ABCD chips have been irradiated separately with X-rays up to a total dose of 10 Mrad, with neutrons from a nuclear reactor up to a fluence of 2×10^{14} n/cm^2 and with a high energy proton beam up to a fluence of 3×10^{14} p/cm^2. The test that were performed confirmed satisfactory radiation hardness of the DMILL technology and of the ABCD design up to the radiation levels expected in the SCT.

I. Introduction

Given a moderate spatial resolution requirement of the ATLAS Semiconductor Tracker (SCT) [1], a binary readout architecture can be employed for the silicon strip detectors. The main advantage of the binary readout system is a significant reduction of data to be read out as only addresses of channels which have recorded hits above the threshold are transmitted off the detector. For a big tracking system like the SCT this is an important aspect resulting in lower cost, reduction of the material required for the data transmission system, and simplified off-detector readout electronics. In order to perform data sparsification in the front-end electronics a very robust front-end readout system is required. Besides the usual requirements concerning the noise, speed and power dissipation, the channel to channel matching of gain and discriminator threshold become very critical issues.

Another aspect, particularly important for the binary readout architecture is the immunity of the overall system, and so of each component of the system, to the external and internal interference usually referred to as common mode noise. If one takes into account the irreducible noise sources present in the front-end system, i.e. the parallel and series noise sources of the preamplifier and the shot noise of the detector leakage current, an achievable signal-to-noise ratio is about 15 at the beginning of the experiment and about 10 after irradiation of silicon strip detectors and front-end electronics up to the doses expected after 10 years of LHC operation. With these signal-to-noise ratios there is a very little room for setting the discrimination threshold in such a way that the detector is fully efficient and the noise occupancy is well below the real data rate. Thus, any degradation of the signal-to-noise ratio will lead to either a drastic reduction of efficiency or an increase of noise occupancy.

The ABCD design is a single chip implementation of the binary readout architecture for silicon strip detectors in the ATLAS Semiconductor Tracker. The design follows a previously developed prototype, the SCT128B chip [2]. Functionally it is fully compatible with another technological

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option being developed for the SCT that employs two separate chips: CAFE [3] - a front-end chip realised in the MAXIM bipolar process and ABC [4] - a binary pipeline chip realised in the Honeywell bulk CMOS process. The BiCMOS DMILL technology [5], in which the ABCD chip is fabricated, makes it possible to implement the complete binary architecture, as required for the ATLAS SCT, in a single chip.

The first ABCD prototype chip met most of the specifications, however, the spread of the discriminator threshold in the front-end was not satisfactory. Analysis of the problem led us to the conclusion that given the intrinsic matching performance of the DMILL technology it would be difficult, if not impossible to guarantee the required performance by following the original circuit concept. In addition, the irradiation tests indicated that matching performance degraded significantly after irradiation. Therefore, we upgraded the design by implementing a threshold correction using a 4-bit digital-to-analogue converter (TrimDAC) per channel. In the end we have designed and manufactured two versions of the ABCD architecture: ABCD2T – employing the TrimDACs and ABCD2NT – following the original idea but with particular attention paid to the matching aspects in the front-end part. Both versions are fully functional and meet the specifications. The ABCD2T design offers, however, better robustness with respect to radiation effects and therefore this is the preferred options for the SCT. In this paper we focus mainly on the ABCD2T design and test results.

II. ABCD2T Architecture

Only a short overview of the architecture of the ABCD design is recounted here since it has been presented and described before [6]. The block diagram of the chip is shown in figure 1. It comprises all blocks of the binary readout architecture; the front-end circuitry employing a bipolar transistor in the input stage, discriminators, binary pipeline, derandomizing buffer, data compression logic and the readout control logic.

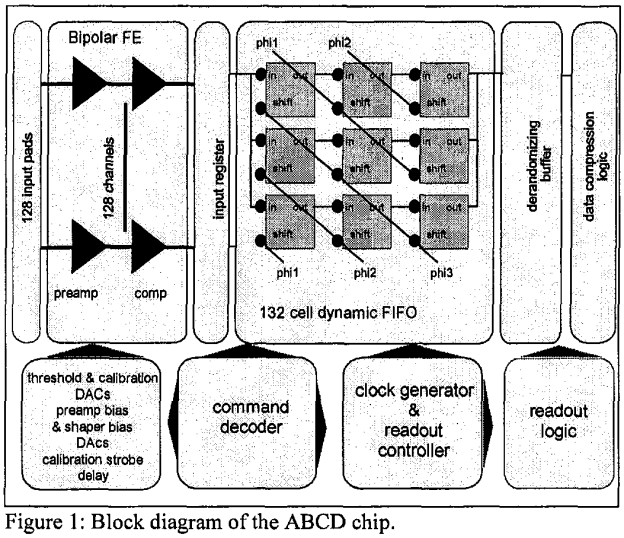

Figure 1: Block diagram of the ABCD chip.

The main blocks of the ABCD chip, the front-end, input register, pipeline, and de-randomizing buffer, are the same as have been prototyped before in the SCT128B chip. The details of these circuits can be found in [2]. Compared to the SCT128B architecture some new features have been introduced in the ABCD design. The most important one is the sparse readout logic which includes zero suppression on the chip so that only addresses of hit channels are read out.

The preamplifier-shaper circuit provides signals with a peaking time of 25 ns. This peaking time is sufficiently short to keep the discriminator time walk in the range of 15 ns and the double pulse resolution below 50 ns. It also provides a reasonable optimum for relative contributions of the series and parallel noise sources, given a total strip capacitance in the range of 15 – 20 pF. The preamplifier-shaper circuit is followed by a discriminator with a common threshold for all 128 channels which is controlled by an internal 8-bit DAC. In the ABCD2T design, in addition to the threshold control common for all channels, we have implemented individual threshold correction per channel using a 4-bit DAC (TrimDAC). The TrimDACs are used only for correction of the threshold offsets and after correction they are kept at fixed settings. The threshold scans which are used for extracting the basic analogue parameters of the front-end circuit are performed employing only the main 8-bit DAC that is common for all the channels on the chip.

The binary data from the discriminator output are latched in the input register either in the edge sensing mode or in the level sensing mode with a time resolution of 25 ns, and clocked into a 132-cell pipeline. The true edge sensing mode puts a more rigorous constraint on the timing performance compared to the level sensing but it minimizes the rate of data to be transmitted from the detector.

Upon receiving a trigger signal the data are transferred from the pipeline to the second level buffer, which is a dual-port static RAM array 128-bit wide and 24-word deep. For each Level 1 trigger signal three columns from the pipeline are stored in the derandomizing buffer, so that the buffer is effectively eight events deep. It removes the fluctuations from the Level 1 trigger rate distribution. The hit patterns from three consecutive events corresponding to each Level 1 trigger signal are held in the buffer pending the readout. The data is then compressed in the data compression logic according to one of four possible criteria and read out via a token ring allowing the read-out of six chips on one optical fibre.

In addition to the basic functional blocks mentioned above, the ABCD2T chip has a calibration circuit for the internal generation of calibration pulses. The amplitude of the calibration pulses is set by an 8-bit DAC and the delay of calibration pulses relative to the clock phase is controlled by a delay buffer with 5-bit resolution.

The chip uses two power supply voltages: 3.5 V for the analogue part and 4.0 V for the digital part. The measured power consumption per chip is 200 mW for the analogue section and 120 mW for the digital section at a clock frequency of 40 MHz, resulting in an average power less than 2.5 mW/channel.

The die area of the ABCD chip is equal to 6550×8400 μm^2. The front-end part is built mainly of bipolar devices and comprises about 30 000 components while the digital part comprises about 200 000 CMOS devices. The pitch of the input pads is 50 μm so that a pitch adapter is needed to match the detector strip pitch of 80 μm.

III. PERFORMANCE TESTS

Basic performance of the ABCD2T chips has been evaluated using the prototype SCT modules built of six chips and two daisy chained silicon strip detectors designed according to the SCT specifications. The chips were assembled on a ceramic hybrid and connected to the detectors in so-called centre-tap configuration, i.e. in the centre where the strips from the two detectors are joined together to form effectively 12.8 cm long strips. All basic parameters of the front-end circuit, gain, noise and offset were extracted from threshold scans for given input signals delivered form the internal calibration circuitry. The timing performance was evaluated from the delay scan of the calibration strobe signal. In all these measurements the data was transferred through the pipeline and readout buffer and read out at nominal clock frequency of 40 MHz.

The performance of the digital circuitry of the ABCD2T chips was evaluated using a general purpose IC tester. The logic functionality was verified against Verilog simulations and speed margins were evaluated for various blocks in the chip. The DAC characteristics were measured separately by probing DC voltages at the dedicated pads, which normally are not connected to the external circuitry on the hybrid.

A. TrimDAC performance

The principle of the TrimDAC operation for a single channel is illustrated in figure 2. The plot shows the results of the threshold scans for a given input charge and sixteen consecutive settings of the TrimDAC. As a result we obtain sixteen S-curves corresponding to sixteen values of the effective threshold of the discriminator. The actual discrimination threshold is the difference between the value set in the main 8-bit threshold DAC, which is common for all 128 channels in the chip, and the value set by the 4-bit TrimDAC, which is individual for each channel. For a perfectly linear TrimDAC one would expect the sixteen S-curves to be separated by the same value, which is not the case as shown in figure 2. At low TrimDAC settings one can notice a significant non-linearity, which degrades the resolution of the TrimDAC in this area, however, does not prevent one from using it for threshold correction. The non-linearity of the TrimDACs brings some complication to the trimming procedure since the correction factor for each channels has to be found from a look-up table instead of from a linear fit to the TrimDAC response characteristic.

Figure 3 shows the response characteristics of 128 TrimDACs in one ABCD2T chip. One can notice that besides the systematic non-linearity at the beginning there are some channels with large deviations of their characteristics from the expected shape. The distribution of non-ideal channels appears

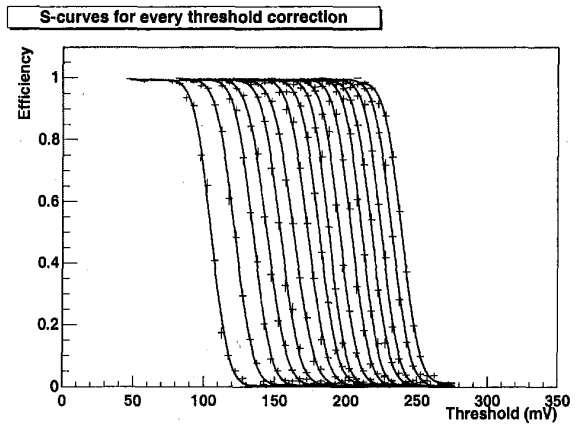

Figure 2: Example of threshold scans measured for 16 consecutive settings of the TrimDAC.

to be completely random and is a result of poor matching in the circuit that generates the correction voltage for the discriminator threshold. The TrimDACs, although non-ideal, can still be effectively used for correcting the threshold offsets. A typical distribution of threshold spread in one chip after offset correction is shown in figure 4. The threshold spread is reduced from a typical value of 12 mV rms before trimming to 3.5 mV rms after trimming. In figure 4 one can notice a few channels with offsets far from thecentral value.

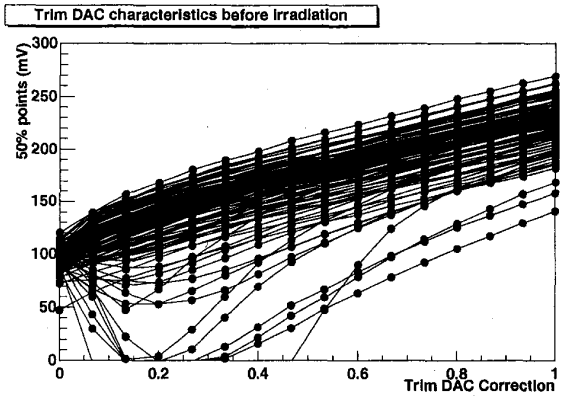

Figure 3: Response characteristics of 128 TrimDACs in one chip.

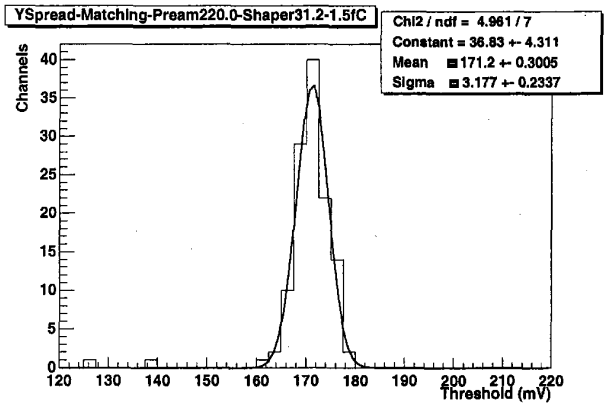

Figure 4: Distribution of threshold after correction in one ABCD2T chip.

These are non-trimmable channels for which the range of the TrimDAC characteristic does not cover completely the initial offset spread.

B. Noise performance

A goal of the binary readout architecture is to keep the threshold spread negligible compared to the noise value for a full strip length. In order to evaluate the noise performance of the ABCD2T chip we built a module with six ABCD2T chips and two daisy-chained silicon strip detectors. Five chips were fully bonded to 12.8 cm long strips, while for one chip in the centre of the module 1/3 of the channels were bonded to 12.8 cm strips, 1/3 of the channels to 6.4 cm strips and 1/3 of the channels were left with open inputs. The rms noise across the module is shown in figure 5. One can notice the regions with open inputs and with 6.4 cm strips in the centre of the module. The noise numbers were extracted from the S-curves obtained as the result of threshold scans for given input signals. The noise is very uniform across the whole module and the average numbers are 14.4, 10.3, and 5.5 mV rms for 12.8, 6.4, and 0 cm region respectively. The few channels for which the noise appears much lower are the non-trimmable channels. The fit to the S-curve for these channels usually fails delivering an artificial value of noise. A comparison of the noise of 14.4 mV rms for 12.8 cm strips with the threshold spread of 3.5 mV rms shows clearly that the threshold spread is negligible compared to the noise and as such, it will not affect the efficiency or the noise occupancy.

From threshold scans taken for different input signals one can extract the gain of the linear part of the circuit in front of the discriminator. For the bias conditions as used for the noise measurements shown in figure 5 the average gain for the whole module was 64.5 mV/fC. Given this value of gain one obtains the ENC as 526, 984 and 1376 electrons rms for 0, 6.4, and 12.8 cm strip length respectively.

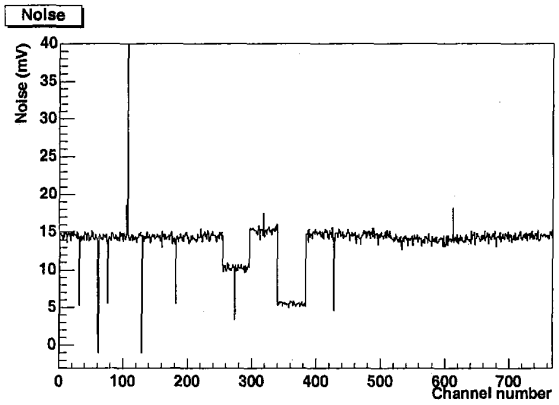

Figure 5: Noise distribution across the module.

C. Timing performance

For the binary readout it is required that the physical events are uniquely associated with the beam crossings which at the LHC happen every 25 ns. This is in the same range as the charge collection time in silicon strip detectors, so it is impossible to resolve two signals on any given strip from two adjacent beam crossings. Due to low occupancy in the silicon tracker, of the order of 1%, probability of such a pile-up is very low. Nevertheless, in order to be able to associate properly the data with the beam crossings, we require that the response of the electronics for a single event is accurate within 25 ns. The main issue for this requirement is the time walk of the discriminator. Given the limitations imposed by the fact that the front-end electronics has to be built in the form of ASICs we have employed a simple leading edge discriminator. A consequence of this is a relatively large time walk because of the large range of amplitudes of the signals from single strips, which in addition to the Landau distribution, includes the effects of charge sharing between the strips, mainly due to inclined tracks and the high magnetic field.

A working requirement assumed for the SCT electronics, which should guarantee full efficiency, specifies the time walk to be below 15 ns for the nominal threshold setting at 1 fC with the range of input charges between 1.25 fC and 10 fC. The results of measurements for 128 channels in one ABCD2T chip connected to the full length strips is shown in figure 6. On average the measured time walk is within the specification, however, we see some spread of the time walk between the channels, which is not due to spread of the speed of the circuit but due to threshold spread. Thus, in addition to noise and efficiency, another important specification is impacted by the threshold spread.

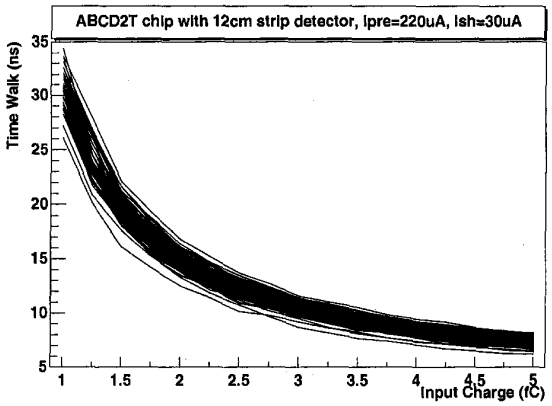

Figure 6: Walk time for 128 channels in one chip.

D. Performance of digital circuitry

The detailed testing of the digital part of the ABCD2T chip was performed using a general purpose IC tester. During measurements of the analogue parameters the data was read out through the pipeline, readout buffer and data compression logic at nominal clock frequency of 40 MHz so these measurements provided a proof of the basic functionality of the digital circuitry. The command decoder was also exercised extensively while taking threshold and delay scans at various bias conditions. However, not all of the functional blocks of the digital circuitry are used in the normal data taking mode so there is a need to perform dedicated digital tests. Therefore detailed testing of the digital part was performed using a general purpose IC tester. These tests allowed us to verify the chip functionality against Verilog simulations and evaluate the speed margins for various digital blocks and various modes of operation. Given the very high radiation dose expected in the SCT we have to anticipate degradation of speed in the digital

circuitry so non-irradiated chips should work at a sufficiently higher frequency than nominal.

For the basic design evaluation the following digital tests were employed:

Test 1: L1/BC counter check

Test 2: Configuration check

Test 3: L1 buffer overflow/error check

Test 4: Data taking; single hit test

Test 5: Data taking; consecutive multiple hits test

Test 6: Data taking; random multiple hits test

Test 7: Data taking; accumulator test

Test 8: Data taking; data compression mode

Test 9: Data taking; pipeline scan

The speed margins were evaluated in two test modes: (a) at the nominal supply voltage of 4 V the clock frequency was increased up to the point where the chips failed to respond correctly, (b) at the nominal clock frequency of 40 MHz the digital supply voltage Vdd was decreased down to the value where the chips failed to respond correctly. The results of both tests for five randomly chosen chips are shown in Table 1 and Table 2.

Table 1.
Maximum operating clock frequency in [MHz] for digital tests at nominal digital supply voltage Vdd = 4 V.

Test	Chip #1	Chip #2	Chip #3	Chip #4	Chip #5
1	77.7	77.7	84.2	78.4	71.4
2	76.2	76.2	79.2	75.5	68.4
3	67.8	67.7	79.2	75.5	67.8
4	68.4	68.7	79.2	75.5	68.4
5	69.0	67.2	79.2	76.2	69.0
6	68.4	66.7	79.2	75.5	68.4
7	67.8	66.7	79.2	75.5	68.4
8	67.8	66.7	79.2	75.5	67.8
9	67.8	66.7	79.2	75.5	68.4

Table 2.
Minimum operating digital supply voltage Vdd in [Volts] for digital tests at nominal clock frequency of 40 MHz.

Test N	Chip #1	Chip #2	Chip #3	Chip #4	Chip #5
1	3.01	3.01	3.01	2.98	3.01
2	3.01	3.01	3.01	2.98	3.01
3	3.01	3.01	3.01	2.97	3.01
4	3.01	3.01	3.01	2.97	3.01
5	3.01	2.98	3.01	2.97	3.01
6	3.01	3.00	3.01	2.97	3.01
7	3.01	3.00	3.01	2.98	3.13
8	3.01	3.01	3.01	2.98	3.01
9	3.01	2.98	3.01	2.98	3.11

One can notice a quite consistent behaviour for all tested chips with respect to both parameters, the maximum operating frequency at nominal supply voltage and the minimum supply voltage at the nominal clock frequency. The observed margins appear to be sufficient to cover the speed degradation of the CMOS circuits after irradiation. The details of the radiation tests are presented later in section V.

VI. Wafer Screening Results

In order to be able to qualify good die we have developed a custom wafer screening system. The system provides the capability to test the analogue and digital performance of the chips as well as to evaluate the speed limits for the digital circuitry. The test features implemented in the ABCD2T chip facilitate the measurements of all basic analogue performance specifications, i.e. gain, noise and threshold spread while the communication with the chip is performed via a digital serial interface. There is no need to send or receive any analogue signals to complete this part of the test. This chip feature makes it easier to build a robust wafer test system.

The system is based on an automatic probe station and a custom readout electronics. The probe card is made in a standard needle technology with a custom design of buffering circuits which are placed on a PCB close to the needles. With this technique the system works robustly at a clock frequency of 50 MHz. A more detailed description of the system and the test procedure can be found in [7]. Here we present only a few selected results.

Since our custom readout system is not as flexible as the dedicated IC tester, which we used for the detailed design evaluation, we use only two clock frequencies, 40 MHz and 50 MHz. The analogue parameters were measured at the nominal clock frequency of 40 MHz and the nominal supply voltages. The speed margins of the digital part were evaluated by testing the chips at 50 MHz and a lowered supply voltage Vdd. Figure 7 shows the results of digital tests for one wafer. On the map we plot the difference between the nominal supply voltage of 4 V and the actual supply voltage for which the chip still works correctly at 50 MHz. One can see that majority of chips have a good margin of about 0.5 V with respect to the supply voltage.

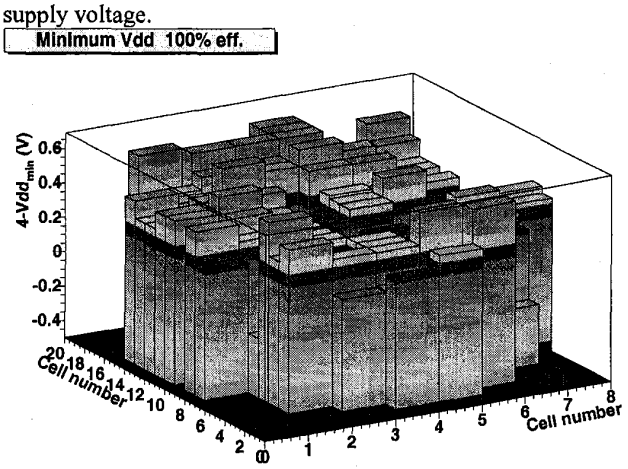

Figure 7: Wafer map of the digital voltage supply margin for which the chips work at 50 MHz.

Combining the results of digital tests at 50 MHz and the results of measurements of analogue parameters of the front-end circuit, measurements of all the DACs in the chip and measurements of analogue and digital power consumption we can plot the yield as a function of Vdd. Figure 8 shows an example of such a plot for one wafer.

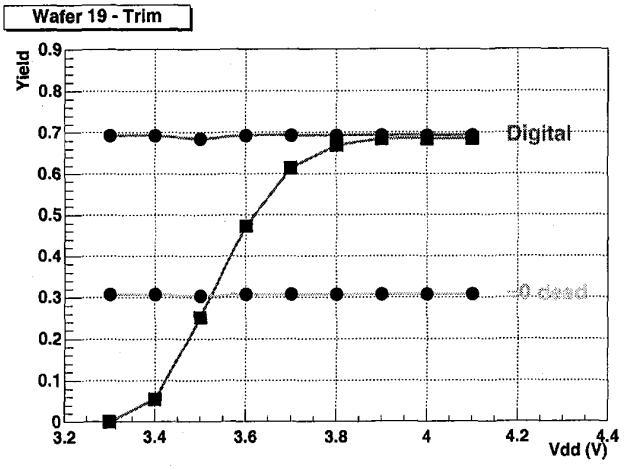

Figure 8: Yield as a function of the digital supply voltage

V. IRRADIATION TESTS

The ABCD2T chips have been irradiated in three different experiments:

- with a 24 GeV proton beam using the T7 irradiation facility at CERN PS accelerator,
- with neutrons from the nuclear reactor at Ljubljana,
- with X-rays of 10 keV using a standard X-ray facility at CERN.

The proton and the neutron irradiation have been performed for the chips mounted on the ceramic hybrids of the same type as used in the evaluation module. On each hybrid there was six chips, three ABCD2T chips and three ABCD2NT chips. In this paper we discuss only the results obtained for the ABCD2T chips with the TrimDACs since this option has been chosen for further evaluation. During irradiation the chips were biased and clocked at nominal conditions and the trigger signal was sent in order to exercise all readout blocks in the chips in a way similar to how they will work in the experiment.

During proton irradiation the hybrid with the chips was kept inside a cold box filled with nitrogen at a temperature of about 2°C, while the measured temperature of the hybrid was higher, about 10°C. The proton beam about 1×2 cm^2, was scanned across the hybrid. The chips were irradiated up to a fluence of 3×10^{14} p/cm^2 during a period of 10 days. The measurements were taken every one or two days, depending on the beam intensity. All basic parameters and characteristics were measured, including the noise and threshold spread, for various bias currents in the input transistor.

During the neutron irradiation the chips were biased and clocked in the same way as during the proton irradiation, however, the thermal conditions were different. The chips were not cooled and the temperature of chips was about 40 °C.

The X-ray irradiation was performed for single chips mounted on an evaluation board. The chips were biased and clocked in a standard way. In the X-ray test we focused on testing the performance of the CMOS digital part of the chip.

In the radiation tests performed until now no particular annealing procedure was applied. The measurements were taken during irradiation or immediately after irradiation. This represents a worst case for the CMOS part since the radiation induced effects in CMOS components exhibit some annealing, which naturally would take place during irradiation with a lower dose rate. For the bipolar components the tests that were performed represent an optimistic scenario because of the dose rate effect, which for bipolar devices means that a higher dose rate is less damaging than an irradiation up to the same total dose but with a lower dose rate.

A. Basic functionality

It is important to note that all the results presented were obtained from standard test procedures in which the signal passes the whole data chain, from the internal calibration circuitry through the front-end, pipeline, and the readout circuitry. Given extreme radiation levels, which we used in our tests, a first question was whether there were any catastrophic failures in the chips which would prevent us from detailed measurements of the chip parameters. For all the irradiations we performed we did not observe any such failure in the ABCD2T chips, i.e. the analogue parts remained biased correctly and the digital parts worked at least to 40 MHz.

B. Noise

The irradiated chips have been measured with open inputs so that the capacitance at the preamplifier input can be neglected in a first approximation. Thus, the equivalent noise charge is determined by the parallel noise sources, i.e. thermal noise of the feedback resistor and the shot noise of the base current. Assuming that the changes of the feedback resistor after irradiation are negligible, one can associate the increase of noise with a higher base current due to degradation of β in the input transistor.

Figure 9 shows the noise as a function of the current in the input transistor. The average noise for 128 channels in one chip is shown. After X-ray irradiation we see a small increase of noise as expected since we do not expect a significant degradation of β in this case. For the chips irradiated with relativistic protons up to a fluence of 3×10^{14} p/cm^2 the increase of noise is significant. The largest increase of noise is observed after neutron irradiation up to 2×10^{14} n/cm^2. Assuming that the shaping function of the overall front-end circuit can be approximated by a CR-RC^3 filter with a peaking time of 25 ns one can evaluate the β values corresponding to the measured noise levels to be about 60 after proton irradiation and about 30 after neutron irradiation.

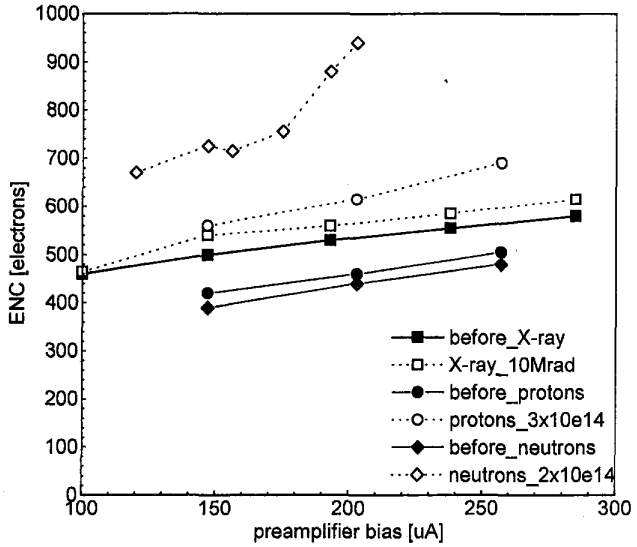

Figure 9: Noise as a function of the current in the input transistors after X-ray, proton, and neutron irradiation.

C. Matching

The irradiation tests were supposed to provide answers for two questions regarding the influence of irradiation on the matching of device parameters:

- does the matching degrade after irradiation and,

- if so, is the range of the TrimDACs sufficient to cover the post radiation offset spread.

Figure 10 shows the distributions of discriminator threshold for 128 channels in one chip before irradiation (without correction), after proton irradiation up to a fluence of 3×10^{14} p/cm^2 (without correction), and after irradiation with threshold correction using the TrimDACs. One can notice a very significant degradation of threshold spread, by a factor of 3.5, after proton irradiation. After irradiation the TrimDACs work correctly and for the majority of channels the offset can be corrected, however, some channels remain outside the range of the TrimDACs.

A similar behaviour of threshold spread was observed after neutron irradiation, however, the effect was smaller. After a fluence of 2×10^{14} n/cm^2 the threshold spread increased by a factor of 2 and in this case the range of the TrimDACs was sufficient for effective correction of the threshold in all of the channels in the chip.

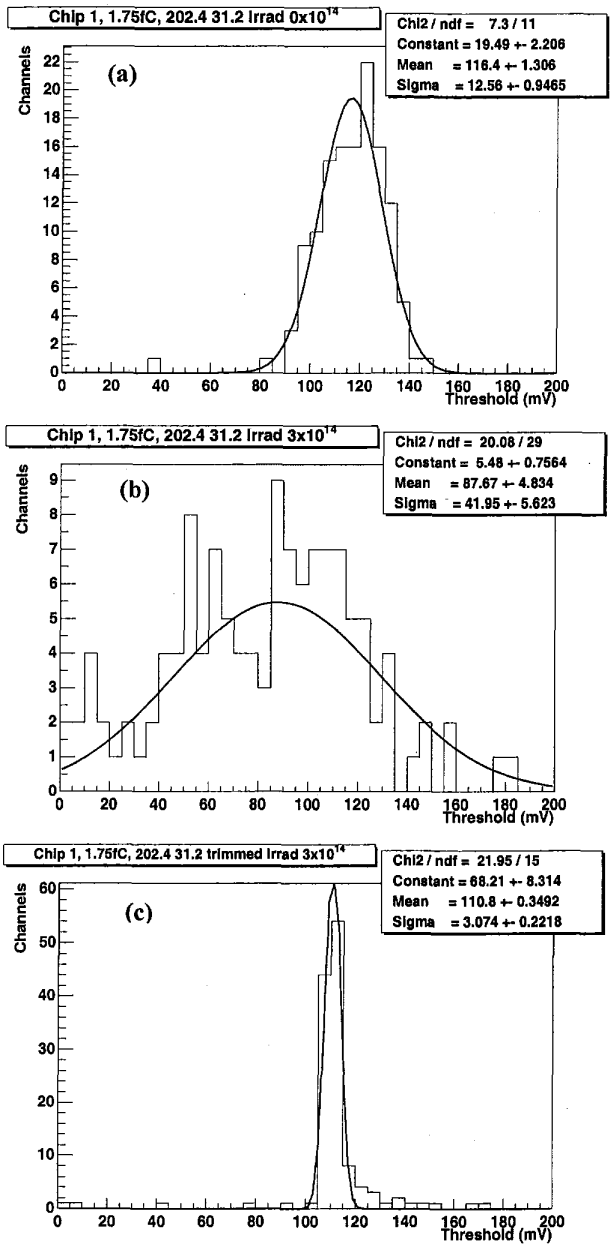

Figure 10: Threshold spread: (a) before irradiation without trimming, (b) after proton irradiation without trimming, (c) after proton irradiation with trimming.

D. Performance of digital circuits

Regarding the radiation effects in the digital CMOS circuitry of the ABCD2T chip, a main concern is the speed, i.e. the maximum clock frequency at which the chip performs all operations correctly. Since the speed of the CMOS circuits depends on the power supply there are two parameters which provide information about the speed margins of the ABCD2T chip:

(a) maximum speed measured at the nominal supply voltage of 4 V,

(b) minimum supply voltage at which the chip works correctly at 40 MHz.

Figure 11 shows the degradation of speed of the ABCD2T chip after X-ray irradiation up to a total dose of 10 Mrad. The results are shown for the following digital tests: TEST 1 - L1/BC counters check, TEST 2 - configuration check, TEST 3 - L1 overflow check, TEST 4 - data taking.

We observe a degradation of speed almost by a factor of 2, nevertheless, after 10 Mrad the chip still meets the requirement of 40 MHz at the nominal supply voltage. It is worthwhile to note that the results shown in figure 11 do not include any

annealing so that they represent worst case post-radiation conditions.

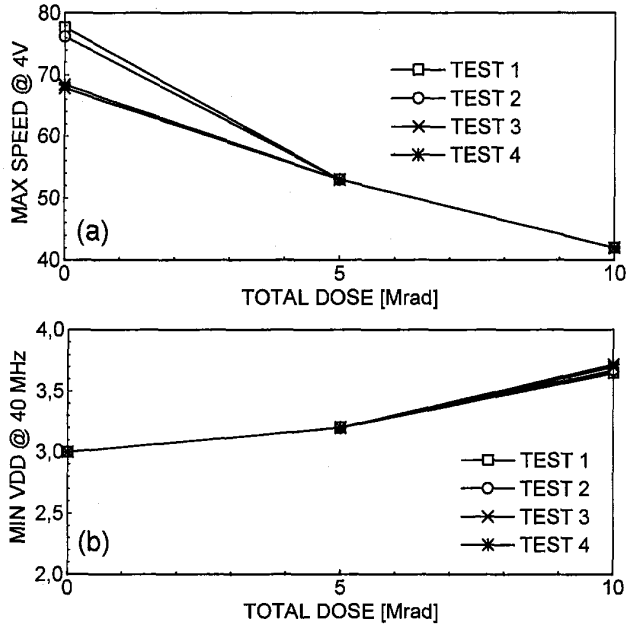

Figure 11: Maximum speed at supply voltage of 4 V (a) and minimum supply voltage at 40 MHz (b) as a function of total ionising dose.

VI. CONCLUSIONS

A complete prototype ABCD2T chip with individual threshold adjustment per channel for the binary readout of the ATLAS Semiconductor Tracker has been developed in the DMILL process. Detailed evaluation of analogue and digital performance of the chip has confirmed that it satisfies all basic requirements of the ATLAS SCT detector. A minor problem resulting in non-ideal characteristics of the TrimDACs has been identified and will be easy to correct in the next prototype.

Fully functional modules using the ABCD2T chips and SCT silicon strip detectors have been built and tested in the lab and in the test beam. Extensive irradiation tests of the ABCD2T prototype chips confirmed satisfactory radiation hardness of the design and of the DMILL technology, in which the chip has been realized. The individual threshold adjustment per channel implemented in the ABCD2T design has proved to work satisfactorily after irradiation.

VII. REFERENCES

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