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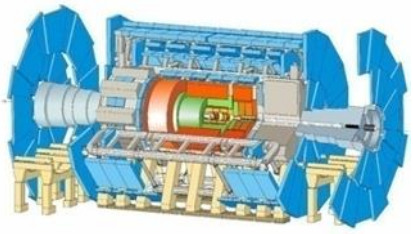

ATLAS

Discussion for IHEP Production Plan of 5k HGTD Modules

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IHEP HGTD Module Group meeting

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Introduction

Aim of this talk is just “cast a brick to attract a jade” (抛砖引玉)，to create a beginning for the details tasks discussion among the HGTD module group

All info come from the public, it’s impossible to make HGTD production plan at current status: since no any tasks details discussion about what we should do and how we can do, what equipment locally available for the production, especially no any time estimation on each step of the production. All these things should be discussed deeply at the HGTD module group weekly meeting to make them more and more clearly and feasibly

How many module will produced (assembly+QA) per day

Assuming to finish 5k (1/2 of 10k total) modules in 1.5 years:

There are 1.5* (365 day – 104 weekend -11 festival) =1.5*250days= **375 days**

Considering 80% time for production and test scheduled time, leave **20%** time to compensate any accident and delay. (extreme case we also can use weekends~**40%**)

So module number averagely finished(including assembly and tests) per day:
5000/(375*0.8) = 5000/300 = **16.7 modules/day** or **17.9 modules/day** (**10711** modules)

Somewhere mentioned: ~4 modules/day/site, if according to this rate, we only can contribute ≤1/8 of HGTD, **why we decide 1/2 modules contribution?**

New (reduced) baseline is 10.7MCHF (including 1 MCHF for TDAQ). It assumes:
- 5% pre-production for most components (all good to be used in the detector)
- 2 modules per HV line (instead of 1)
- A production model for modules production ,sensors, asics leading to a produced amount of modules = 10711 (instead of 12000 assumed in the TDR draft 1)
- If 12000 modules were considered and 1HV channel/module HGTD Core would increase by 1MCHF. From 08/April/2019 3-Day HGTD Meeting Introduction A. Henriques, L. Serin

From 3-Day HGTD Meeting Introduction A. Henriques, L. Serin 08/April

New Core costs table baseline for TDR

PBS/WBS	HGTD Deliverable	TDR Cost (KCHF)	TP cost	(TDR-TP) KCHF	Cost TDR/TP	Nominal Quantity (NQ)	Purchased Q (NP)	NQ/NP	prod model
8.1	**Sensors**	**2275**	**1700**	**575**	1,3	7 984	10790	1,35	7984/.74+0% pre-prod
8.2	**Electronics**	**3199**	**2744**	**455**	1,2				
8.2.1	ASIC	833	730	**103**	1,1	15 968	26950	1,69	2x10790/.80 +0% pre-p
8.2.2	Peripheral Electronics cards	767	717	**50**	1,1	160	180	1,13	
8.2.3	High Voltage power supplies ; crates	532	897	**-365**	0,6	84 ;	88;	1,05	
8.2.4	LV in US15 ; DCDC(300->10V) ;crates	299	400	**-101**	0,7	14; 28 ; 4	16;32 ; 4	1,14 ; 1,14	
8.3	**Luminosity/TDAQ**	**395**	**280**	**115**	1,4				
8.3.1	Luminosity boards	315	200	**115**	1,6	20	21	1,05	
8.3.2	DCS and Interlocks	80	80	**0**	1,0				
8.4	**Module assembly and staves Loading**	**1483**	**1500**	**-17**	1,0				
8.4.1	Bump-bonding ASIC/Sensor	450	900	**-450**	0,5	7984	10790	1,35	
8.4.2	Flex cables	547	400	**147**	1,4	7984	10790	1,35	
8.4.3	Modules assembly	386	100	**286**	3,9	7984	10790	1,35	
8.4.4	Modules loading on staves/plates	100	100	**0**	1,0				
8.5	**Mechanics, Services and Infrastructure**	**2264**	**1305**	**959**	1,7				
8.5.1	HGTD hermetic vessel	160	150	**10**	1,1	1	1	1,00	
8.5.2	Moderator	0	0	**0**		4	4	1,00	
8.5.3	On detector cooling/support plate	180	155	**25**	1,2	8	8	1,00	
8.5.4	CO2 +water Cooling + Nitrogen systems	1237	450	**787**	2,7				
8.5.5	Tools for assembly and installation	100	100	**0**	1,0				
8.5.6	Services (cables,fibers,connectors,..)	526	450	**76**	1,2				
8.5.7	Patch panel boxes	61	50	**11**	1,2				
8.6	**Detector Assembly and QA on surface**	**100**	0	**100**					
8.6.1	Test bench for detector certification	100							
HGTD TOTAL		9716	**7529**	2187	1,3				
(*) TDAQ total		995	970	25	1,0				
HGTD+TDAQ		10711	8499	2212	1,3				

exchange rates to be used for HGTD TI
1 Euro=1.085 CHF
1 USD =0.986
Japanese Yen [100 JPY]=0.942
Chinese Yuan [CNY]=0.1461

Module assembly total cost
1383 kCHF, ~9.5M yuan
1/7 relative to HGTD TOTAL

1CHF=6.845 Yuan
Now: 1CHF=6.934 Yuan, -1.28%

HGTD TOTAL 66.51M Yuan

Content of HGTD Module production

Distilled by Kevin on 08/April/2019:

Need to develop a much more detailed production plan for the ~10K modules needed - bottom-up time to assemble and test modules => number of assembly and testing sites => how much time and manpower is required to build and test ~10K modules ? Historically, the testing development is complex and requires significant specialized hardware, and the time required in production for testing is significantly underestimated.

HGTD TDR(ATL-COM-UPGRADE-2019-003): Sec.7 Module Assembly and Loading:

A HGTD **module assembly**, consists of **a sensor bump-bonded** to **two readout chips** which are in turn connected to a **flexible printed circuit** (**FPC, flex cable**) for communication, power distribution and data output. The flex cable also provides high voltage for the silicon sensor. Modules quality assurance (**QA**) by various control tests are necessary.

Module Production == module assembly + module QA

Module assembly == Bare module assembly (1 15x30 sensor + 2 15x15 ASIC **bump-bonding/** hybridization process) and to **be connected** on **FPC**

Module QA == various **tests and inspections** at each quality control step/stage

How much average time a bare module assembly will take ?

A bare module assembly: made by sensor, ASIC, and bump bonding foundry, how long a bare module assembly finish averagely ?

- **A LGAD sensor** has a total size of 20.0mm x 39.5mm, with an array matrix of 15 x 30 1.3mm x 1.3mm pads,produced in 150mm wafers, current baseline: active and total thickness is 50 μm and 300 μm. After under-bump metalization (**UBM**) the wafers will be diced and the selected sensors will be destined for hybridization.
- **An ALTIROC ASIC** has a total size of 21.7mm x 19.9mm and a matrix of 15x15 channels, produced in 200mm wafers with current baseline thickness is 300 μm. The chips will be probed to identify the good dies. This will be followed by **UBM** and **solder bump deposition**
- **A bump-bonding (hybridization process):** an LGAD sensor interconnected through solder bumps to two ALTIROC front-end chips. The **flip-chip process** is the final step in the hybridization procedure.
- The baseline bump-bonding technology for HGTD relies on **solder bumps.**. Inspection of the bare assemblies with a high resolution (sub-micron) **x-ray machine** to discard devices with disconnected pad bumps

More specification pls see HGTD TDR (ATL-COM-UPGRADE-2019-003)

Production hybridization strategy

Full size tests will be carried out as soon as the **final sized sensor and ASIC** become available. However, an effort is being made to advance this critical step in module assembly to **avoid** possible **bottlenecks** later in the overall activities.

The specifications have already been provided to **two companies** (one in **Germany** an done in China) and discussions of a possible early qualification of the bump bonding process with the currently available devices (**ALTIROC1**) is being discussed.

The possibility of using **dummy ASICs and sensors for the vendor qualification** will also be investigated.

The target is to eventually carry out **the final hybridization qualification** on two to four companies, though the impact on cost and schedule will have to be evaluated.

How much average time all QA tests/inspections will take ?

Mechanical testing: (equipment, environment, manpower, technical operation ?)

- ✓ **Bump shear force**: typical **60 gr/bump**
- ✓ **thermal cycling tests**:
  1. IFAE fromat : about **1 week** of: **4 hour** cycles between **-30C and +120C**, **1000gr shear test before and after cycling.**

  2. TDR-HGTD format: **2 weeks** the modules will be thermally cycled between **–40 C and 130 C**. The solder connections will be then verified with **x-ray imaging** and **shear tests** were carried out on the modules. The devices should be able to sustain the maximum applied **shear force of 1000 gf**. And should sustain a **perpendicular (with respect to the plane of the sensor) pull test of 100 gf before and after the two week thermal cycling**.
- ✓ **Wire bond tests**: typical **8 gr/wire**;

More QA inspection

1. Bare modules will be **optically inspected and weighted**.

2. The **distance** between the substrates (**dump height**) will also be **measured**.

3. **Inspection with x rays for disconnected channels** before module assembly (dressing with the flex hybrid) will follow. If the yield of the bump-bonding process is found to be high after the initial production and the modules are found to be highly uniform, these time consuming steps (X-ray inspection and substrate separation) can be performed only on a small fraction of devices.

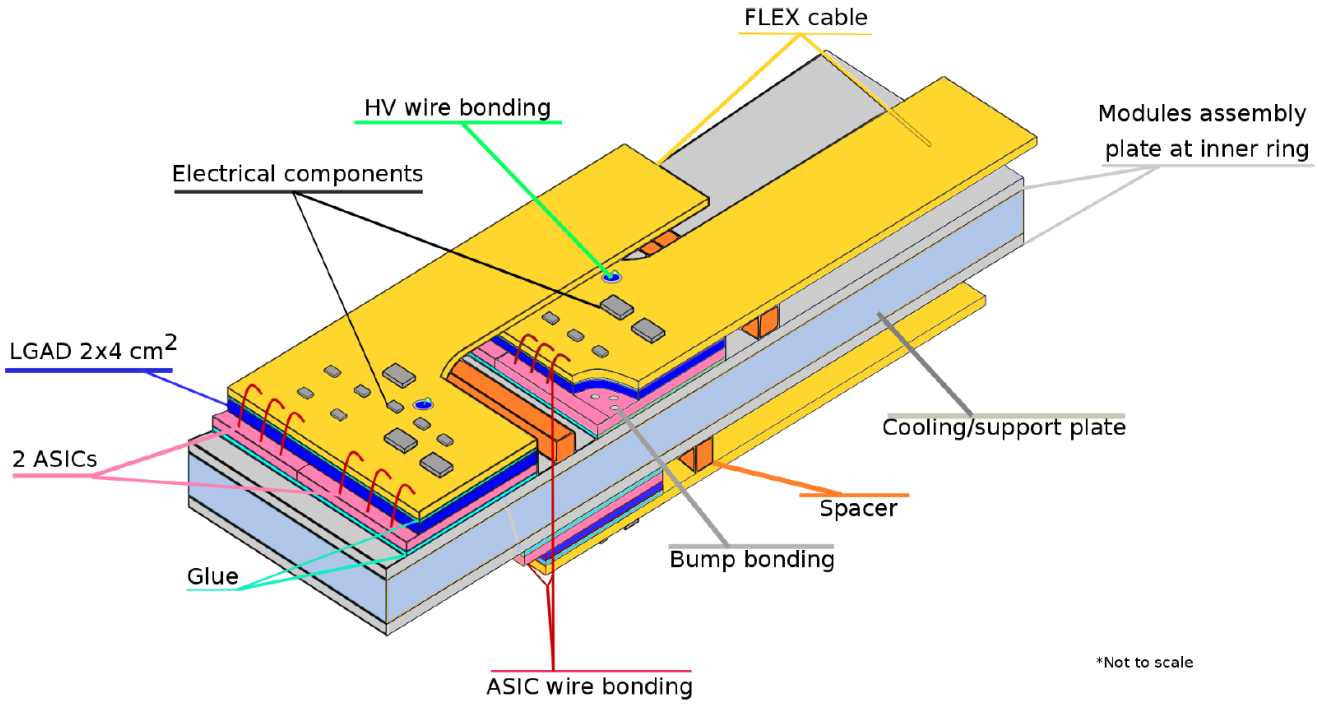
4. Note that the **channel connectivity** will be anyhow tested during the **module electrical tests**.

5. A small number of ASICs will be sacrificed to test the bump quality with **shear tests** before flip-chipping.

6. a small number of devices will be **tested destructively** to verify the robustness of the hybridization process. **Burn-in tests** will be carried out on some devices to test specifically for the degradation of the bump-bonding.

Module design and assembly

The bare module described above is glued with accurate positioning to the flex cable. ASIC signals and low voltage, as well as bias voltage for the sensor (HV) will be connected by wire bonding. Fig. 7.4 shows three modules with the different components stacked in the z direction of the HGTD. The total thickness of a module is about 1 mm with the sensor, the ASIC and the flex cable contributing about 300 µm each.



FCP Design ?

Position glue ?

Wire bonding ?

Figure 7.4: Schematic drawing of two adjacent modules on the top side and one on the bottom side of the cooling plate; the modules are mounted on thin support plates.

FPC design

Signal name	Signal type	No. of wires	Comments
HV	1 kV max.	1	Clearance
POWER	1 × Vdda, 1 × Vddd, 1.2 V	2	2 planes, $R < 2.7\,\mathrm{m\Omega\,cm^{-1}}$
GROUND	Analog, Digital	1(2) plane(s)	Dedicated layer $R < 0.7\,\mathrm{m\Omega\,cm^{-1}}$
Slow control	Data, Ck (opt. + rst, error)	2 to 4	I^2C link
Input clocks	320 MHz, Fast command e-link (opt. 40 MHz (L1))	4 or 8	CLPS
Data out lines	Readout data (TOT, TOA, Lumi)	4 pairs	4 e-links differential CLPS
ASIC reset	ASIC_rst	1	Digital
Monitoring	Temperature, Vdda, Vddd	6	DC voltage
Debugging	ASIC_debug	2	Analog

Table 7.4: Type and number of signal lines for two ASICs included in the flex cable design

Finally, the same radiation tolerance is required as for sensors and ASICs, i.e. up to at least 4.7 MGy, as well as operation at a temperature of about –30 °C (see Fig. 7.15).

More specification pls see HGTD TDR (ATL-COM-UPGRADE-2019-003)

Gluing and wire bonding

Gluing

Wire bonding

Tests