Full size pixel chip for high-rate CEPC Vertex Detector

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On behalf of the CEPC MOST2 Vertex detector design team

CEPC MOST2 Annual Meeting

2019-4-29

Outline

- **Motivation of the MOST2 Vertex detector design**
- **Specification**
- **Limitation of the existing CMOS sensors towards the high-rate CEPC Vertex Detector**
- **Key improvement for fast readout**
- **Preliminary design & schedule**

CEPC Vertex Detector Design

Detector Requirements

- Efficient tagging of heavy quarks (b/c) and τ leptons

  ⟶ impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\,\sin^{3/2}\theta}\,(\mu m)$$

- Detector system requirements:
  - σ_{SP} near the IP: *<3 μm* ⟶ ~16μm pixel pitch
  - material budget: *≤ 0.15%X $_0$/layer* ⟶ power consumption < 50mW/cm^2 , if air cooling used
  - first layer located at a radius: *~1.6 cm*
  - pixel occupancy: *≤ 1 %* ⟶ ~ μs level readout

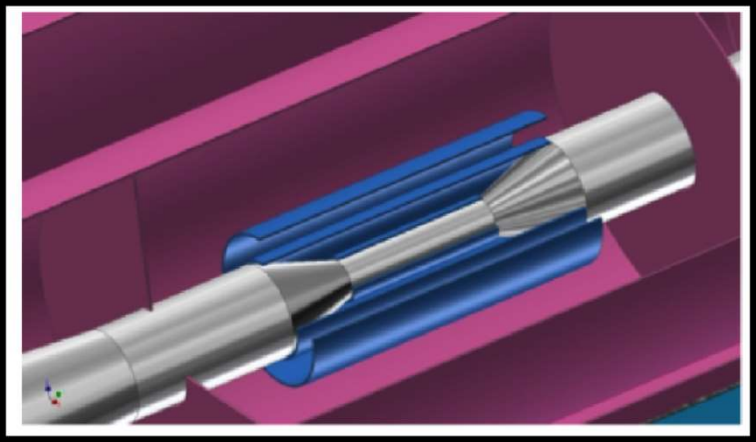
Target: fine pitch, low power, fast pixel sensor + light structure

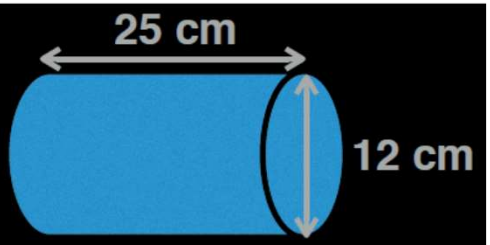
- **Ref: Status of vertex detector, Q. Ouyang, International workshop on CEPC, Nov. 7th 2017**

Baseline Vertex Detector design

Baseline Pixel Detector Layout

3-layers of double-sided pixel sensors



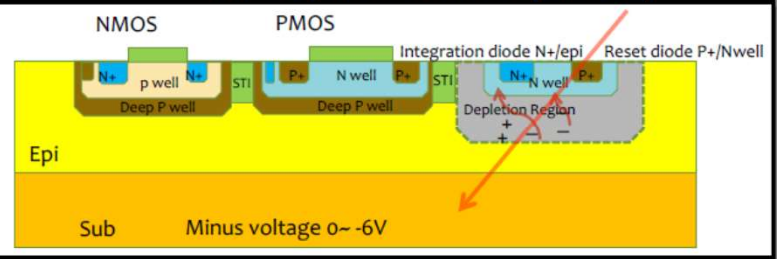


- ILD-like layout
- Innermost layer: σ_{SP} = 2.8 μm
- Polar angle θ ~ 15 degrees

Implemented in GEANT4 simulation framework (MOKKA)

		$R(mm)$	$\|z\|(mm)$	$\|cos\theta\|$	$\sigma(\mu m)$	$Readout\ time(us)$
Ladder 1	Layer 1	16	62.5	0.97	2.8	20
	Layer 2	18	62.5	0.96	6	1-10
Ladder 2	Layer 3	37	125.0	0.96	4	20
	Layer 4	39	125.0	0.95	4	20
Ladder 3	Layer 5	58	125.0	0.91	4	20
	Layer 6	60	125.0	0.90	4	20

CMOS pixel sensor (MAPS)



Integrated sensor and readout electronics on the same silicon bulk with "standard" CMOS process:
- low material budget,
- low power consumption,
- low cost …

- Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

Ladder Prototype

Silicon Vertex Detector Prototype – MOST (2018–2023)

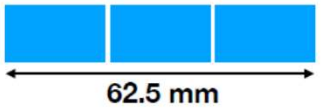
Sensor technology CMOS TowerJazz

- Design sensor with large area and high resolution
- Integration of front-end electronic on sensor chip

Benefit from MOST 1 research program

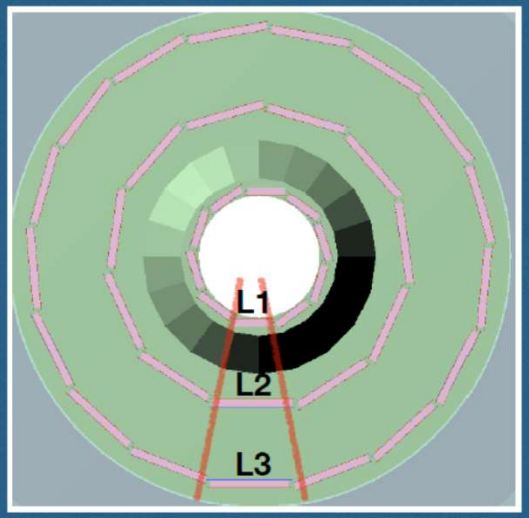
Double sided ladder

Layer 1 (11 mm x 62.5 mm)
Chip size: 11 mm X 20.8 mm



3 X 2 layer = 6 chips

3-layer sector



Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

L1
L2
L3

3-layers
same size
same chip

Goals:
1 MRad TID
3-5μm SP resolution

Integrate electronics readout

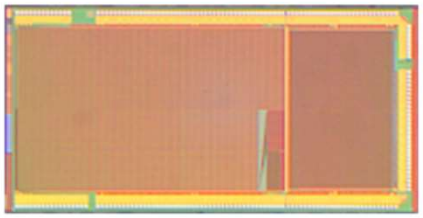
Design and produce light and rigid support structures

8

- Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

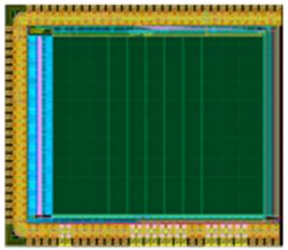
Previous CMOS pixel sensor prototypes

Prototype	Pixel pitch (μm^2)	Collection diode bias (V)	In-pixel circuit	Matrix size	R/O architecture	Status
JadePix1	33 × 33 16 × 16	< 1.8	SF/amplifer	96 × 160 192 × 128	Rolling shutter	In measurement
JadePix2	22 × 22	< 10 V	amp., discriminator	128 × 64	Rolling shutter	In measurement
MIC4	25 × 25	reverse bias	amp., discriminator	112 × 96	Asynchronous	In measurement



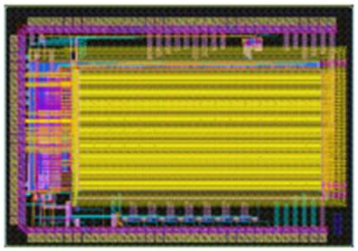
JadePix1 (IHEP)

3.9 × 7.9 mm^2



JadePix2 (IHEP)

3 × 3.3 mm^2



MIC4 (CCNU & IHEP)

3.2 × 3.7 mm^2

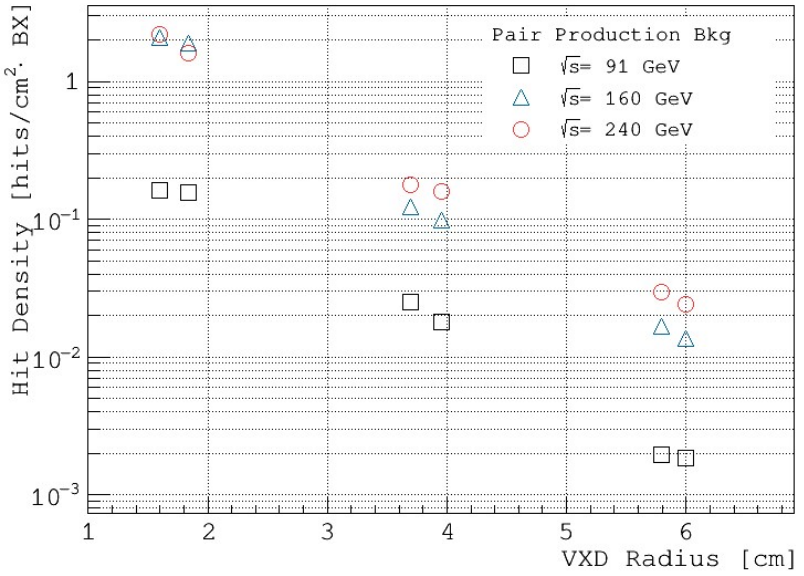
All prototypes in TowerJazz 180 nm process

- **Slides from Y. Zhang: "IHEP CMOS pixel sensor activities for CEPC", 2018.3**
- **Y.P. Lu, "Pixel design and prototype characterization in China", The 2018 International Workshop on the High Energy Circular Electron Positron Collider**

Main specs of the full size chip for high rate vertex detector

- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**

From the CDR of CEPC



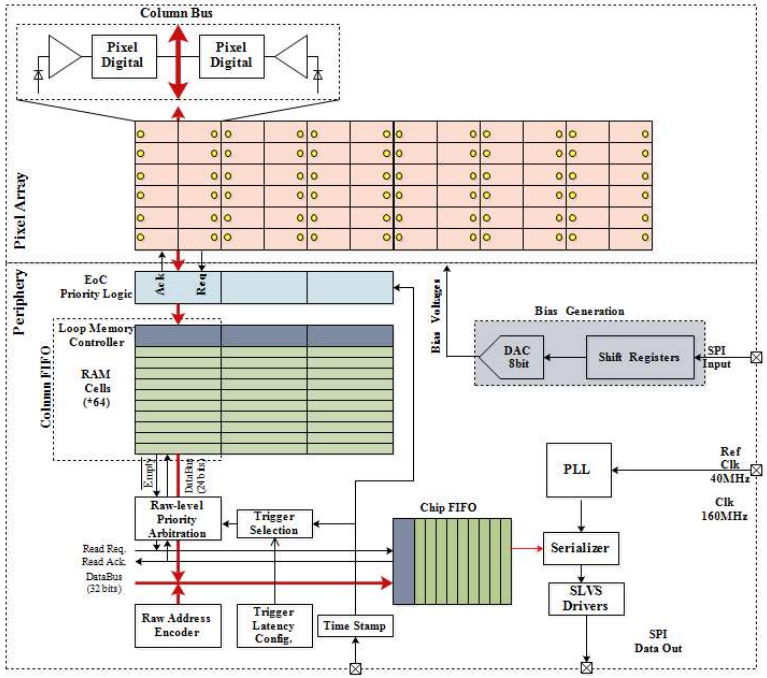
For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

Limitation of the existing CMOS sensors

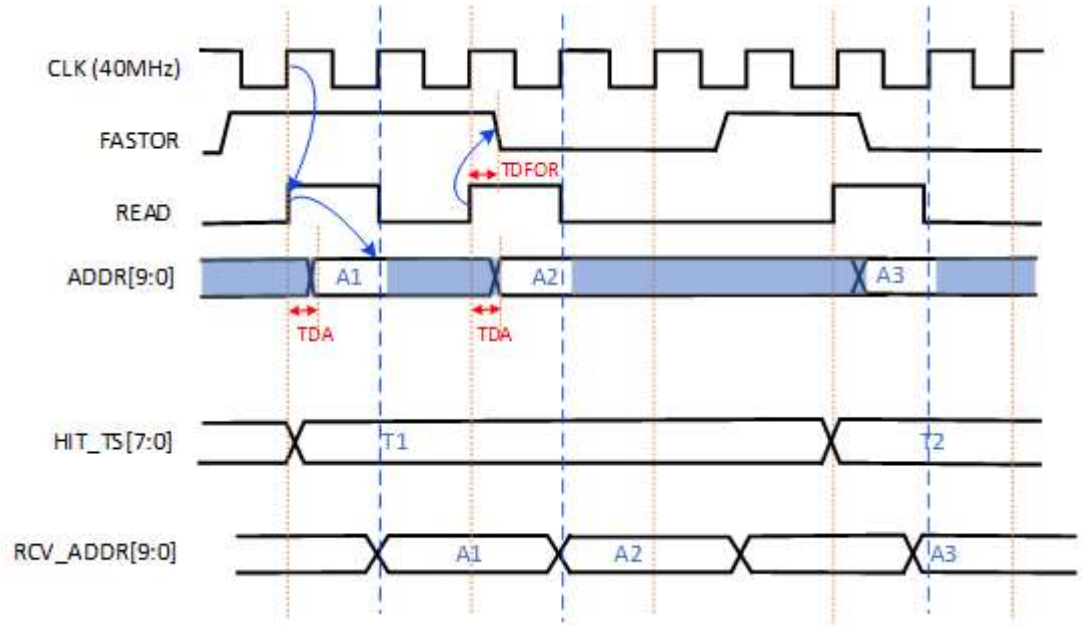
- **None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector**
- **Two major constraints for the CMOS sensor**
  - **Pixel size: should be < 25um* 25um, aiming for 16um*16um**
  - **Readout speed: bunch crossing @ 40MHz**
- **TID is also a constraint, but 1Mrad is not so difficult**

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA	JadePix/ MIC4 (MOST1)
Pixel size	✔	X	✔	✔
Readout Speed	X	✔	X	X
TID	X (?)	✔	✔	To be tested

New proposed architecture for MOST2



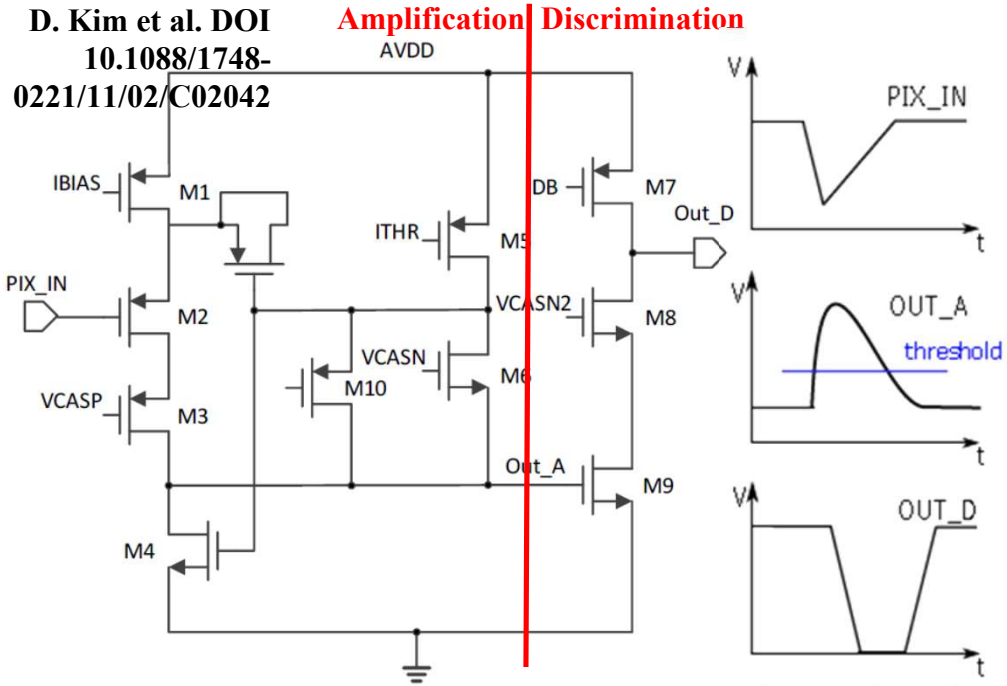
From X.M. Wei for the CEPC Vertex MOST2 group meeting

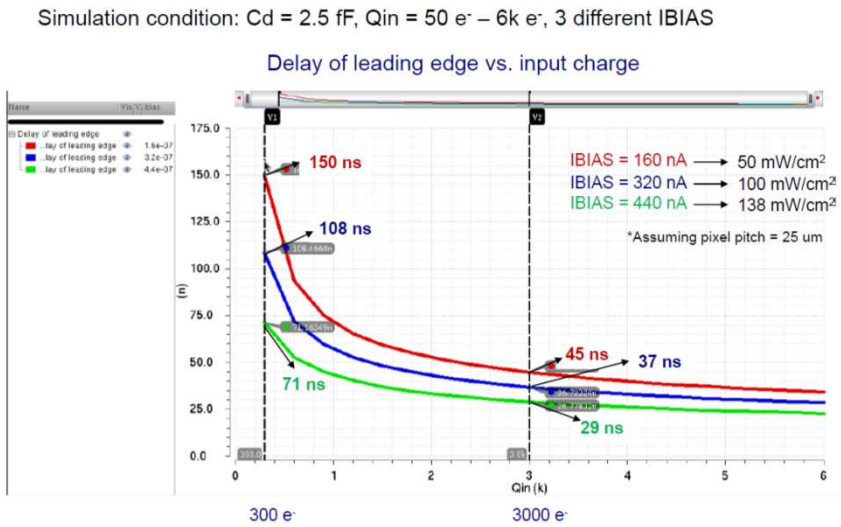


- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - **Priority based data driven readout**
  - **Modification: time stamp is added at EOC whenever a new fast-or busy signal is received**
  - **Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate**
- **2-level FIFO architecture**
  - **L1 FIFO: In column level, to de-randomize the injecting charge**
  - **L2 FIFO: Chip level, to match the in/out data rate between the core and interface**
- **Trigger readout**
  - **Make the data rate in a reasonable range**
  - **Data coincidence by time stamp, only the matched event will be readout**

Pixel architecture – Analog

D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

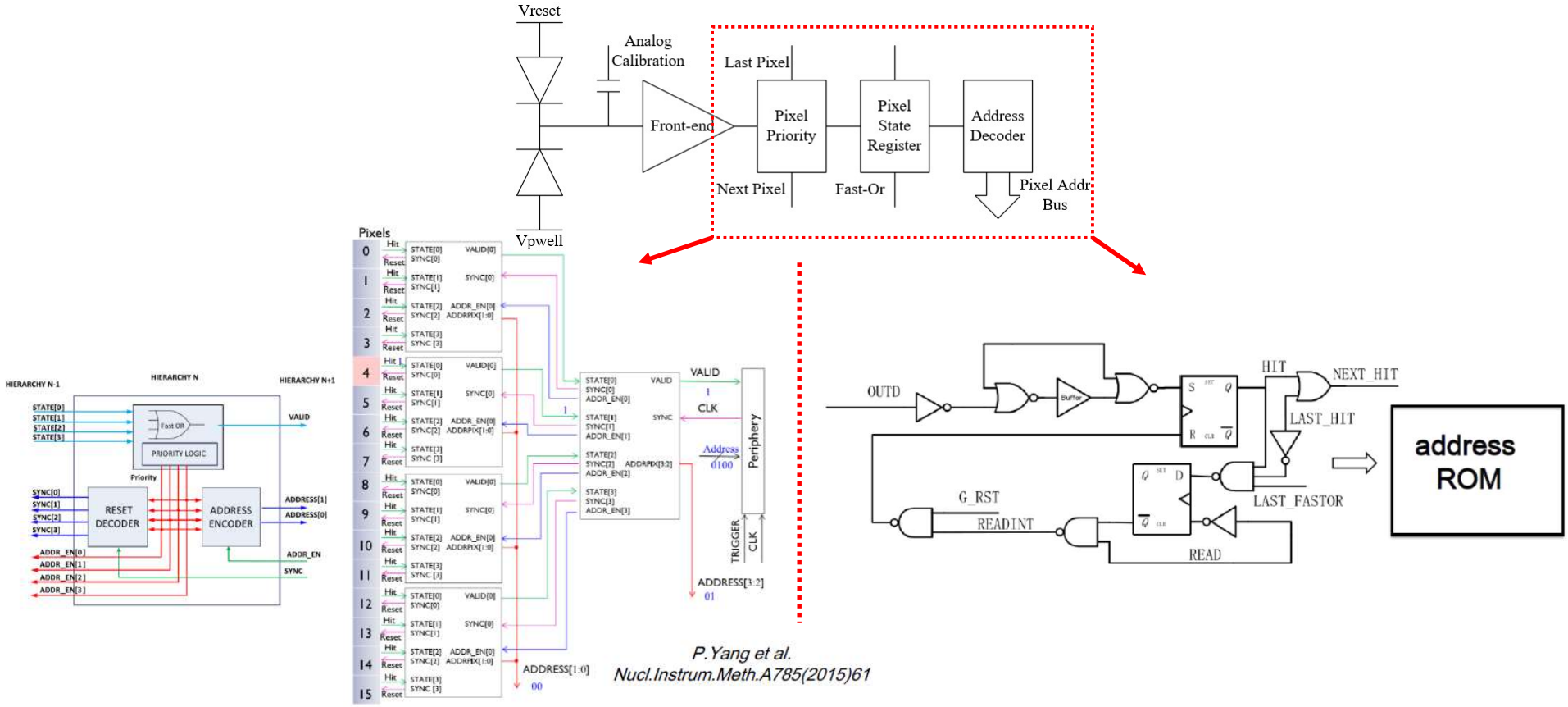




Y. Zhang for the CEPC Vertex MOST2 group meeting

- **Digital-in-Pixel scheme: in pixel discrimination & register**
- **Pixel analog is derived from ALPIDE (and benefit from MIC4 for MOST1)**
  - **As most of ATLAS-MAPS sensors' scheme**
- **Biasing current has to be increased, for a peaking time of ~25ns**
  - **Now in MOST1 ~2us peaking time was designed, too slow for 40MHz BX**
- **Consequence:**
  - **Power dissipation increased**
  - **Modified TJ process for ATLAS has to be used**
    - **With faster charge collection time, otherwise only fast electronics is of no meaning**

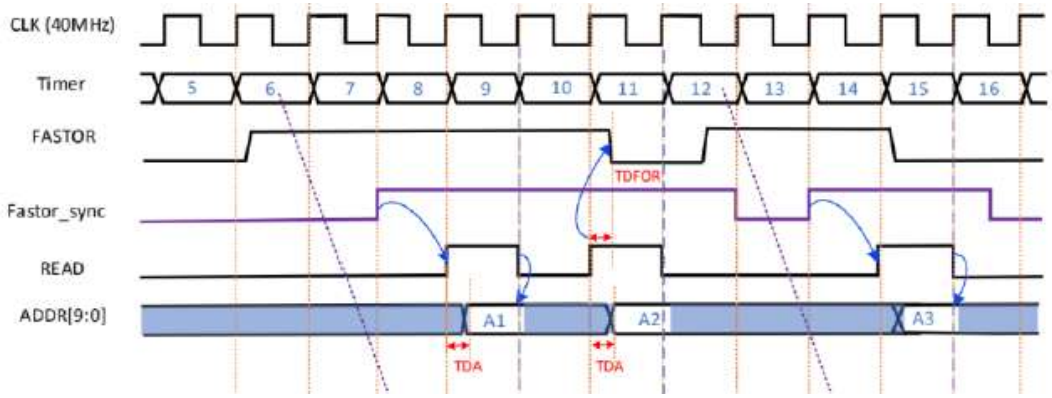
Pixel architecture – parallel digital schemes



- **Two parallel digital readout architectures were designed:**
  - **Scheme 1：ALPIDE-like: benefit from the proved digital readout in small pixel size**
  - **Scheme 2：FE-I3-like: benefit from the proved fast readout @40MHz BX (ATLAS)**

Design effort aiming for 40MHz BX on digital

- **ALPIDE-like scheme：**
  - **Fast-Or bus added to record the column hit time stamp**
  - **Boosting speed of the AERD (Address-Encoder & Reset-Decoder）**
    - **To shift the Fast-Or by a half of the clock cycle**
      - **More margin in the timing constraint of the periphery circuit**



Normal AERD

SS ; 1.6V ; 50°C	
Signal	Delay
FASTOR	14. 3ns
READ	14. 3ns
TDA	28ns
TDFOR	1. 3ns

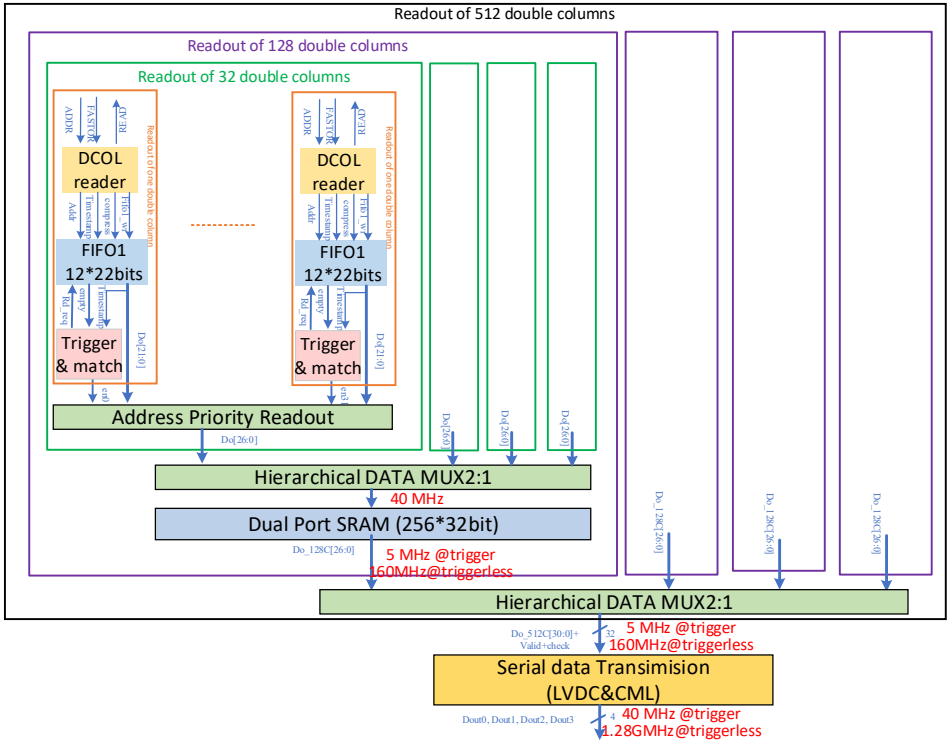
Boost AERD

SS ; 1.6V ; 50°C	
Signal	Delay
FASTOR	14. 3ns
READ	14. 3ns
TDA	25. 5ns
TDFOR	1. 3ns

TY. Wu for the CEPC Vertex MOST2 group meeting

- **FE-I3-like scheme：**
  - **Simplify the pixel cell logic**
  - **All the logic gates were re-designed with fully customized layout**
    - **For smaller pixel size**

Full chip periphery logic design



- **Main Functionality:**
  - **Trigger/Triggerless readout mode compatible**
    - **Data coincidence and trigger window logic**
  - **Two level FIFOs for hit derandomization**
  - **High speed serialization for data readout**
    - **4Gbps data rate capability**

From X.M. Wei for the CEPC Vertex MOST2 group meeting

- **Other necessary blocks**
  - **Slow control of the pixel array and full chip via SPI interface**
  - **Bias generation by current- and voltage- DACs**
  - **Clock management: Phase Lock Loop and serializer**
  - **Power management: LDOs for on-chip low ripple power supply**
  - **High speed interface: CML & LVDS Drivers**

Team organization

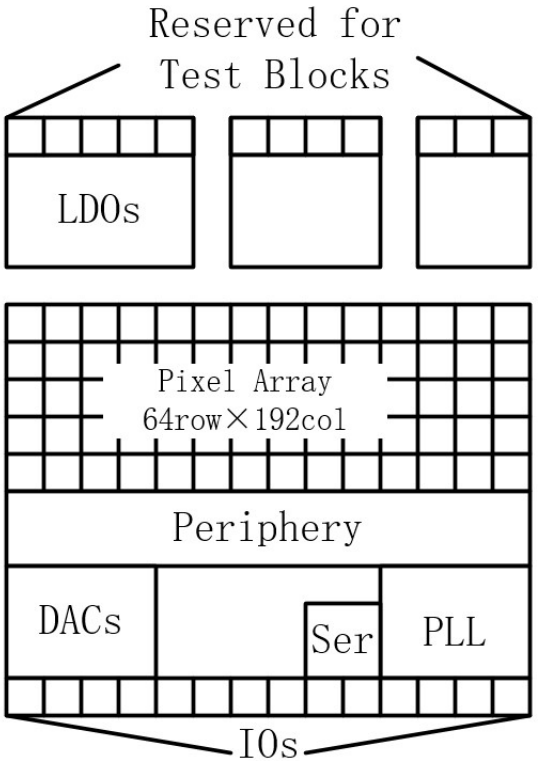
- Slides from Y. Zhang, Satellite meeting of MOST2 in Oxford, 2019.4

- **Design team:**
  - **IHEP, SDU, NWPU, IFAE & CCNU**
  - **Biweekly/weekly video design meeting on chip design (convened by IHEP)**

Institutes	Tasks	Designers
IHEP	Full chip modeling & simulation Pixel Analog, TCAD simulation High speed interface: PLL + Serializer	Wei Wei, Ying Zhang Xiaoting Li, Weiguo Lu, Mei Zhao
CCNU/IFAE	Pixel Digital	Tianya Wu, Raimon Casanova
NWPU	Periphery Logic, LDO	Xiaomin Wei, Jia Wang
SDU	Bias generation	Liang Zhang

- **Chip characterization**
  - **Test system development: SDU & + other interested parties**
  - **Electrical test: all designers supposed to be involved in the related module + other interested parties**
  - **Irradiation test: X-ray irradiator + beam line**

Current Status and recent schedule



To be submitted in May

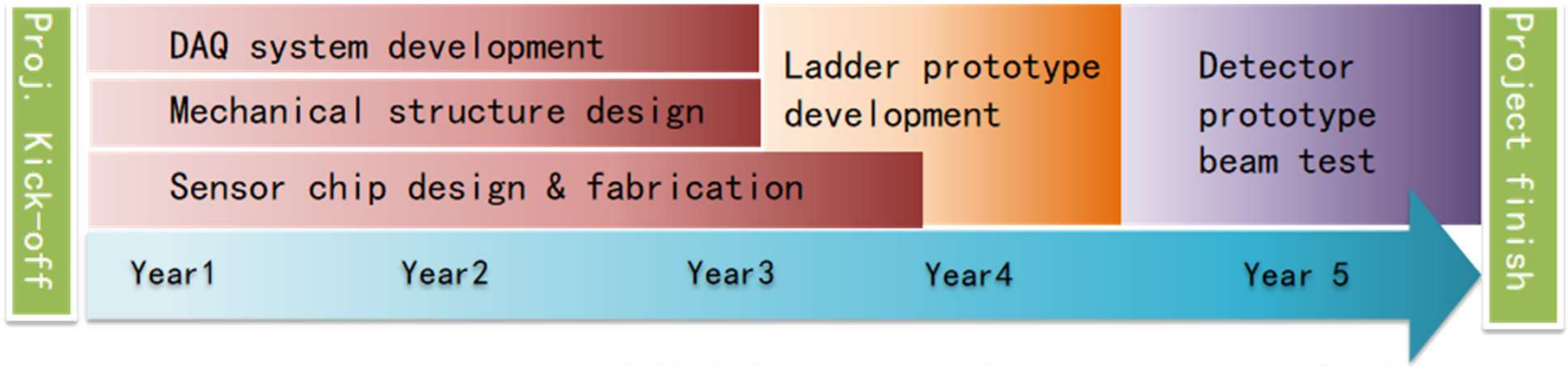
Expected to receive in Sep.

Test Board design will be in parallel

- **Design Status**
  - **Schematics of the main blocks are ready**
  - **Layout in progress**
    - **The first version of the pixel cell layout will be ready before the Mid of April**
- **First MPW tapeout**
  - **Shuttle booked for May 13th via IFAE**
    - **One block for 5mm×5mm**
  - **Organized with a full functional pixel array (small scale), plus other test blocks (less critical)**
    - **A 64×192 Pixel array + Periphery + PLL + Serializer**
    - **Bias generation included**
    - **I/O arranged in one edge, as the final chip**

Chip design schedule

- **MOST2 project: May 2018 ~ April 2023 (5 years)**



- **Chip design plan (3 MPW & 1 engineering run in 3 years)**
  - **Year 1: complete the preliminary design of the main functional modules of the sensor chip, submit the 1st MPW prototype, complete the design of all the functional modules**
  - **Year 2: test the first prototype, integrate all the modules in a fully functionality chip, submit the 2nd MPW prototype, complete the 2nd prototype test**
  - **Year 3: solve the detected bugs and finish circuit modification & improvement, fabricate and test the 3rd MPW prototype, complete the full size chip design and tapeout (engineering run)**

- **Slides from Y. Zhang, Satellite meeting of MOST2 in Oxford, 2019.4**

Summary

- **Challenge considering the real CEPC's requirement**
  - **Pixel size**
  - **High rate & power dissipation**
  - **None existing chip can fully satisfy the CEPC Vertex**
- **New proposed architecture**
  - **Modified column-drain readout with time stamp for each hit**
  - **Parallel verification with modified ALPIDE readout**
  - **Trigger/Triggerless mode compatible**
- **Chip design for MOST2 Vertex detector is progressing almost as scheduled**
  - **First chip submission will be delivered very soon**

Thank you !

The ALPIDE readout architecture

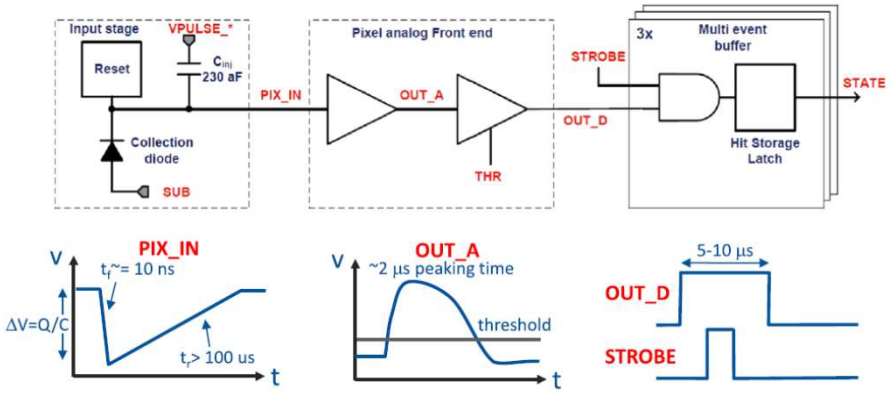


Fig. 2. Block diagram of the ALPIDE pixel cell.

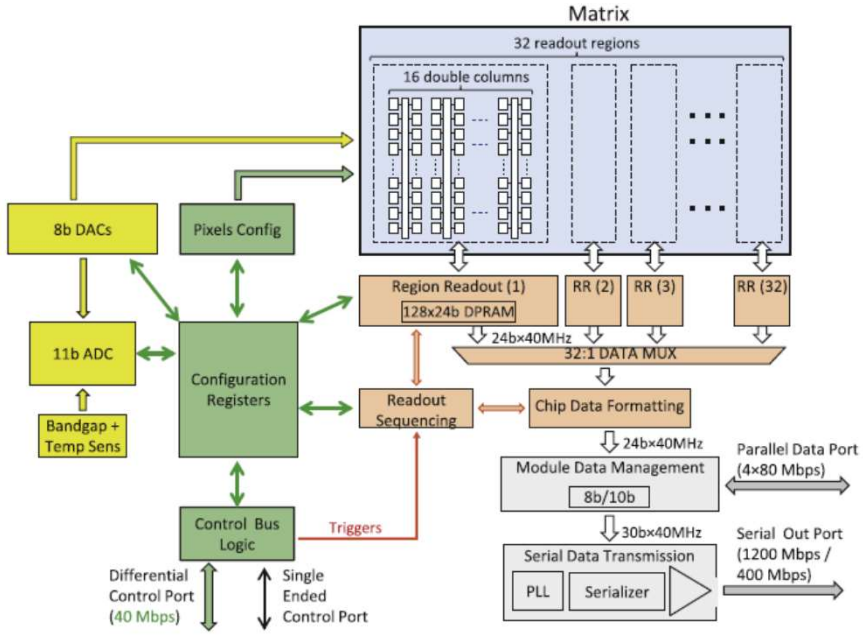


Fig. 3. Block diagram of the ALPIDE chip.

G. Aglieri Rinella et al. NIM. A 845 (2017) 583–587

Table 1
General requirements for the pixel sensor chip for the Upgrade of the ALICE Inner Tracking System. In parentheses: ALPIDE performance figure where above requirements.

Parameter	Inner barrel	Outer barrel
Chip dimensions (mm × mm)	15 × 30	
Silicon thickness (µm)	50	100
Spatial resolution (µm)	5	10 (5)
Detection efficiency	>99%	
Fake hit probability (evt^{-1} $pixel^{-1}$)	$<10^{-5}$ ($<< 10^{-5}$)	
Integration time (µs)	<30(10)	
Power density (mW/cm^2)	<300(~ 35)	<100(~ 20)
TID radiation hardness[a] (krad)	2700	100
NIEL radiation hardness[a] (1 MeV n_{eq}/cm^2)	1.7×10^{13}	1×10^{12}
Readout rate, Pb–Pb interactions (kHz)	100	

[a] 10 × the radiation load integrated over the approved program (6 years of operation).

- **The ALPIDE architecture, as MOST1 referenced, uses strobe signal as the "trigger"**
- **However, the readout rate is only ~100kHz, and more like frame readout**

Discussion on ALPIDE – analysis & conclusion

- **ALPIDE is not fully compatible with CEPC vertex & other high hit rate, high bunch crossing applications (like ATLAS)**

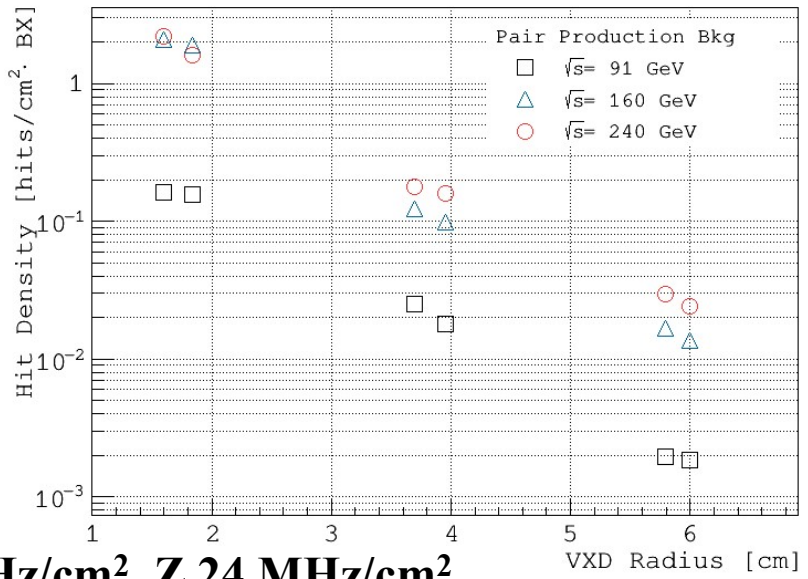
1. **Bunch crossing too high**
   - **Now bunch crossing at 100~200kHz (i.g. frame rate)**
   - **While CEPC 1.5MHz (Higgs) ~ 40MHz(Z pole)**
     - **Not possible for the chip level frame-like readout, because:**
       - **At least 120MHz clk has to run at periphery-column level (3pixel per hit)**
       - **ALPIDE is "triggerless", no further data reduction, data rate too high (*32bits per hit)**
2. **Pixel analog should be (much) faster**
   - **now 2us peaking, 10us duration**
   - **CEPC: "Hit rate: 120MHz/chip, or 225Hz/pixel (average), 120kHz/col (ave)", Meaning every 8.3us, the column will be hit, however, very unlikely to be at the same pixel**
   - **For CEPC, peaking time should be much faster (25ns level)**
     - **Otherwise leads to too large delay for the arrival time stamp (although can be covered by the configurable trigger match error)**
   - **For CEPC, duration should also be faster**
     - **Better ends earlier than 8.3us, avoiding continuous hit in the same pixel**
   - **Larger power expected than ALPIDE**

From vertex detector MOST1 projects towards MOST2

- **To build a prototype ladder mounted with silicon pixel sensors**
  - **Spatial resolution 3-5 μm**
  - **TID 1 Mrad**
- **Compared with MOST1 project target:**
  - **Pixel sensor prototype design**
  - **Spatial resolution 3-5 μm**
  - **Power consumption <100 mW/cm2**
  - **Integration time 100 μs**
- **MOST1 focused on key performance, however we should focus more on a full function chip that can work in a prototype system**
- **Baseline design for MOST2:**
  - **Reuse the pixel design from MOST1, with necessary modification**
  - **Focus on full chip readout architecture design, esp. fast readout and full data readout chain**

The full size chip for high rate vertex detector

From the CDR of CEPC

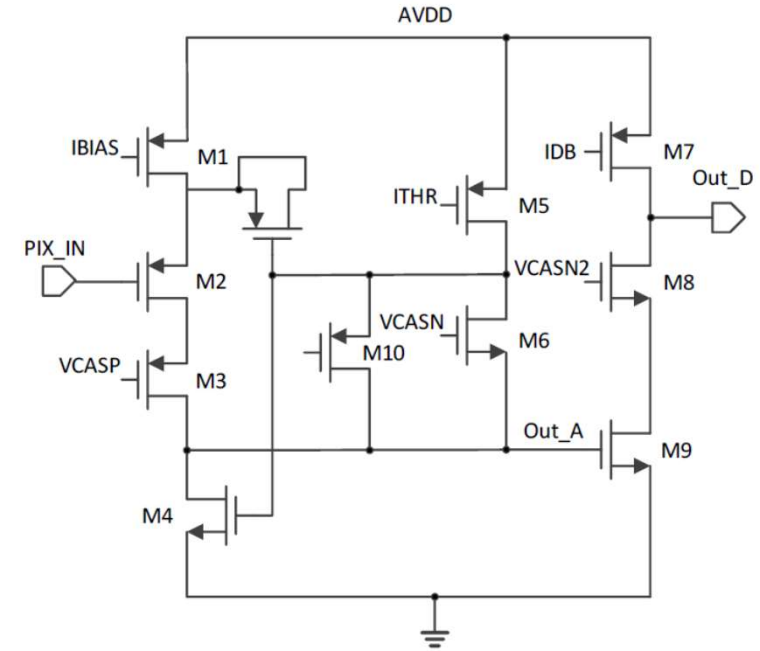


- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
- **The hit rate: Higgs 11 MHz/cm^2, W 36MHz/cm^2, Z 24 MHz/cm^2**
- **The chip should be capable with 36MHz/cm^2 hit rate**
- **Suppose the pixel array size is 512rows*1024cols (ALPIDE), 25um*25um pixel size, and 1.28cm*2.56cm pixel array area**
- **→ Hit rate: 120MHz/chip, or 225Hz/pixel (average), 120kHz/col (ave)**
  - **Meaning every 8.3us, the column will be hit, however, very unlikely to be at the same pixel**
- **In order to readout without data loss, time stamp has to be added for every hit**
  - **According to the readout speed of MOST1(10~100us), it is not capable for this large hit rate**
  - **Also MOST1 chip design (MIC4) is currently base on ALPIDE readout architecture, which is still more or less frame-based, not fully capable with trigger readout**

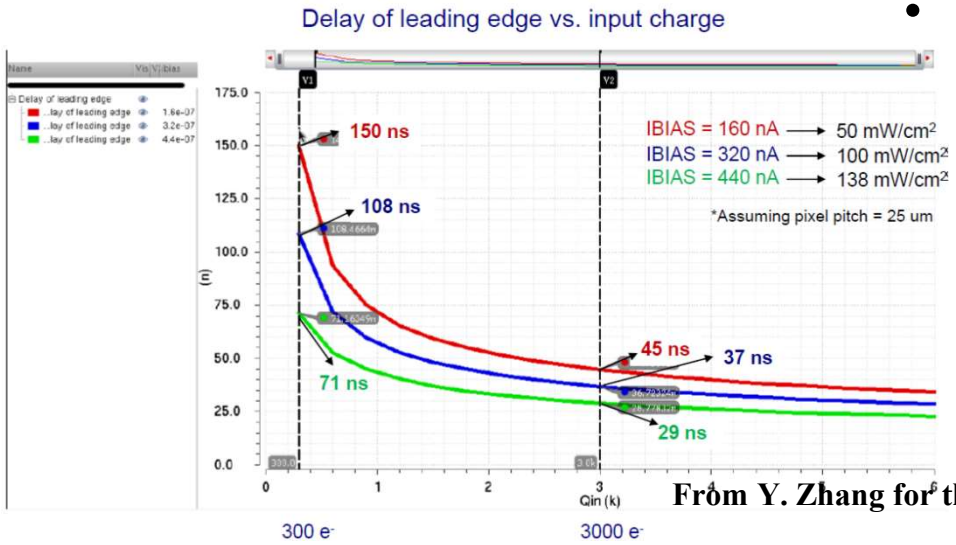
Increased data rate as for the real CEPC

- Every hit has 27~32bits (async): col addr 9bits (512), row addr 10bits (1024), time stamp ~8bits (suppose 40MHz clock, covers 6.4us time region)
- If triggerless, all the raw hit data should be sent off chip
  - The data rate: ~32bits*120MHz= 3.84Gbps, possible, but risk too high in the current stage
- If trigger, on-chip buffer should be designed
  - Suppose trigger latency 3us. Trigger rate was said 20kHz~50kHz
  - Triggered data rate:
    - 2.5/hits/bunch/cm^2*3pixels/hit*1.28cm*2.56cm*32bit=786bit/bunch/chip
    - W@20kHz trigger rate -> 15.7Mbps/chip as the triggered data rate
  - In order to cover any trigger error(mismatch of the edge in different column, time walk of the hit peaking…)
    - A trigger window can be set, so that the data within the ±σ of the trigger time stamp can all be read out
    - In this way, the readout data rate will be (suppose trigger window of ±3LSB time stamp):
      - 15.7Mbps * 7 ~ 110Mbps
      - Can still be read out by a single LVDS interface

Other necessary modification for the pixel cell



Simulation condition: Cd = 2.5 fF, Qin = 50 e⁻ – 6k e⁻, 3 different IBIAS



- **Pixel analog in the same architecture as ALPIDE (and benefit from MIC4 for MOST1) but with different parameters**
  - **Aiming especially for fast readout**
- **Biasing current has to be increased, in order to achieve a peaking time of ~25ns**
  - **Otherwise there will be timing error for the event, and has to open a trigger window in this case**
  - **Now in MOST1 ~2us peaking time was designed, which is too slow for 40MHz BX**
- **Consequence:**
  - **Power dissipation increased:**
    - **bias@440nA with peaking time 29ns, but 138mW/cm² for analog**
    - **Total power density may exceed 200mW/cm²**
  - **Modified TJ process for ATLAS has to be used**
    - **With faster charge collection time, otherwise only fast electronics is of no meaning**

From Y. Zhang for the group meeting