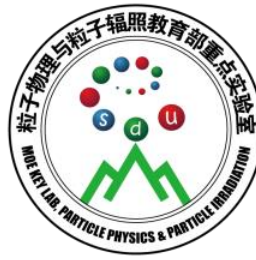




山东大学
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粒子物理与粒子辐照
教育部重点实验室

Readout electronics for the MPW chip

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on behalf of SDU pixel group

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Outline

■ Structure of the readout electronics

- ↪ Main board with chip bonded, power supply, connectors to the outside, etc.
- ↪ FPGA board with related configurations, data transmission, etc.

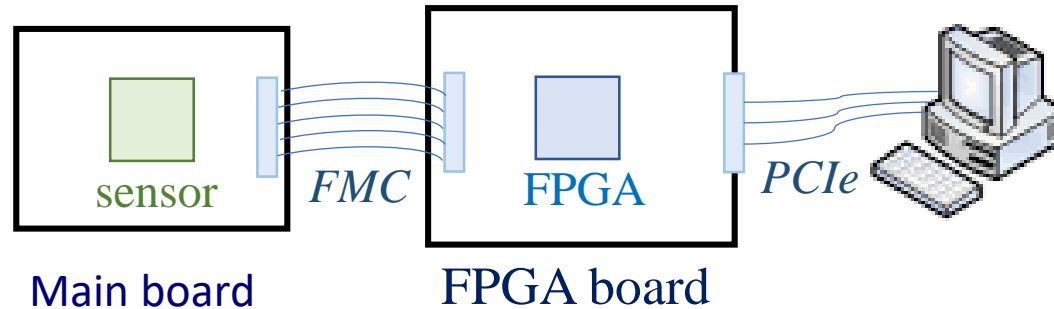
■ Status of the readout electronics

- ↪ The structure has been used for the test of SUPIX

■ Schedule of the test boards

■ Summary & outlook

Structure of the readout electronics



■ The test electronics for MPW consists of:

↪ Main board:

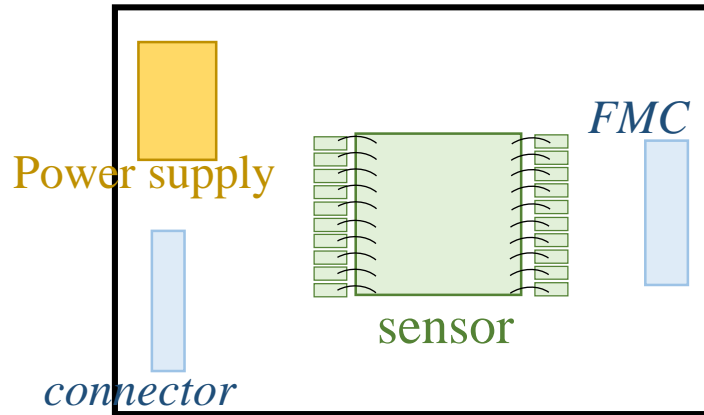
- chip is bonded
- supply the bias for the chip
- the output is transmitted through buffers
- supply the power to the chip
- buffer the control signals

↪ FPGA board (KC705 evaluation board):

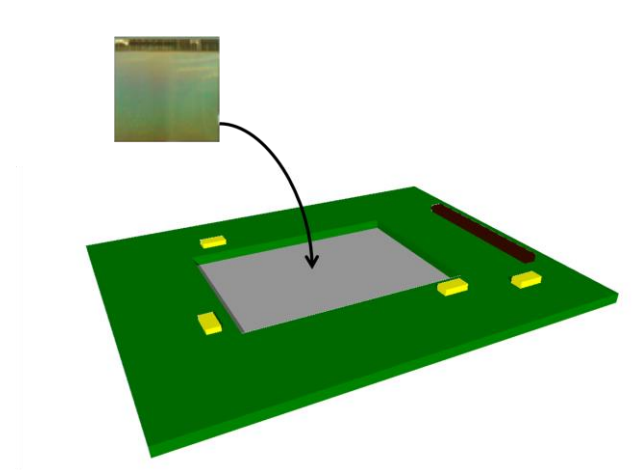
- communicate with PC via PCIe, control the data loading/receiving

Structure of the readout electronics

Main board



Main board

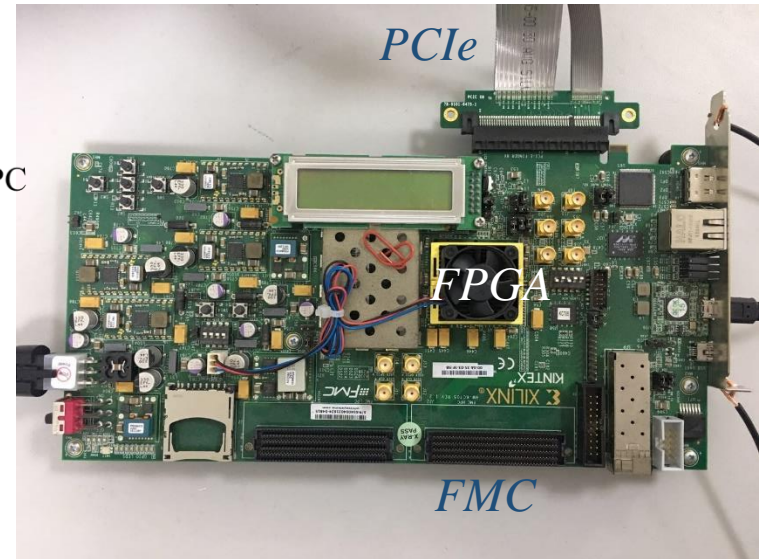
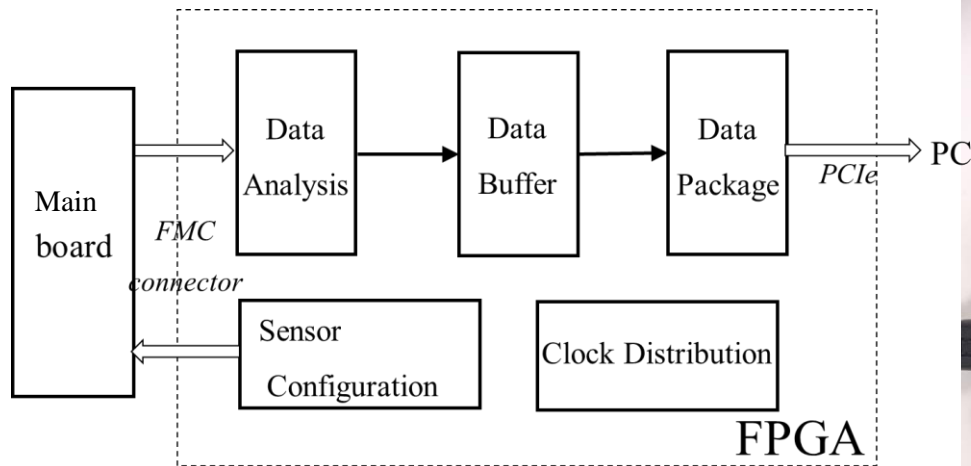


■ A pixel sensor is wire-bonded on the main board

- ↪ Signal readout
- ↪ Data buffer
- ↪ Data transmission to FPGA board
- ↪ Power supply
- ↪ Other circuits if needed

Structure of the readout electronics

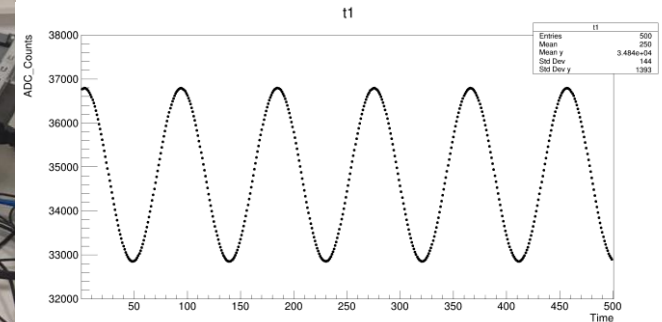
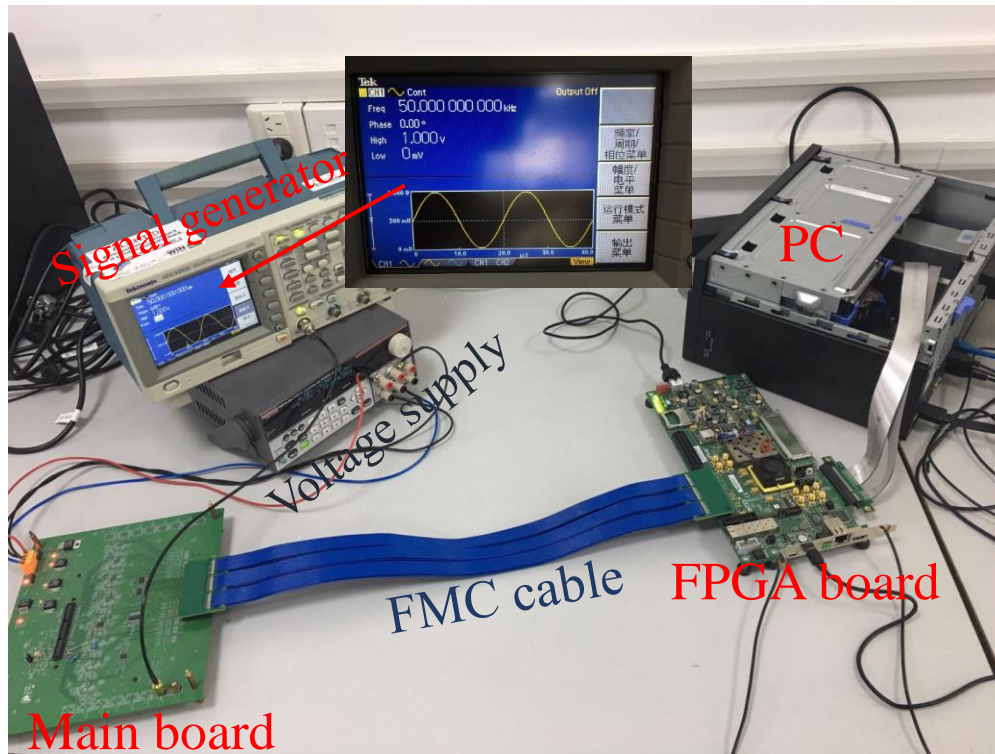
FPGA board



■ FPGA board receives (sends) data from (to) the main board

- ↪ KC705 evaluation board: Kintex-7 FPGA (XC7K325T)
- ↪ Sensor configuration
- ↪ Data analysis, data buffer & data package
- ↪ Data transmission to PC over PCI express

Status of the readout electronics



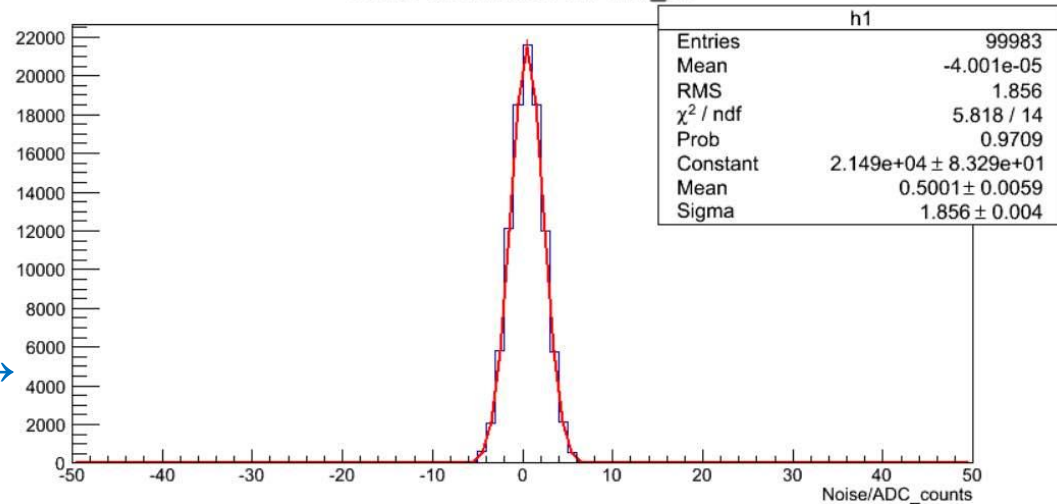
Data acquired from PC

- The MPW electronics is based on the test electronics for SUPIX in SDU, which is under testing now
- Currently, the SUPIX electronics perform well

Status of the readout electronics

Preliminary results

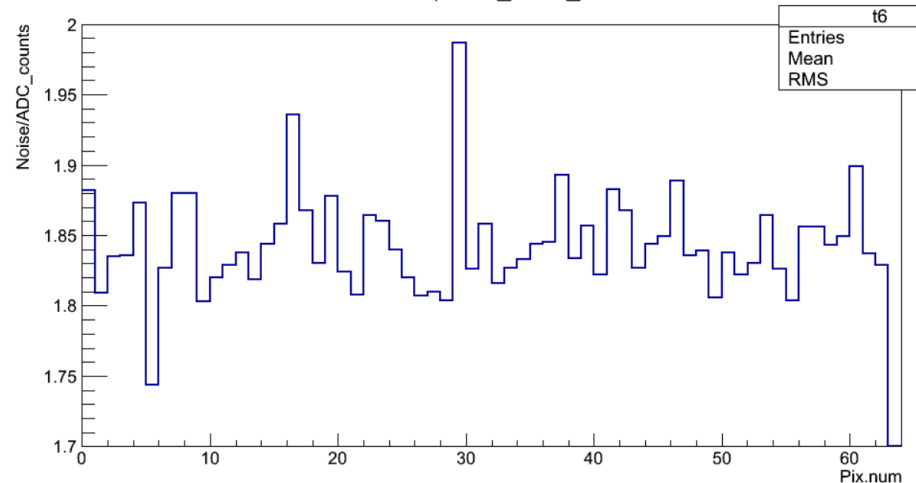
Noise distribution of Pixel_59



Noise distribution for a typical pixel

$\text{Sigma} \sim 1.86$

Noise in pixels_0000_ADC8



Noise distribution of 64 pixels

$\text{Sigma} < 2$

Schedule of the readout board

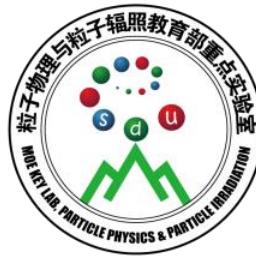
- **The readout board will start as soon as the chip design report or layout design is finished**
 - ↪ Schematic & PCB design of main board ~ 40 days
 - ↪ PCB processing ~ 20 days
 - ↪ Component solder ~ 15 days
 - ↪ Wire-bonding ~ 7 days
 - ↪ FPGA code and DAQ testing ~ 30 days

Summary & outlook

- **The MPW electronics are composed of main board and FPGA board, which are based on the current design of test electronics for SUPIX in SDU**
- **The test electronics and preliminary DAQ for SUPIX perform well currently**
- **The MPW electronics design is scheduled to start as soon as the sensor layout is done**
 - ↪ The PCB and FPGA design will be based on the current design for SUPIX
 - ↪ The DAQ design may be improved if anyone is interested in it



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Thanks for your attention