Development of a batch testing system of scintillator tiles and cooling studies for CEPC Calorimeters

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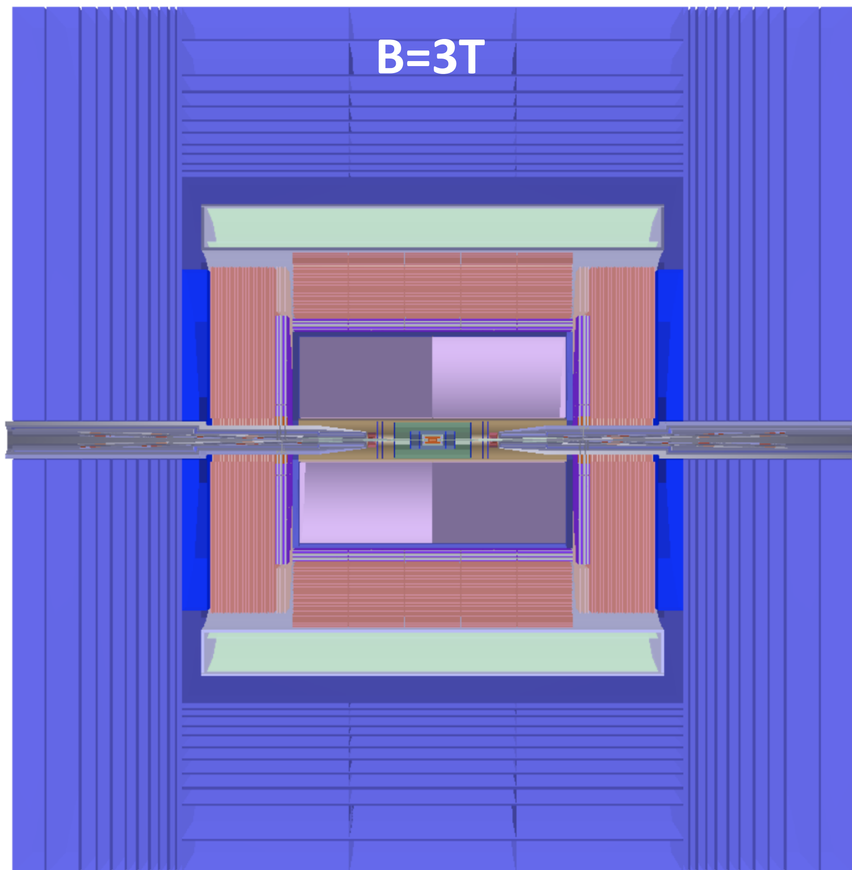
Outline

- **Discuss the result when Fan and water cooling methods applied on ECAL**
- **Discuss the result when Water cooling method applied on HCAL and gravity influence on Temperature**
- **The progress of scintillator batch test system of AHCAL**

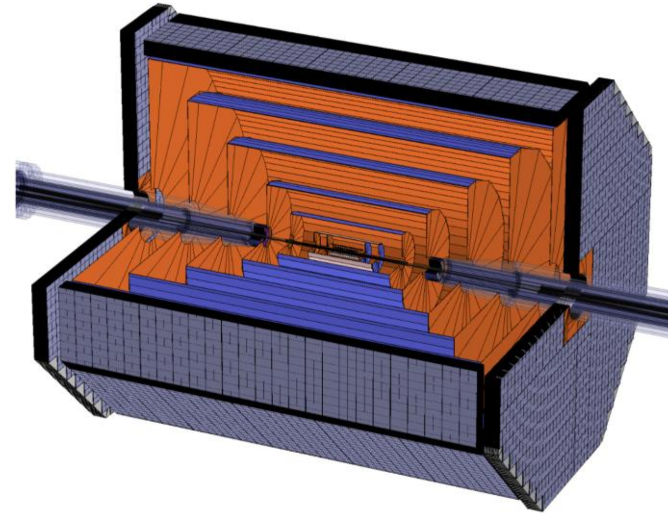
Schematic of CEPC Detectors

Baseline : PFA approach (ILD-like)

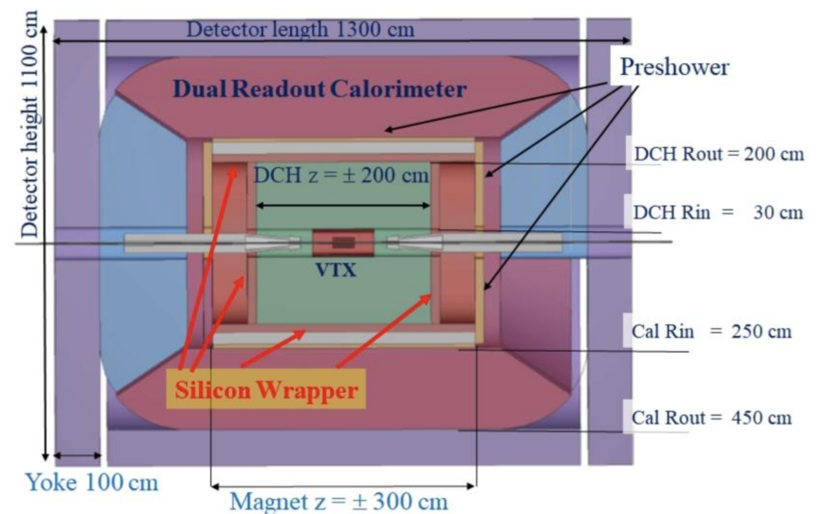
Silicon + TPC + ECAL&HCAL + Muon



Full Silicon Tracker

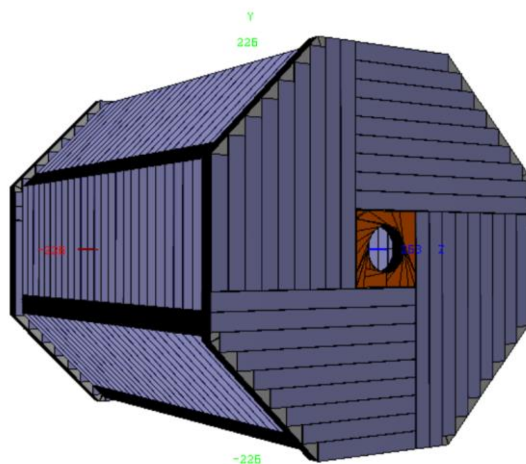


Dual Readout

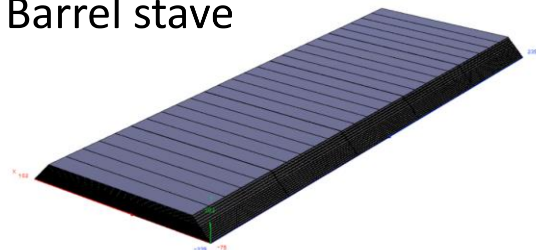


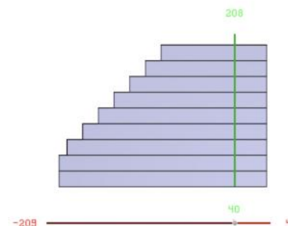
ECAL Layout and Structure

- One cylindrical barrel + two disk-like endcaps
- ~2 m in radius, and ~5.3 m long (Z direction).
- 8 barrel sections: 1 section → 8 staves, 1 stave → 5 modules,
  1 module → 5 columns
- Each endcap → 4 quadrants, 1 quadrant → 9 columns
- Column: slabs integrated into supporting structures
- Best possible hermeticity and minimum crack regions



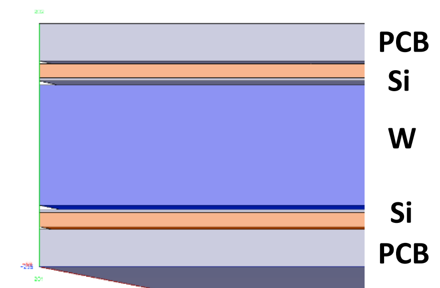
Barrel stave





Endcap quadrant

Slab

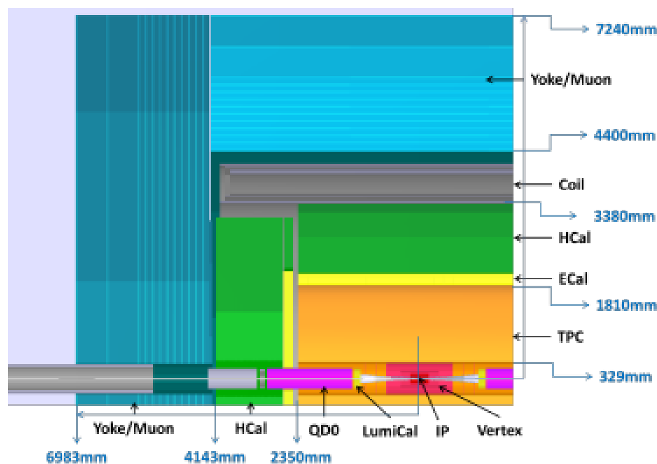


ECAL Channel Count, Power Consumption

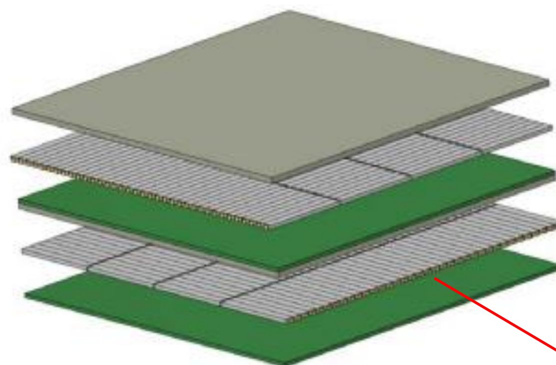
- Numbers of channels
  - **17.3 M for barrel, 7.43 M for endcaps**
- Total power consumption: 146 kW
  - **124 kW (5mW/ch, SKIROC)**
  - **22 kW (9mW/DIF/m^2 × 2400m^2)**
- Active cooling is likely required
- Passive cooling might be possible with a reduced number of channels

  → **larger cell-size (degrade PFA performance?)**

ECAL Model Structure (ScW)



One quarter of CEPC-v1 detector concept

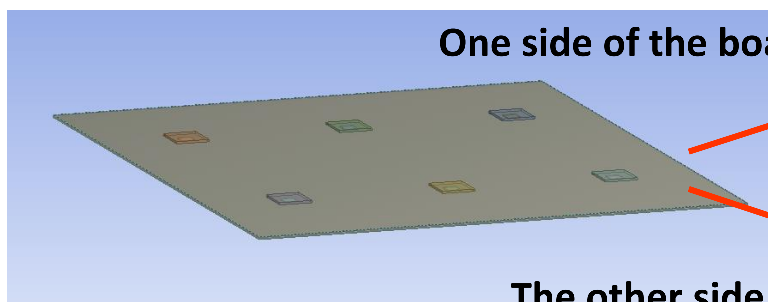


Sandwich Structure

30 layers in total

For each layer：
Tungsten (2.8mm)+
PSD (2mm)+
PCB+ASIC (3.1mm)
SPIROC2B

The First Step

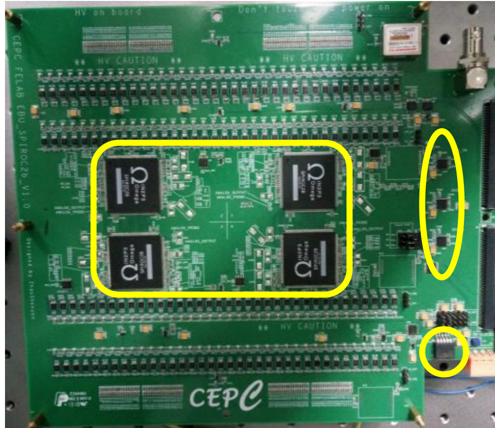


One side of the board: Chips, LDO etc.

The other side of the board: Temperature-sensitive electronic equipment.

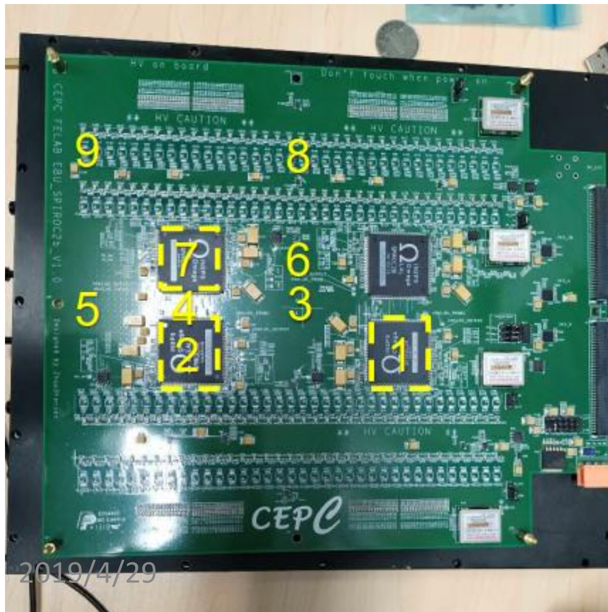
Simulation vs Experimental Setup

USTC+SJTU



Sample Board

Model



Thermal Conductivity:

$$\text{Silicon(Chips)}: 148W \cdot m^{-1} \cdot C^{-1}$$

$$\text{FR-4}: 0.294W \cdot m^{-1} \cdot C^{-1}$$

$$\text{Copper}: 401W \cdot m^{-1} \cdot C^{-1}$$

Specific Heat:

$$\text{Silicon(Chips)}: 712J \cdot kg^{-1} \cdot C^{-1}$$

$$FR-4: 1150J \cdot kg^{-1} \cdot C^{-1}$$

$$\text{Copper}: 385J \cdot kg^{-1} \cdot C^{-1}$$

Default Analysis settings

Convection: Stagnant Air

Film coefficient: $5e-06W / mm^2 \cdot °C$

5~25 for Natural flowing air

- ✓ Environment temperature changes from 26 to 40 by 2 degrees
- ✓ Define chip side as top side and scintillator side as bottom side.
- ✓ Put 9 sensors on each side and 2 sensors for the environment temperature.

Simulation vs Measured: 4-chip PCB

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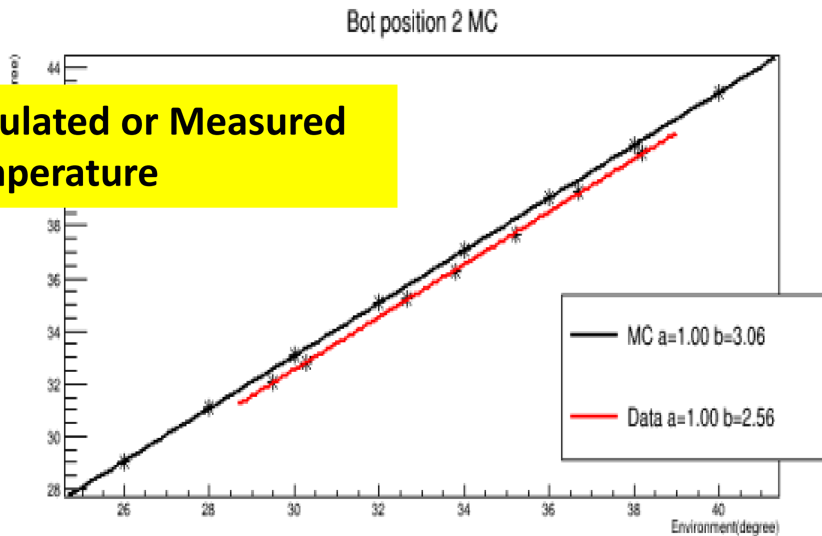
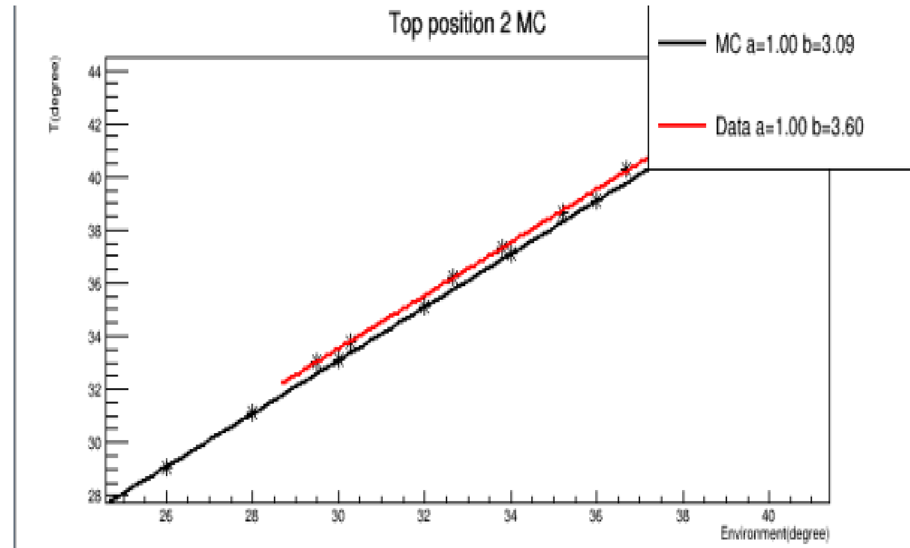
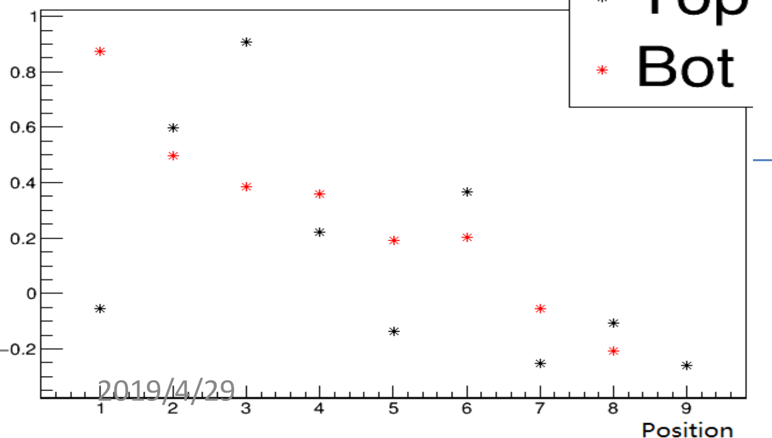




Simulated or Measured Temperature

Temperature of environment

Data-Simu



- Measured results has a good agreement with simulation results
- Take advantage of the good linearity to do the temperature reconstruction
- Small difference between simulation and measured temperatures

Simulation of Double W + PCB

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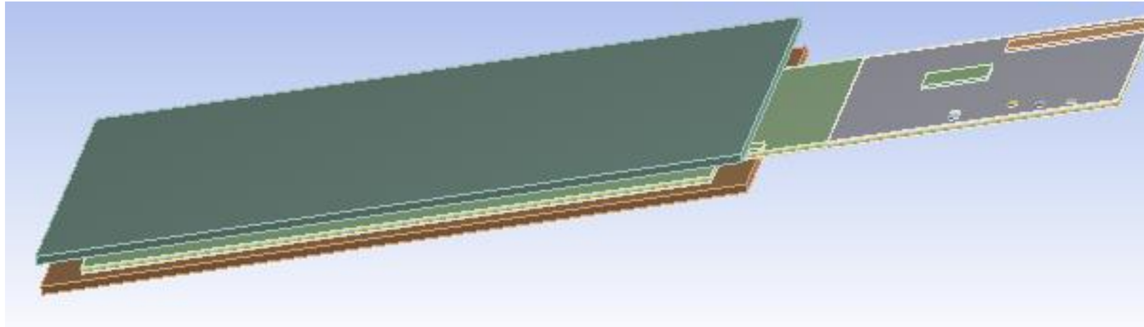
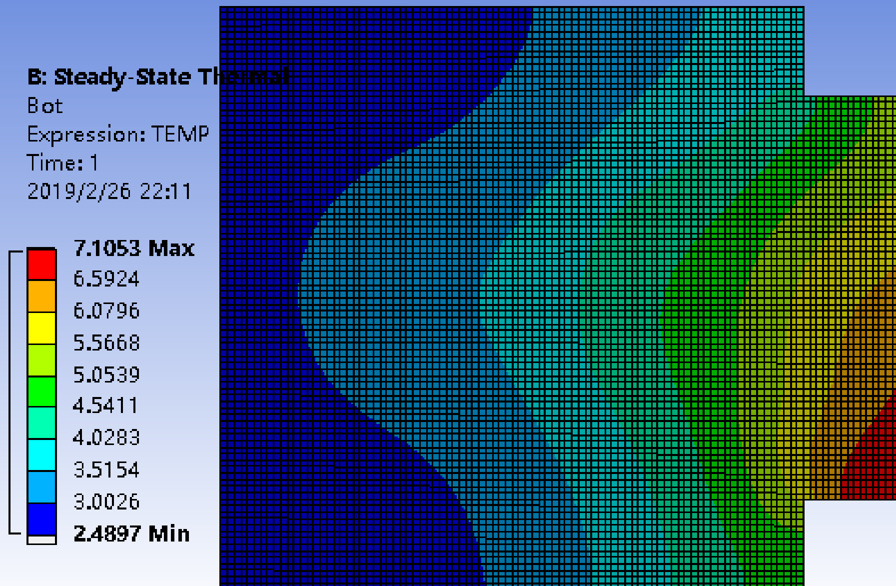


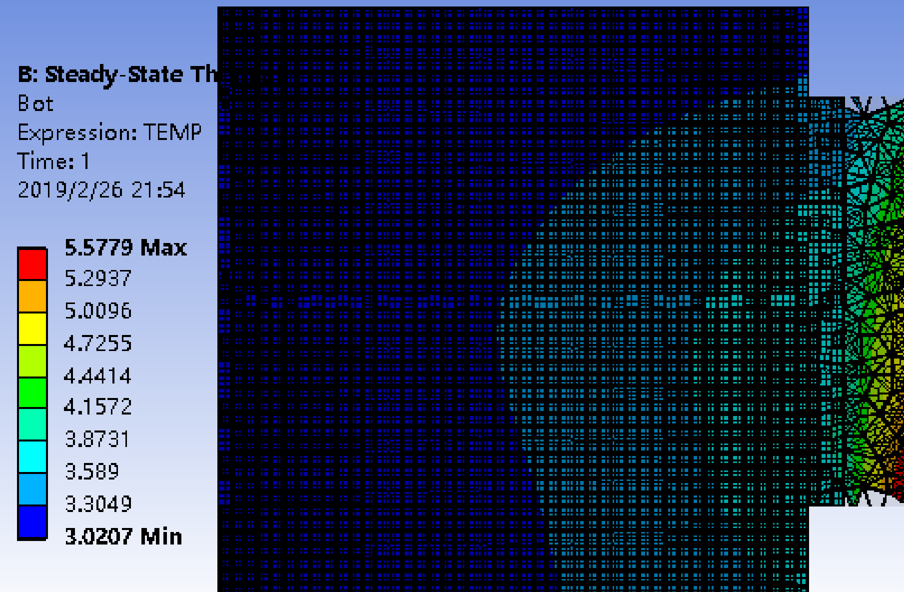
Two tungsten plates (2.8mm) are put on the top and the bottom side

Standalone



Temperature: 2.5-7.1 ℃

Double Tungsten



Temperature: 3.0-5.6 ℃

Ambient Temperature: 0 ℃

Difference Value in One Face

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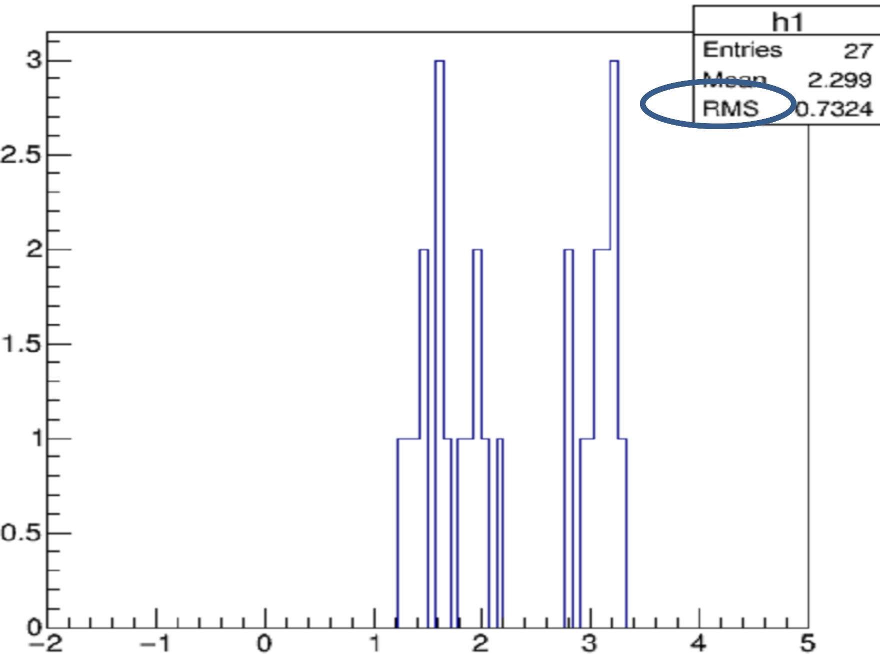

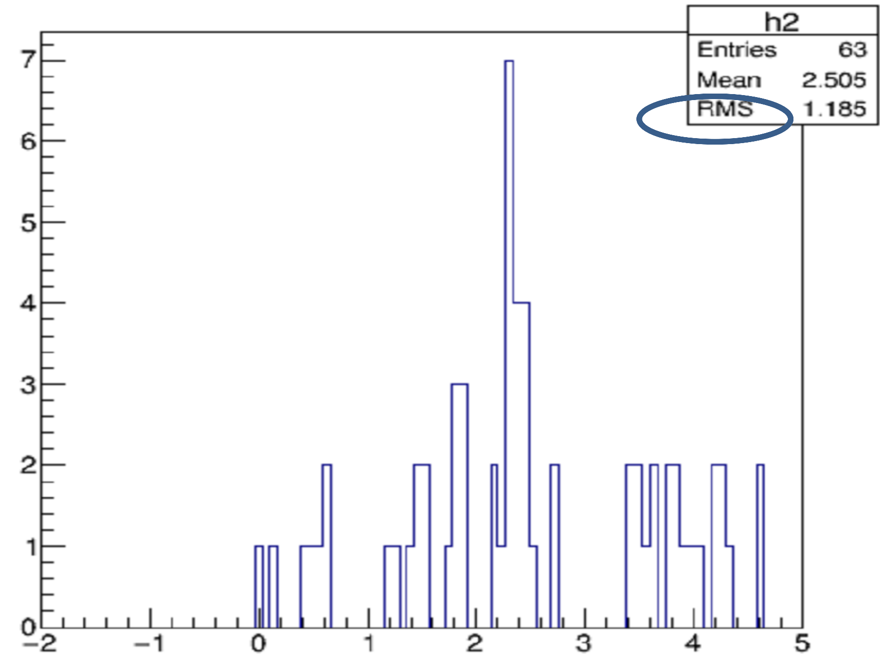

- Temperature Difference between 9*3 & 9*7 measured points and environmental Temperature from data
- The existence of Wolfram will relatively reduce the difference value of the temperature distribution.(Based on simulation and experiment we have done before.)

30-Layer with 6-chip PCB

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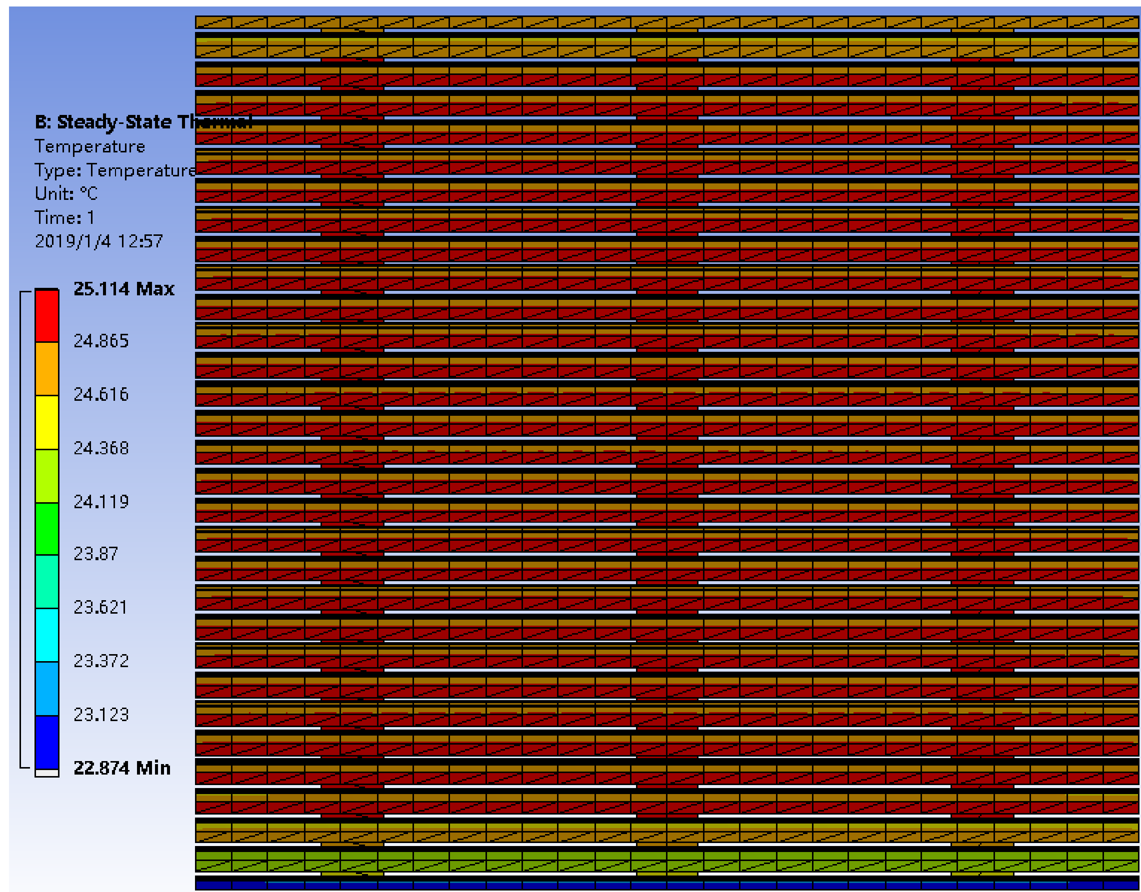

Ambient Temperature:22℃

- Simulation of a 30-Layer model with ScW
- Only 6-chip on each layer's PCB
- Due to the influence of adjacent layers, middle layers have higher temperature.

Temperature vs Layer

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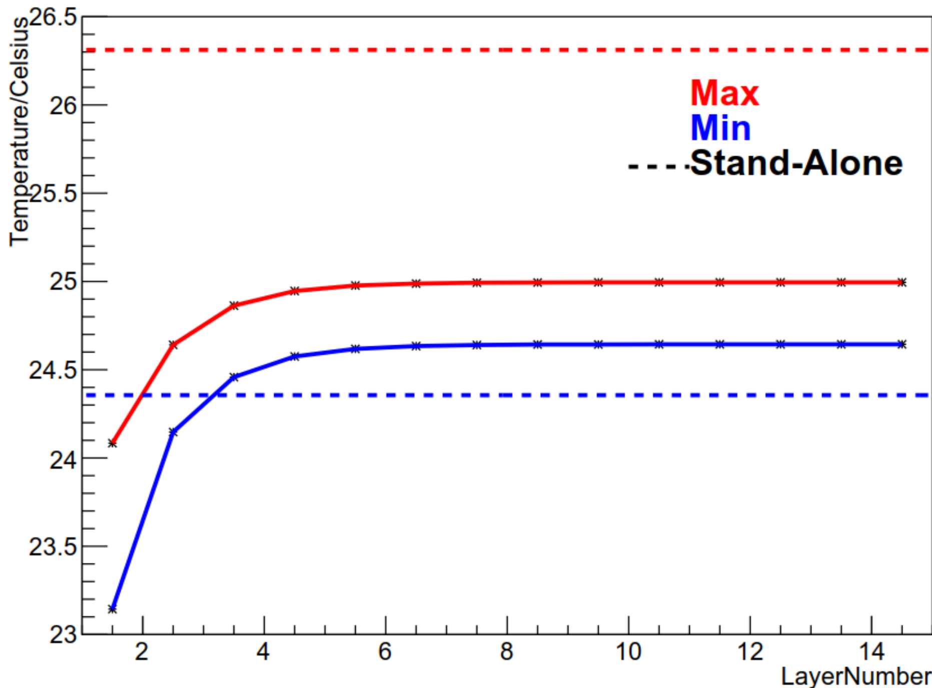

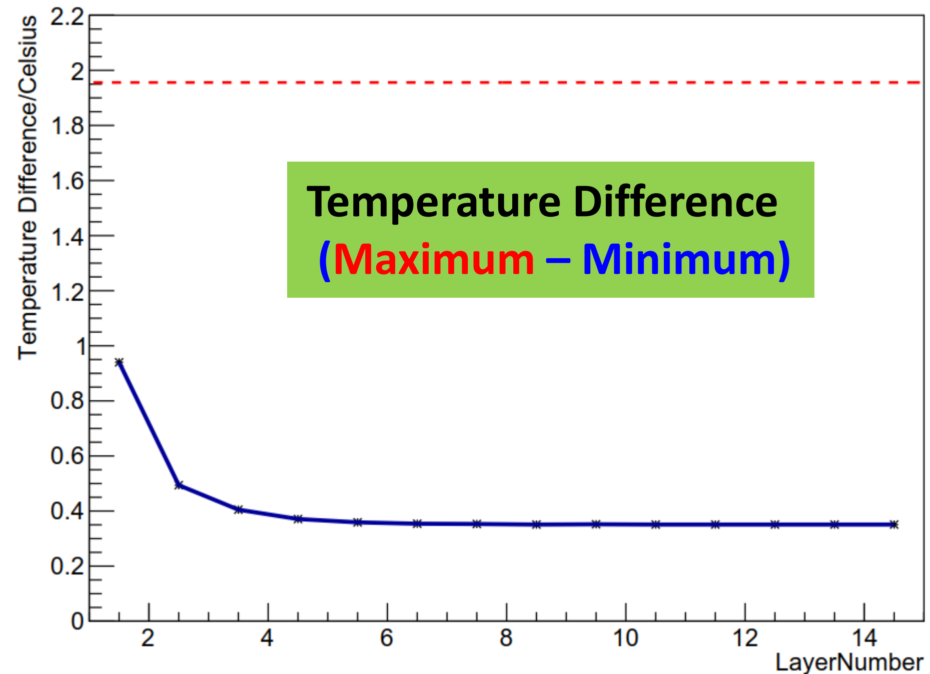

- **Due to the influence of adjacent layers, middle layers have higher temperature than layers in the front or end. Temp in the middle part keeps stable.**
- **With absorbers, the model has a better thermal conductivity, it results in a temperature difference value which is lower than that in a stand-alone PCB.**

Model with different cooling conditions

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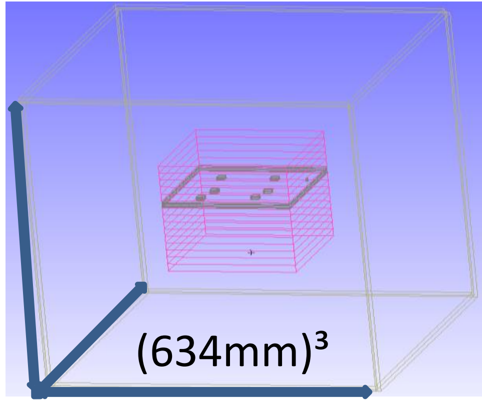
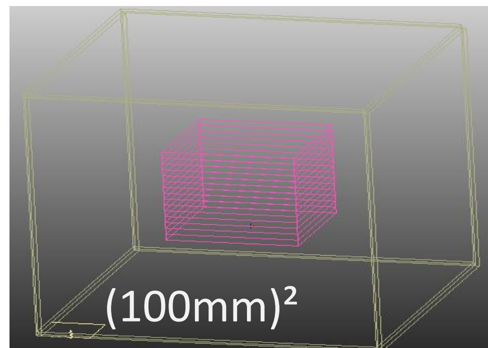


No cooling+ closed

W
PSD
Electronics+ Si heat transfer
W
Electronics+ Si heat transfer
PSD



No cooling+ an opening

Environment temperature: All set to 20 ℃.

Material of closed shading box: Aluminium (10mm).

30-Layer With Fan and water cooling

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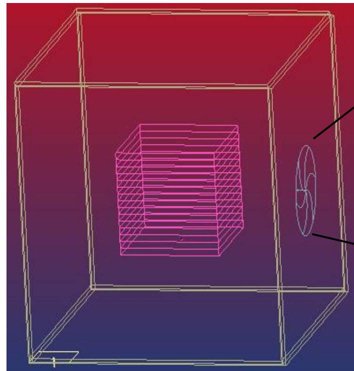
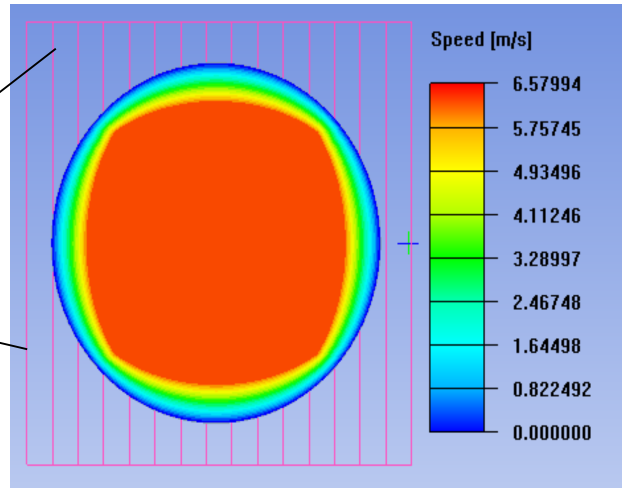


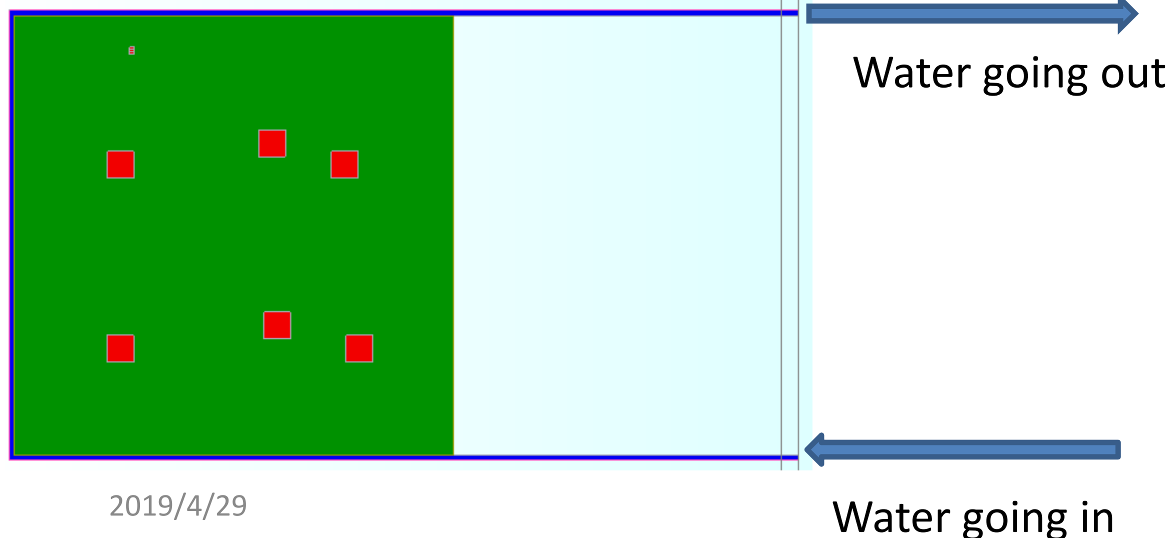
Fan cooling (r=0.1m)



Intake of the fan: 0.2066 m^3/s

Water temperature: 20 at the entrance

Water velocity: 0.5m/s



Water going out

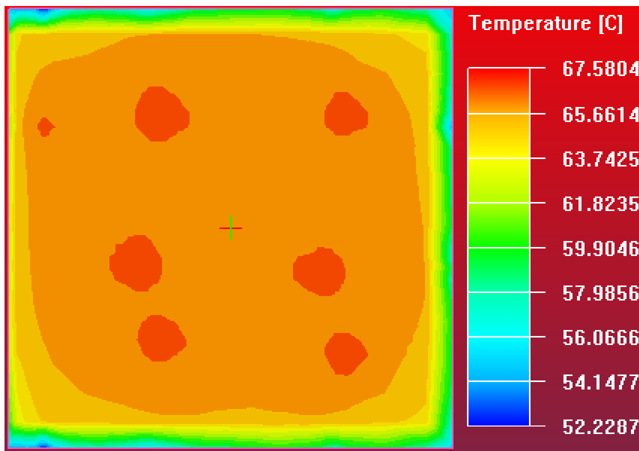
Water going in

Water comes in-N-out

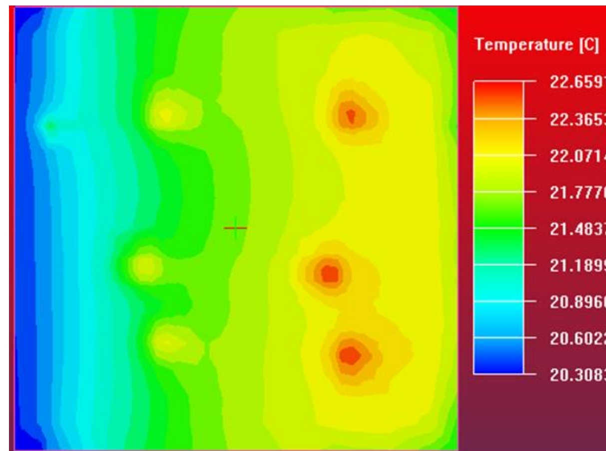
Profile of pipe

Results of different cooling methods

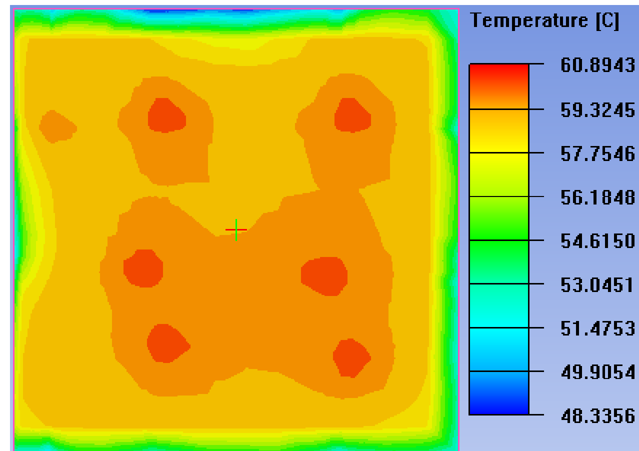
USTC+SJTU



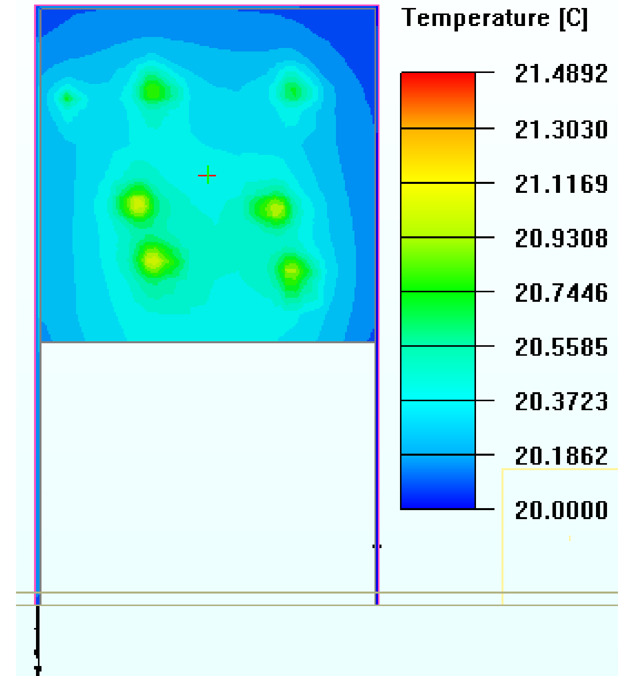
Layer15 without cooling



Layer15 with fan cooling



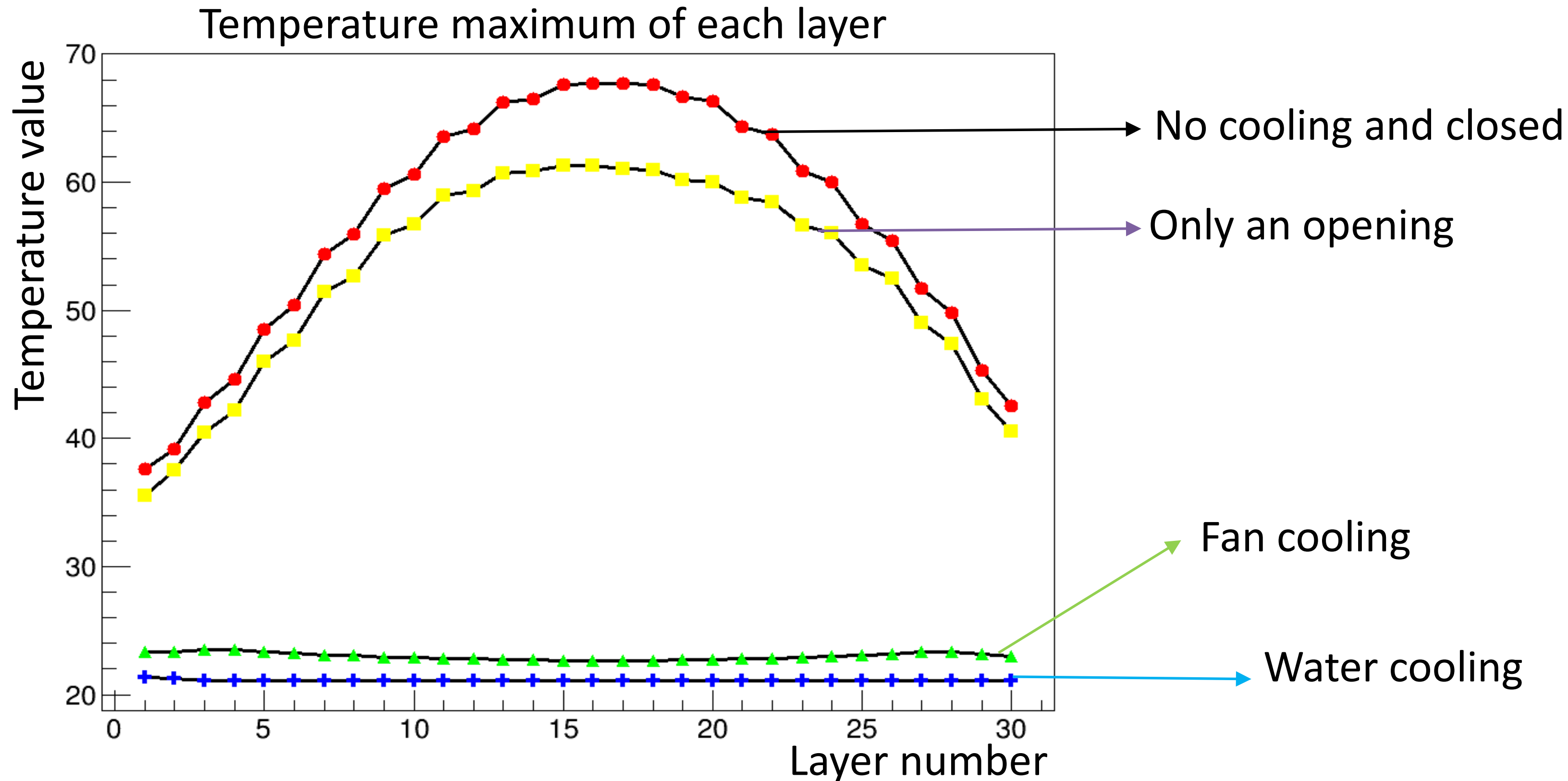
No cooling+ an opening



Water cooling Layer 15

Result of different cooling methods

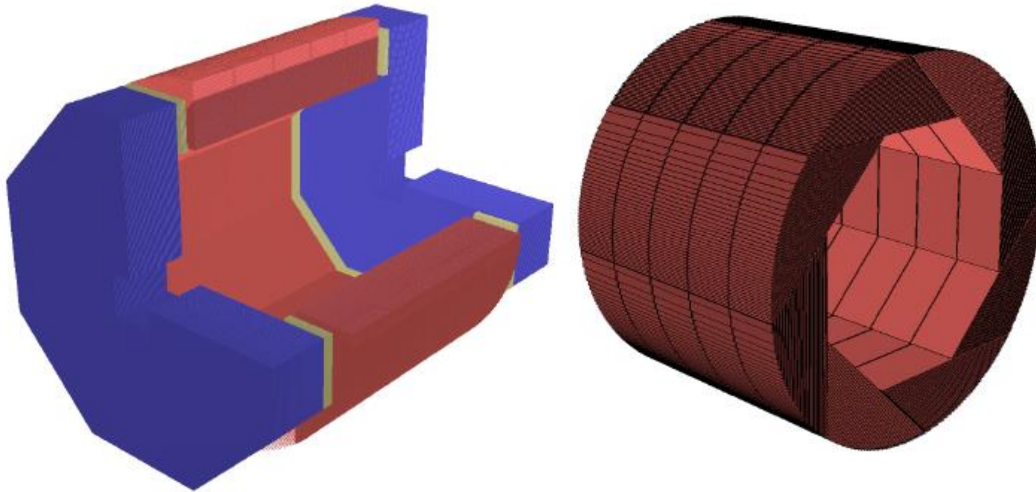
USTC+SJTU

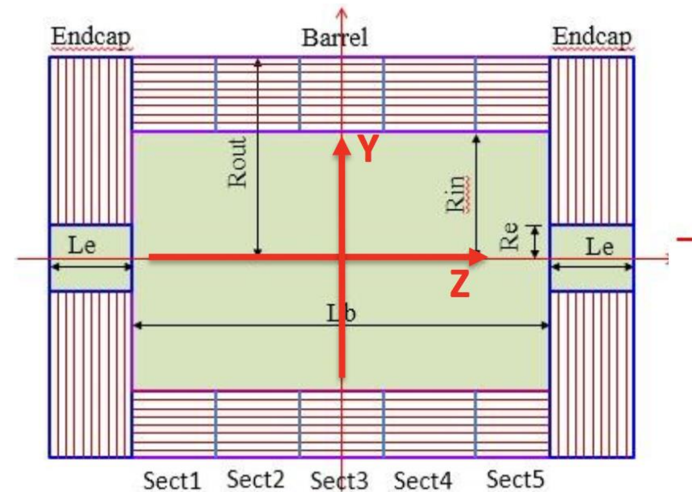


1. **A cooling system is currently needed.**
2. **For a prototype, fan cooling is nearly enough.**
3. **Water cooling may be a difficulty from the perspective of mechanics**

HCAL: Geometry and Layout

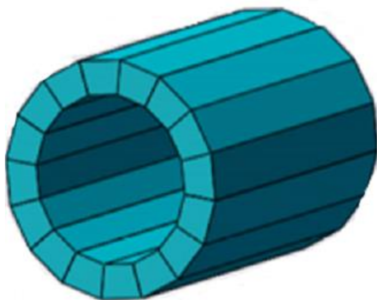
SDHCAL



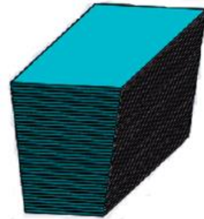


AHCAL

AHCAL barrel



AHCAL super module



AHCAL endcap

- Inner radius in X-Y plane R_{in} = 2300mm
- Outer radius R_{out} = 3340mm
- Inner & outer of HCAL endcap in Z-axis are 2670mm and 3710mm

HCAL Channel Counts, Power Consumption

- **HCAL Barrel, R_{in} = 2.3m, R_{out} = 3.34m, length = 2.67*2=5.34m, N_{layer}=40**
  Area of HCAL barrel = $2*PI*[(R_{in}+R_{out})/2]*L*N_{layer}$ = 3782 m^2
- **HCAL Endcap (2), R_{in} = 0.35m, R_{out} = 3.34m, N_{layer}=40**
  Area of HCAL endcap = $2*PI*(R_{out}*R_{out} – R_{in}*R_{in})*N_{layer}$ = 2772 m^2

Cell Size \ channels	HCAL Barrel	HCAL Endcap	Channels (N_{ch})	Power AHCAL	Power SDHCAL
1cm x 1cm	**37.82M**	**27.72M**	**65.5M**		**101 kW**
2cm x 2cm	9.455M	6.93M	16.4M		52 kW
3cm x 3cm	**4.2M**	**3.08M**	**7.3M**	**110 kW**	**43 kW**
4cm x 4cm	2.36M	1.73M	4.1M	88 kW	
5cm x 5cm	1.51M	1.11M	2.6M	77 kW	

Power Consumption (rough estimation):

AHCAL: 7mW/ch * N_{ch3} + 9W/DIF/m^2 * 6554 (59kW)

SDHCAL: 1mW/ch * N_{ch1} + 5.4W/DIF/m^2 * 6554 (35.4kW)

Active cooling is likely needed.

Electronics channels / m^2

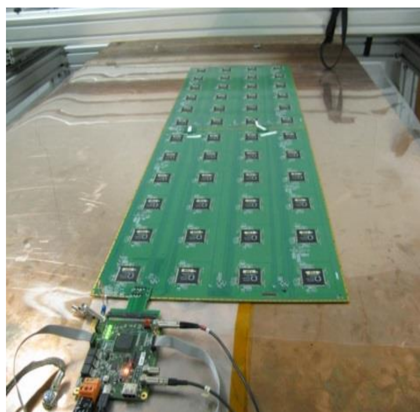
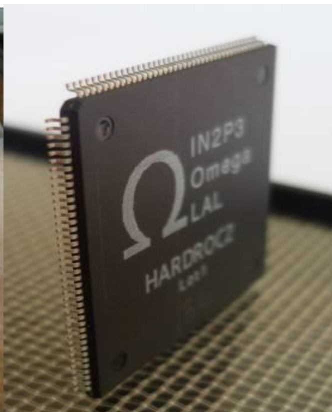
IPNL

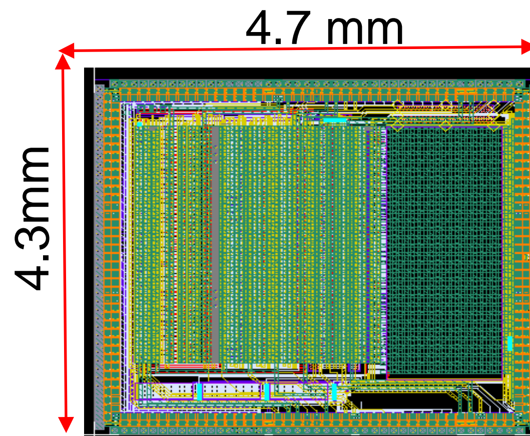
$(0.12\lambda_I, 1.14X_0)$

Stainless steel Absorber(15mm)
Stainless steel wall(2.5mm)
GRPC(6mm $\approx 0\ \lambda_I, X_0$)
Stainless steel wall(2.5mm)

- ➔ SDHCAL for CEPC has 40 layers
- ➔ Each layer: 3 mm RPC
  + 1.2 ~ 1.4 mm PCB
  + 1.6 mm ASIC (Hardroc)
- ➔ 20mm steel absorber (2.5+2.5+15mm)

- ➔ 6 PCB to cover $1m^2$ RPC
- ➔ Each PCB size: 31 cm * 50cm ~ 1536 channels
- ➔ ASIC chip (Hardroc) has 64 channels, 4.3mm*4.7mm, cover (2.8cm*2.8cm)
- ➔ Each PCB with 1536-channel needs 24 ASIC chips (4*6)
- ➔ Power: 1mW/ch * 64 ch = 964 mW/Chip
- ➔ **Power: 1mW/ch * 6*24*64 ch = 1mW/ch*9216ch/m^2 = 9.2W/m^2**



PCB with ASICs

IPNL

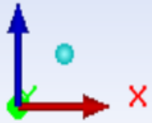
- ➔ Each PCB size: 31 cm * 50cm
- ➔ 24 ASIC * 64 ch = 1536 ch
- ➔ 6 PCB to cover $1 m^2$ RPC
- ➔ Each PCB has 24 ASICs and 1536-ch

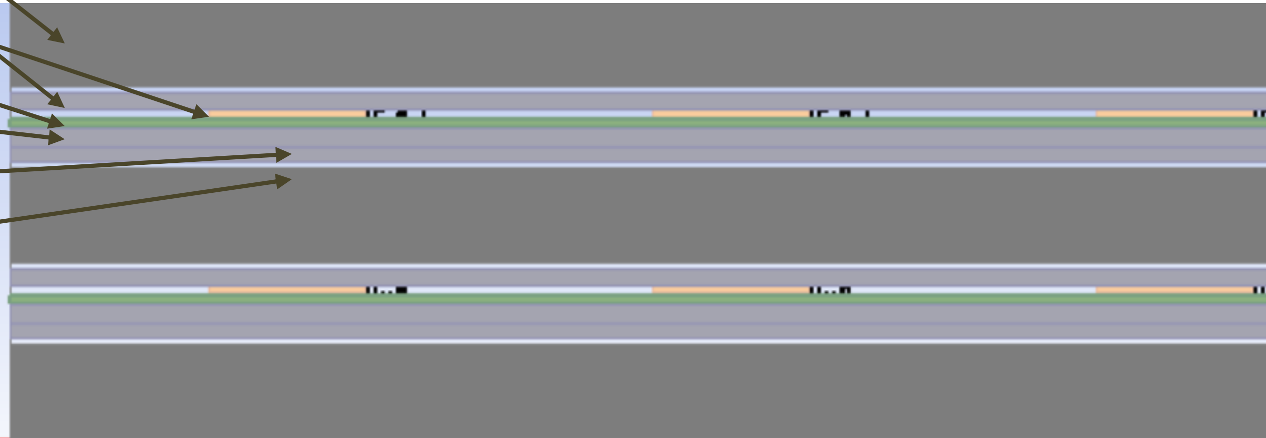
Geometry with 5-Layer

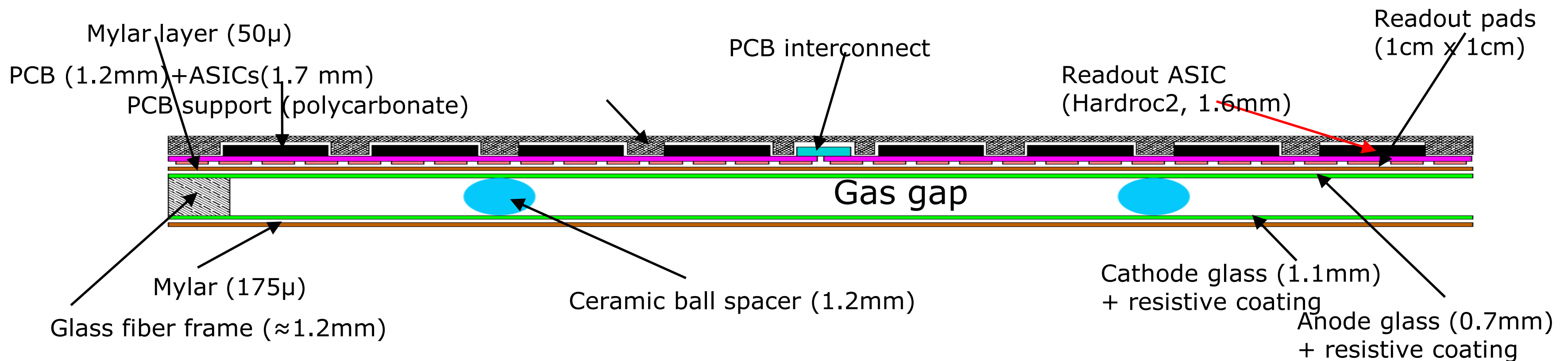
IPNL+SJTU

15mm absorber(Fe)
2.5mm absorber
1.6mm ASIC
1.4mm PCB
3mm RPC
2.5mm absorber
15mm absorber

A 5-layer model without cooling, gravity along -z







Simulation vs Measurements

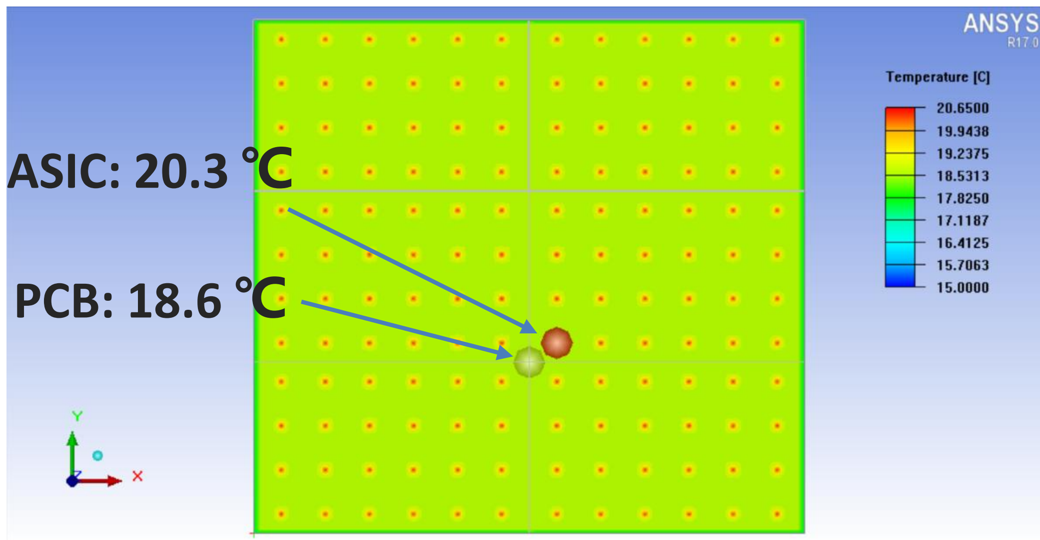
IPNL+SJTU

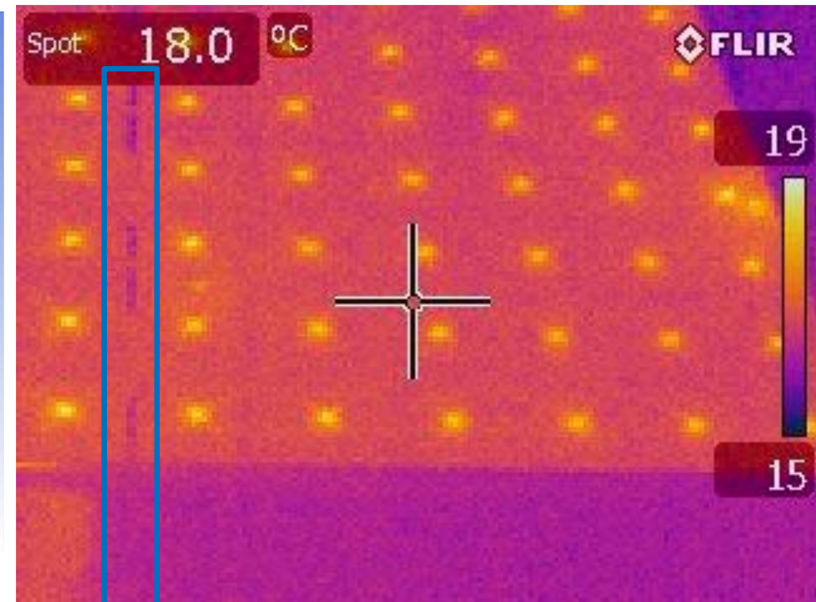
Temperature Simulation:
- PCB+ASIC: 18.6 – 20.3 ℃
- ΔT: 1.5℃

Temperature Measurements:
- PCB+ASIC: 18 – 19 ℃
- ΔT: 1.0 ℃

Simulation at SJTU

Measured at IPNL

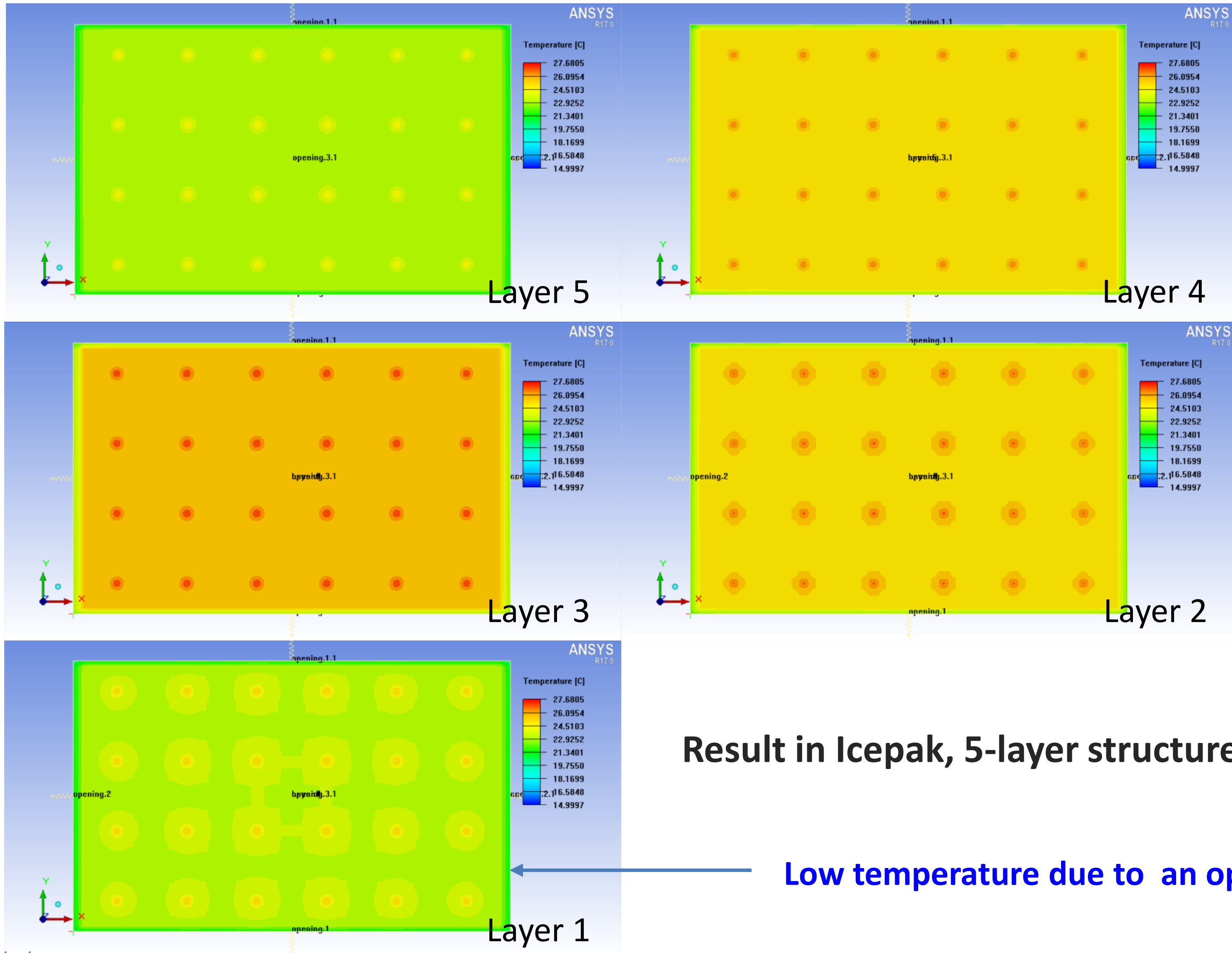




Initial temperature: 15℃,
convection parameter: 3W/(K*m²)
Simulation with Icepak

Low temperature at the gap region between two PCBs

Simulation Results: 5-Layer



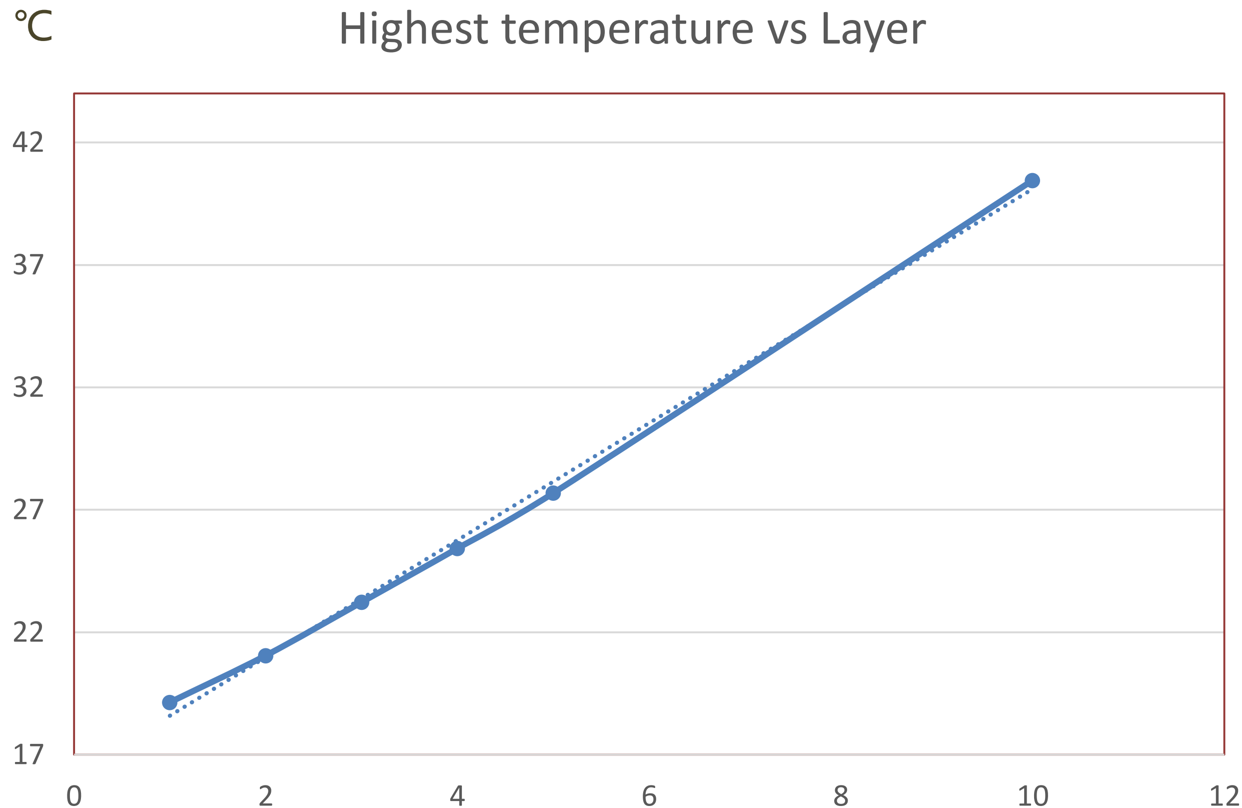
Result in Icepak, 5-layer structure

Low temperature due to an opening

Increase the Layer of RPC on HCAL

IPNL+SJTU

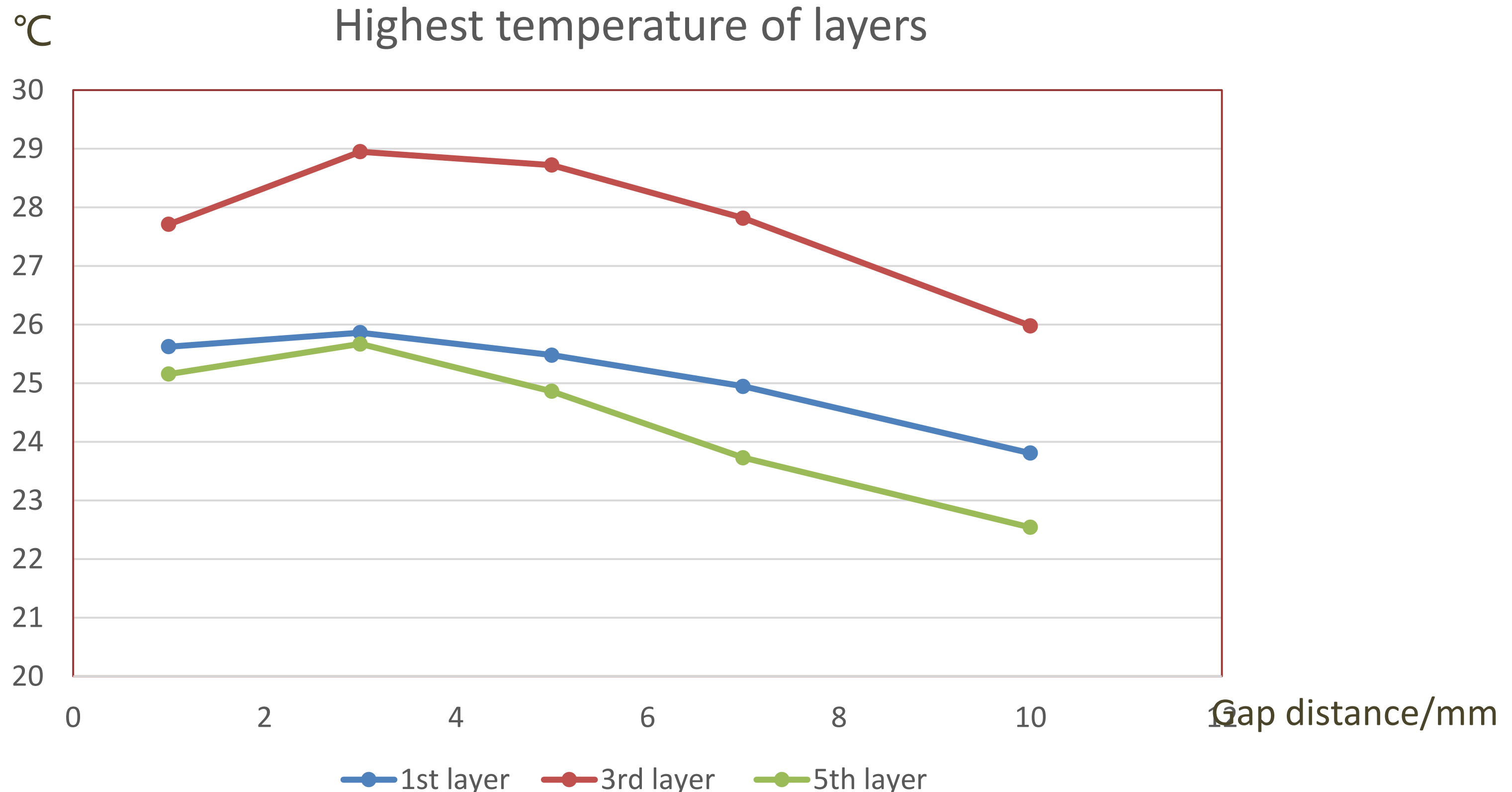
- Ambient Temperature:15℃
- Linearity increase of Temp but will not always increase when layer increase



Comparison between with different air gaps

IPNL+SJTU

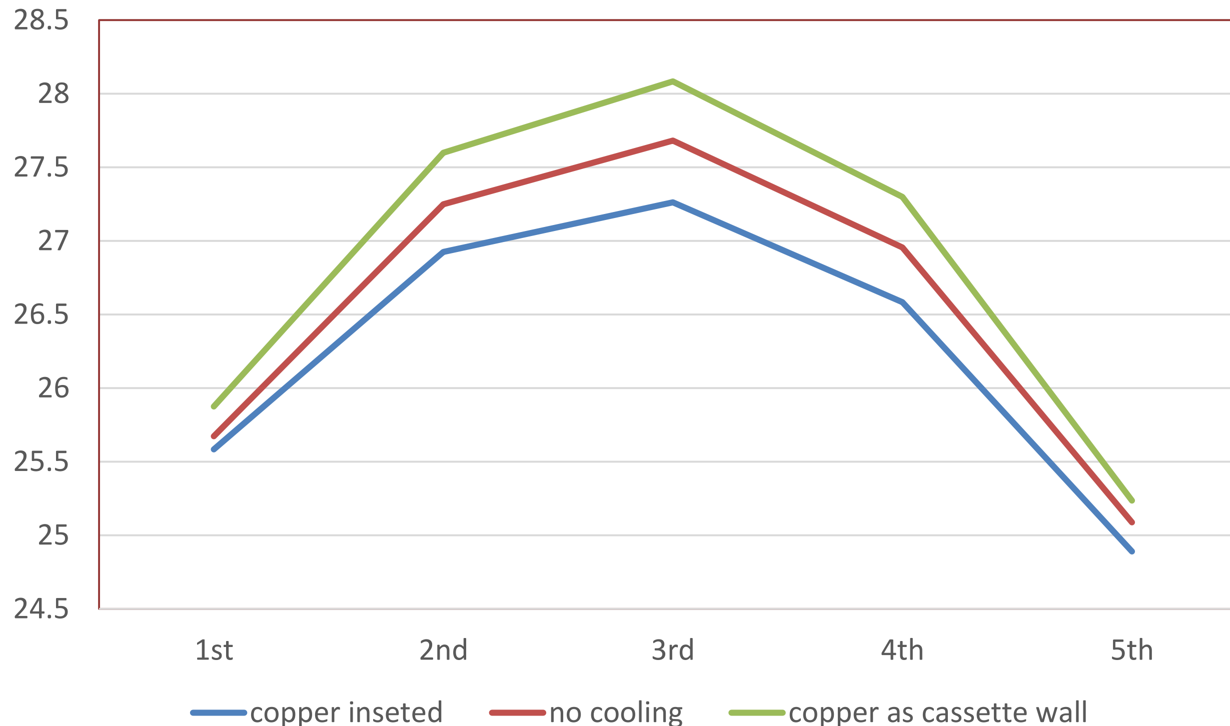
- **Ambient Temperature: 15℃**
- **Here the are gaps means the gap between the stainless steel absorber and supporter layer(the holder box)**
- **The temp Increases first and then declines**



Results with copper plates

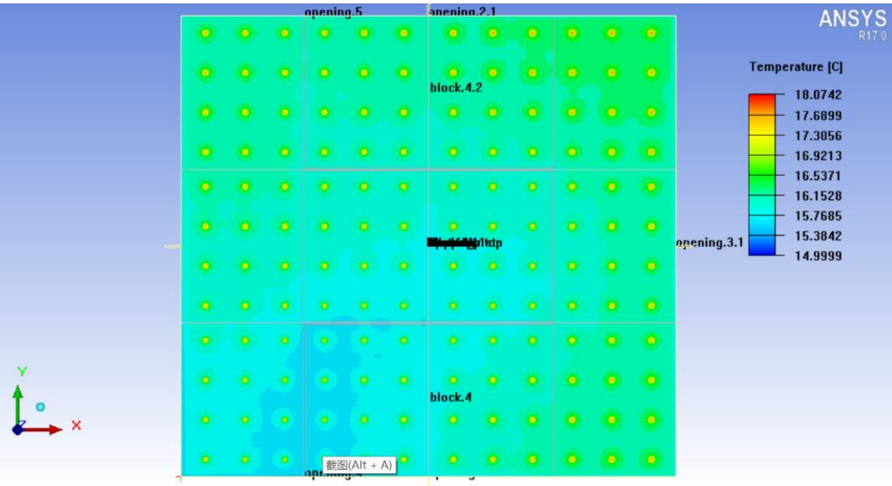
IPNL+SJTU

- **Green Line: The 2.5mm stainless steel absorber is replaced by 2mm copper plates**
- **Blue Line: The 4mm copper plates are putted on the top face**
- **Comparison of maximum Temp with/without copper plates**

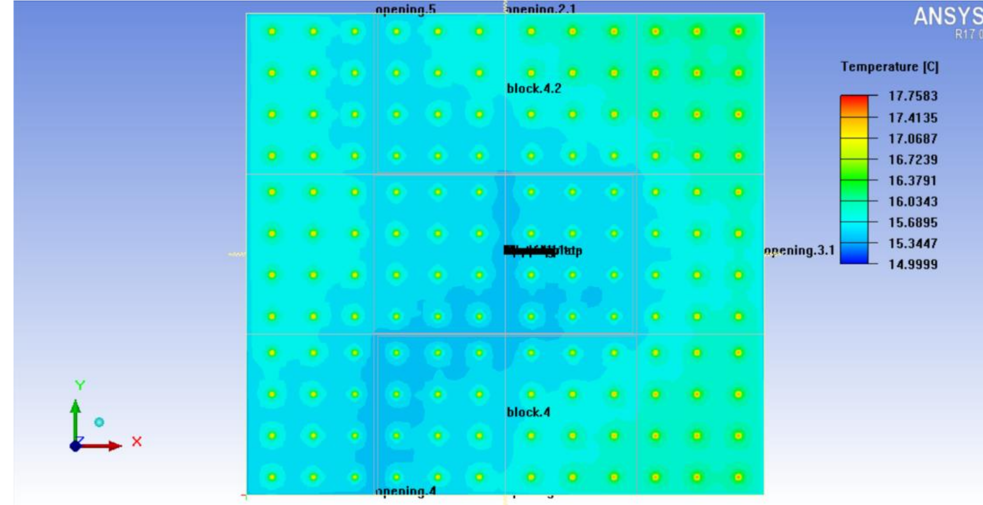


Different Water Flow velocity

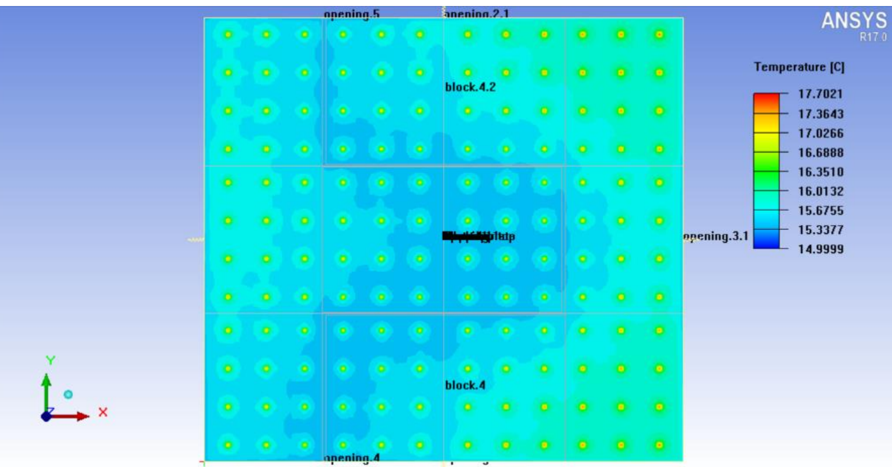
IPNL+SJTU



Flow velocity 0.1m/s



Flow velocity 0.5m/s

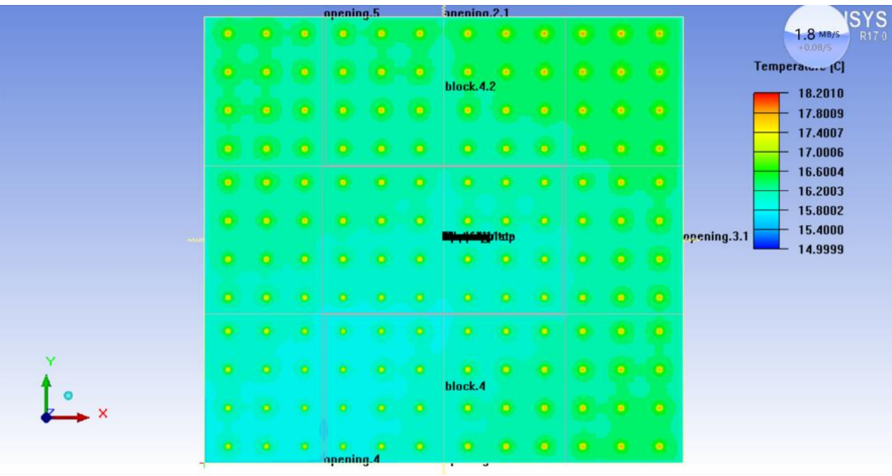


Flow velocity 1m/s

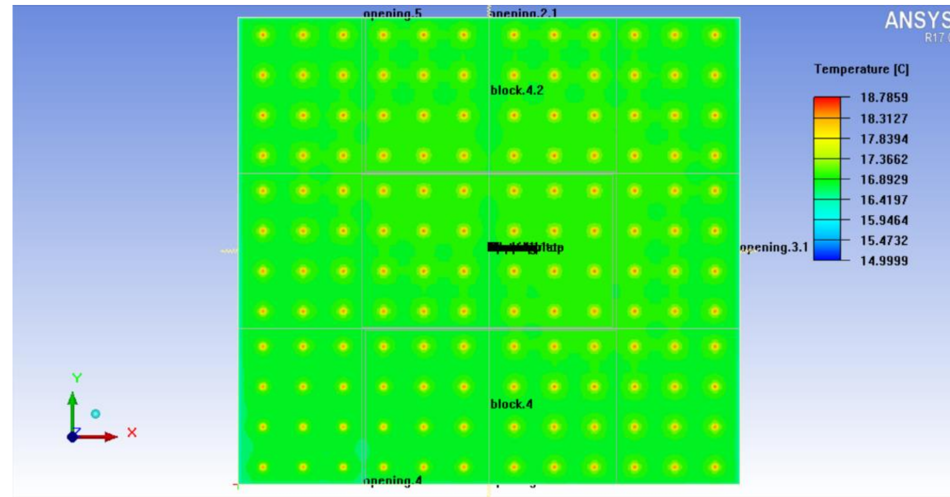
- **One layer**
- **Water cooling**
- **Higher rate, lower temperature**

Different Co2 Flow velocity

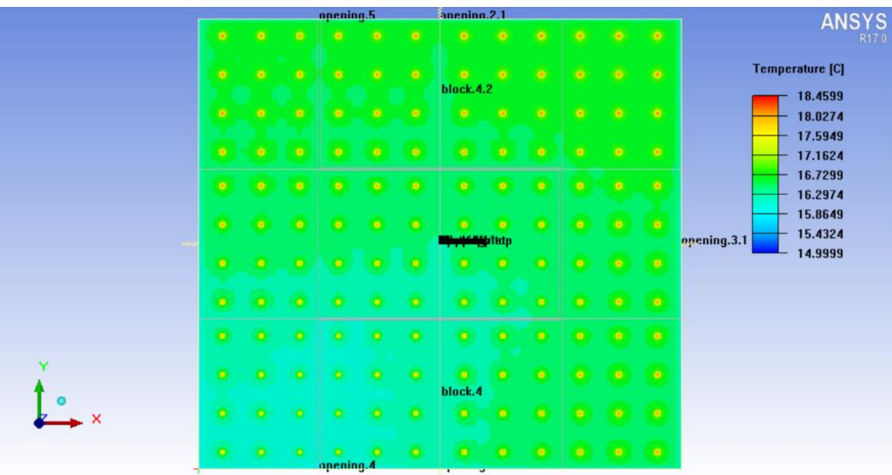
IPNL+SJTU



Flow velocity 0.1m/s



Flow velocity 0.5m/s

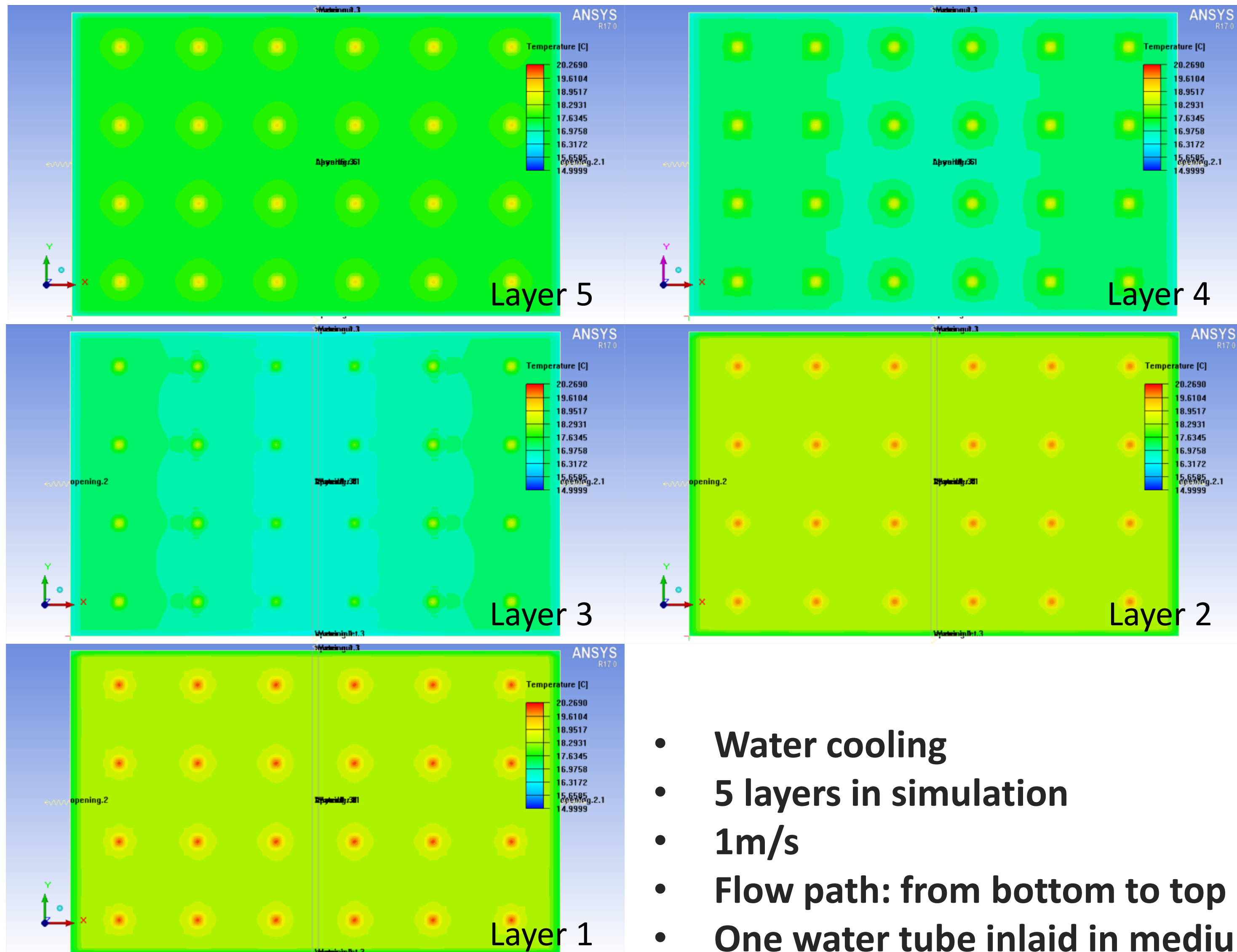


Flow velocity 1m/s

- **One layer**
- **Co2 cooling**
- **Water cooling is more efficient**

Add 4mm copper absorber plates and one water tube in third layer

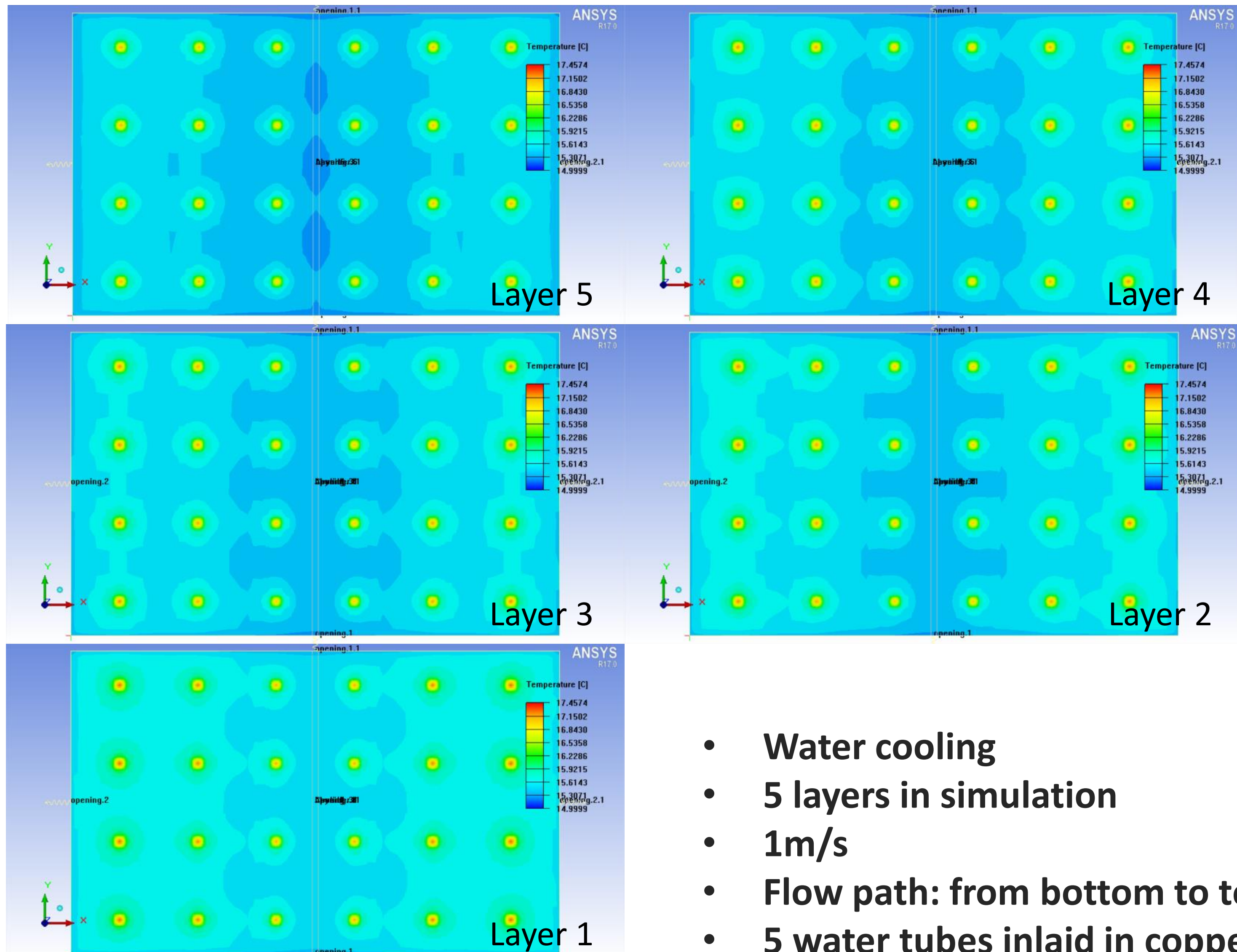
IPNL+SJTU



- Water cooling
- 5 layers in simulation
- 1m/s
- Flow path: from bottom to top
- One water tube inlaid in medium copper layer

Add 4mm copper absorber plates and water tubes in those plates

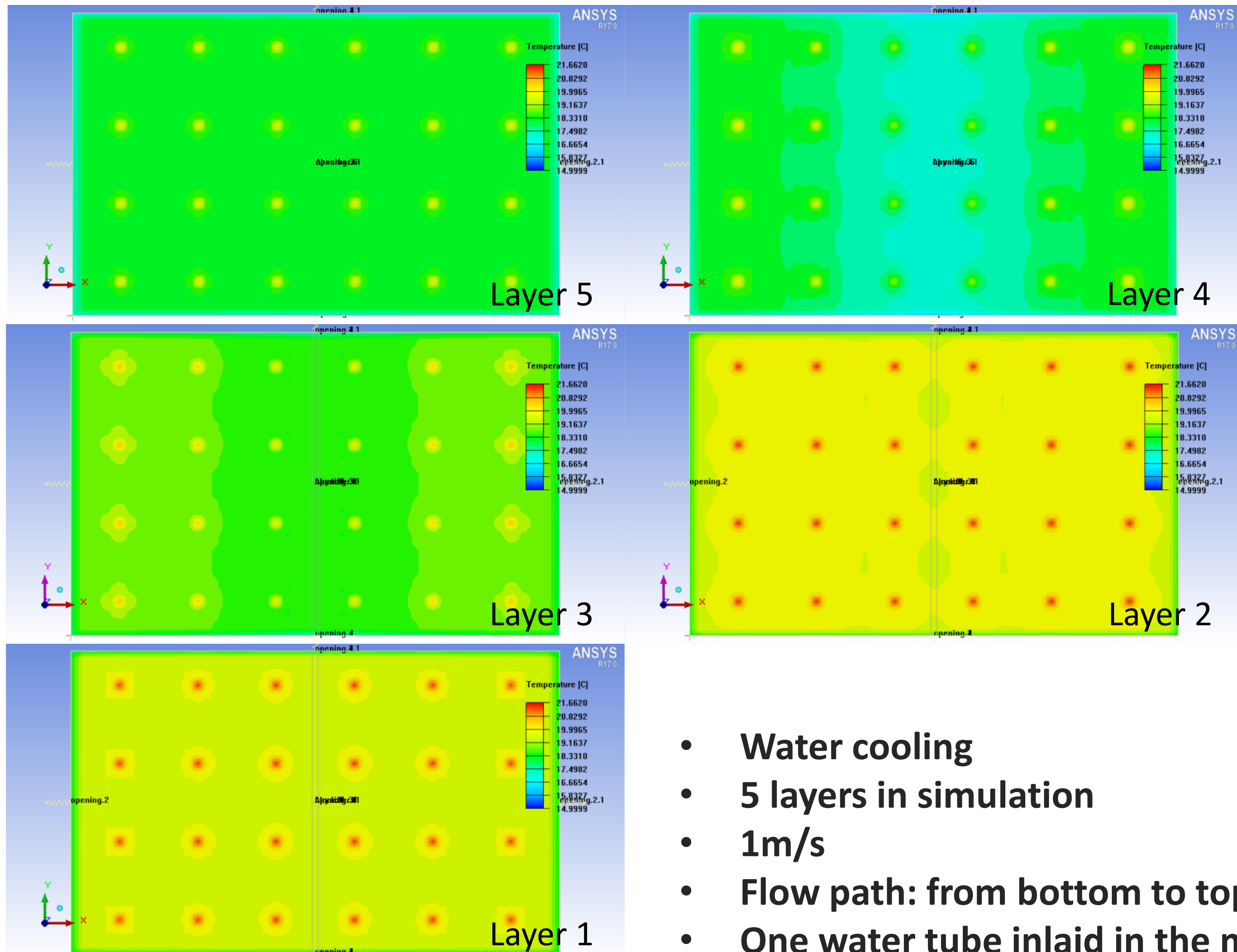
IPNL+SJTU



- Water cooling
- 5 layers in simulation
- 1m/s
- Flow path: from bottom to top
- 5 water tubes inlaid in copper layers
-

We put water pipe inlaid in the third layer's absorber

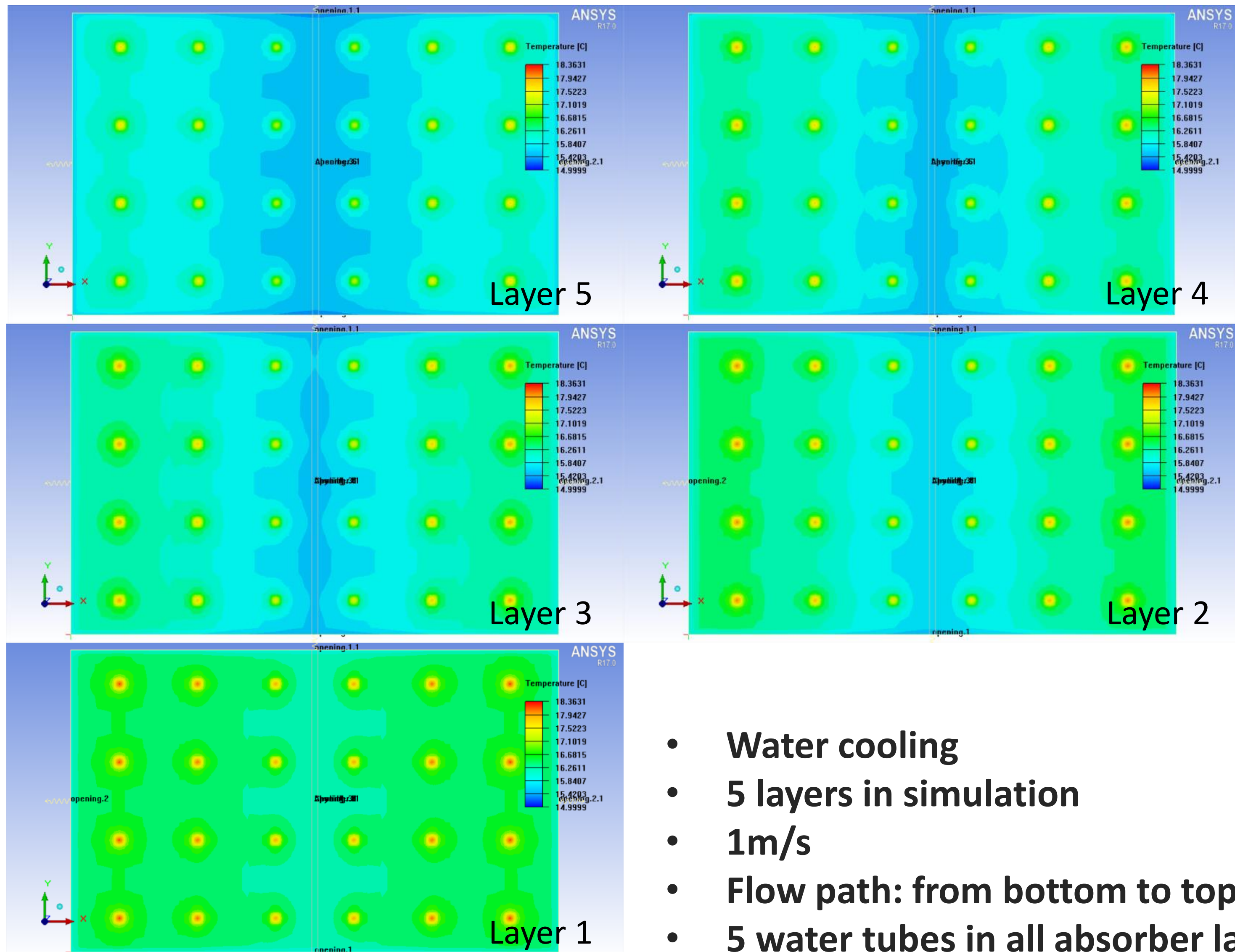
IPNL+SJTU



- Water cooling
- 5 layers in simulation
- 1m/s
- Flow path: from bottom to top
- One water tube inlaid in the medium absorber layer

We put water pipe in all absorber layers

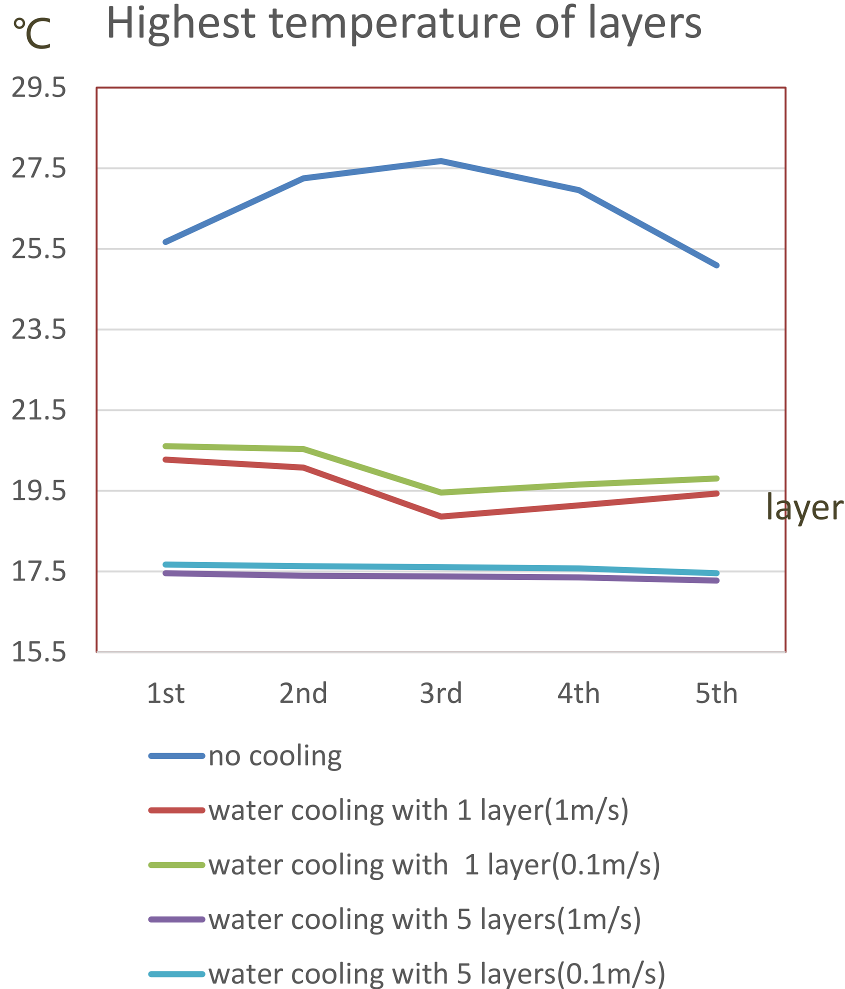
IPNL+SJTU

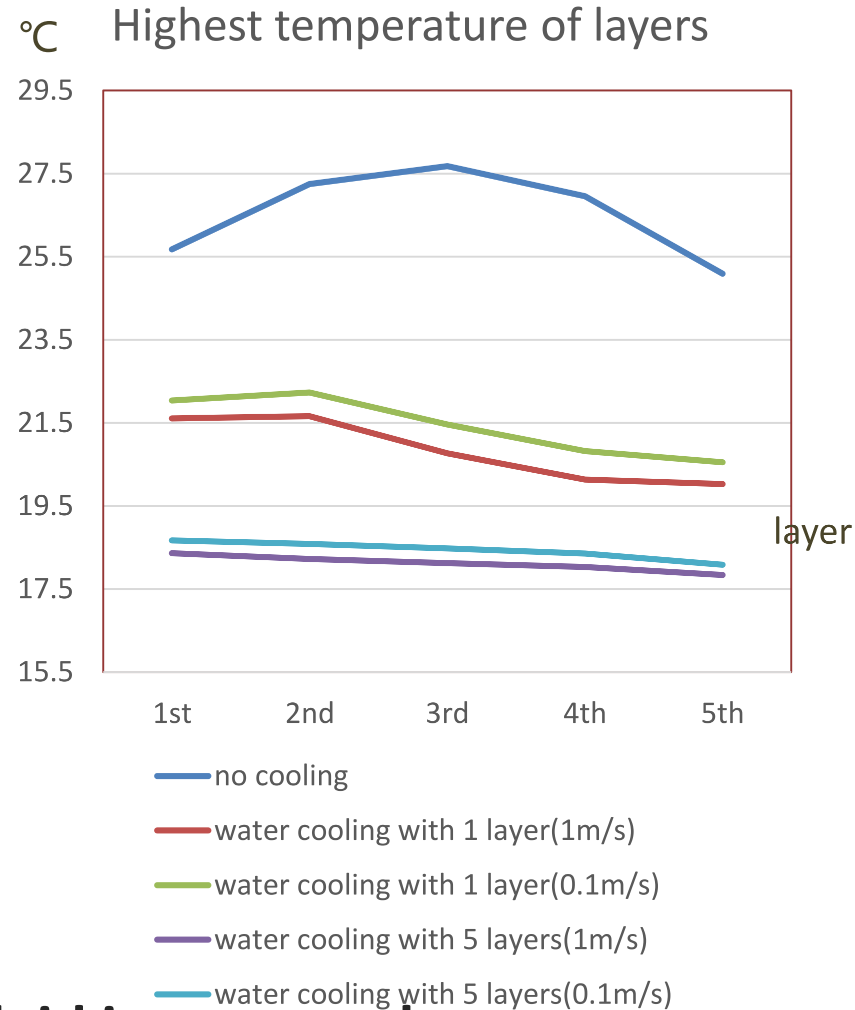


- Water cooling
- 5 layers in simulation
- 1m/s
- Flow path: from bottom to top
- 5 water tubes in all absorber layers

The comparison with two methods

IPNL+SJTU

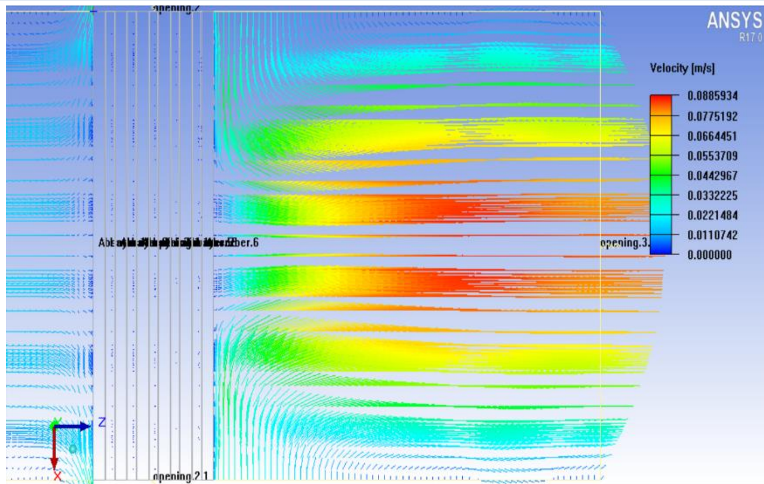




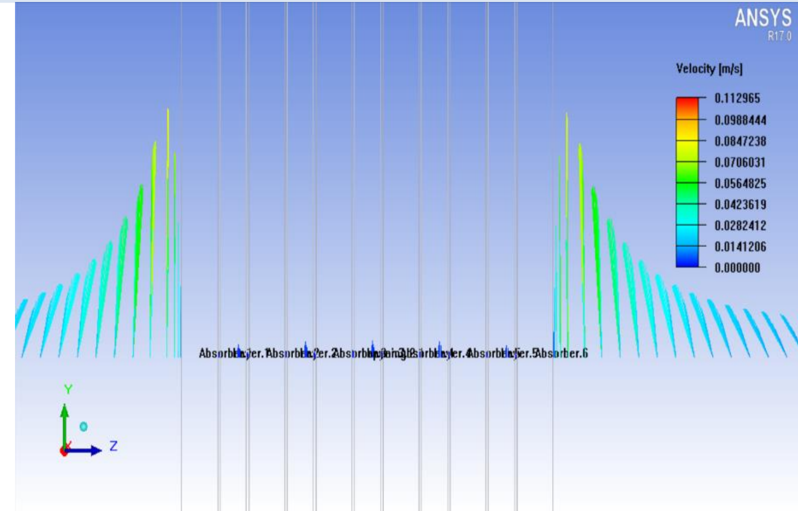
- **Left: copper plates + water tubes inlaid in copper plates**
- **Right: water plates in the absorber layer**
- **Left method is better**

The gravity influence on temperature

IPNL+SJTU

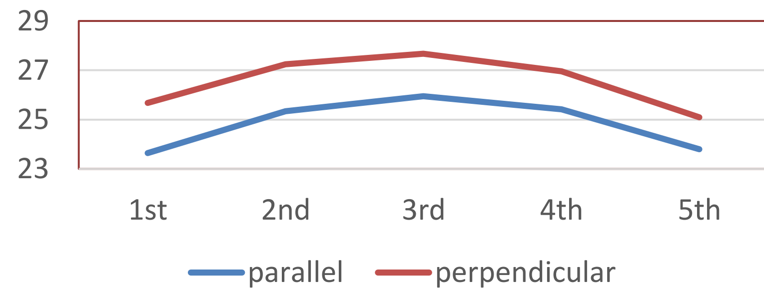


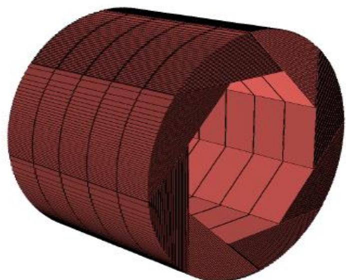
Gravity perpendicular to PCB plane



Gravity parallel to PCB plane

- **The upper two graphs show the neighbouring air velocity disturbed by heat**
- **When parallel, around 2 degrees lower**





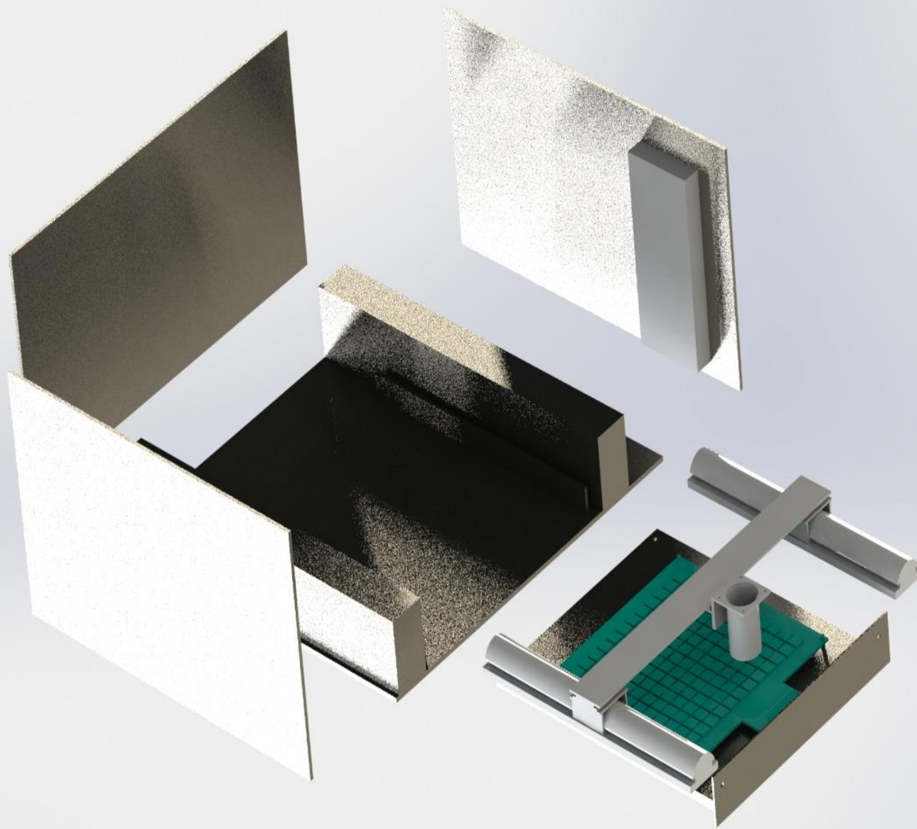
Results with Power Pulsing: 1% duty cycle

- 64mW/chip → 0.64mW/chip
- Temperature can be well controlled in power pulsing mode

Layer	Highest T (℃)	Lowest T (℃)	Standard deviation (℃)
1	15.1900	15.1112	0.00724
2	15.2025	15.1208	0.00746
3	15.2047	15.1231	0.00740
4	15.1966	15.1185	0.00702
5	15.1784	15.1067	0.00635

Physics motivation of the scintillator test system

USTC+SJTU



- Scintillator batch test for AHCAL
- Measure the fluorescence yield of scintillator through the beta-ray radiated from Sr90
- Radioactive source can move in x-y plane hanged by mechanical arm
- Plastic scintillators are placed on a specialized PCB
- The whole system need to be placed within a dark , no dust environment

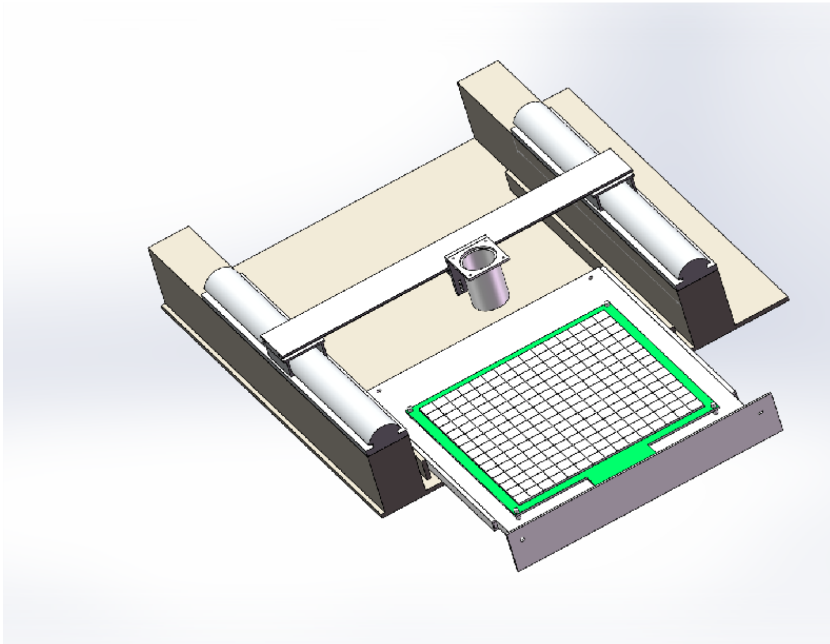
Overview of the scintillator test system

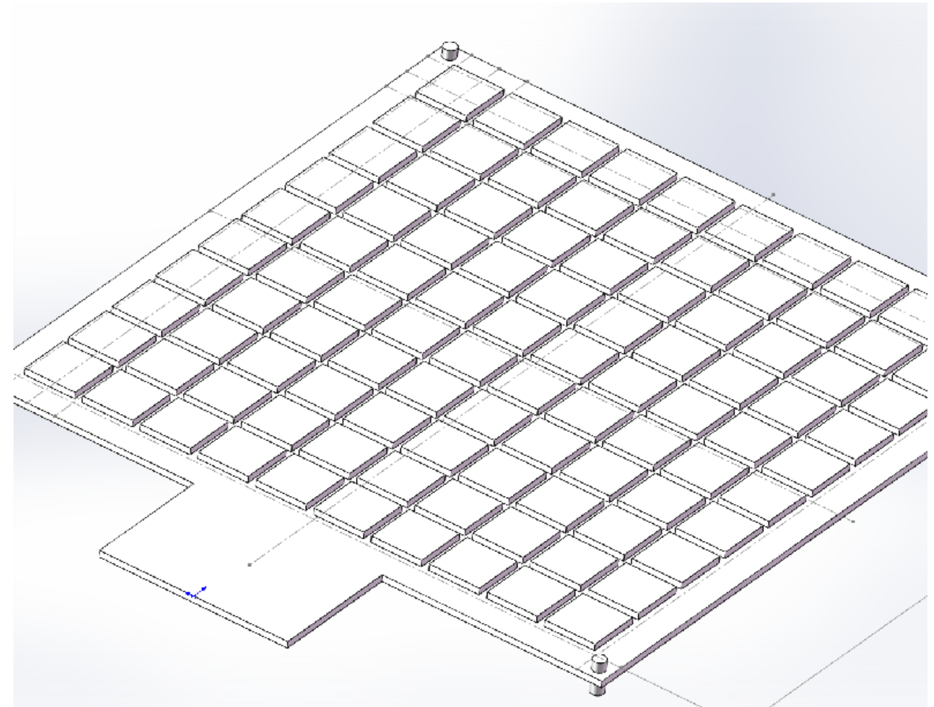
USTC+SJTU

- The outer box has been finished
- 1200mm*1185mm*620mm
- Those holes in the front are prepared for future cables from PCB

The system will realize

USTC+SJTU

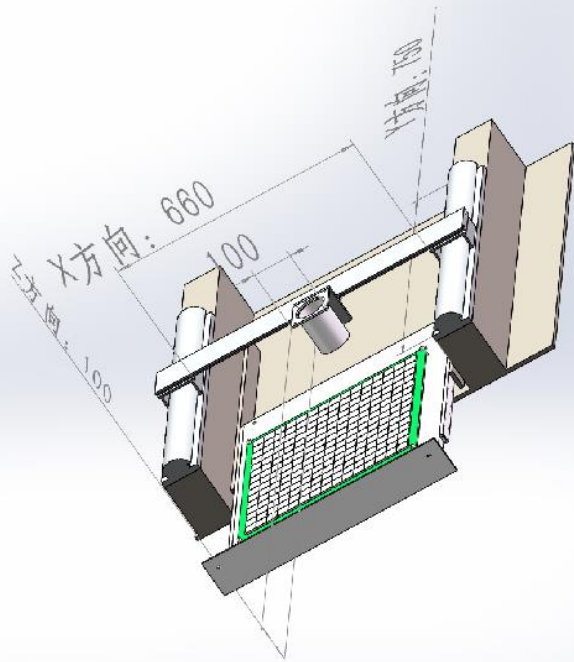


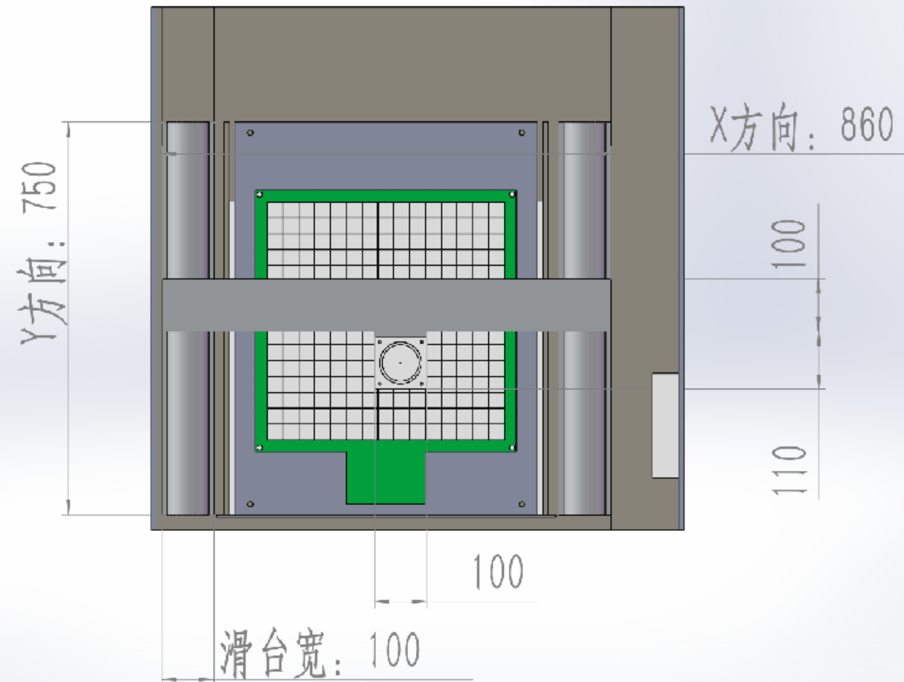


- PCB size: 60cm*60cm , each batch we could place 360 scintillators, 1min*360 = 6h/batch
- control on the computer

The design of structure

USTC+SJTU





- the slipway should be longer? 1000mm?
- Depends on the size of PCB
- Even though the pcb design not fixed, we can still place an overplate on drawer
- To avoid reflect light: all those apparatuses in the box should be black

Requirements of each apparatuses

USTC+SJTU

If slipway length: X and Y direction ~ 800mm, Z ~ 5mm, then:
Servo motor: 0.2kW
Install the steel ball guide rail on the drawers' two sides

Requirements of each apparatuses

USTC+SJTU

专业承接各类电气自动化，PLC编程，触摸屏编程，组态开发设计，电气设计，电气安装

服务电话：18105733766 章工

Left： Control by computer, choose this method!

Right: Control by touch screen

Budget of control and power system and questions

USTC+SJTU

序号	名　称	品牌	数量	单价（元）	合计（元）	备　注
1	伺服电机(0.2KW)	日本三菱	3	2350	7050	
2	高柔性联轴器	国产	3			
3	PLC(FX5U)	日本三菱	1	2850	2850	
4	光电开关	欧姆龙/松下	9	100	900	
5	开关电源	明纬	1	300	300	
6	2P 空开带漏保	施耐德	1	200	200	
7	1P 空开	施耐德	4	60	240	
8	滤波器	国产	4	50	200	
9	继电器	欧姆龙	10	20	200	
10	电源开关	施耐德	1	200	200	
11	电控箱	国产定制	1	1000	1000	
12	端子排+线+其他	国产	1	500	500	
13	安装调试费，运费				4000	
13	电气图纸，电气设计费				3000	
	合计				20640	
	税				2680	13%
	合计				23323	

Total price : Box 18000+ holder 3000+23323+slipway 4000+other 3000 ~ 51323

Emitter size?
HCAL PCB size?

Summary and Future Plans

- Active cooling is needed for CEPC calorimeters operating at continuous mode
- Simulation results are comparable to measured temperature on PCB and Chips.
- Temperature goes higher with multi-layer structure
- Copper plates help to extract heat from the structure
- Water cooling helps to extract addition heat
- The slipway installation of batch test system are under consideration now.

Future Plans:

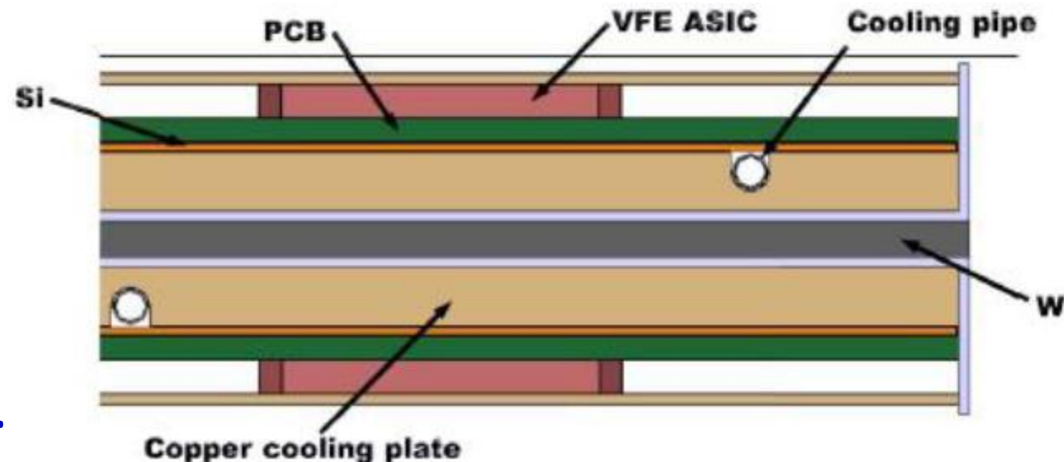
- Design cooling system for both ECAL and HCAL
- To build multi-layer cooling module with copper plate and tubes, use water or evaporative CO_2 as cooling agent

Active Cooling

- CEPC is designed to operate at continuous mode with beam crossing rate: 2.8×10^5 Hz. Power pulsing will not work at CEPC.
- Compare to ILD, the power consumption of VFE readout electronics at CEPC is about two orders of magnitude higher, hence it requires an active cooling
  - Evaporative CO_2 cooling in thin pipes embedded in Copper exchange plate.
  - For CMS-HGCAL design: heat extraction of 33 mW/cm^2, allows operation with 6×6 mm^2 pixels with a safety margin of 2
- To be modelled for Mokka simulation

➔ Transverse view of the slab with one absorber and two active layers.

➔ The silicon sensors are glued to PCB with VFE chips, cooled by the copper plates with CO_2 cooling pipes.



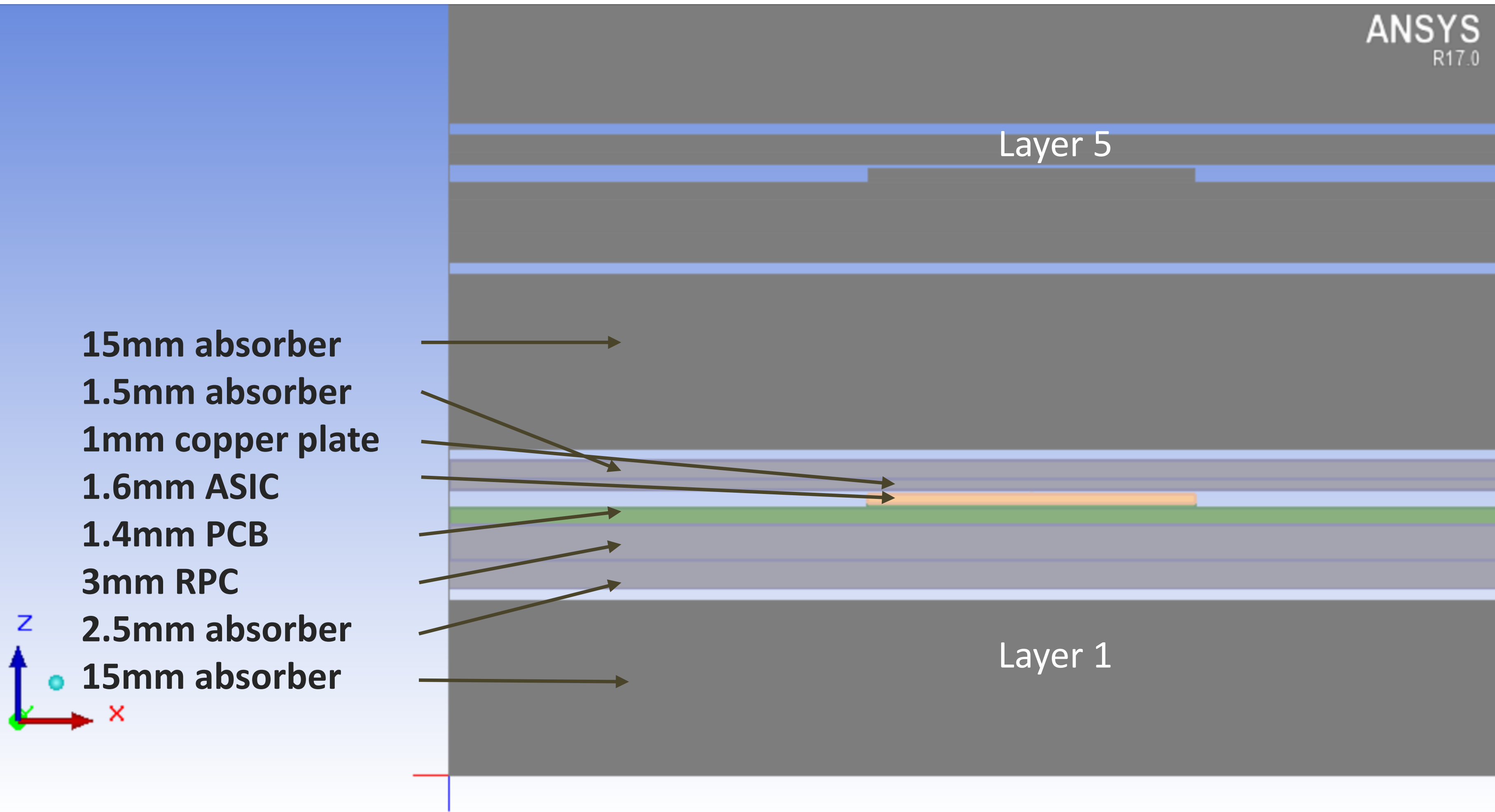
Simulation setup

- Turbulent mode
- Radiation: all solids
- Air flow: triggered by gravity
- Convection: natural convection
- Heat source: 64mW per chip /0.64mW

Thermal conductivity:

- absorber: stainless steel 14.4W/(m*K)
- RPC: glass 1.5W/(m*K)
- PCB: FR-4 0.35W/(m*K) copper 387.6W/(m*K)
- ASIC: silicon 180W/(m*K)

Geometry with Copper Plates



A 5-layer model with copper plate, gravity along -z

Comparison with photos: DAQ

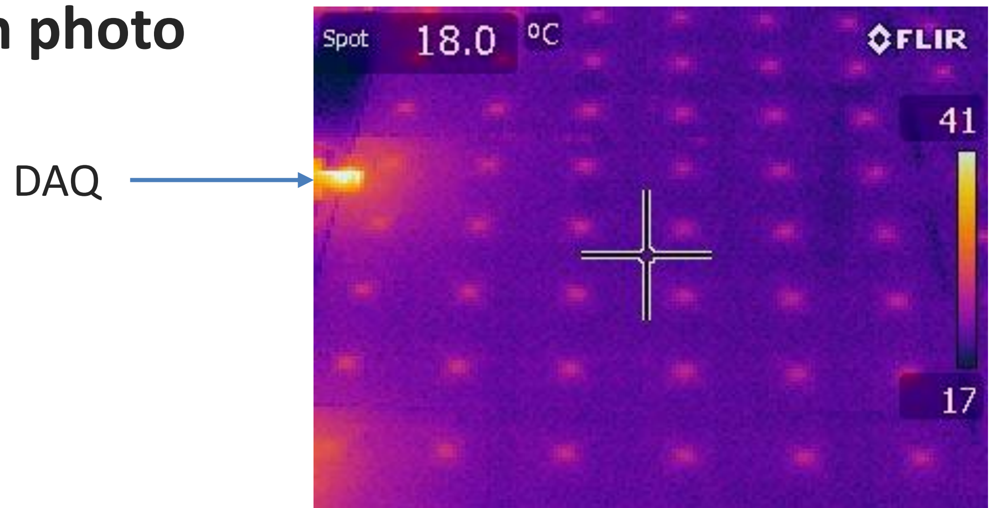
Icepak vs steady-state thermal

- higher resolution on chips

Icepak vs photo

- similar temperature difference between ambient and electronics
- both uniformed distribution on PCB
- a greater heat source in photo

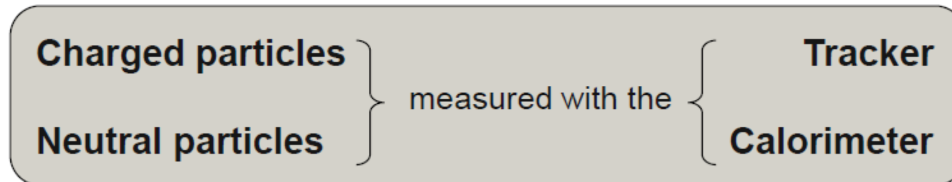
DAQ

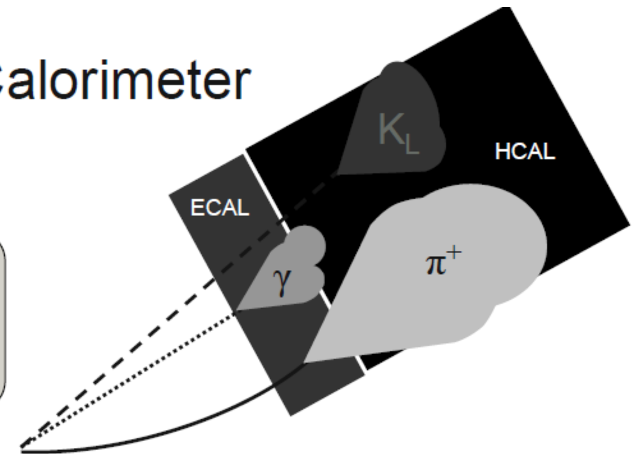


Particle Flow Algorithm

Particle Flow Algorithms and Imaging Calorimeter

The idea…





Particles in jets	Fraction of energy	Measured with	Resolution [σ^2]
Charged	65 %	Tracker	Negligible
Photons	25 %	ECAL with $15\%/\sqrt{E}$	$0.07^2\ E_{jet}$
Neutral Hadrons	10 %	ECAL + HCAL with $50\%/\sqrt{E}$	$0.16^2\ E_{jet}$
Confusion	Required for $30\%/\sqrt{E}$		$\leq 0.24^2\ E_{jet}$

Charged + Photons + Neutral Hadrons: $18\%/\sqrt{E}$

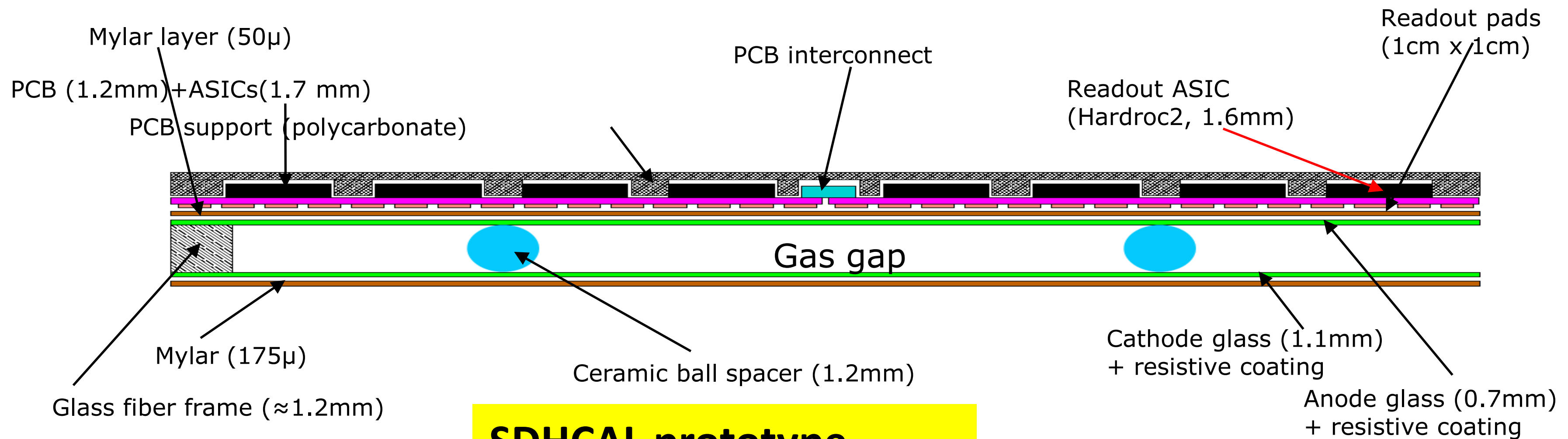
Requirements for detector system

- → Need excellent tracker and high B – field
- → Large R_I of calorimeter
- → Calorimeter inside coil
- → Calorimeter as dense as possible (short X_0, λ_I)

(Calorimeter inside coil; Calorimeter as dense as possible) → **thin active medium**

- → Calorimeter with **extremely fine segmentation**

SDHCAL based on RPC



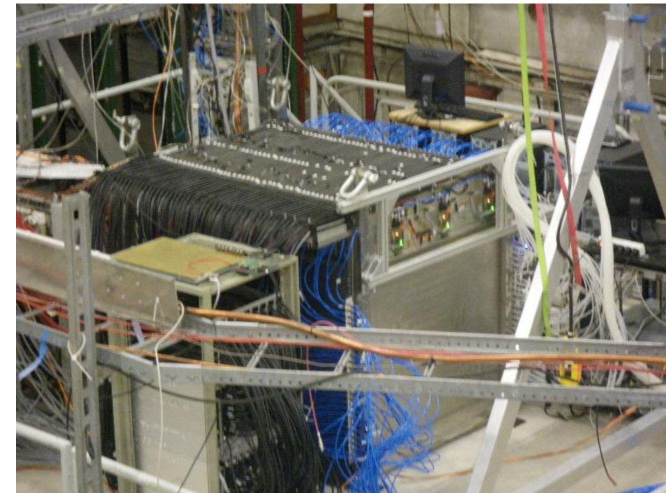
Large GRPC R&D

- ✓ Negligible dead zone
- ✓ Large size: 1 x 1 m^2

$(0.12\lambda_I, 1.14X_0)$

Stainless steel Absorber(15mm)
Stainless steel wall(2.5mm)
GRPC(6mm≈ $0\ \lambda_I, X_0$)
Stainless steel wall(2.5mm)

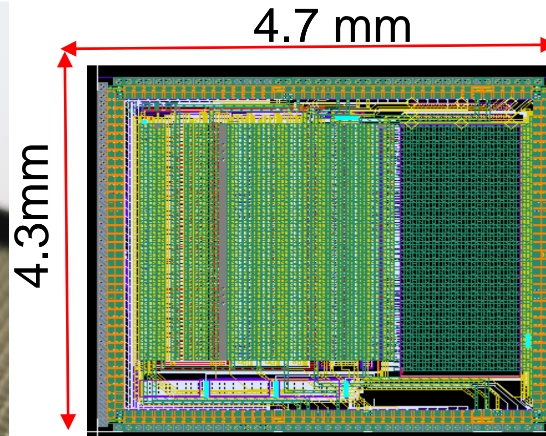
SDHCAL prototype
Size: 1m x 1m x 1.4m
No. of layers: 48
Cell size: 1cm x 1cm
No. of channels: 440K
Power: 1.4mW/ch

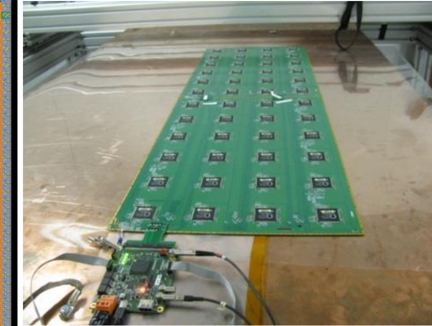


ASIC HARDROC (64 ch)
3-threshold: 110fC, 5pC, 15pC

Electronics Readout

ASICs : HARDROC2
64 channels
Trigger less mode
Memory depth : 127 events
3 thresholds
Range: 10 fC-15 pC
Gain correction → uniformity

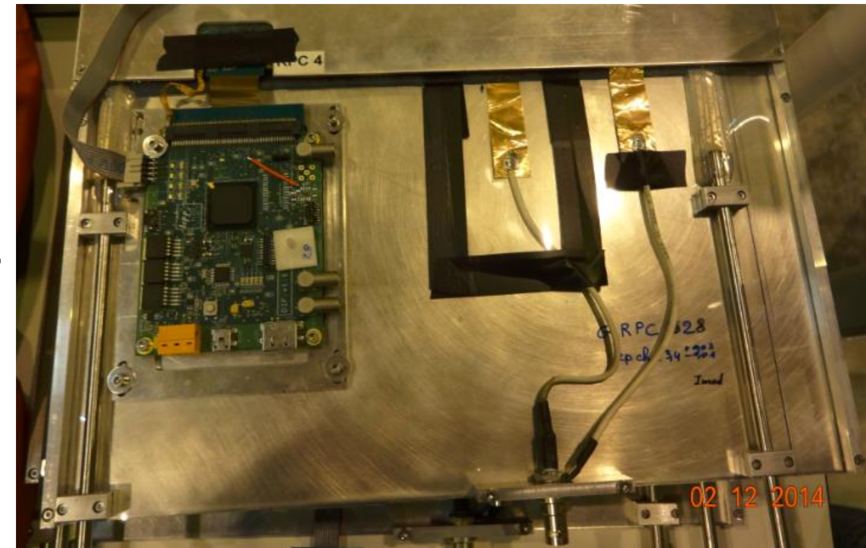




Printed Circuit Boards (PCB) were designed to reduce the cross-talk with 8-layer structure and buried vias.

Tiny connectors were used to connect the PCB two by two so the 24X2 ASICs are daisy-chained. 1×1m^2 has 6 PCBs and 9216 pads.

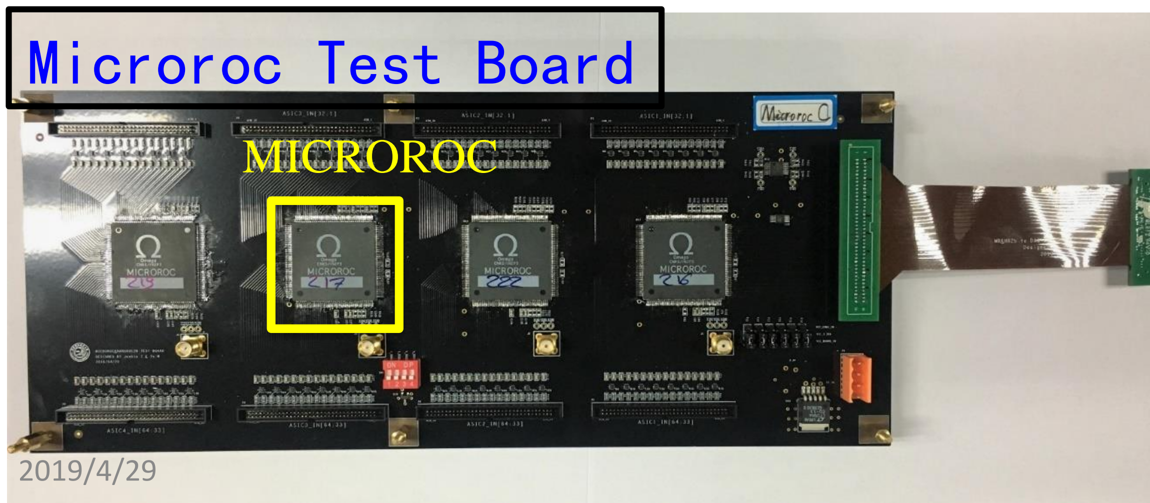
DAQ board (DIF) was developed to transmit fast commands and data to/from ASICs.



Readout ASIC

Readout ASIC	Channels	Dynamic Range	Threshold	Consumption
GASTONE	64	200fC	Single	2.4mW/ch
VFAT2	128	18.5fC	Single	1.5mW/ch
DIRAC	64	200fC for MPGD	Multiple	1mW/ch, 10μW/ch
DCAL	64	20fC~200fC	Single	——
HARDROC2	64	10fC~10pC	Multiple	1.42mW/ch,10μW/ch
MICROROC	64	1fC~500fC	Multiple	335μW/ch, 10μW/ch

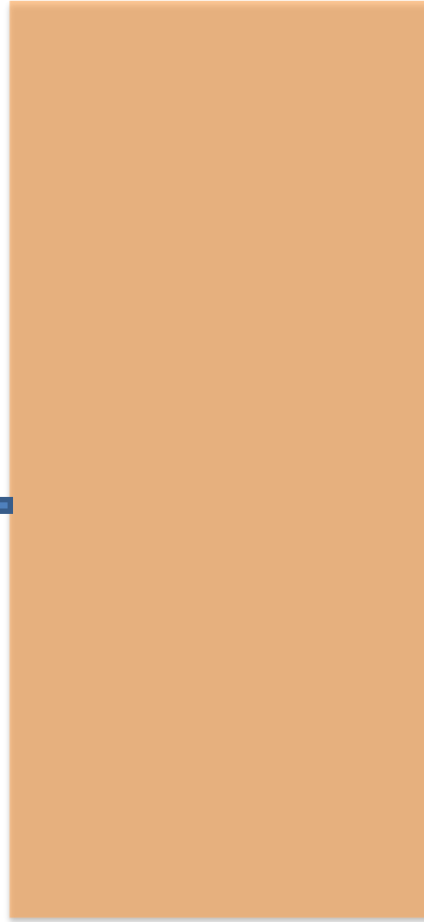
Considered the multi-thresholds readout, dynamic range and power consumption, MICROROC is an appropriate readout ASIC

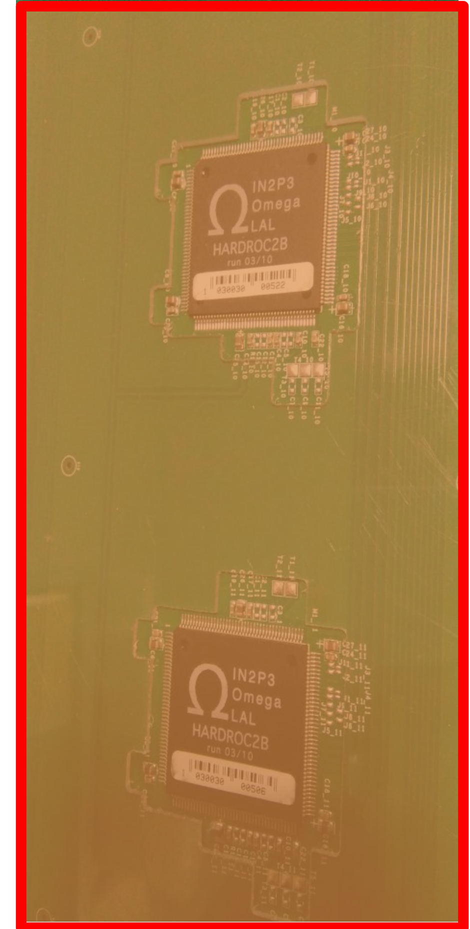


MICROROC Parameters

- Thickness: 1.4mm
- 64 Channels
- 3 threshold per channel
- 128 hit storage depth
- Minimum distinguishable charge:2fC

Active Cooling on RPC+PCB





RPC+PCB+ASIC
H ~ 6mm

Copper/Al sheet on top H ~ 1mm

Watering cooling along sides

PCB with ASICs

- ASIC chip (Hardroc) has 64 ch, 4.3mm*4.7mm, cover (2.8cm*2.8cm)

- Thick of stainless steel box is 2.5mm in each side, gap is 7mm (RPC+PCB+ASIC=6mm)

Choice of Material

Material	Thermal Conductivity [W / (m K)]	Price ($/lb)
Stainless Steel	16	1
Aluminum	205	1
Cooper	401	2.8
Silver	429	230
Water	0.606	-
Air	0.0262	-

Cooper or Aluminum has good thermal conductivity and reasonable price !