ARCADIA CMOS Monolithic sensors for frontier vertex and silicon detectors

CEPC Workshop IHEP 2019

The 2019 International Workshop on the High Energy Circular Electron-Positron Collider (CEPC)
IHEP, Beijing
Novembre 19th, 2019

Manuel Da Rocha Rolo
on behalf of the ARCADIA Collaboration

Outline

- Trends on Monolithic Active Pixel Sensors for HEP
- Boundary conditions on the use of DMAPS for future Leptonic Colliders
- ARCADIA: design and characterisation program for CMOS DMAPS

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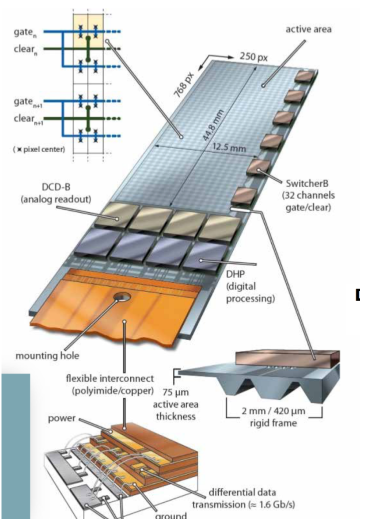
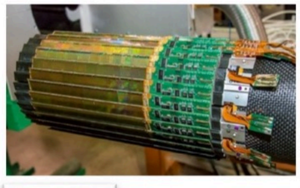
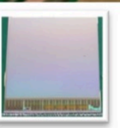
- *Trends on Monolithic Active Pixel Sensors for HEP*
- Boundary conditions on the use of DMAPS for future Leptonic Colliders
- ARCADIA: design and characterisation program for CMOS DMAPS

MAPS: The Evolution of the Species

Partially adapted from:
W. Snoeys, TWEPP2018

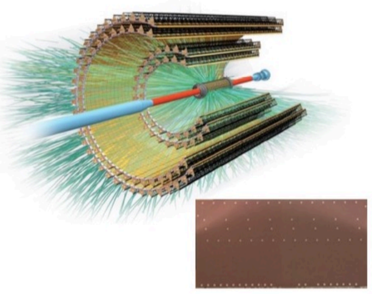




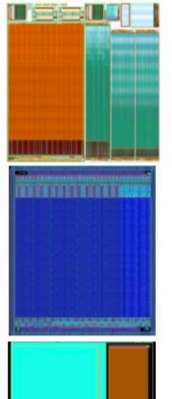


ULTIMATE in STAR
IPHC Strasbourg
First HEP MAPS system

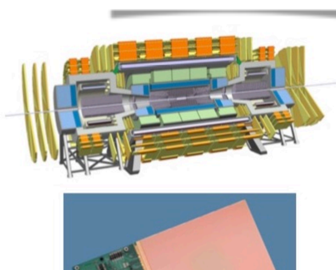
TJ-Monopix: 20 x 10 mm



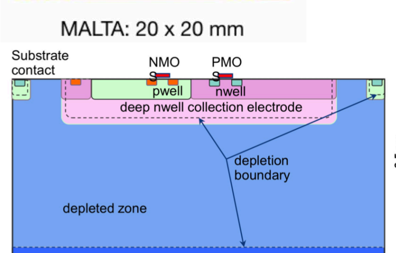
ALPIDE in ALICE
First MAPS with sparse readout similar to hybrid sensors
Chip-to-chip communication for data aggregation



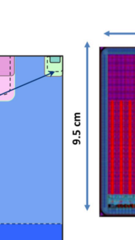
ATLAS CMOS
Depleted radiation hard MAPS with:
Sparse readout
Chip-to-chip communication
Serial power
...



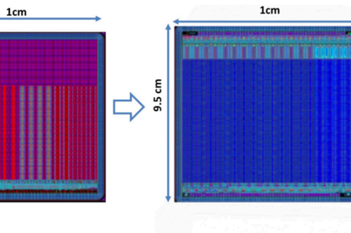
FCC, CLIC, ...
Large stitched fast radiation hard MAPS with:
Sparse readout
Chip-to-chip communication
Serial power



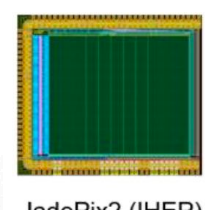
MALTA: 20 x 20 mm



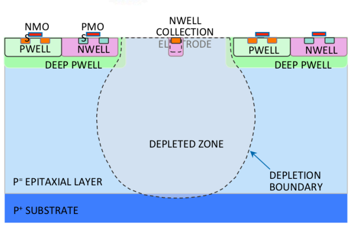
LF-CPIX (Demonstrator)



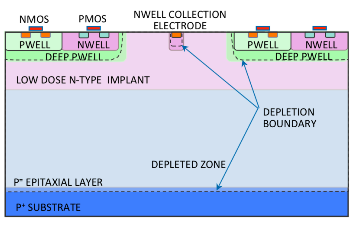
LF-Monopix (monolitic FE-I4)



JadePix2 (IHEP)
3 × 3.3 mm²

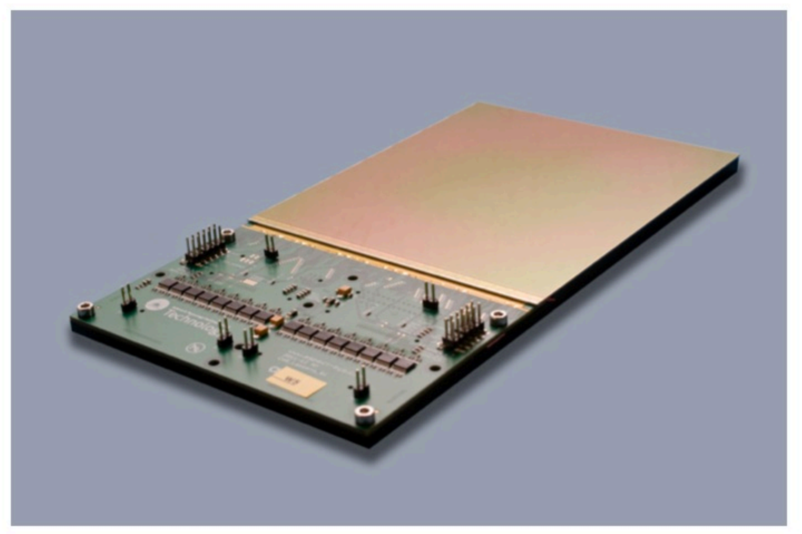


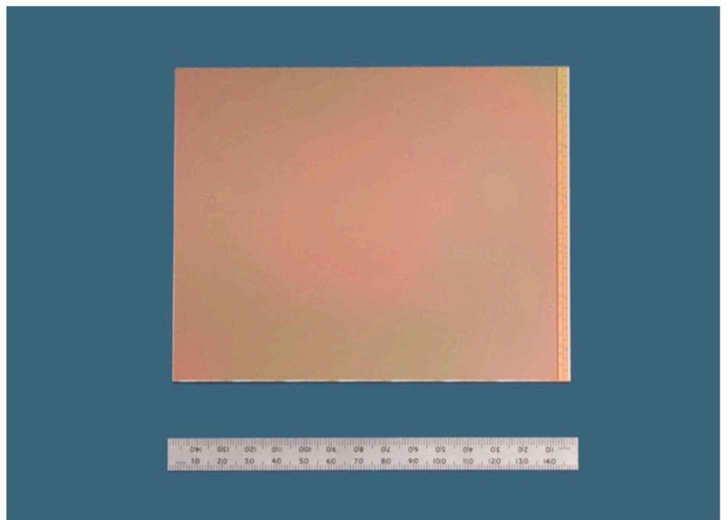
Standard: no full depletion



Modified: full depletion, better radiation tolerance

Trending up: Bigger, Stitched Silicon





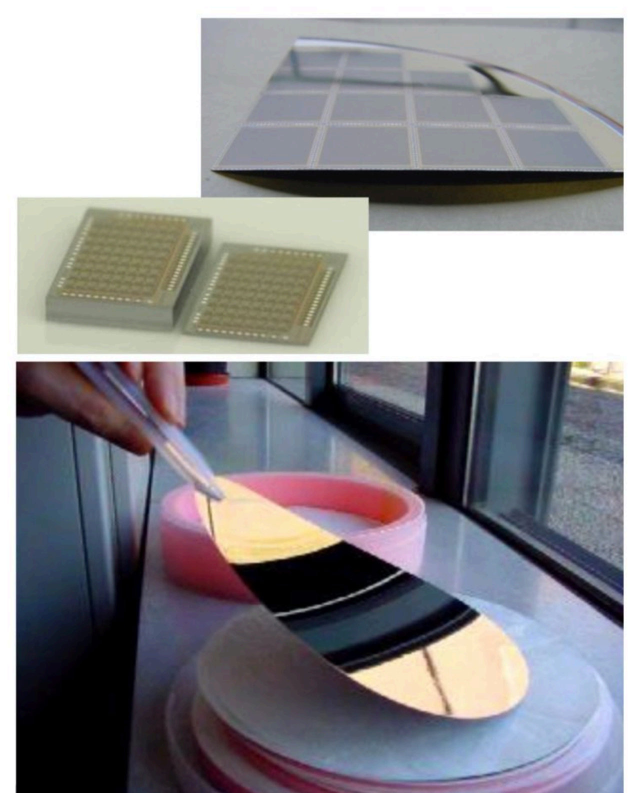
- Example of a wafer-scale imaging sensor chip for X-Ray applications developed at RAL (UK)
- 139.2 mm x 120 mm CIS, abutment 2x2 allows for a 278.4 mm x 240 mm active area!
- Towerjazz 180nm on 200 mm (8”) wafers, 1 sensor per wafer

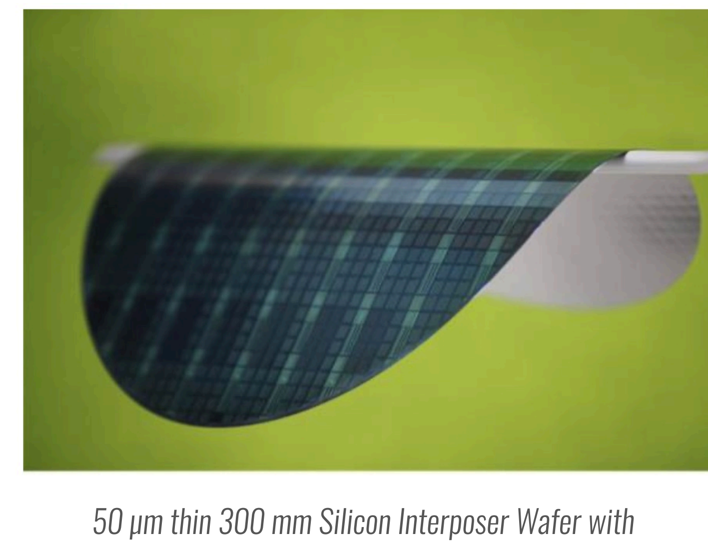
> *Paves the way for all-silicon CMOS active interposers*
> - ☑ *substrate handles signal, power and data interconnects*
>
> *particularly interesting assuming 12” wafers*

Trending up: Thinner Silicon

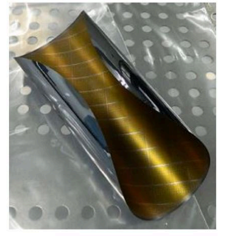
- Technology:
  - Course + fine grinding
  - Critical: thinning damage, impact on devices
- Wafer handling:
  - Very thin wafers (< 100 um): use of carrier wafers and temporary wafer (de-)bonding technology
- IMEC results:
  - Thinning down to 15 um
  - Total thickness variation ~ 2 um on 200 mm wafer

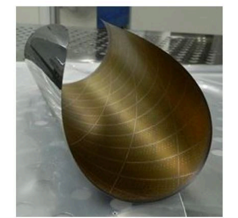
P. De Moor (IMEC)

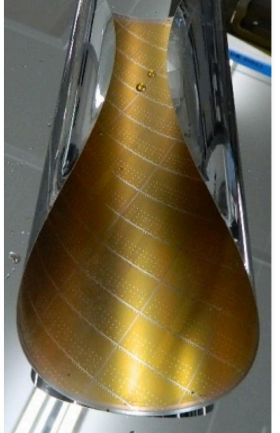




50 µm thin 300 mm Silicon Interposer Wafer with Cu-RDL metallisation. Source: Fraunhofer IZM







Magnus Mager, VERTEX2019

* ***Wafer-scale ultra-thin (< 20 µm) stitched MAPS could bend into a cylindrical** mechanically stable **self-supporting shape:***

☑ *purely Si based collider detector for tracking and PID with a VERTEX with an unprecedented low material budget of < 0.05 % X_0 per layer*

Depleted MAPS for Future Detectors

	RHIC STAR	LHC - ALICE ITS	CLIC	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp
NIEL [n_{eq}/cm^2]	10^{12}	10^{13}	$<10^{12}$	10^{15}	10^{16}	10^{15}-10^{17}
TID	0.2Mrad	<3Mrad	<1Mrad	80 Mrad	2x500Mrad	>1Grad
Hit rate [MHz/cm²]	0.4	10	<0.3	100-200	2000	200-20000

Heinz Pernegger, Vertex 2018

- **Hit rate and radiation hardness for Frontier Detectors could require improvements of ~2 orders of magnitude in respect to the state-of-the-art technology**

* **Charge collection by drift: faster signals, better radiation hardness**
* **New architectures for higher event rate capability**
* **Advanced integration and interconnect technology for large sensor area**

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Setting the stage… for leptonic colliders

The exploitation of the physics reach at the next generation **electron-positron colliders** requires outstanding flavour tagging performance with a precise determination of the track parameters of charged particles very close to the IP ⇢ reconstruction of the displaced decay vertices of short-lived particles.

Impact on the vertex detector characteristics:

- **state-of-the-art granularity for resolutions at the few micron level shall be guaranteed while preserving a high event rate capability;**
- **minimum multiple scattering at the innermost radius calls for a material budget at the level of 0.15% X0 per layer;**
- **"compact" detectors requires advanced integration and packaging technologies, innovative cooling and assembly solutions.**

Requirements for the CEPC Vertex

intrinsic single-point resolution of the vertex detector in the absence of multiple scattering (depends on the geometry and number of layers)

effects of Coulomb multiple scattering, depends on the material budget of the beam pipe and inner-most detector

impact parameter resolution →

$$\sigma_{r\phi} = a \oplus \frac{b}{p(\,\mathrm{GeV})\sin^{3/2}\theta}$$

track momentum

polar track angle

Accelerator	a [μm]	b [μm · GeV/c]
LEP	25	70
SLC	8	33
LHC	12	70
RHIC-II	13	19
ILC	<5	<10
CEPC	**5**	**10**

- **3 concentric cylinders of double-layer pixelated vertex detector with:**
  - Single-point resolution of the first layer better than 3 μm;
  - Material budget below 0.15% X_0 per layer;
  - Innermost tracker radius of 16 mm (material budget of 0.15% X_0 for the beam pipe);
  - Detector occupancy below 1%

CEPC CDR IHEP-CEPC-DR-2018-02

Boundary Conditions for a CMOS APS VTX

- excellent impact parameter resolution O(3-5 μm) ⇢ pixel pitch below 25 μm
- very low material budget O(0.15% X_0 per layer) ⇢ thin sensors, low power
  - *CepC has a bunch spacing of 0.68 μs for the Higgs factory operation, 25 ns for the Z factory operation ⇢ no power pulsing possible ("a la ILC")*
  - *the power consumption of the sensors and readout electronics should be kept below 20 mW/cm^2, if the detector is to be air cooled (otherwise use silicon micro-channels)*
- lightweight but robust support structure and related mechanics
  - *low material budget detector modules need to integrate mechanical support, power and signal connections, and have sufficient stiffness to avoid vibration.*
- low to moderate requirements for radiation tolerance
- moderate rate capability

Manuel Da Rocha Rolo (INFN) — *darochar@to.infn.it*

Extrapolation to an Outer Silicon Tracker

- the requirements for the single point resolution are a function of the position of the tracker components, but necessarily more relaxed than for a vertex detector;
  - *pitch below 50 µm*
  - *silicon thickness below 200 µm, needs to minimise multiple scattering*
- considering material budget and power density, silicon strips are the natural candidate, but… a fully-pixelated CMOS silicon tracker would allow for:
  - better single point resolution
  - potentially lower material budget (CMOS wafer thinning down to 50 µm is relatively standard), lower cost and high throughput from a production of the APS silicon in a standard CMOS foundry
- **Practical implementation:**
  - *CMOS passive strip sensors (volume, low-cost)*
  - *larger, or longer, APS pixels with ADC, zero suppression, time stamp, or*
  - *binary readout with DSP and clustering on-chip (periphery)*

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ARCADIA (INFN CSNV Call Project)

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Towards a CMOS sensor design and fabrication platform allowing for:

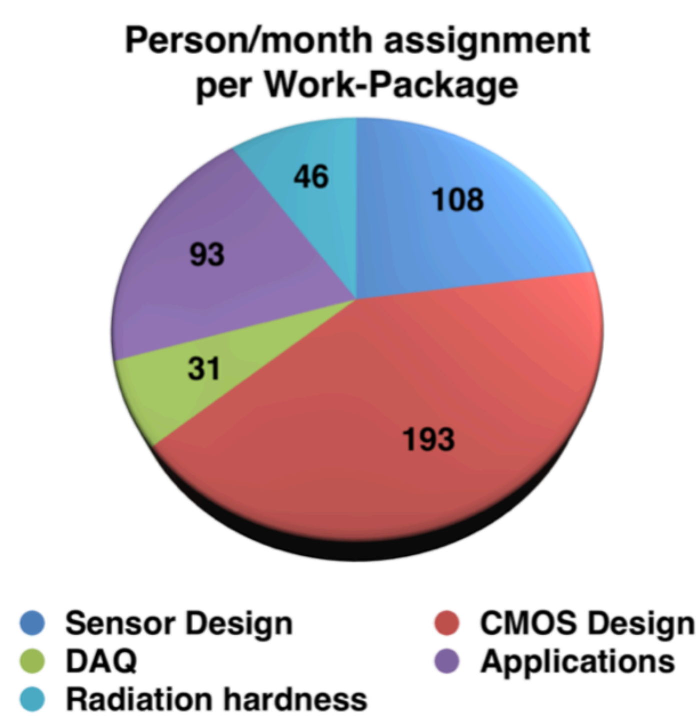
- Active sensor thickness in the range 50 µm to 500 µm or more;
- Operation in full depletion with fast charge collection only by drift;
- Small charge collecting electrode for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability (O(10 mW/cm2));
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Use of a deep sub-micron 110nm CMOS node for higher gate density

ARCADIA (INFN CSNV Call Project)

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

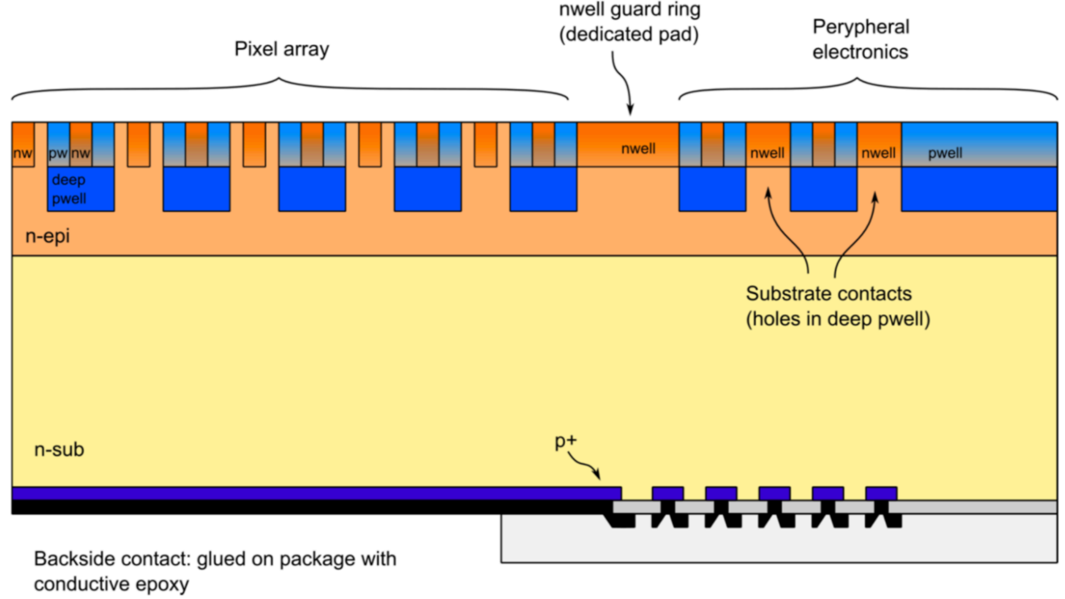
INFN - Bologna, Milano, Padova, Perugia, Pavia, TIFPA, Torino

F Alfonsi, G Ambrosi, A Andreazza, S Beolè, M Caccia, A Candelori, D Chiappara, T Croci, M Da Rocha Rolo, G-F Dalla Betta, A De Angelis, G Dellacasa, N Demaria, B Di Ruzza, A Di Salvo, D Falchieri, M Favaro, A Gabrielli, L Gaioni, S Garbolino, R A Giampaolo, N Giangiacomi, P Giubilato, R Iuppa, M Mandurrino, M Manghisoni, S Mattiazzo, F Nozzoli, J Olave, L Pancheri, D Passeri, A Paternò, M Pezzoli, P Placidi, L Ratti, E Ricci, S B Ricciarini, A Rivetti, H Roghieh, R Santoro, A Scorzoni, L Servoli, F Tosello, G Traversi, C Vacchi, R Wheadon, J Wyss, M Zarghami, P Zuccon



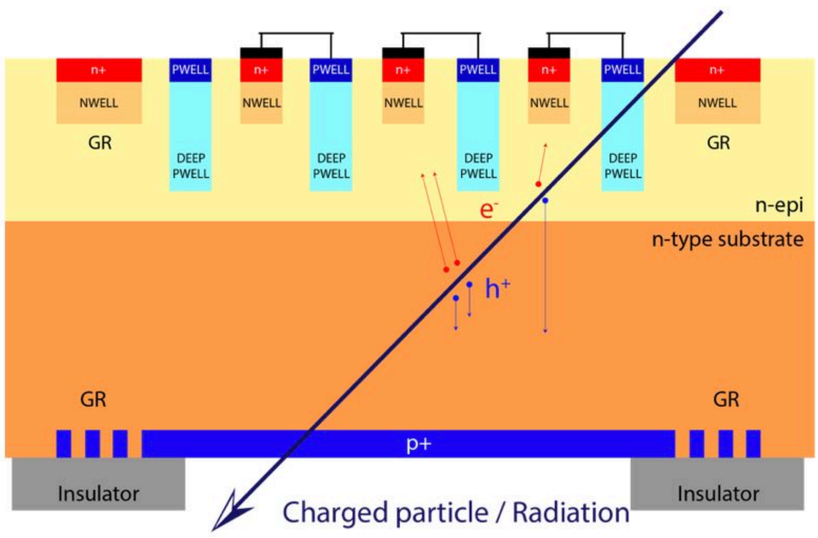
- 3-year >1M€ R&D project 2019-2021
- Sensor&CMOS design, DAQ, System characterisation (medical, future colliders, space)

ARCADIA - Proposed Sensor

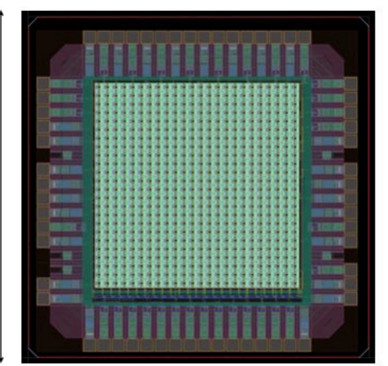


- Technology: 110 nm CMOS CIS technology (quad-well, both PMOS and NMOS), high-resistivity bulk
- SEED : Sensor with Embedded Electronics Development (INFN CSNV Project)
- Backside: diode surrounded by a guard-ring
- Custom patterned backside, process developed in collaboration with LFoundry
- Pixel size 25 µm x 25 µm: process, back-side pattern and geometry validated in silicon (both MATISSE and pseudo-matrices, electrical, laser, radioactive source and microbeam)

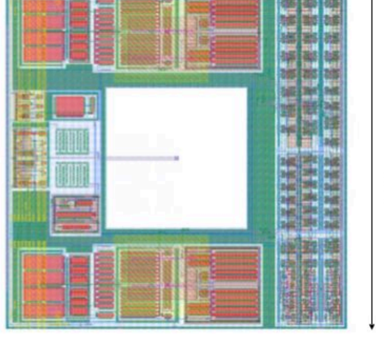
Small-scale demo: MATISSE



PIXEL ELECTRONICS		
	DESIGN SPECs	RESULTS
Technology	CMOS 110 nm	
Voltage Supply	1.2 V	
Measurements	Hit Position Energy Loss	
Number of Channels	24 × 24	
Input Dynamic Range	Up to 24 ke-	
Sensor Capacitance	~20 fF	
Analog Gain	131 mV/fC	116 mV/fC
CSA Input Common Mode Voltage	> 600 mV	
Local Memories	2 (~70 fF each)	
Noise	< 100 e-	~40 e-
Shutter Type	Snapshot	
Readout Type	Correlated Double Sampling Double Sampling	
Readout Speed	Up to 5 MHz	
Other Features	Internat test pulse Mask Mode Baseline Regulation	



MATISSE



Pixel CAD Layout

Small-scale demo: MATISSE

Charge Sensitive Amplifier
With a RESET transistor

Correlated Double Sampling

Sensor

I_d C_d

C_f

RESET

CSA

Test Pulse

In-pixel digital logic

Read Out

$S1_{out}$

$S2_{out}$

C1

C2

B1

B2

Baseline

Signal

Next Pixel

Previous Pixel

PIXEL MATRIX 24 x 24

SECTOR 1

SECTOR 2

SECTOR 3

SECTOR 4

6 x 24

6 x 24

6 x 24

6 x 24

EoC

24

23

22

3

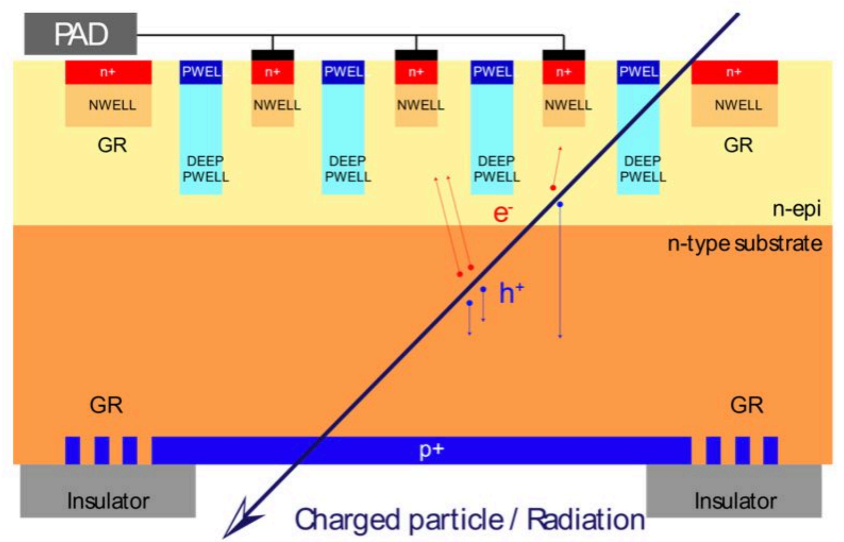
2

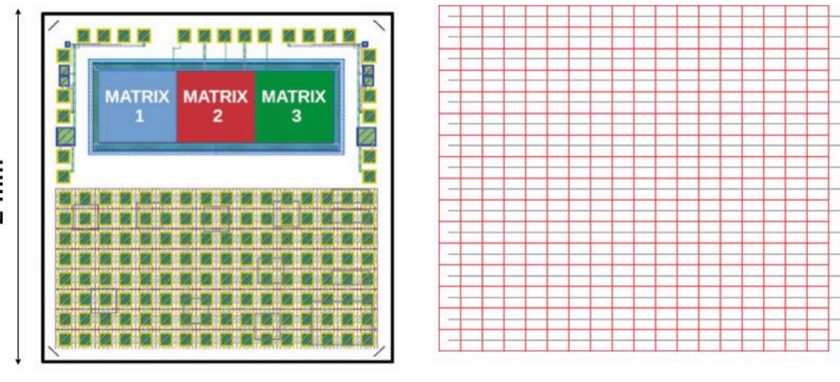
1

BASELINE

SIGNAL

Small-scale demo: pseudo-matrices





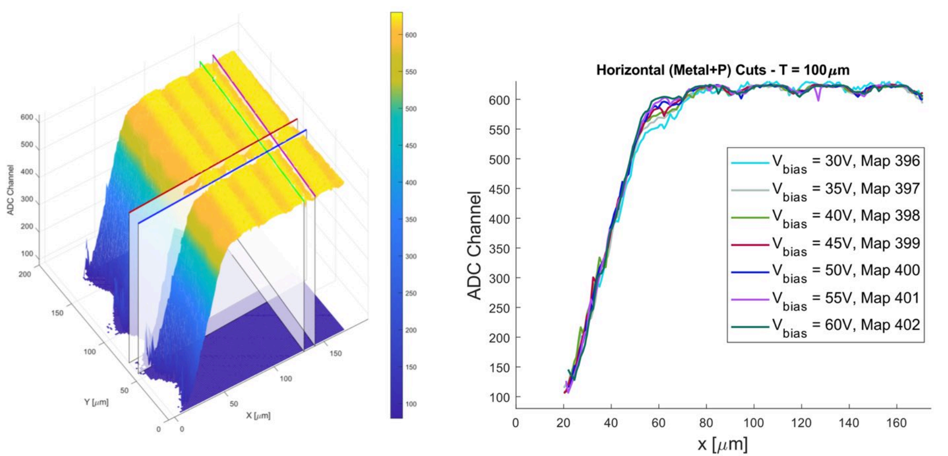
Pseudo-matrix Layout

Pixel Scheme

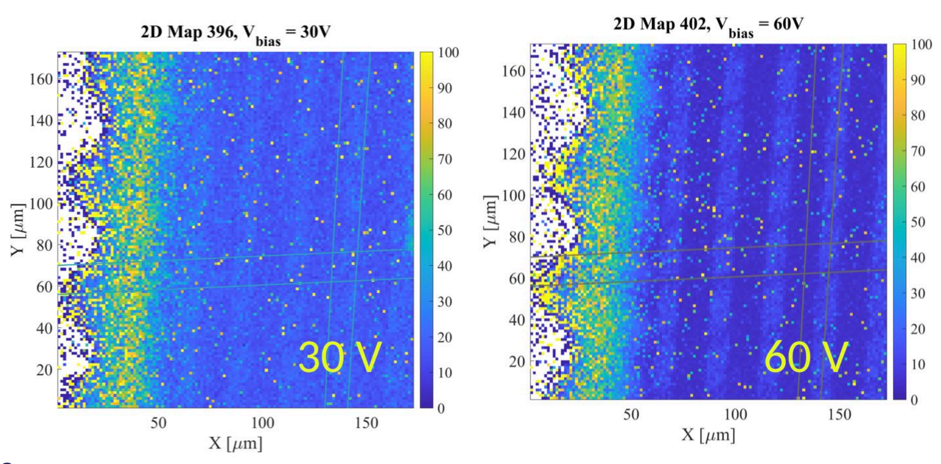
- Sensor thicknesses: 100 µm, 300 µm, 400 µm
- Three matrices with different pixel sizes: 10 µm (40 x 45), 25 µm (16 x 18) and 50 µm (8 x 9)
- Front-side deep-pwell, would host the CMOS electronics (no electronics on PMs)
- All the collector nodes of a matrix are shorted and connected to a PAD
- Each pixel is shorted using Al metal lines of increasing width per PM: 6, 8 and 15 µm

Results in a nutshell: pseudo-matrices

Cuts along the Metal + P and Metal + N lines on the energy map with varying bias voltages show uniform CCE above FD with ~1.7 % loss over metals (100 µm thick)

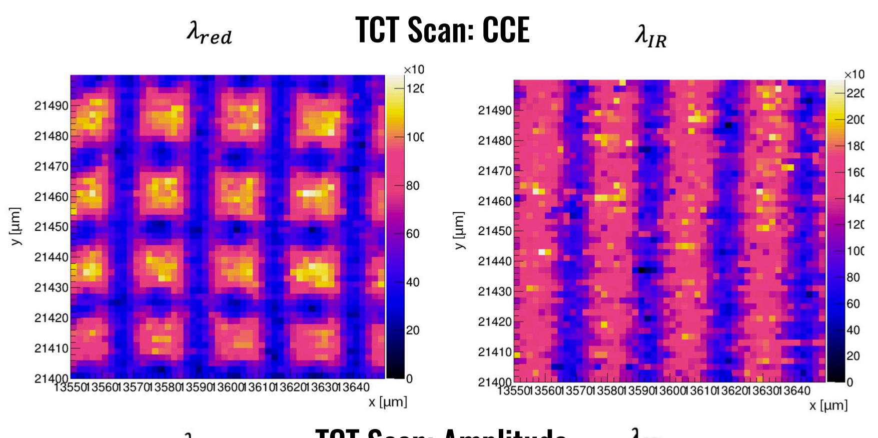


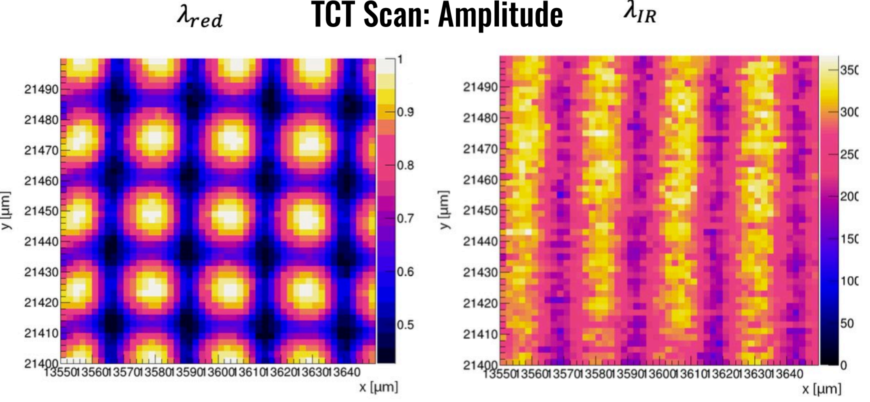
Standard deviation maps show the expected higher electronic noise when the sensor is not depleted (below 30 V), due to the higher top capacitance.



(RUĐER BOŠKOVIĆ INSTITUTE)* Zagreb, Croatia

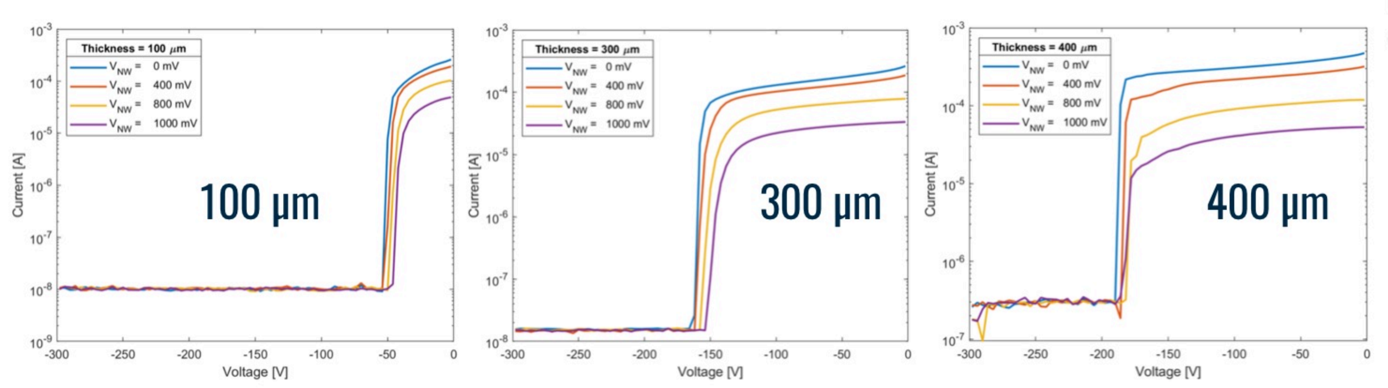
- 600 keV to 2 MeV Tandetron
- TANDEM 1-6 MeV proton source
- LASER TCT laboratory



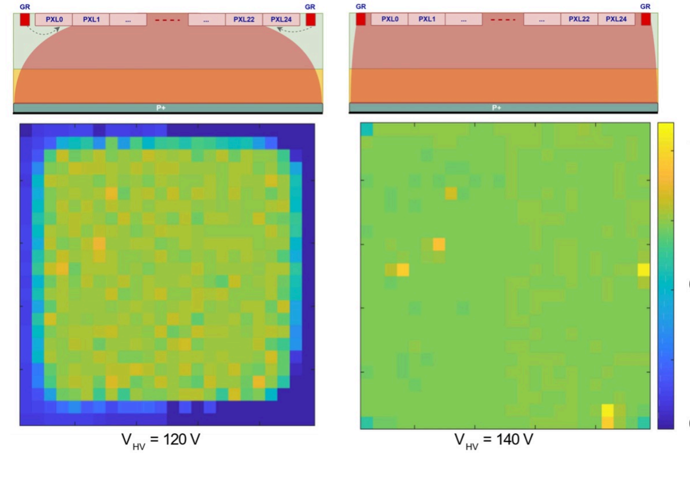


Results in a nutshell: MATISSE

Full depletion studies in 100-300-400 µm prototypes

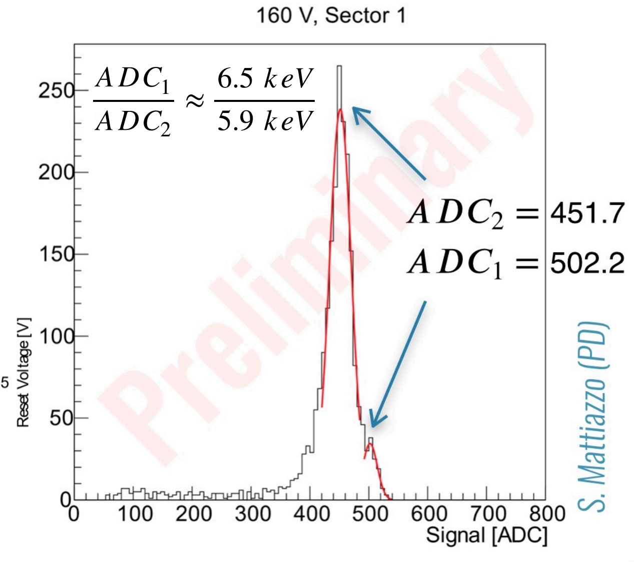


Map of pixel reset voltage (MATISSE 24x24 pixel matrix) as a function of the back-side voltage applied to the sensor. Depletion starts from the back-side.



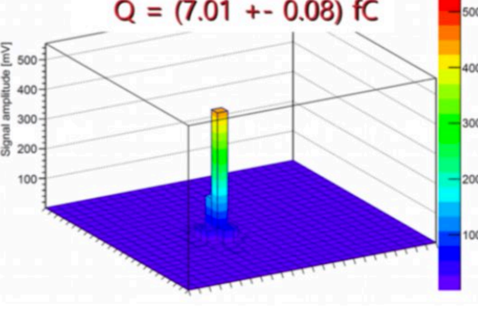
L. Pancheri (TN)

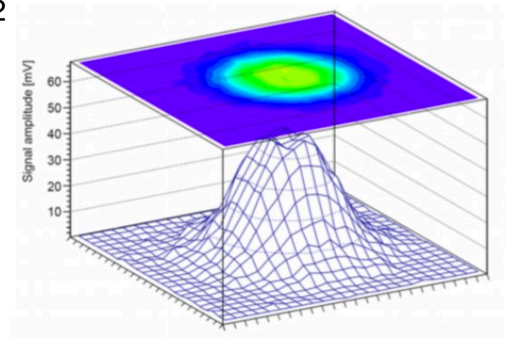
Preliminary results with ^{55}Fe



S. Mattiazzo (PD)

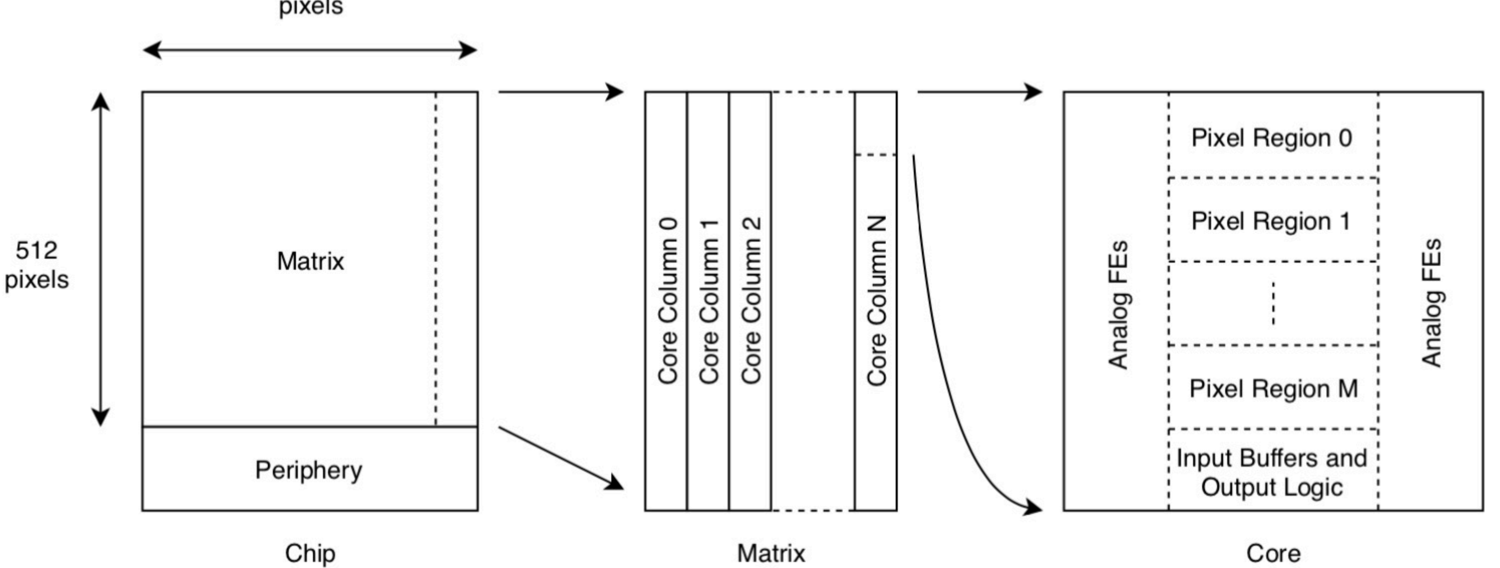
The ^{55}Fe emits monochromatic X-rays at 5.9 keV (K_α). A K_β line at 6.5 keV is also emitted with a relative probability below 5%.





J. Olave FEE2018

ARCADIA - Demonstrator Chip Design



- Pixel size 25 µm x 25 µm: process, back-side pattern and geometry validated in silicon (both MATISSE and pseudo-matrices, electrical, laser, radioactive source and microbeam)
- Matrix core 512 x 512, “side-abuttable” to accomodate a 1024 x 512 silicon active area (2.56 x 1.28 cm^2). Matrix and EoC architecture, data links and payload ID: scalable to 2048 x 2048[(1)]
- Triggerless binary data readout, event rate up to 10 MHz/cm^2
- “Strip-like” data-compressed column configuration

[(1)] 1D and 2D stitching available at LFoundry

ARCADIA: ongoing activities

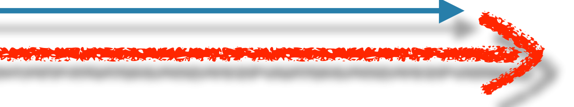
01/2019 — 01/2022

* TCAD 2D/3D sensor simulation: geometry, p-well spacing, node capacitance, transient
* CMOS Analogue IP block design: continuous and discrete-time VFE design; 12-bit SAR ADC IP-core, custom LVDS Tx/Rx: LF11is prototyping run September 2019
* CMOS Digital IP block design and Chip Integration:
  - SPI and Serialiser (8b/10b) soft-IP Cores 110nm ready
  - PnR of full double-column, full-matrix integration ongoing
* Data acquisition: started development of DAQ for the full-chip
* Characterisation: laser and microbeam tests with 100-300 µm pseudo-matrices @RBI (Zagreb), tests with Fe^{55}, new laser test setup (spot size 8 µm) under construction

1st engineering run (dedicated front/back-side maskset): mid-2020

Future Roadmap and Perspective

01/2019 01/2022



- ARCADIA will build a design, characterisation and production framework for fully-depleted MAPS in a CMOS commercial foundry
- design of 2D-stitched wafer-scale demonstrators, scalable DAQs, mechanics and cooling for large systems, flexible ultra-thinned silicon handling and assembling, integration of system-grade design:
  - EoI for AIDA++: INFN (IT), PSI+ETH+UZH (CH), Uni. Oxford (UK), IHEP (CN)
- Future collaborations, funding and resources will allow for the development of application-specific wafer-scale sensors for frontier detectors, medical, space and industrial applications

ARCADIA CMOS Monolithic sensors for frontier vertex and silicon detectors

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Thank You for your time !

Cost of a CMOS MAPS-based Silicon Tracker

stitched lithography needed in manufacturing process

cost threshold

die per wafer
yield
@ 3000$/wafer
@ 2000$/wafer
@ 1000$/wafer

die per wafer or yield [%]
0 10 20 30 40 50 60 70 80 90 100

cost per square meter [$]
10,000 100,000 1,000,000 10,000,000

Chip Edge Dimension [mm]
20 30 40 50 60 70 80 90 100 110 120 130 140

Stefan Lauxtermann (Sensor Creations) PIXEL2018

Cost of $100,000/m² tracking area is achievable with the following assumptions

- **> 75% Yield**
- **No stitching**
- **Wafer cost <$2,000 (only achievable using high volume CMOS manufacturing)**