LHCb VELO Readout

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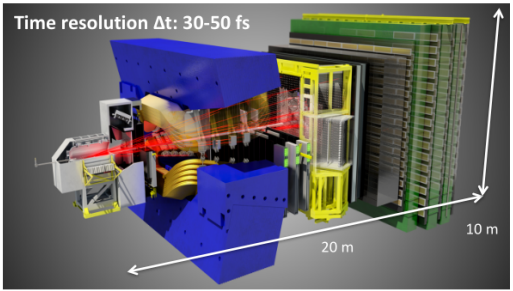
on behalf of LHCb

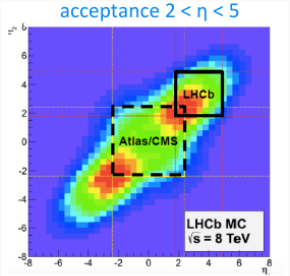
November 18, 2019

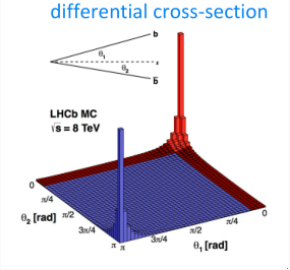
University of Liverpool

LHCb

Covering about 4% of the solid angle in the forward region, the detector captures 40% of the beauty cross-section





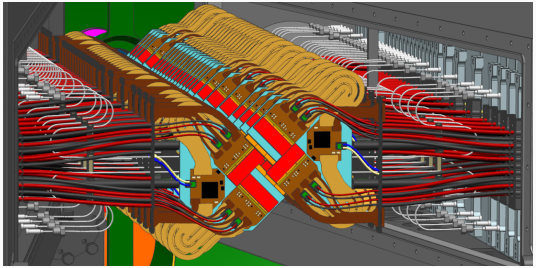


- Beam crossing rate 40 MHz
- 10^5 beauty pairs per second
- Selection of interesting events is mandatory

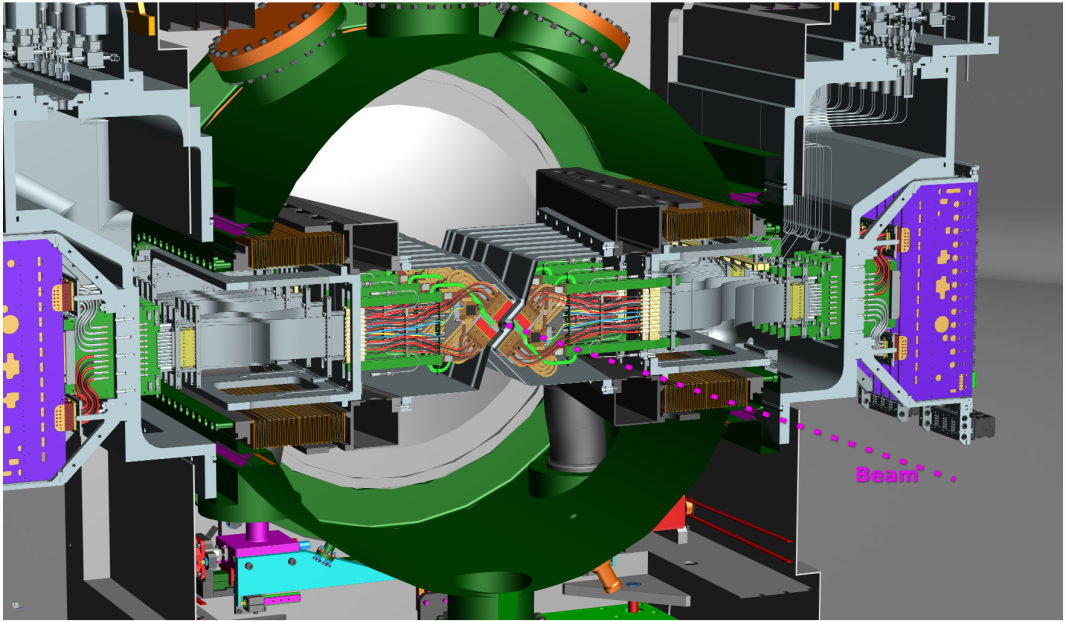
VELO

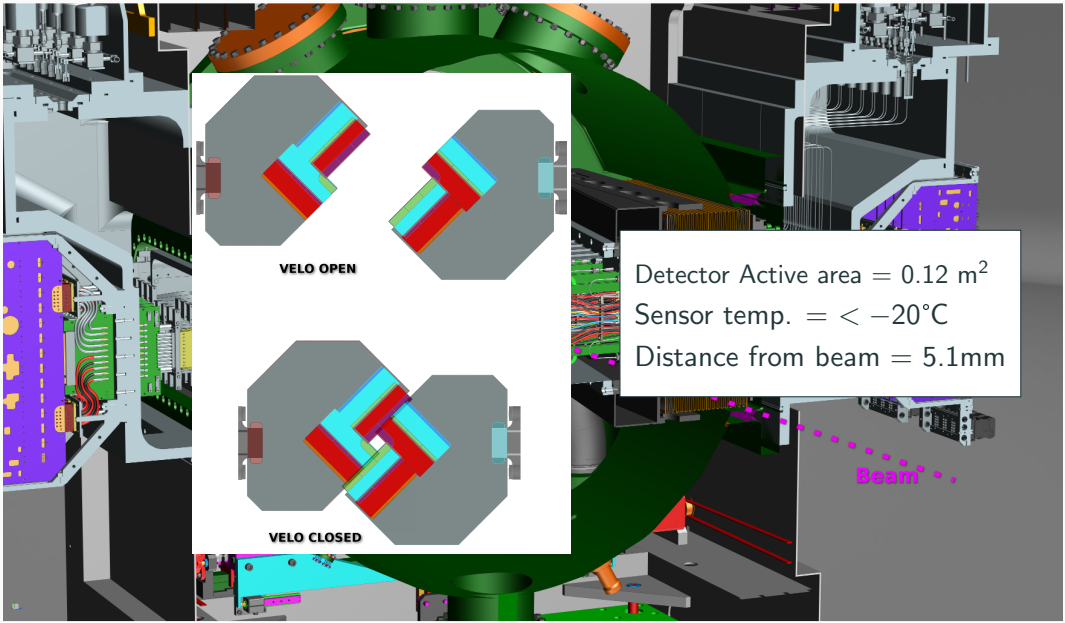
- Vertex Locator (VELO) for the upgraded LHCb detector
- Silicon pixel modules around the LHC beam interaction region
  - 50fb^{-1} integrated luminosity for LHC Runs 3 & 4
  - Very high radiation environment
  - maximum fluence approx. 8×10^{15} $\mathrm{MeV}\cdot\mathrm{n_{eq}}/\mathrm{cm}^2$
  - In vacuum and under active cooling

- LHCb has triggerless readout - full detector readout @ 40 MHz



LHCb Vertex Locator


Beam

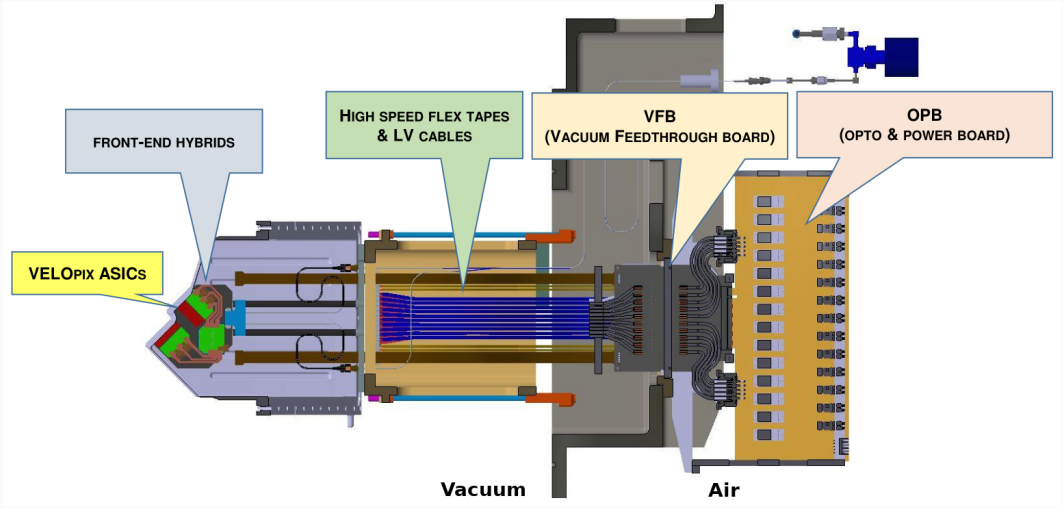


Detector Active area $= 0.12$ m^2

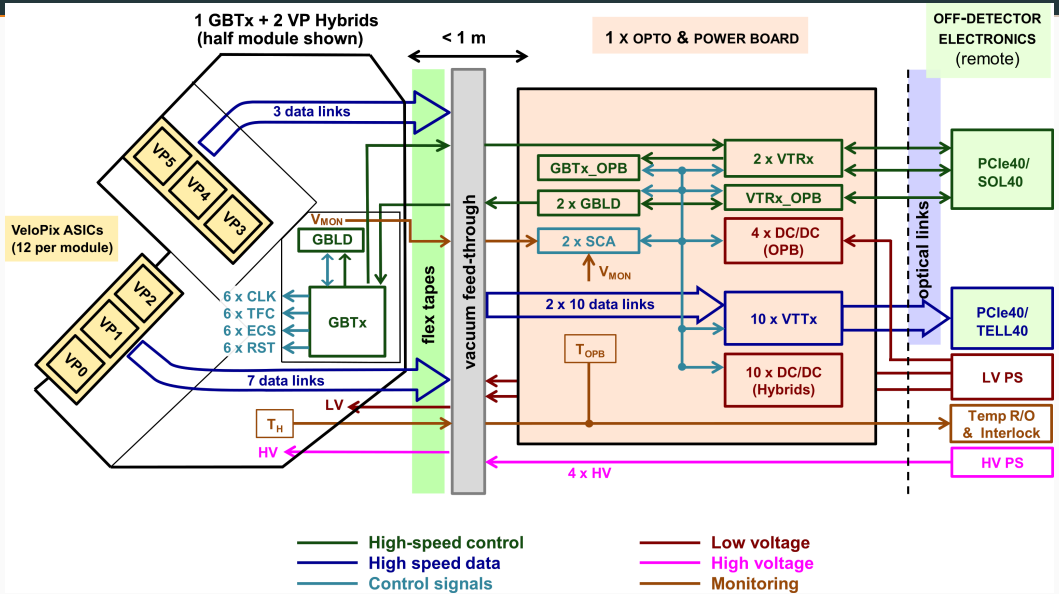
Sensor temp. $= < -20$°C

Distance from beam $= 5.1$mm

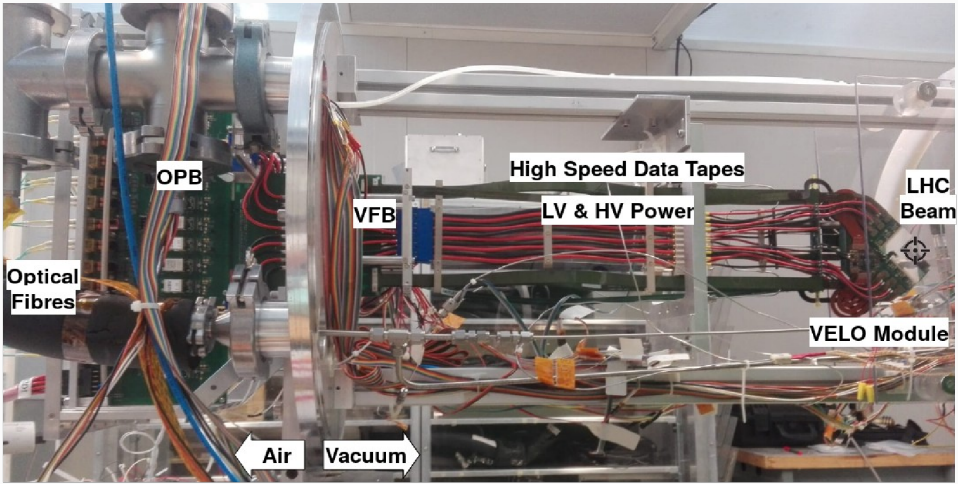
VELO CAD


FRONT-END HYBRIDS
HIGH SPEED FLEX TAPES & LV CABLES
VFB (VACUUM FEEDTHROUGH BOARD)
OPB (OPTO & POWER BOARD)
VELOPIX ASICS
Vacuum
Air

VELO Electronics



VELO Electronics Lab



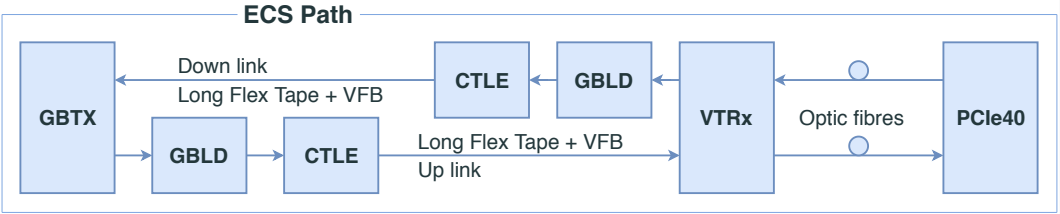
VELO in Numbers

Feature	
Sensors	Pixels
# of modules	**52**
Detector Active area	0.12 m^2
	$\sim$41 M pixels
Technology	electron collecting
	200 μm thick
Max fluence	8×10^{15} $\mathrm{MeVn_{eq}/cm^{-2}}$
HV tolerance	1000 V
ASIC Readout rate	**40 MHz**
Total data rate	**2+ Tb/s**
Total Power consumption	2.2-2.3 kW

High Speed Pathways

ECS - Experiment Control System

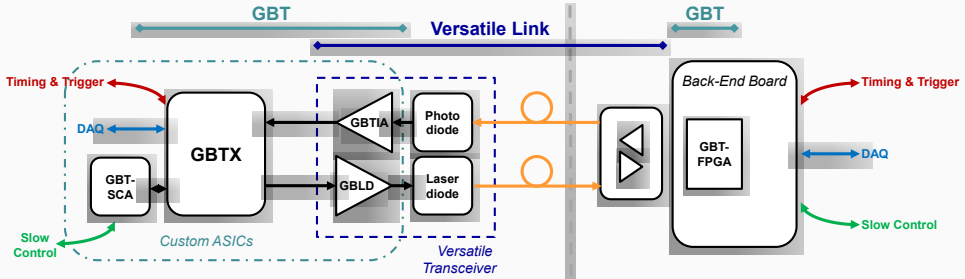
- Bi-directional with **GBTx** ASIC
- 4.8 Gb/s
- Use of GBLD as electrical line driver (emphasis and amplification functionality)



CTLE - Continuous Time Linear Equaliser

GBT - ECS interface

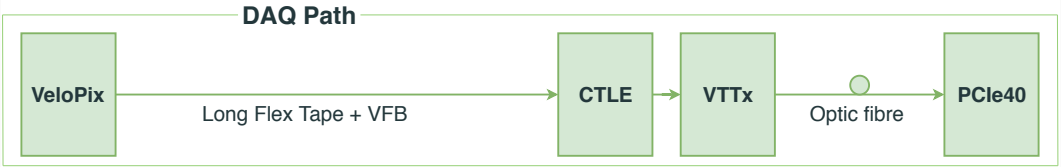
- The **GBTX** chip is a radiation tolerant chip for LHC experiments
- GBT Protocol can utilise three logical data paths
  - Trigger and Timing Control (TTC)
  - Slow Control (SC) - via companion SCA chip
  - Data Acquisition (DAQ) - *(NOT used for VELO)*
- All three logical paths can be encapsulated on a single physical interface



High Speed Pathways

DAQ - Data Acquisition

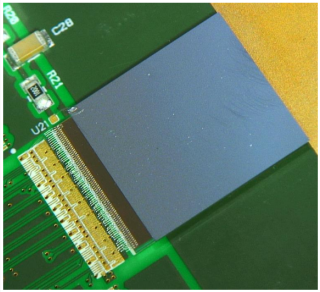
- Uni-directional (from **VeloPix** to back-end)
- 5.12 Gb/s
- VeloPix has some internal emphasis

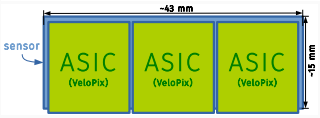


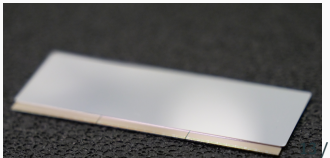
Similar electrical transmission lines for ECS and DAQ - expect similar performance.

VeloPix ASIC

- Front-end ASIC driving the design of the VELO data acquisition system
- Operates at LHC clock rate $\sim$ 40MHz
- Designed for high radiation tolerance and low power consumption
- Custom output serialiser - Gigabit Wireline Transmitter (GWT)
- Slow control via SLVS protocol
- 12 VeloPix chips per module
- 20 readout links (more links for hotter chips)





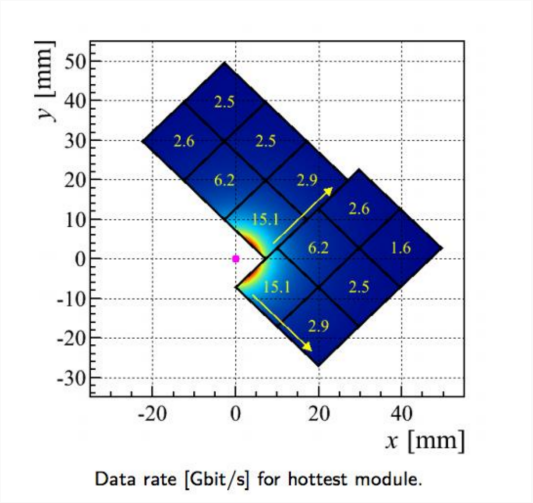


VeloPix ASIC

- Readout is data driven - *only* read out when they have "hits above threshold" (a.k.a. zero-suppression)
- **Binary readout** @ 40 MHz
- VeloPix is optimised for high speed readout

Peak hit rate	900 Mhits/s/ASIC
Max data rate	19.2 Gb/s
Total VELO	2.85 Tb/s

- Power consumption < 1.5 W$\cdot cm^{-2}$
- Radiation hard 400 Mrad, and SEU tolerant
- Non-uniform radiation dose

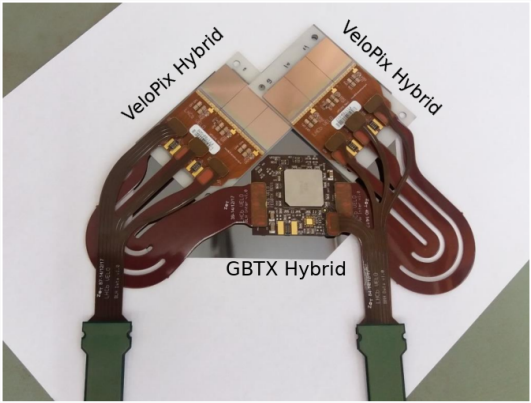


Average data rate

Hybrids

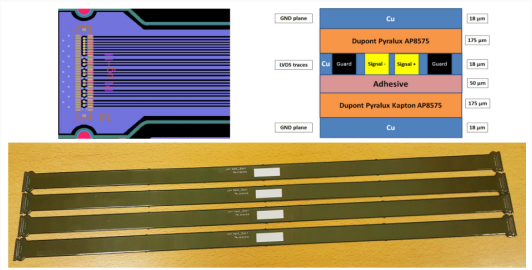
- VeloPix Hybrids
  - 20 high-speed data links @ 5 Gb/s
  - 4 hybrids per module (2 per side)
- GBTx Hybrid
  - Timing and control signals
  - GBLD as a line driver

GBT - http://cern.ch/go/6rsK

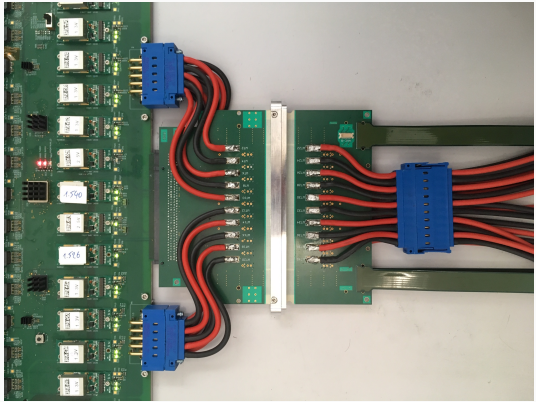


Hybrid, Cables, Feedthough

- High speed flex tapes
  - Stripline tech. 200 µmtrack & gap, 175 µmPyralux
  - length 550, 561, 575 mm



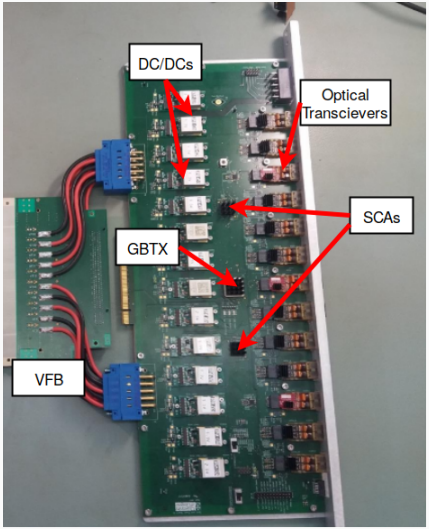
- Vacuum Feedthrough board
  - bringing all LV, HV, data, control signals to/from modules in vacuum



Opto-Power Board

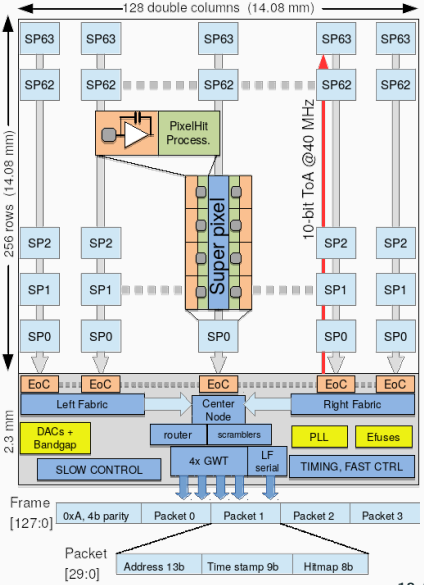
- Situated on VELO tank exterior
  - Connects to Vacuum Feedthrough Board
  - Fibres to counting room at surface ($\sim 300\,\mathrm{m}$)
- Interface for data, control, monitoring signals and powering for VELO modules
  - FeastMP DC/DCs for power
  - Voltage monitoring
  - Optical transceivers (VTTx/VTRx) for driving to/from backend
- Control via GBTx and SCA

GBT-SCA - http://cern.ch/go/Zcc9



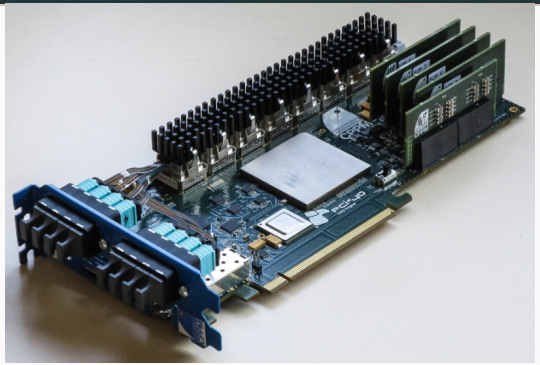
VeloPix Data readout

- Pixel data is aggregated into groups of 2×4 called **SuperPixels**
  - 30% reduction in data size
- Data is sent out-of-time ⇒ timestamp stored in SuperPixel data packet
- Custom serializer - Gigabit Wireline Transmitter (GWT)
  - Low power - 60 mW
  - 5.12 Gb/s line rate
- GWT protocol
  - scrambled data
  - parity check, no error recovery
  - ⇒ minimise bit error rate



Backend DAQ and Slow Control - PCIe40

- Single control and readout board for the entire experiment
- Can be used for TFC, SC, or DAQ or all
- Common hardware, shared firmware components
- PCIe Gen3 x16
- Intel **Arria10 FPGA** (10AX115S4F45E3SG)
  - High power consumption - up to 80W FPGA, ∼57W card
- up to 4 PCIe40 per chassis (ASUS ESC4000-G3, 2x Xeon 3 GHz, 8x 8 GB DDR4)

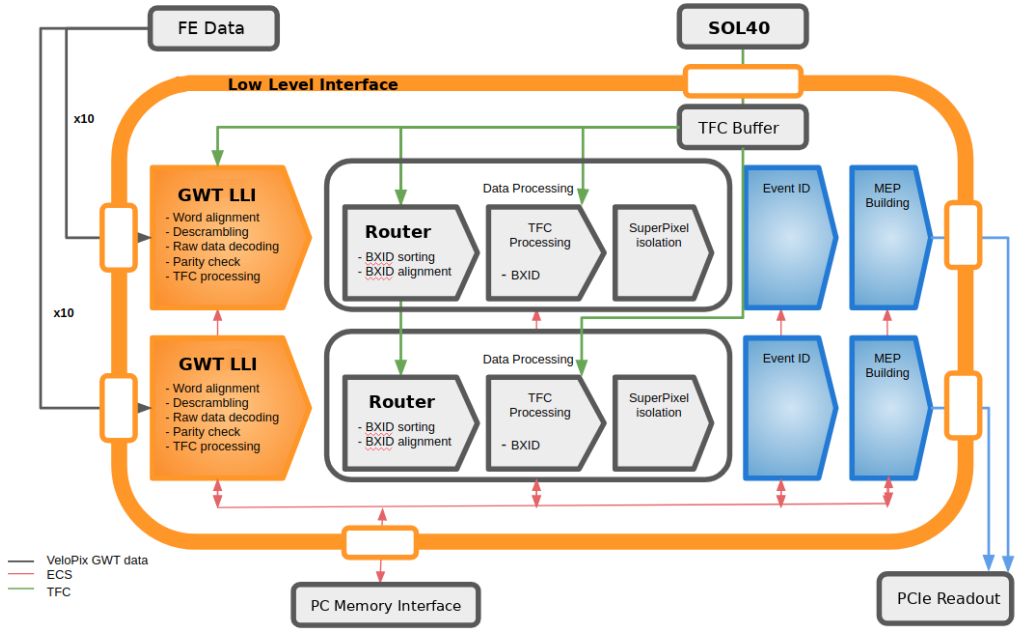


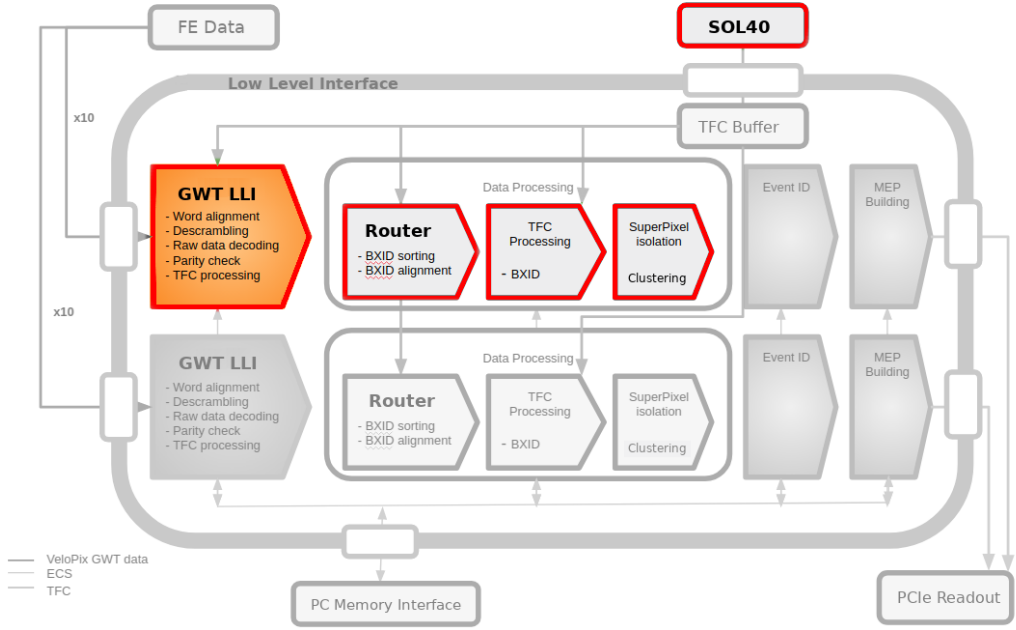
PCIe40 - http://cern.ch/go/HQ6P

- 48 bi-directional links (or 96 uni-directional) @ ∼5 Gb/s
- **Output bandwidth 100 Gb/s** (measured).

LHCb/VELO Firmware

- Common PCIe hardware allows for software-like firmware design
  - Custom components in a global framework
- Common build and simulation environment
- Gitlab allows for continous integration/deployment
  - Automated Versioning and tracability
  - Automated testing
  - Issue tracking
  - User extensible
- Same hardware deployed to labs/institutes with timing, control and DAQ in one box


FE Data
SOL40
Low Level Interface
x10
x10
TFC Buffer
GWT LLI
- Word alignment
- Descrambling
- Raw data decoding
- Parity check
- TFC processing
GWT LLI
- Word alignment
- Descrambling
- Raw data decoding
- Parity check
- TFC processing
Data Processing
Router
- BXID sorting
- BXID alignment
TFC Processing
- BXID
SuperPixel isolation
Data Processing
Router
- BXID sorting
- BXID alignment
TFC Processing
- BXID
SuperPixel isolation
Event ID
MEP Building
Event ID
MEP Building
VeloPix GWT data
ECS
TFC
PC Memory Interface
PCIe Readout


FE Data
SOL40
Low Level Interface
x10
TFC Buffer
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- Word alignment
- Descrambling
- Raw data decoding
- Parity check
- TFC processing
Data Processing
Router
- BXID sorting
- BXID alignment
TFC Processing
- BXID
SuperPixel isolation
Clustering
Event ID
MEP Building
x10
GWT LLI
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- Raw data decoding
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Data Processing
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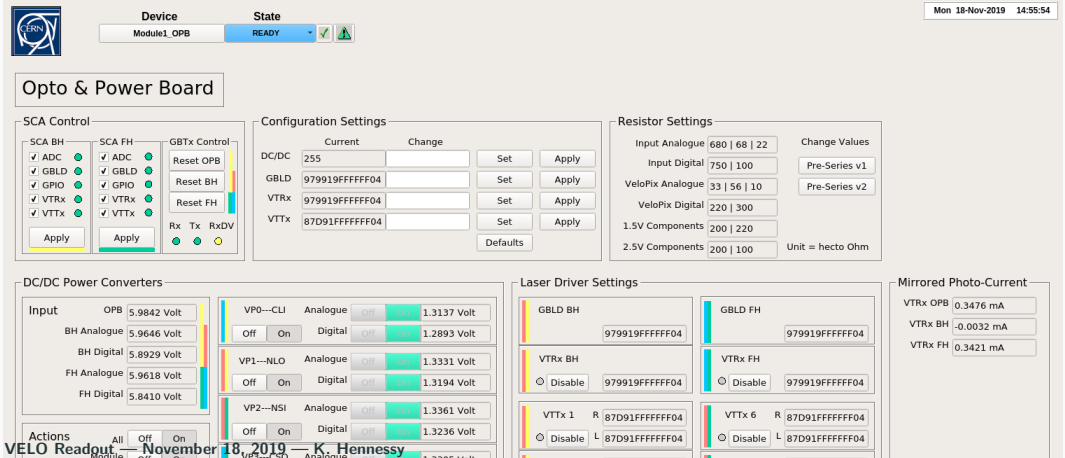
- BXID sorting
- BXID alignment
TFC Processing
- BXID
SuperPixel isolation
Clustering
Event ID
MEP Building
VeloPix GWT data
ECS
TFC
PC Memory Interface
PCIe Readout

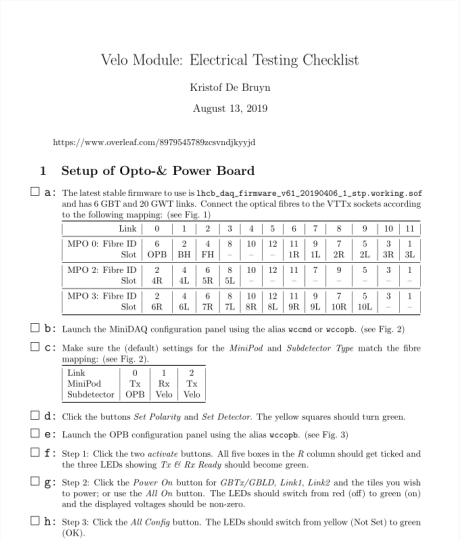
Control Software

- Software for configuring the electronics and readout
- Siemens WinCC-OA & Joint COntrols Project @ CERN (JCOP)



Quality Assurance

- IV curves, power consumption monitoring, voltage drops
- Band Gap Calibration - best estimate of sensor temperature
- VeloPix equalisation and Noise scan
- Testpulse data taking over high speed links
- Bandwidth saturation tests of HS links
- All full module tests compared to individual component tests



Velo Module: Electrical Testing Checklist

Kristof De Bruyn

August 13, 2019

https://www.overleaf.com/8979545789xcsvndjkyyjd

1 Setup of Opto-& Power Board

☐ a: The latest stable firmware to use is `lhcb_daq_firmware_v61_20190406_1_stp.working.sof` and has 6 GBT and 20 GWT links. Connect the optical fibres to the VTTx sockets according to the following mapping: (see Fig. 1)

Link	0	1	2	3	4	5	6	7	8	9	10	11
MPO 0: Fibre ID	6	2	4	8	10	12	11	9	7	5	3	1
Slot	OPB	BH	FH	–	–	–	1R	1L	2R	2L	3R	3L
MPO 2: Fibre ID	2	4	6	8	10	12	11	7	9	5	3	1
Slot	4R	4L	5R	5L	–	–	–	–	–	–	–	–
MPO 3: Fibre ID	2	4	6	8	10	12	11	9	7	5	3	1
Slot	6R	6L	7R	7L	8R	8L	9R	9L	10R	10L	–	–

☐ b: Launch the MiniDAQ configuration panel using the alias `wccmd` or `wccopb`. (see Fig. 2)

☐ c: Make sure the (default) settings for the *MiniPod* and *Subdetector Type* match the fibre mapping: (see Fig. 2).

Link	0	1	2
MiniPod	Tx	Rx	Tx
Subdetector	OPB	Velo	Velo

☐ d: Click the buttons *Set Polarity* and *Set Detector*. The yellow squares should turn green.

☐ e: Launch the OPB configuration panel using the alias `wccopb`. (see Fig. 3)

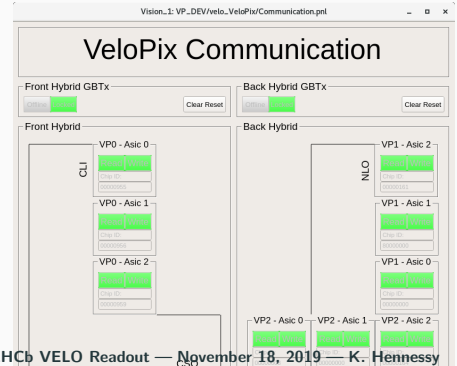
☐ f: Step 1: Click the two *activate* buttons. All five boxes in the *R* column should get ticked and the three LEDs showing *Tx & Rx Ready* should become green.

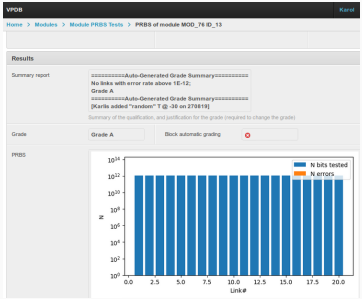
☐ g: Step 2: Click the *Power On* button for *GBTx/GBLD, Link1, Link2* and the tiles you wish to power; or use the *All On* button. The LEDs should switch from red (off) to green (on) and the displayed voltages should be non-zero.

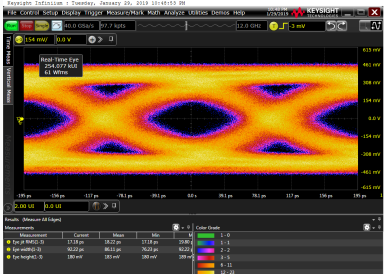
☐ h: Step 3: Click the *All Config* button. The LEDs should switch from yellow (Not Set) to green (OK).

QA of High speed links

- PRBS test for high speed readout
- Slow control communication tests with OPB and VeloPix
- Timing and fast control checks

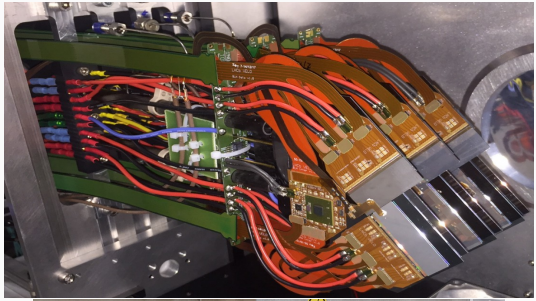






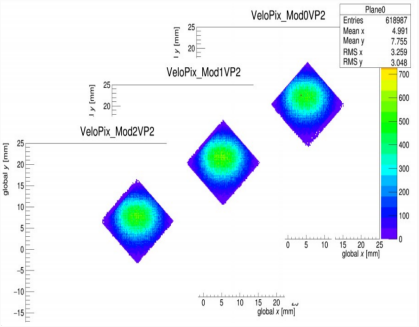
Testbeam Q4 2018

- Performed at CERN just prior to the Long Shutdown of SPS
- VeloPix and sensors had been tested in previous beam tests, but never with **full high-speed readout**, and **complete LHCb slow control and DAQ chain**
- Synchronised with Timepix 3 telescope. Allows to check time alignment $< 1\,\text{ns}$



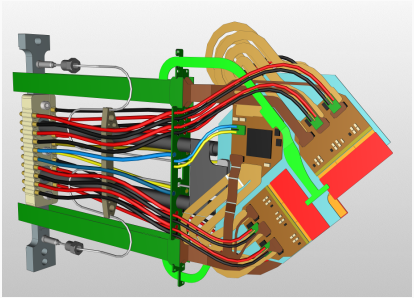
Testbeam Q4 2018

- Successfully took high-speed data from VeloPix synchronised between 3 module planes
- HV scans, Time-over-Threshold scans, Ikrum (Krummenacher current) scans
- Synchronisation tests
- Integrated with LHCb PCIe40 firmware and software
- Several other testbeam and irradiation campaigns to qualify VELO sensors



Conclusion

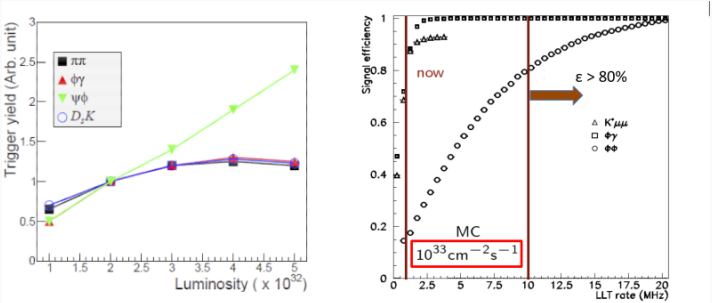
- Vertex Locator with high-speed readout in vacuum
- Leveraging many rad-hard components developed at CERN and within the collaboration
- VeloPix culmination of many years of rad-hard ASIC development for tracking
- Common readout platform for LHCb - with VELO customisations
- Good performance of high speed links with full module control and readout chain



Thank You

Backup

The need for an upgrade



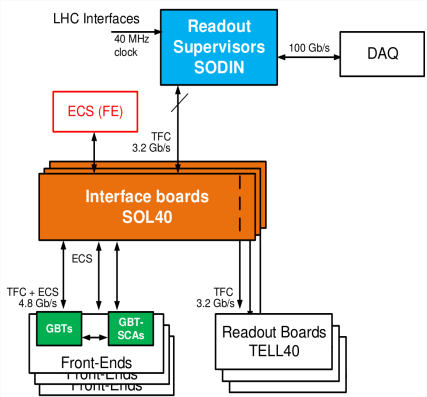
Due to the available bandwidth and the limited discrimination power of the L0 trigger, LHCb experiences the **saturation of the trigger yield** on hadronic channels at around 4. $\times 10^{32}$ cm^{-2}s^{-1}.

With the **upgraded detector it** will be possible to increase the physics yields by a factor 10 in the decays with muons, a factor 20 for hadronics channels, collecting **~ 50fb^{-1}** running at 1-2 $\times 10^{32}$ cm^{-2}s^{-1}

10 times the current design luminosity but with increased complexity (pileup greater a factor 5).

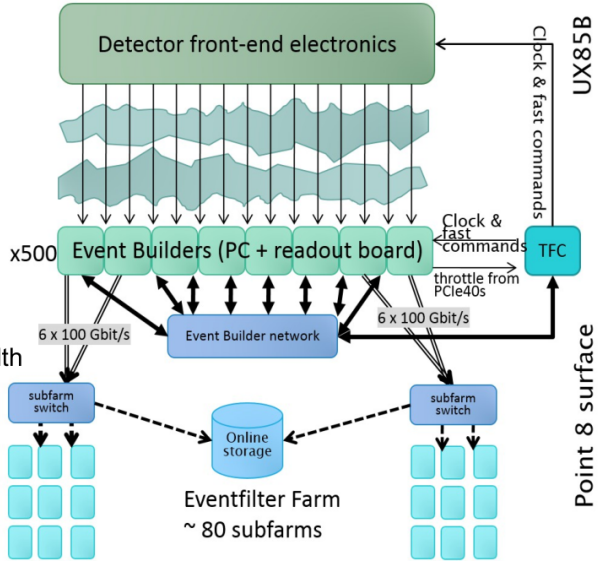
Timing and Fast Control (TFC)

- Single Readout Supervisor provides a clock and timing commands to front-end and back-end electronics
  - BXID Reset, FE Reset, BE Reset, Sync, ...
- Interfaces with LHC
- TFC commands are fixed latency
- Data are *NOT* fixed latency
- For VELO, TFC synchronisation commands form "special" GWT packets and sent immediately from front-end
  - (standard data packets are sent out-of-time)
- 10G PON network with optional feedback



Architecture

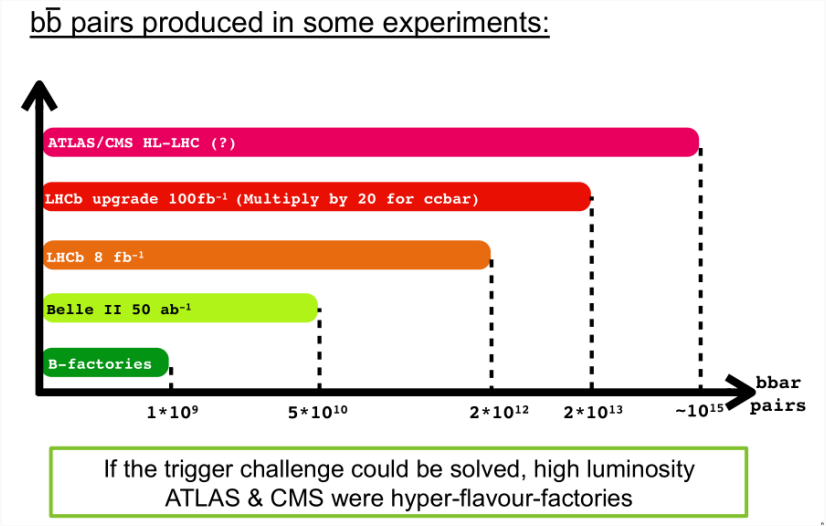
- Readout located on surface
  - Distance between FE and RO : ~350m
- ~15000 optical links
- ~ 500 readout boards
- ~24 links in average on each board
- ~100 kbytes per event
- ~32 Tb/s aggregate bandwidth



MiniDAQ - All in one solution

- MiniDAQ = PCIe40 + server
- The MiniDAQ platform allows for controls, DAQ, and software all to run in a **standalone system**
- The server is provided with the PCIe40 installed, necessary programming cables and OM3 fibres
- WinCC JCOP software comes pre-installed (a licence is needed)
- All necessary drivers and support software is installed
- With one server, one can control the front-end hardware and at the same time read out its data.

b-b pairs produced

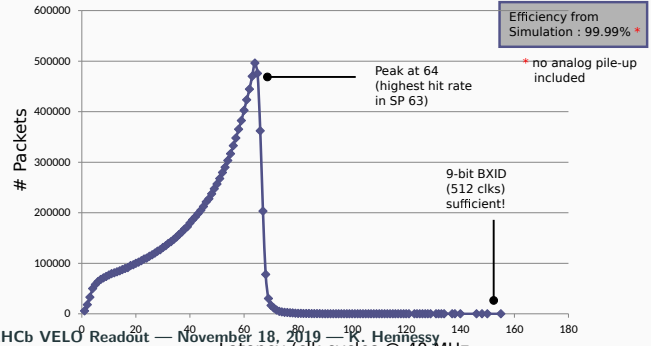


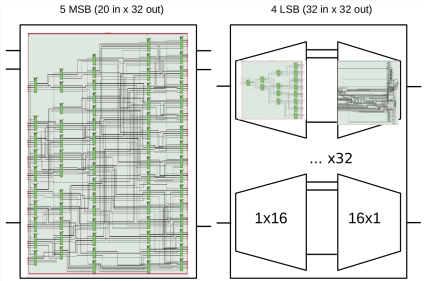
LHCb facts

- New data centre being constructed (2 MW)
- 4000 U in 6 container modules
- 400+ Gb/s to CERN IT
- Studying HPC - FPGA, GPU, ML...
- Biggest/fastest readout system to date

BXID Router

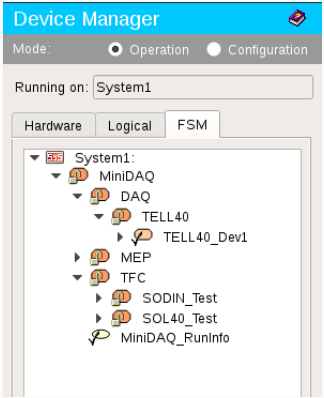
- Time-ordering SuperPixel data
  - 9-bit **router** sorts data 1 bit at a time
  - Extensive simulation required - both to maximise speed (¿160 MHz) and minimise FPGA resource usage
  - Latency limit ¡ 512 clock cycles



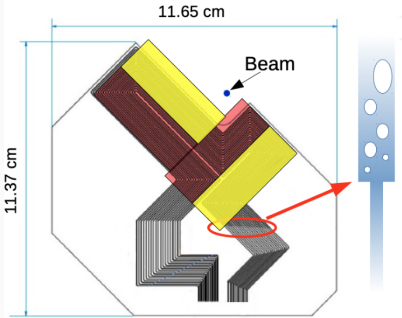


ECS Software

- Control system modelled with finite state machine tree
  - commands propagate down; status propagates up
- Integrates with SOL40, TELL40, SODIN
- Can integrate with COTS hardware (CAEN, ISEG, Wiener...)
- Rapid development
- Oracle database backed
- Archiving, trending, alarm functionality...



Micro-channel cooling



500 µm thick silicon substrate

Input restrictions:

- 60 x 60 µm , 40 mm long
- Dominant pressure drop
- Prevent instabilities among the channels

Main channels

- 120 x 200 µm
- [230, 290]mm long
- Heat is absorbed by the CO_2: change in gas/liquid ratio

Increase in cross section between the restriction and the main channels triggers the boiling

Refs

- GBT
- GBT-SCA
- PCIe40