R&D on sensors for the silicon pixelated tracker

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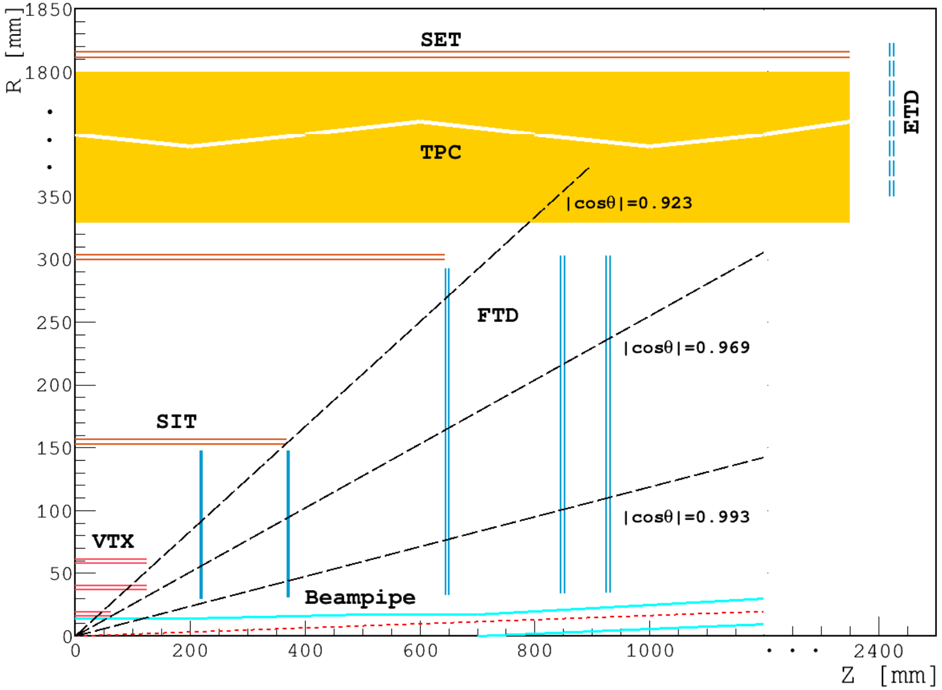
Outlines

1. **Brief introduction of CEPC silicon tracker**
2. **Introduction of SUPIX-2, a prototype of CMOS Pixel Sensor developed at Shandong University**
3. **TCAD simulation on sensors**
4. **Pixel circuit design**
5. **Electronics for test system**
6. **Status and prospects**

CEPC silicon tracker



Functionalities:

- **Improving tracking efficiency and precision by high precision hit points along the trajectories,**
- **monitoring possible field distortion in the TPC,**
- **contributing detector alignment,**
- **separating events between bunch crossings with relative time-stamping, and**
- **potentially the dE/dx measurement.**

Primary requirements

✓ **Single point resolution: σ_{SP} < 7μm,**

✓ **Material budget: X_0 < 0.65%,**

✓ **Radiation hardness: 3.4MRad (TID) and 6.2×10^{12} 1MeV n_{eq}/cm^2 (NIEL) per year.**

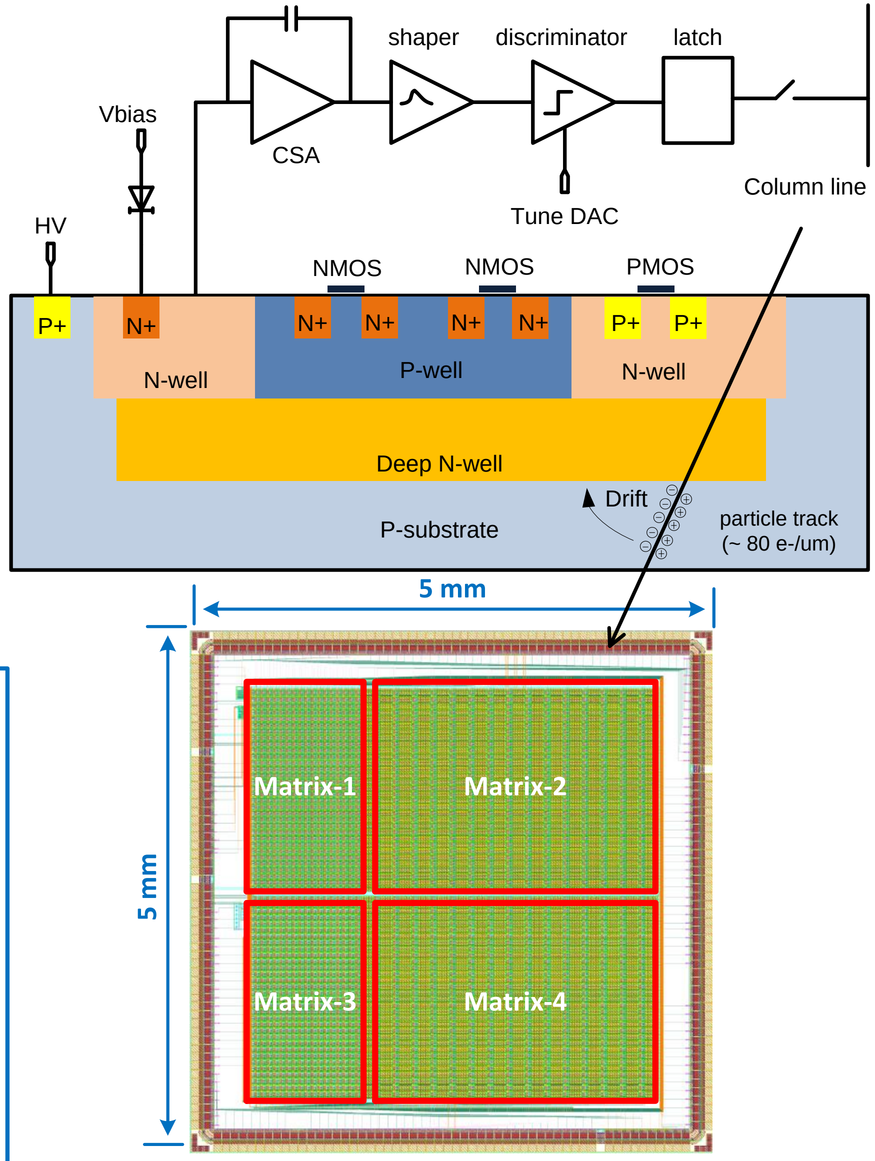
SUPIX-2 – A CMOS Pixel Sensor for CEPC

- - SMIC 0.18 μm technology - -

- ✓ **Triple well: Nwell, Pwell, Deep Nwell**
- ✓ **No EPI-layer**
- ✓ **10 Ω·cm substrate**
- ✓ **d ~ $\sqrt{\rho \cdot V}$**
- ✓ **SMIC 0.18 μm process → 15 V**
- ✓ **Circuits are realized mainly by NMOS transistors**
- ✓ **PMOS is coupled with collection electrode**

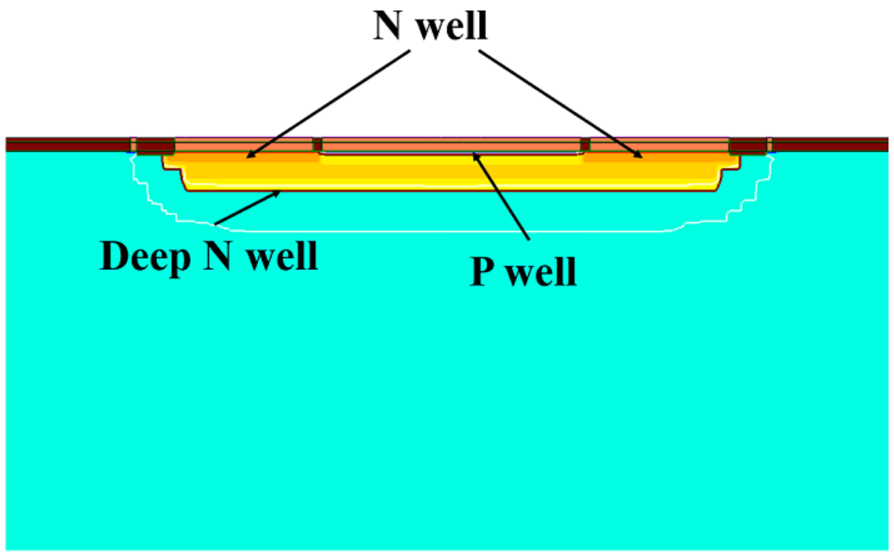
-- Architecture of SUPIX-2 --

- ◆ **4 submatrices, each matrix is 32×16**
- ◆ **Pixel size: $60 \times 60\ \mu m^2$, $60 \times 180\ \mu m^2$**
- ◆ **Rolling shutter readout mode**
- ◆ **16 parallel digital outputs**
  - ■ **Each pixel is implemented with a charge sensitive amplifier (CSA), a shaper, a discriminator and a latch**
- ◆ **Sensitive area: ~$3.84 \times 3.84\ mm^2$**

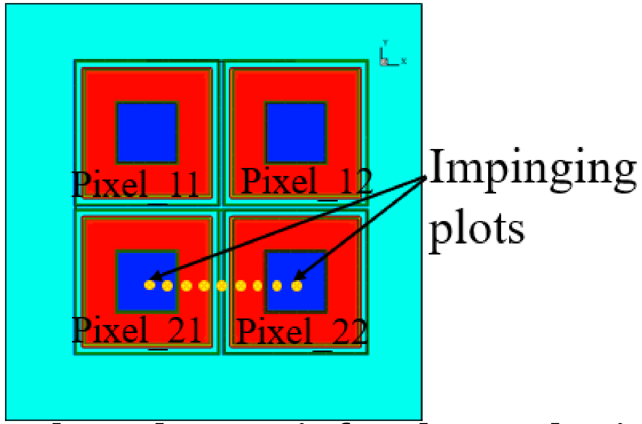


Layout of SUPIX-2

TCAD simulation on sensor



Side view of a pixel sensor



Impinging plots along the X-axis for charge sharing simulation

Before the circuit design, the geometry of the sensor has been optimized via TCAD.

Toolkit: Sentaurus SYNOPSYS Inc.

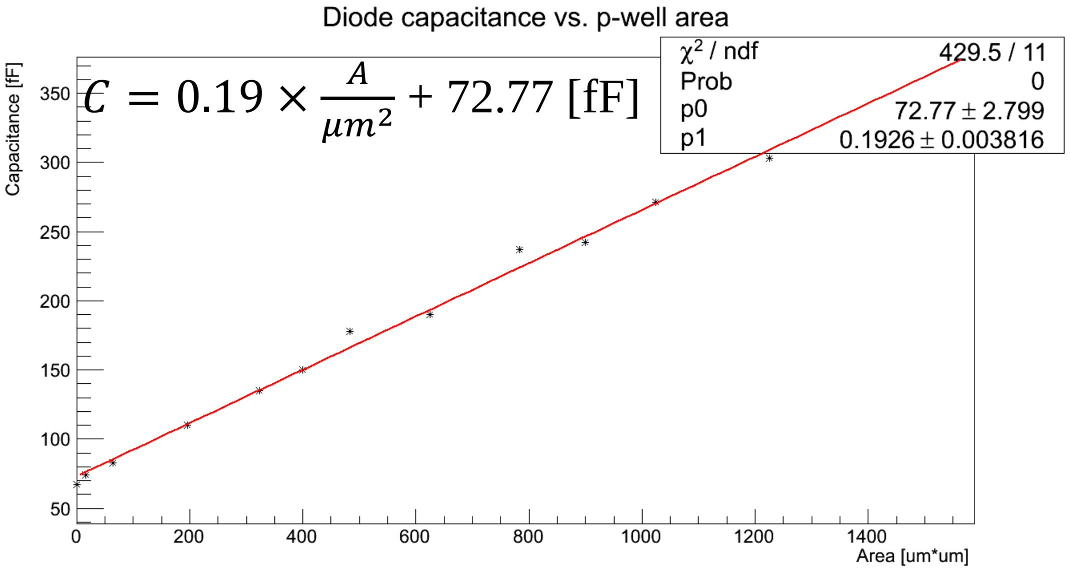
Pixel size: 50 × 50 μm^2 (according to the CEPC CDR)

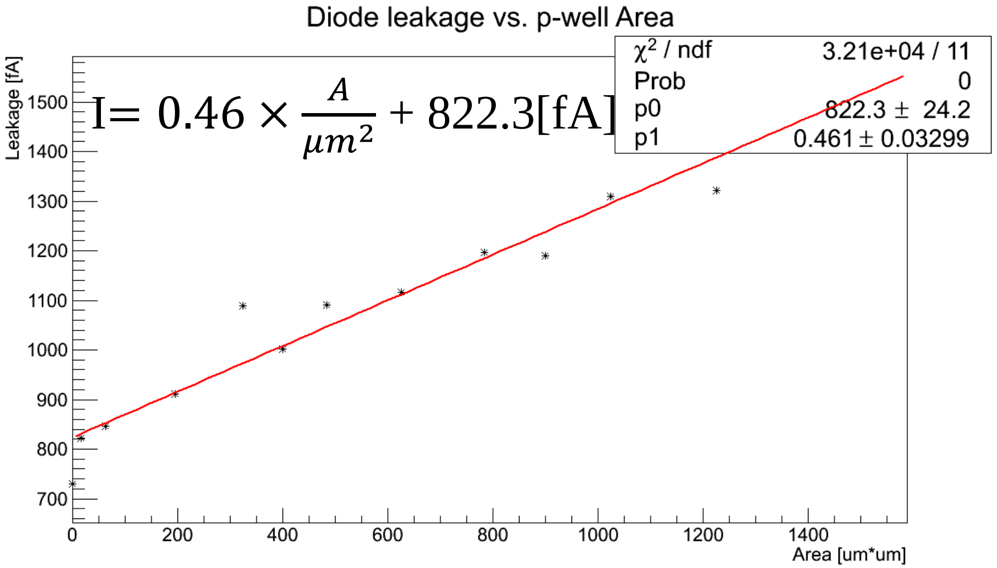
Variable: Area of the p-well

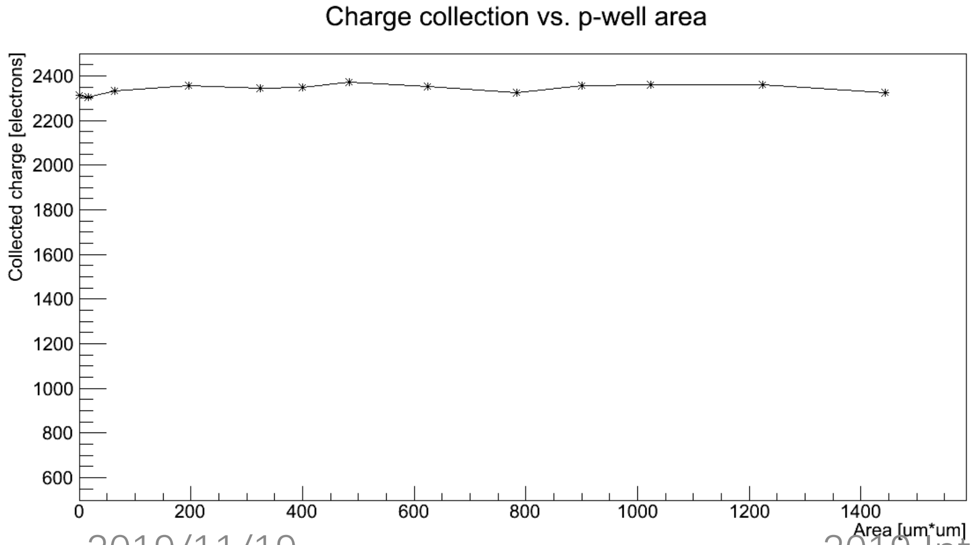
Simulated performance:

- ✓ **Diode capacitance**
- ✓ **Diode leakage**
- ✓ **Charge collection (charge collecting time 100ns)**
- ✓ **One dimensional charge sharing**
- ✓ **Radiation effects (NIEL)**

Sensor performance variations caused by p-well area

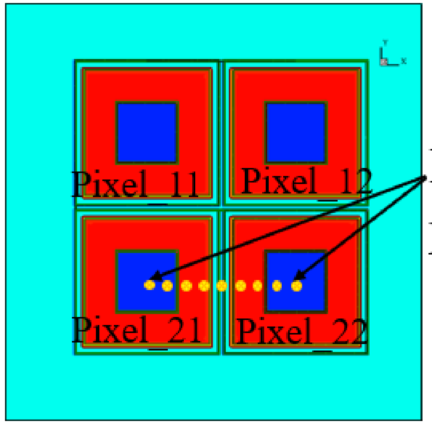


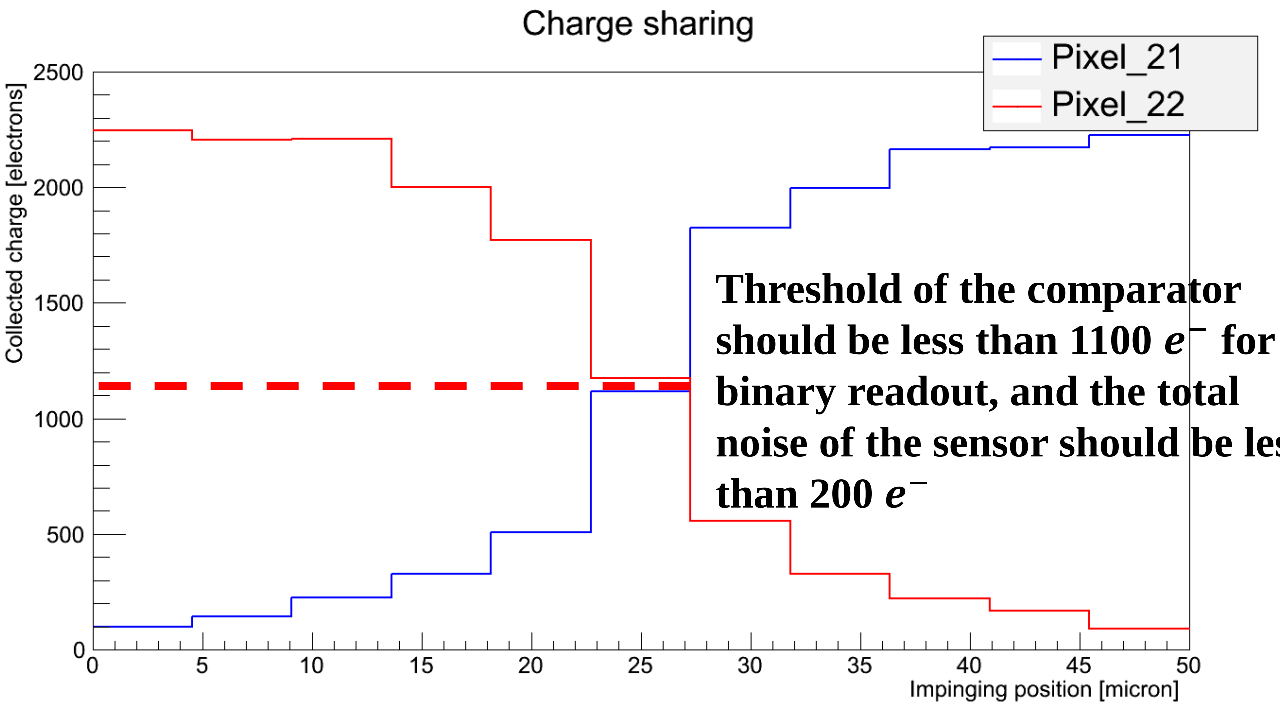




The area of p-well has much effect on the diode capacitance and leakage, and roughly increase linearly against the p-well area. But it has little impact on the charge collection. In order to keep the sensor noise low, the area of the p-well should be as small as possible. For SUPIX-2, $60\times 60\ \mu m^2$ pixel size and140 μm^2 p-well have been chosen considering the circuit design.

Charge sharing and radiation effects





Threshold of the comparator should be less than 1100 e^- for binary readout, and the total noise of the sensor should be less than 200 e^-

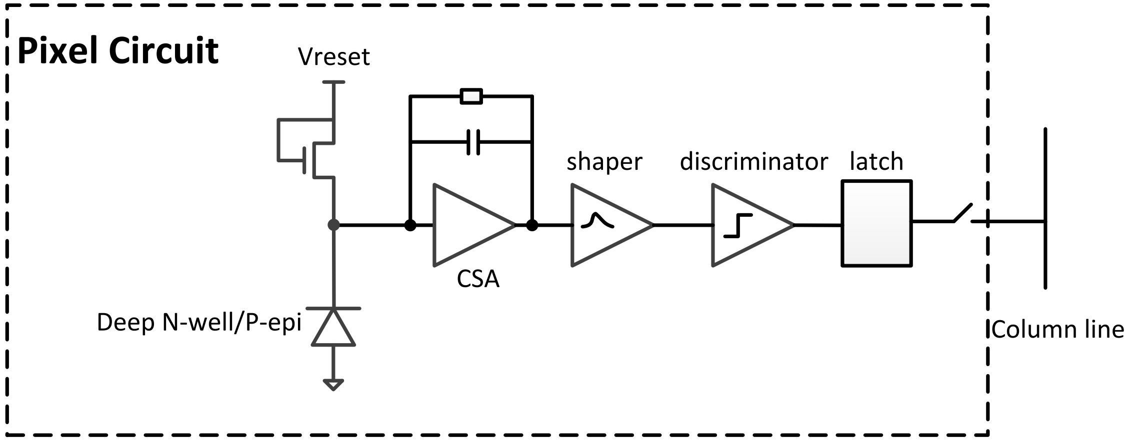
Sensor performance comparison before and after radiation

Flux(1MeV n_{eq}/cm^2)	Capacitance(fF)	Leakage(fA)	Collected charge(100ns)
0	150	1002	2350 e^-
6.2×10^{12}	153	2992	1780 e^-

The increased leakage current and lower charge collection would lead to the decrease of the SNR and lower detection efficiency after irradiation.

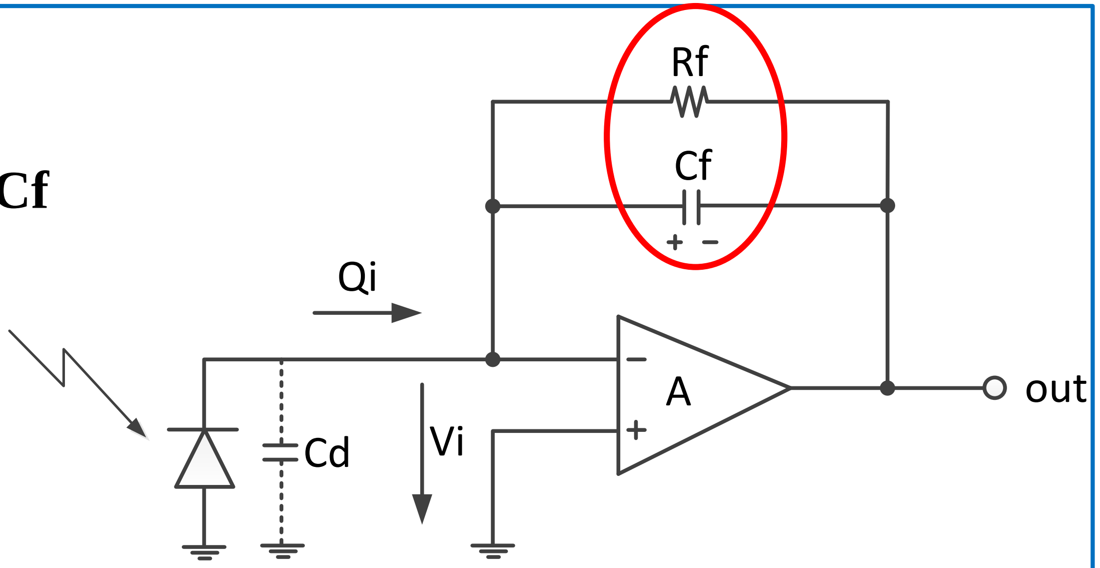
Pixel circuit

- **Pixel circuit:**
  - **Charge gain (CSA + shaper): ~ 110 mV/ke$^-$**
  - **Response time: ~ 2.6 μs**
  - **Total current: ~ 7.5 μA**
  - **The number of PMOS transistors has be kept as low as possible**
    - **CSA: single-stage cascode amplifier with 2 PMOS**
    - **Shaper: CR-RC using only NMOS transistors**
    - **Discriminator: fully differential amplifier using only NMOS**
    - **Latch: NOR gates with 4 PMOS**



Pixel circuit

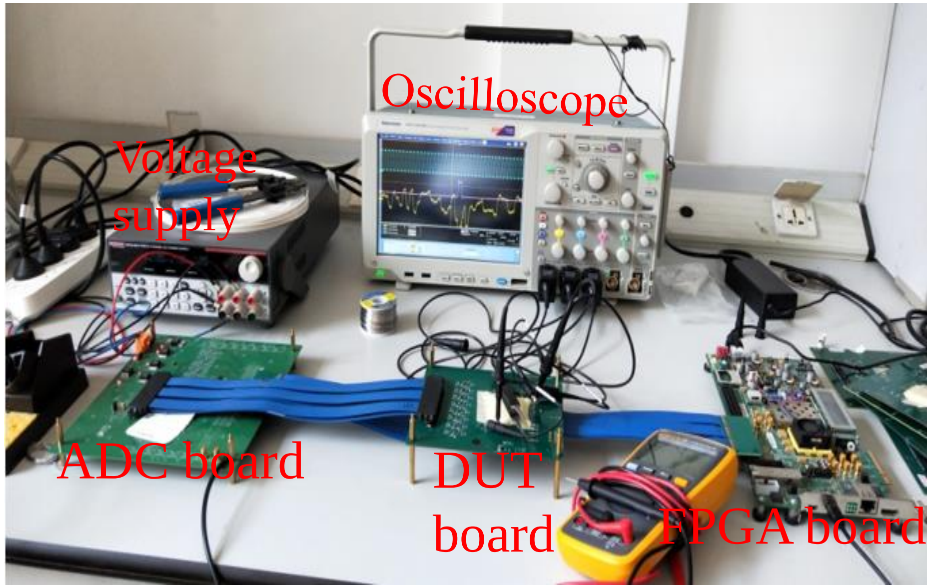
- **Requirements of CSA:**
  - **Large gain of amplifier**
    - **Improve "dynamic" input capacitance: (A+1)Cf**
      - **Gain of CSA ~ 1/Cf**
      - **Increase charge transfer efficiency**
  - **Small Cf (feedback capacitance)**
    - **Improve gain of CSA**
      - **NMOS capacitor**
      - **MOM (Metal-Oxide-Metal) capacitor to realize below 1fF**
  - **Large Rf (feedback resistance)**
    - **Amplifier needs DC feedback to discharge the input node and stabilize the operation point**
    - **Usually a resistor in the MΩ – GΩ is used**
    - **CMOS process don't have high value resistors**
      - **Use a current circuit to realize above 100 MΩ**
      - **NMOS switch**



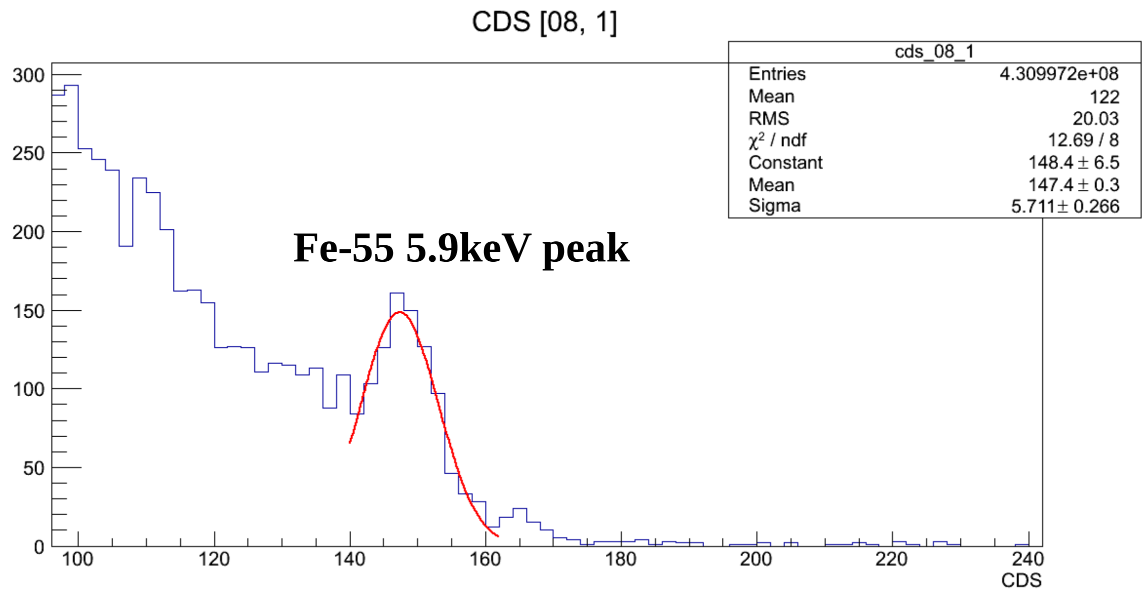
Architecture of CSA

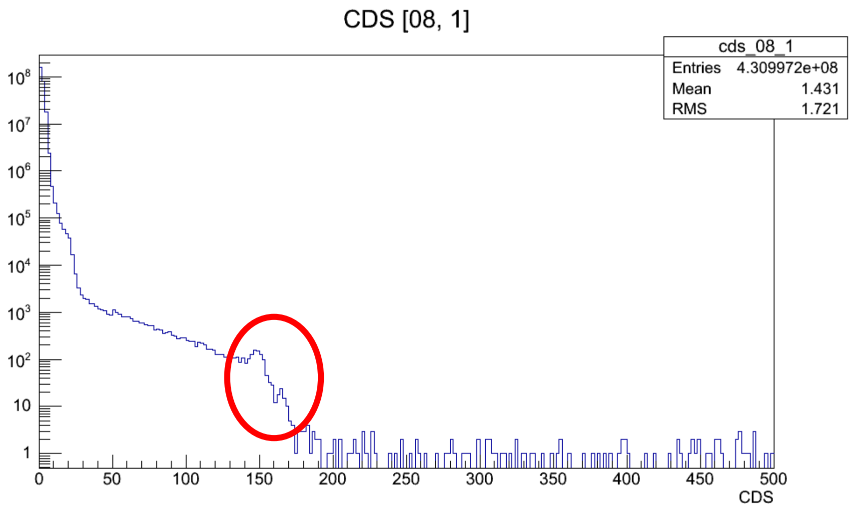
Test system for SUPIX-1

- The test system for SUPIX-1 is running in SDU.
  - DUT board: carry the pixel sensor
  - ADC board: digitize the analog output for pixel sensor
  - FPGA evaluation board: process and transmit the data



Current test system for SUPIX-1

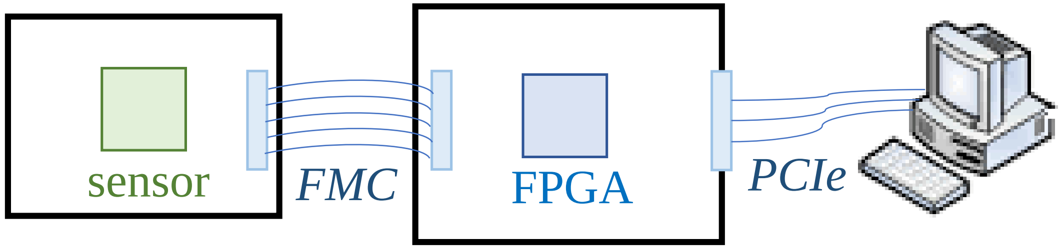




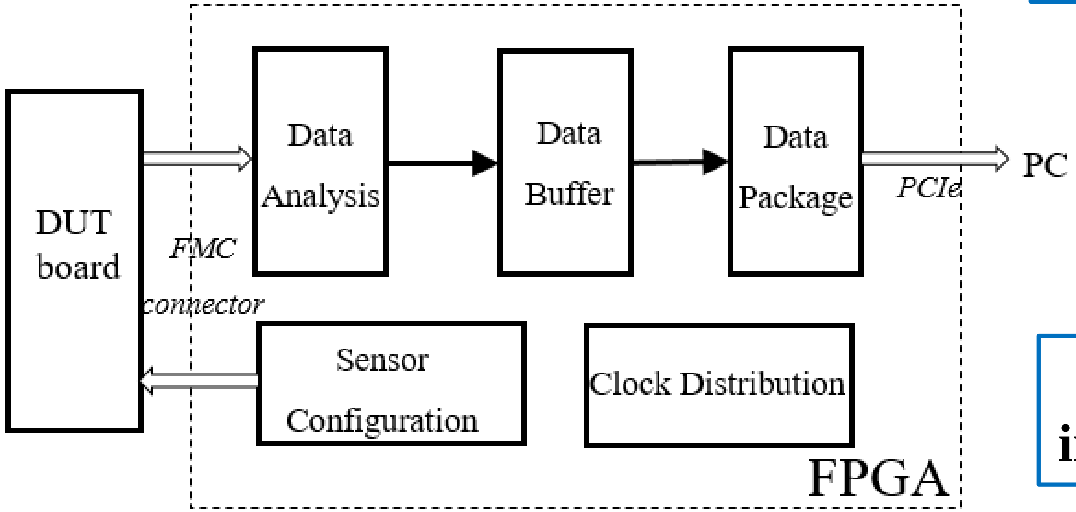
Radiative source test with Fe-55

Test system for SUPIX-2

**based on the SUPIX-1 test system*



SUPIX-2 test system scheme



- DUT board: carry the sensor, bias the sensor, supply the power, transfer the digital signal put out by the sensor though FMC connector and cable
- FPGA board (KC705 evaluation board): communicate with PC via PCIe, control the data loading/receiving

Time Over Threshold method in FPGA will be realized in SUPIX-2 test system to achieve multi-bits resolution.

Status and prospects

- **The technology is feasible for the tracker via the simulation, but the noise and the radiation hardness performance would be challenges. Test data is in need to verify the feasibility.**

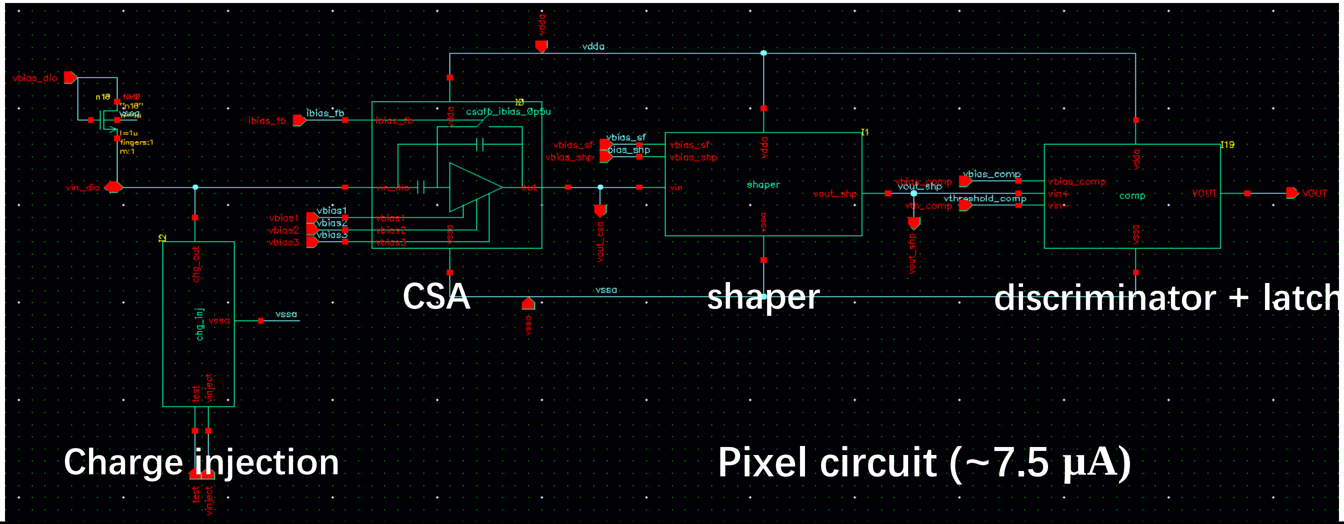
- **Final design has been submitted on Nov. 11, and the chip is available around March 2020.**

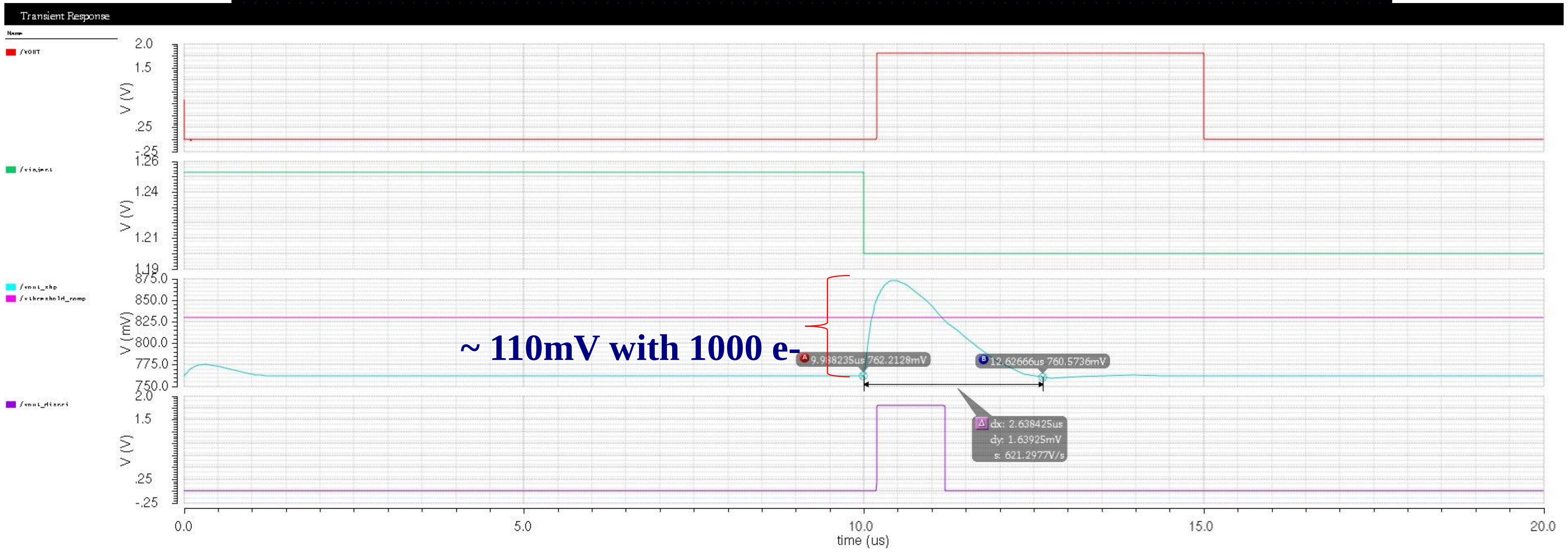
- **Design of the test board is in progress.**

Thanks!

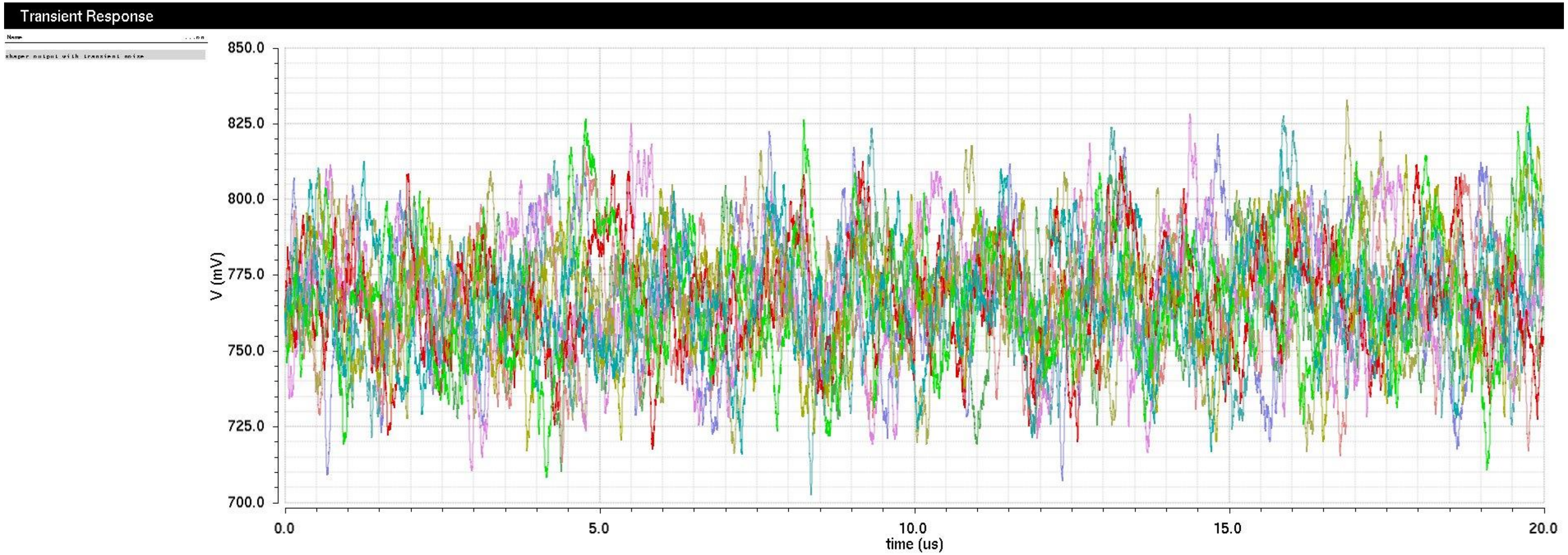
Back up

Pixel circuit



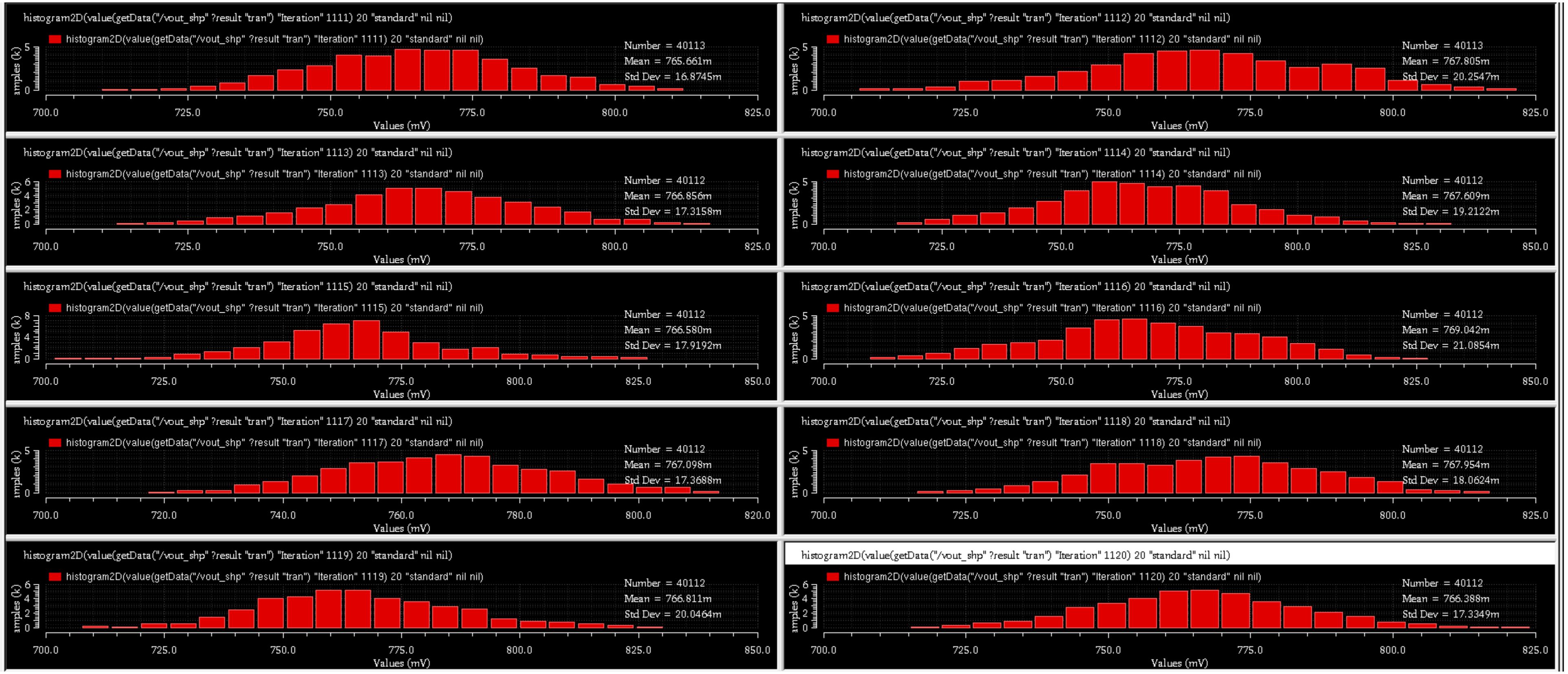


Noise simulation



Shaper output without charge

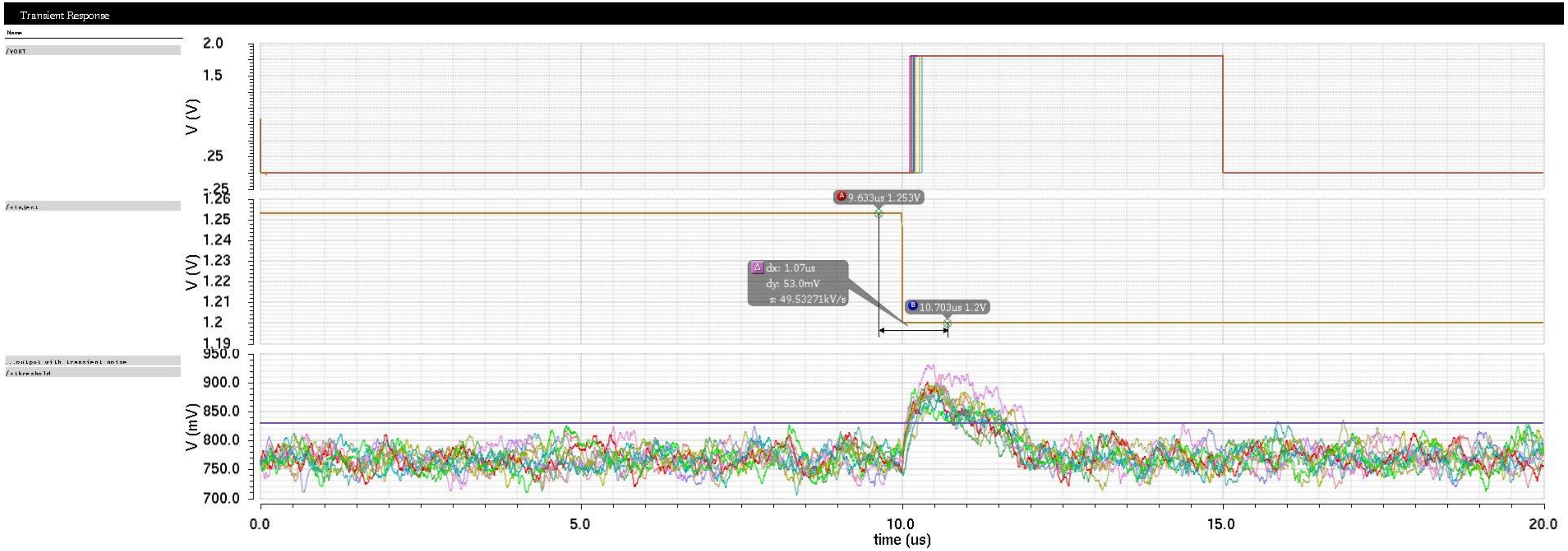
Noise simulation



Output histogram with transient noise

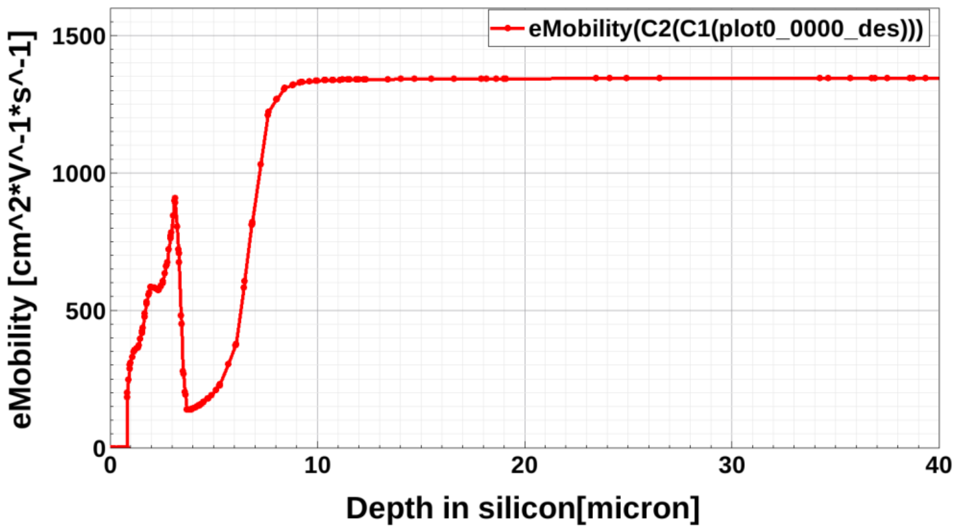
Standard deviation ~ 18.5 mV

Noise simulation

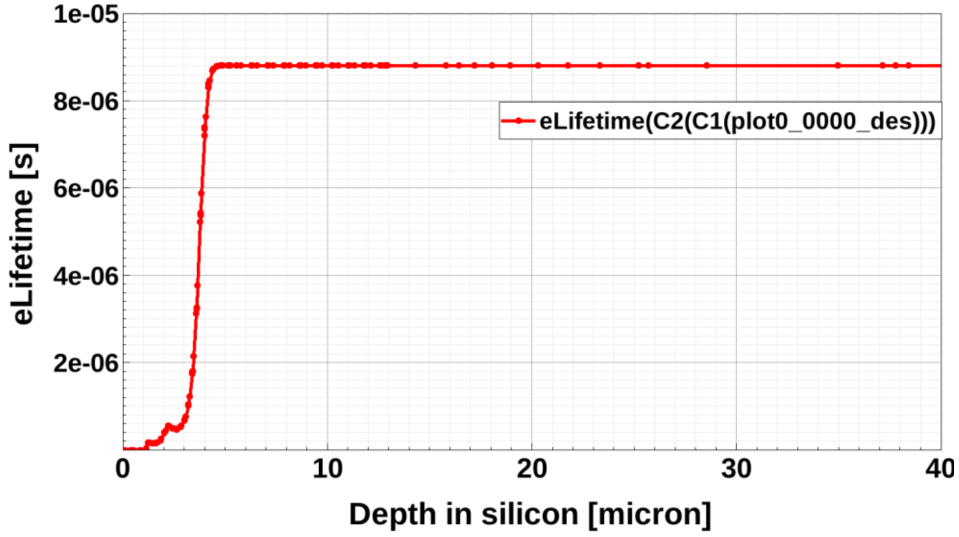


Simulation results with ~ 1000 e-

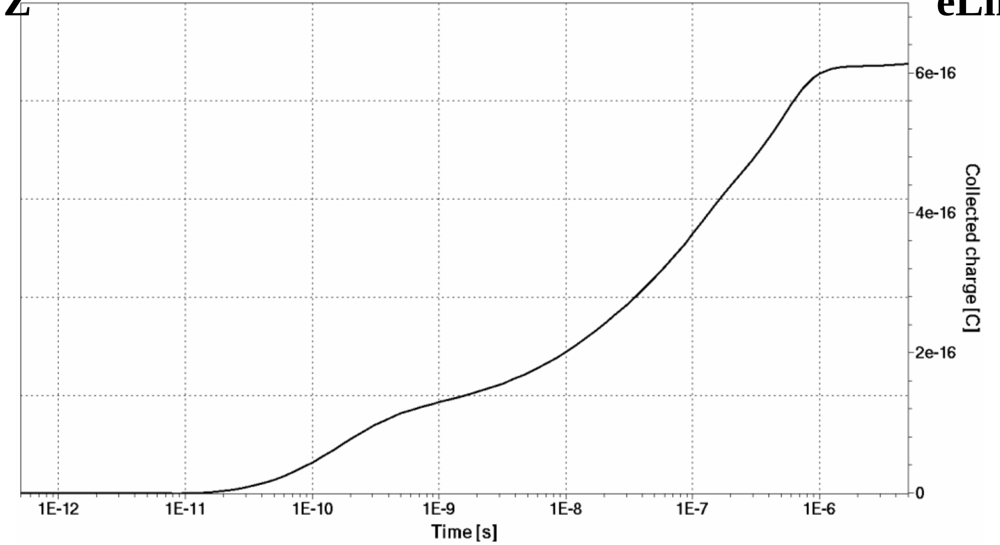
Charge collection simulation



eMobility vs. Z



eLifetime vs. Z



Collected charge vs. time