HV-CMOS sensors for the outer Tracker

Marcello Borri, John Dainton, Harald Fox, Yanyan Gao,
Roy Lemmon, Daniel Muenstermann, Ivan Peric, Rudolf Schimassek, Hongbo Zhu

STFC Daresbury Laboratory
Lancaster University
The University of Edinburgh
Karlsruhe Institute of Technology
Institute of High Energy Physics, CAS

Introduction and Overview

Progress and developments since the first idea was presented by Daniel Muenstermann at the Oxford CEPC workshop this year:

https://indico.cern.ch/event/783429/contributions/3379826/attachments/1831027/2998576/Muenstermann_CMOS-for-CEPC.pdf

In this talk:

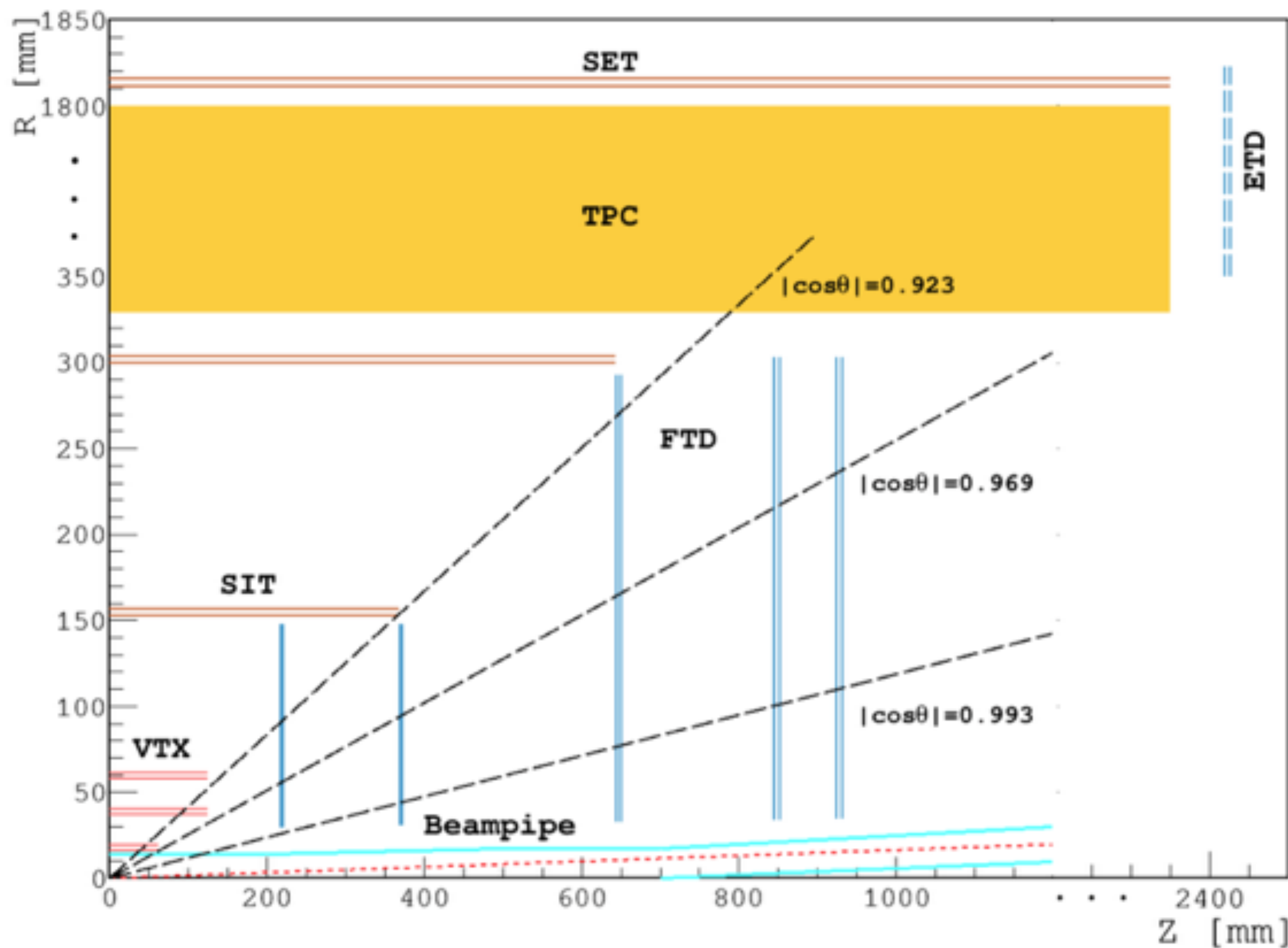
1. CEPC tracker layouts and requirements from CDR
2. Sensors: ATLASPix3
3. Sensor readout: Flex & YARR
4. Staves: The ALICE experience
5. Conclusions and summary

CEPC tracker designs: TPC/Si

Baseline tracker design: TPC

and 3 layers / 5 disks of silicon sensors,

50 m^2 if built in CMOS pixels (strips default)



Detector		Radius R [mm]		$\pm z$ [mm]	Material budget [X_0]
SIT	Layer 1	153		371.3	0.65%
	Layer 2	300		664.9	0.65%
SET	Layer 3	1811		2350	0.65%
		R_{in}	R_{out}		
FTD	Disk 1	39	151.9	220	0.50%
	Disk 2	49.6	151.9	371.3	0.50%
	Disk 3	70.1	298.9	644.9	0.65%
	Disk 4	79.3	309	846	0.65%
	Disk 5	92.7	309	1057.5	0.65%
ETD	Disk	419.3	1822.7	2420	0.65%

Operation mode	H (240)	W (160)	Z (91)
Track multiplicity (BX^{-1})	310	300	32
Bunching spacing (ns)	680	210	25
SIT-L1 occupancy (%)	0.19	0.58	0.52
FTD-D1 occupancy (%)	0.17	0.54	0.48

Table 4.6: Estimated occupancies of the first layers of the SIT (SIT-L1) and the FTD (FTD-D1). See context for more details.

CEPC tracker designs: FST / FST2

Full silicon alternatives:

FST: 98 m^2 in CMOS

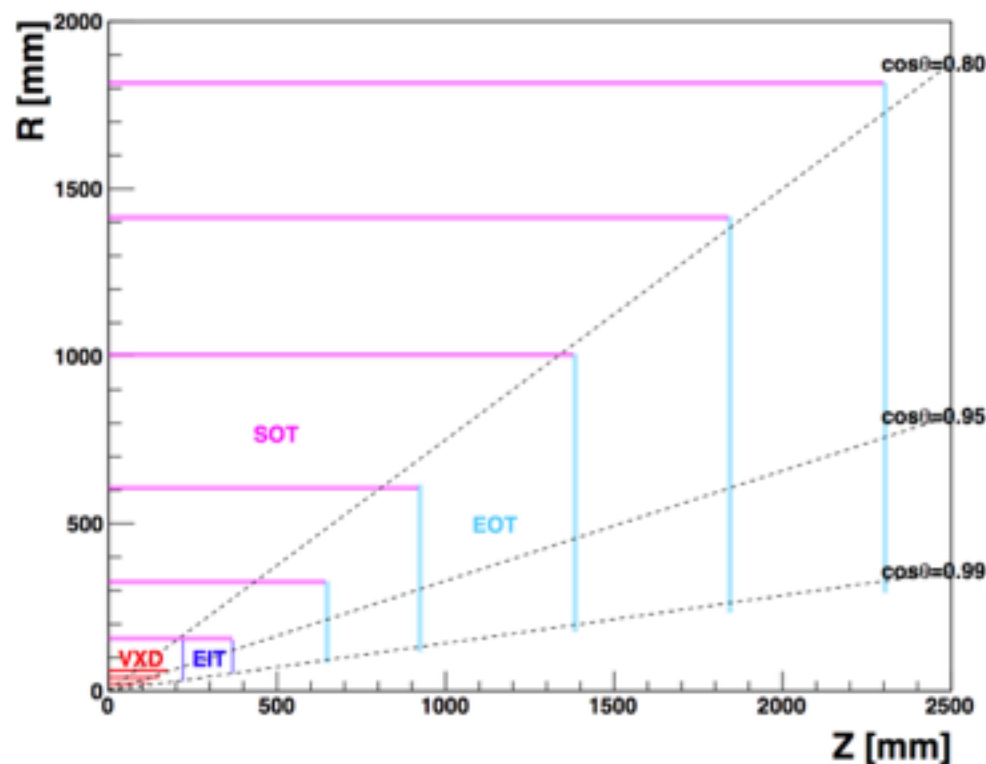
FST2: 101 m^2 in CMOS

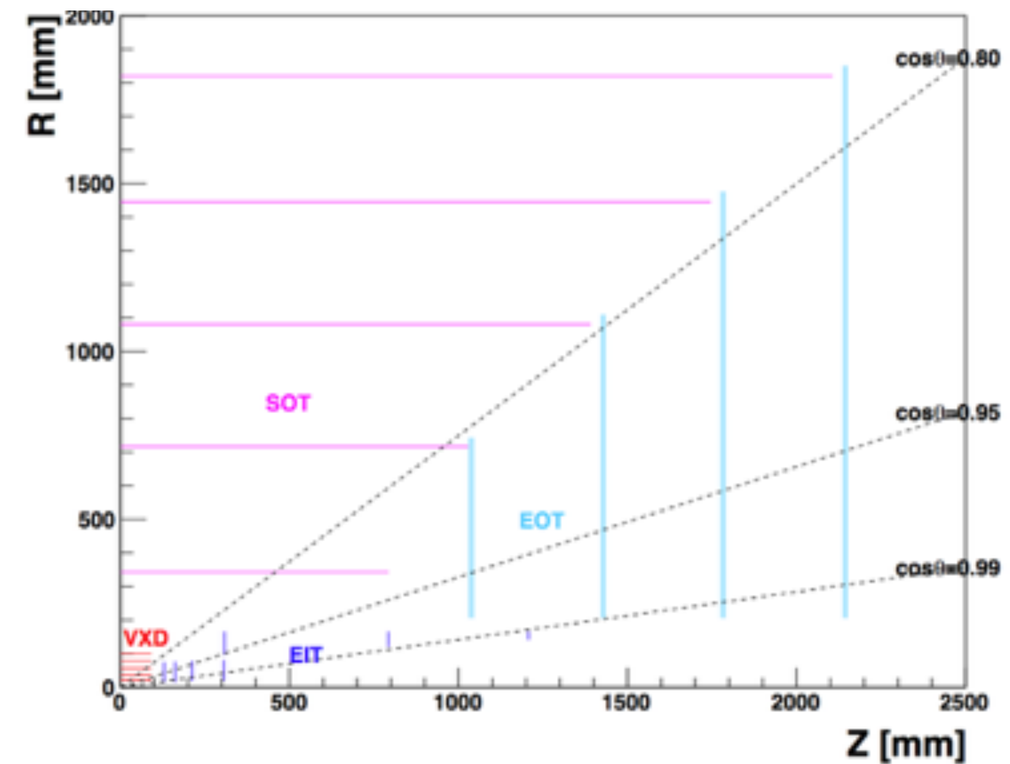
Alice ITS: ~10 m^2; ATLAS upgrade Pixel ~14m^2

FST and FST2 configurations. The total radiation length, including dead material such as the readout, for the entire tracking system is about 5–7% X_0 for the FST and 7–10% X_0 for the FST2.

	FST				FST2			
SOT	R (m)		$\pm z$ (m)	Type	R (m)		$\pm z$ (m)	Type
Layer 1	0.153		0.368	D	0.344		0.793	S
Layer 2	0.321		0.644	D	0.718		1.029	S
Layer 3	0.603		0.920	D	1.082		1.391	S
Layer 4	1.000		1.380	D	1.446		1.746	S
Layer 5	1.410		1.840	D	1.820		2.107	S
Layer 6	1.811		2.300	D				
EOT	R_{in} (m)	R_{out} (m)	$\pm z$ (m)	Type	R_{in} (m)	R_{out} (m)	$\pm z$ (m)	Type
Disk 1	0.082	0.321	0.644	D	0.207	0.744	1.034	D
Disk 2	0.117	0.610	0.920	D	0.207	1.111	1.424	D
Disk 3	0.176	1.000	1.380	D	0.207	1.477	1.779	D
Disk 4	0.234	1.410	1.840	D	0.207	1.852	2.140	D
Disk 5	0.293	1.811	2.300	D				

Figure 4.23: $R-Z$ views of the full-silicon tracker options, FST (top) and FST2 (bottom). In the FST layout, the full strip detector (SOT and EOT) is composed of double silicon strip layers. In the FST2 layout, the SOT consists of single layers, while the EOT consists of double-strip layers.





ATLAS/ALICE concepts for the CEPC

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Comparison:

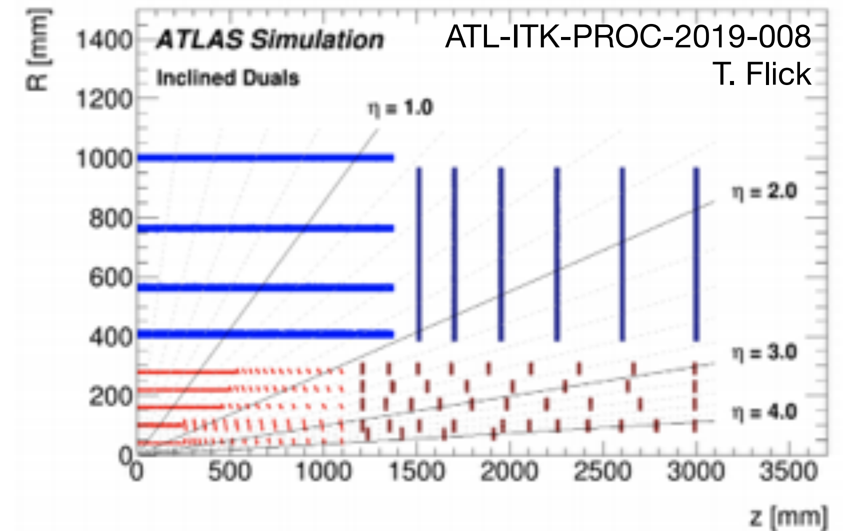
25ns bunch spacing (Z-mode): same for ATLAS

O(100 m^2) of silicon tracker: comparable for the ATLAS ITK

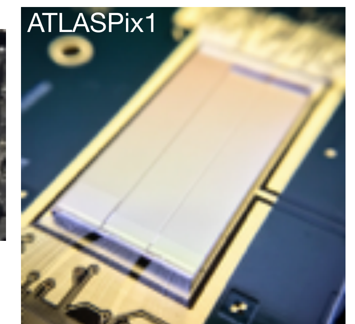
pitch/resolution: 50 µm in ϕ

ALICE ITS: 29µm x 27µm monolithic CMOS

ATLAS ITK Pixel CMOS: < 50µm x 150µm



L. Musa, ECFA HL-LHC workshop

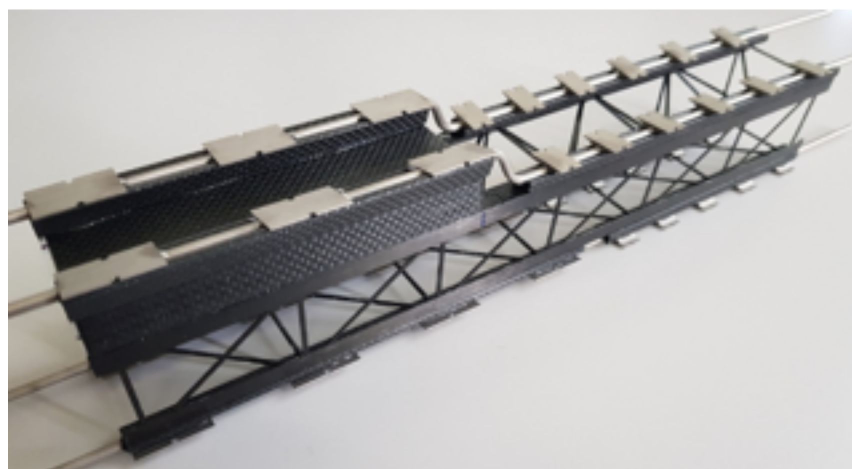


H. Augustin eg. al,,
Uni Heidelberg

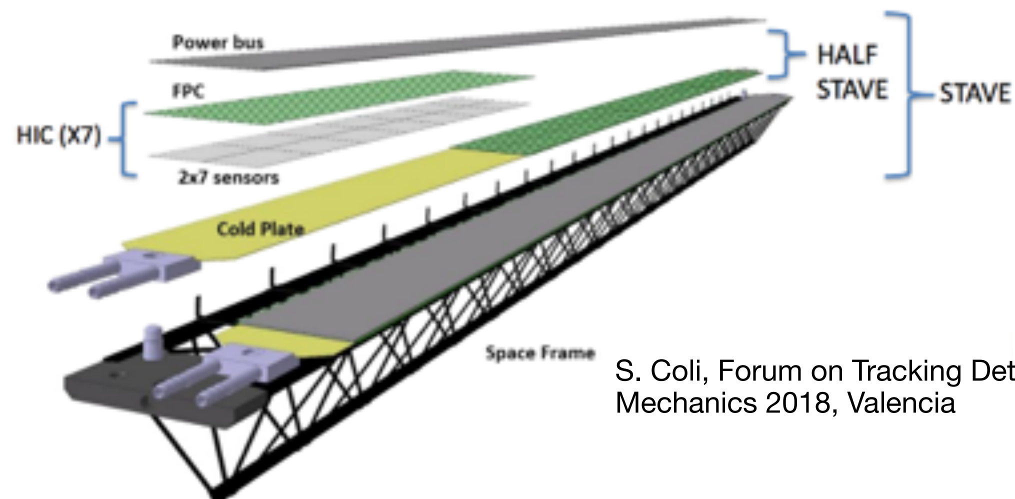
material budget for tracker layers:
0.65% (TPC/Si)/~1% (Full Si) X/X_0 / layer

ALICE: 0.8%/layer outer barrel staves

ATLAS: ITK Pixel <1X_0 total (standard hybrid, Ti cooling pipes, all supports & services)



https://www.unige.ch/dpnc/en/groups/giuseppe-iacobucci/research/slim-mechanics/



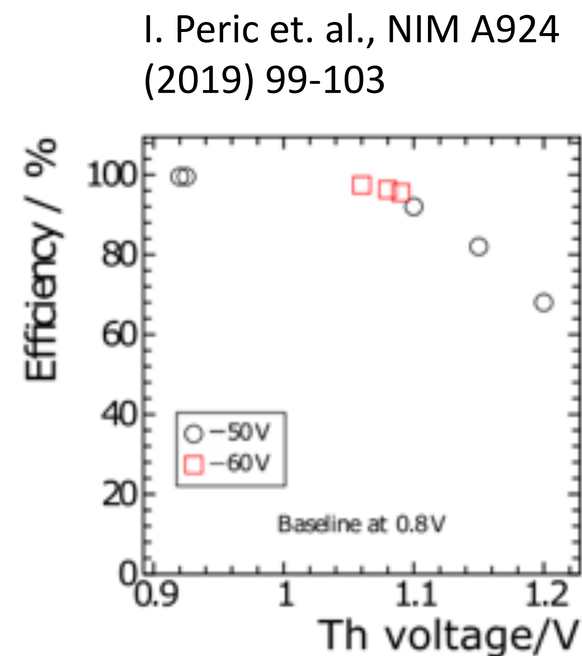
S. Coli, Forum on Tracking Detector Mechanics 2018, Valencia

Sensor proposal: ATLASPix

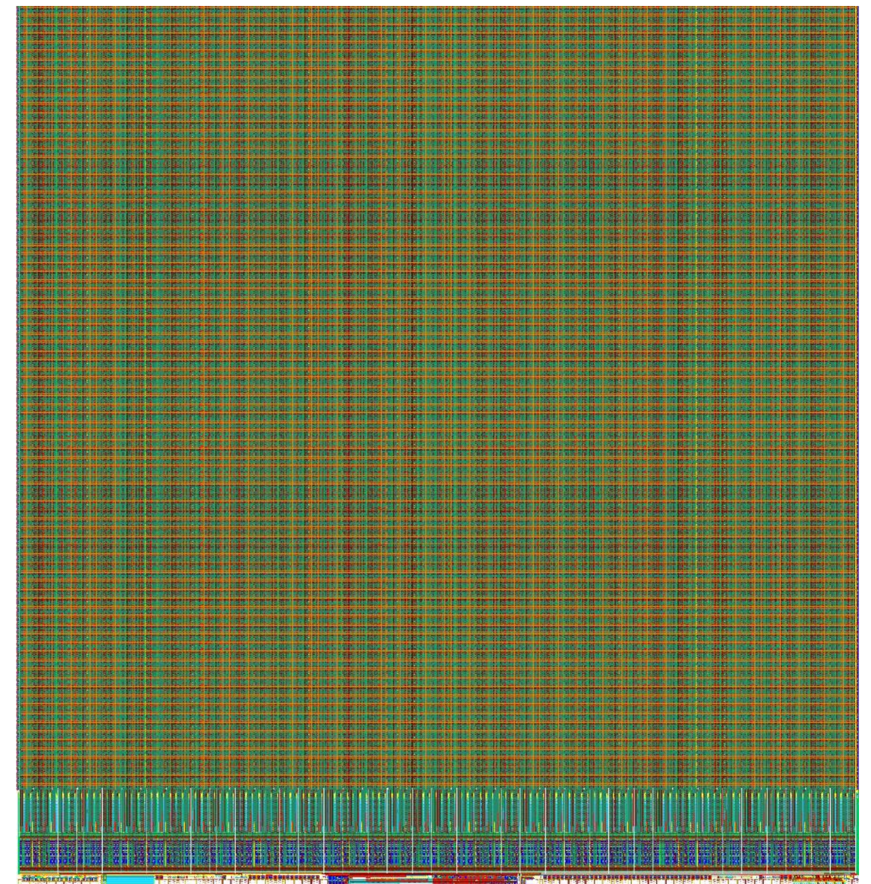
ATLASPix is a CMOS sensor developed to fulfil the requirements for the ATLAS upgrade

- Not strictly an ATLAS development
- **Monolithic CMOS** allows to produce **large** areas **fast** and **cheap**
- No hybridisation – wirebonds or C4NP bumps possible
- **25ns timing** compliant
- Hit efficiency 99.5% (ATLASPix1)
- Pixel size **150 µm by 50 µm** (or smaller)
- Triggered or triggerless readout possible
- 1.28 GBit/s downlink

I. Peric et. al., NIM A924 (2019) 99-103



ATLASPix3



ATLASPix3

- Reticule size: **2.02 cm by 2.1 cm**
- Full-size sensor, ATLASPix3 (TSI, 200Ωcm, 180nm) **just delivered**
- 132 columns with 150µm pixel
- One column contains 372 pixels, a configuration register block, 372 hit buffers, 80 trigger buffers and two **end of column (EoC) blocks**. EoC1 is attached to hit buffers and EoC2 to trigger buffers.

ATLASPix3: First measurements

Sensor:

Chip powered during measurement.

Low leakage current of < 50 nA @ -20 V

Breakdown around -66 V

- There are ideas how this could be increased if necessary.

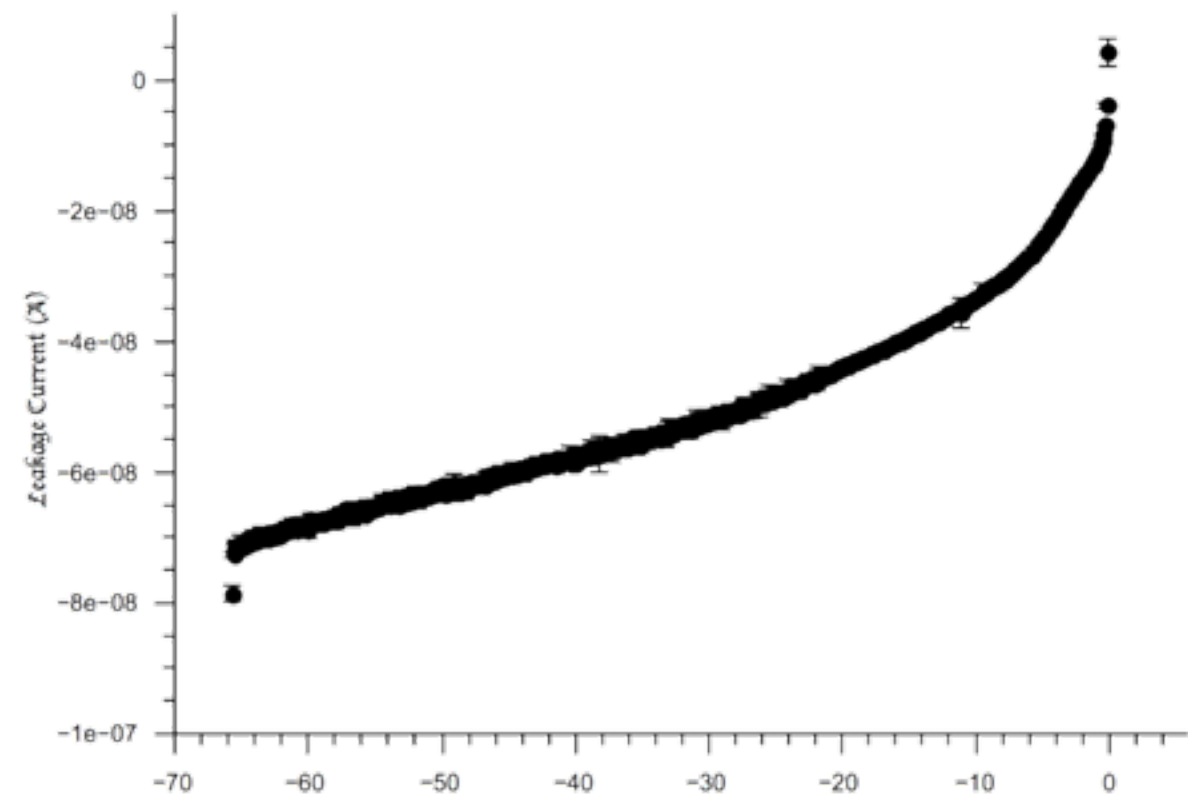
Configuration and Readout:

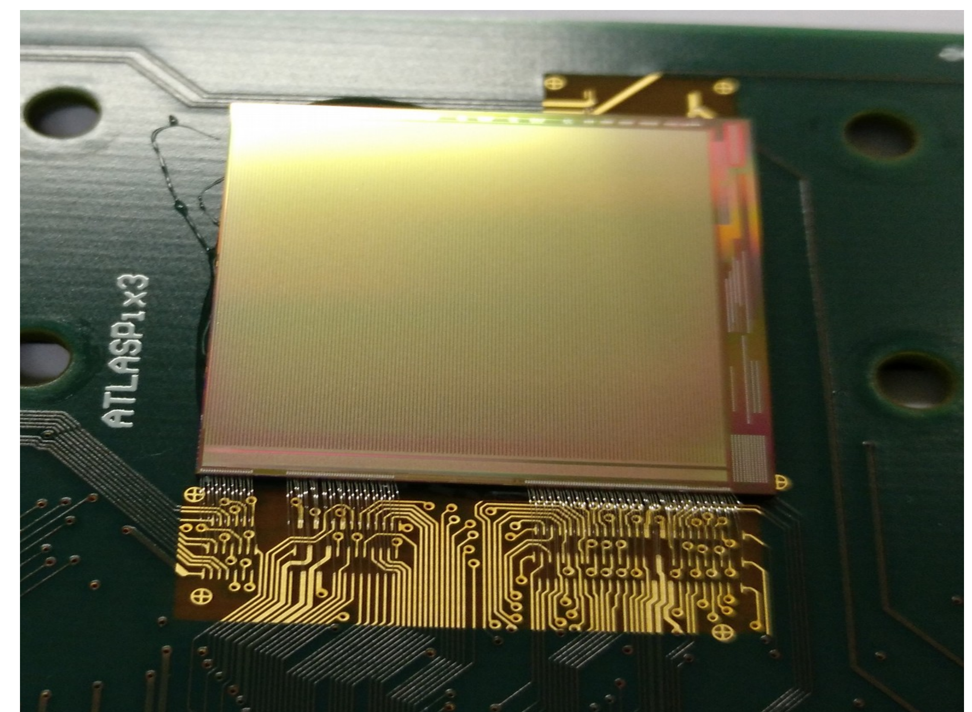
SPI (Serial Peripheral Interface in, out, clock, select) configuration tested to work

RAM writing is working

Untriggered **readout** tested to work at 400 Mbps (DDR, results in 25 ns time stamp)

To do: High speed link (data-clock-in, data-out) at full speed for e.g. YARR; Triggered readout; Command decoder; Clock recovery



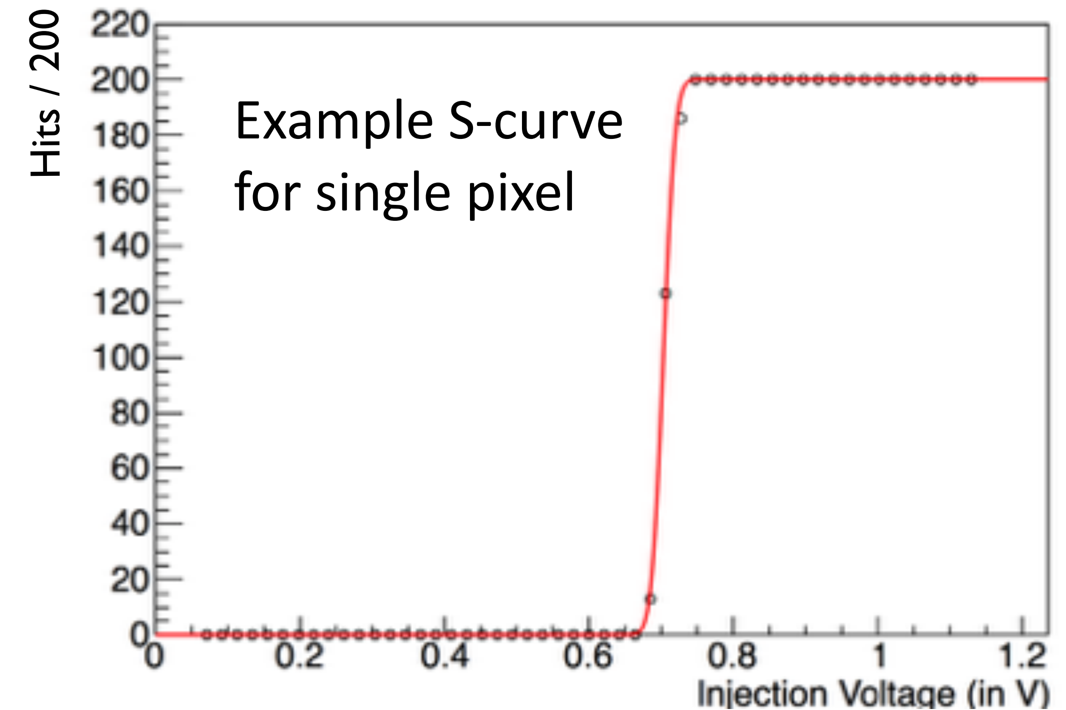


Threshold and Noise

Charge of increasing strength **injected** into the pixels

Fraction of detected signals measured

Shifted and scaled **step function convoluted with a Gauss is fitted** to the data points

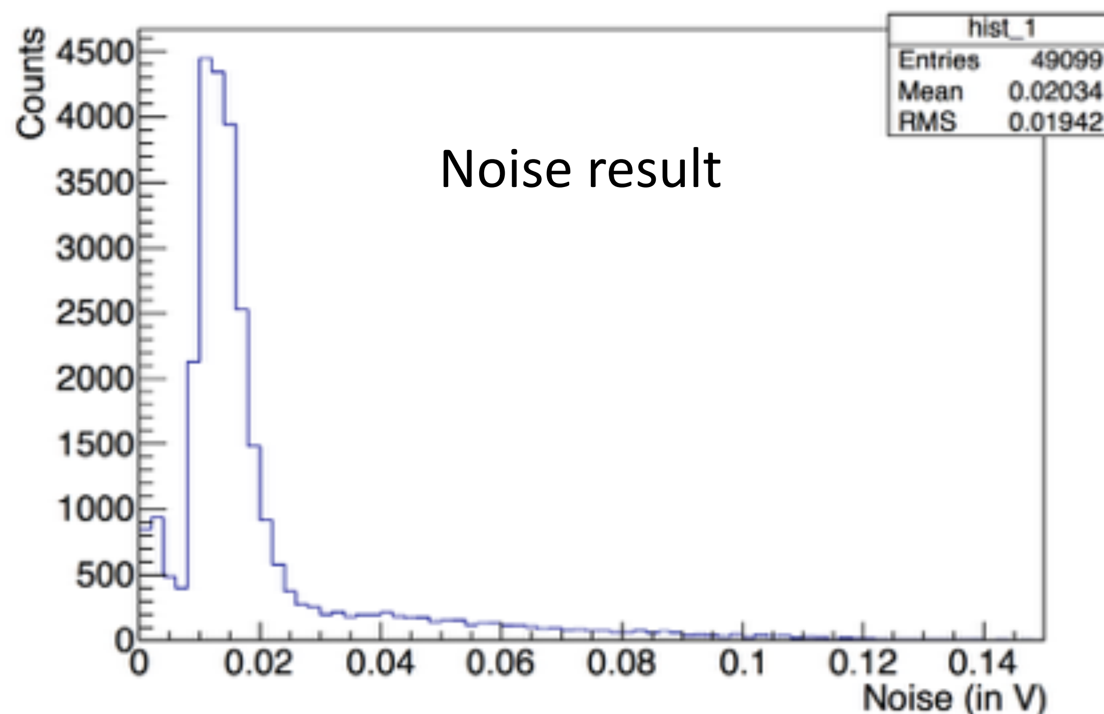


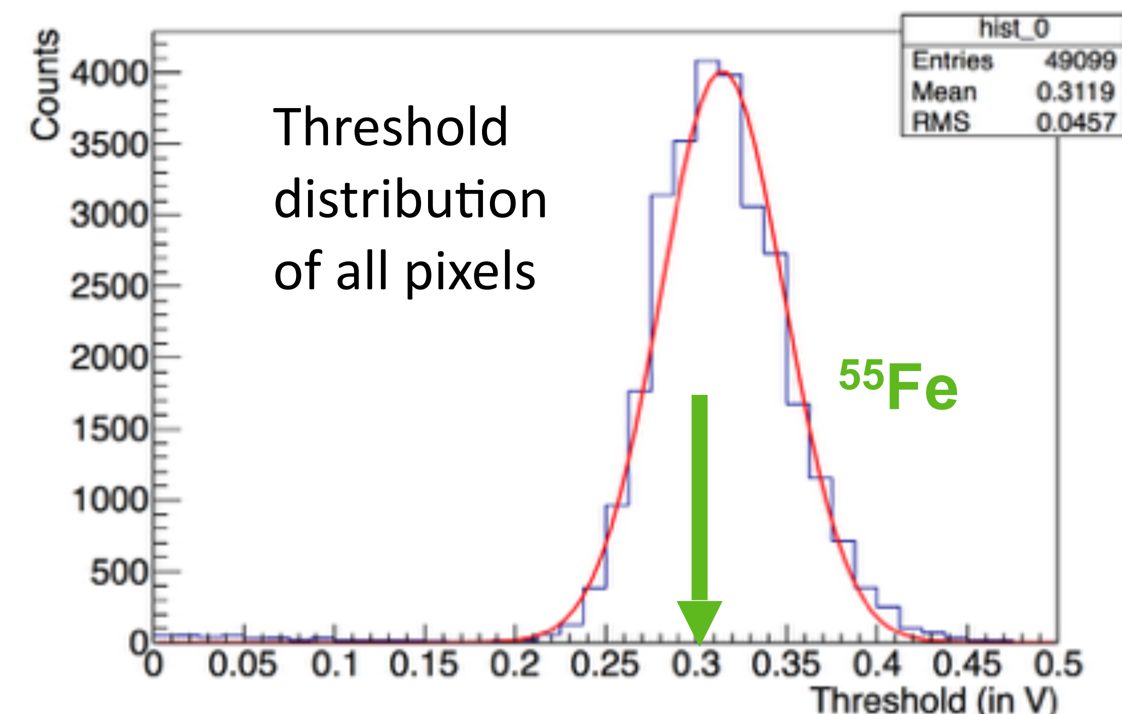
Using un-triggered digital readout, a **threshold scan** was performed for the whole matrix

Untuned matrix, GDAC setting

^{55}Fe signal equals a charge injection of about **300mV** (measured on this sensor)

1 σ noise value corresponds to **80 e$^-$**



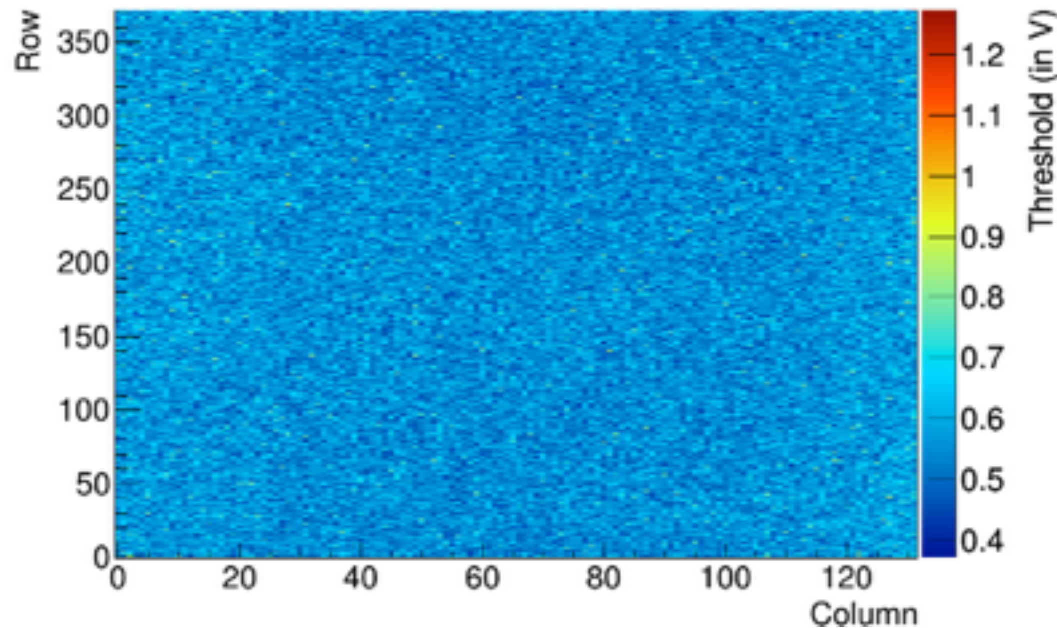


H. Fox

Tuning of Pixel Matrix

Threshold map, untuned sensor

All 49104 pixels work !



Each pixel contains a **3 bit tuning DAC (TDAC)** and a disable bit

Writing of the pixel memories is working and the detection **threshold changes linearly** with the TDAC setting

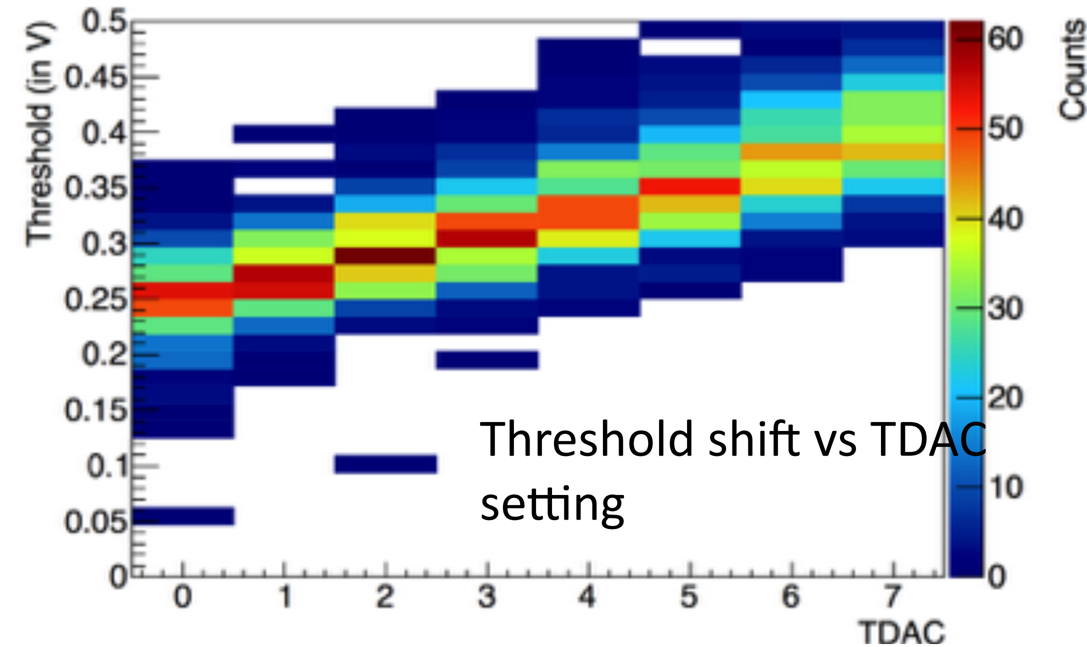
Threshold tuning:

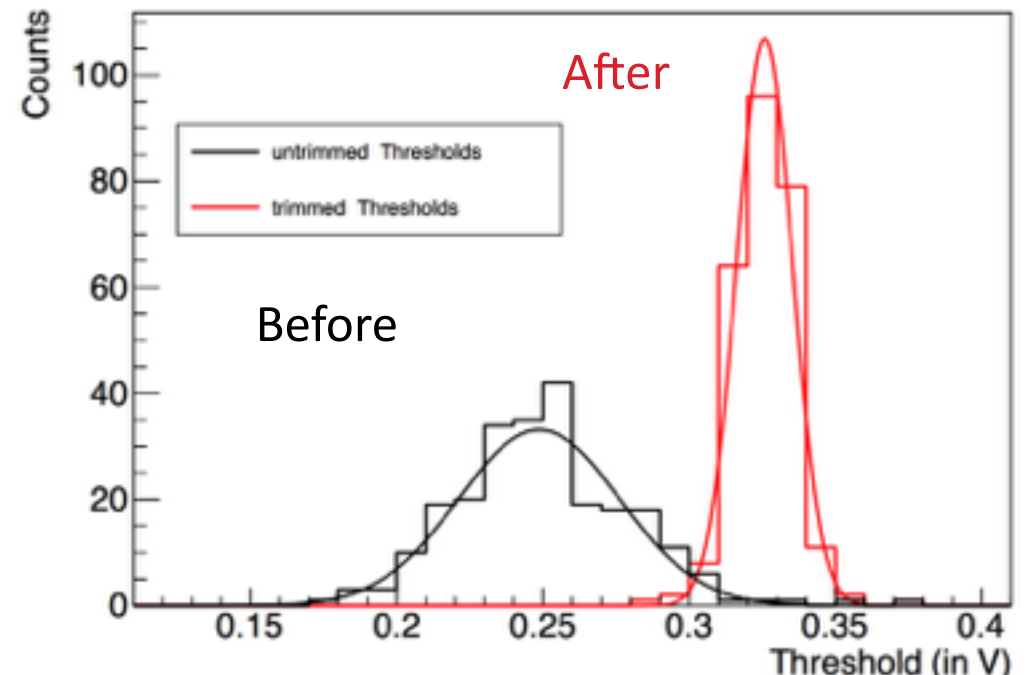
Detection thresholds are adjusted to **μ+3σ of untuned** distribution

Subset: conducted for 2 rows (in total 264 pixels):

Distribution width ~3× smaller

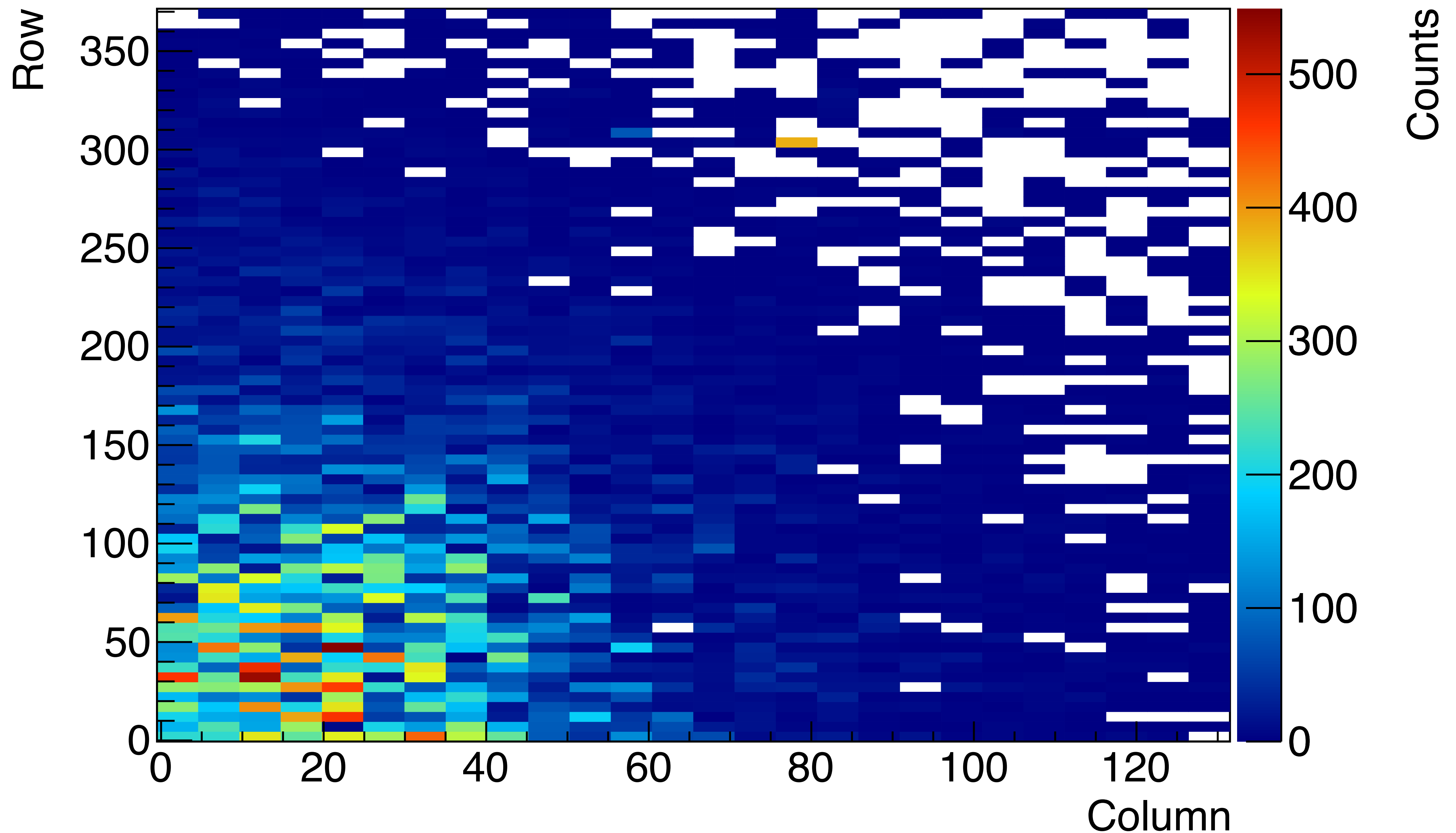
$\sigma_{trimmed}$ = 9.5mV ↔ ~ 50 e^{-}





Signal Detection

A ^{55}**Fe source** was held over the corner of an ATLASPix3 sensor.



Chinese Foundry?

Physics | Lancaster University

SMIC MPW Shuttle Schedule

MPW Notice To serve all customers smoothly, following items must be noticed:

1. Only standard Process/Layers products can attend MPW. No bumping, No Bank and No Corner Split allowed.
2. On one shuttle, 4 seats (including sub-chip in one seat) are the maximum that one customer can get.
3. **MPW only provides 50 dies for function verification.**
4. Shuttles are subject to cancellation if there are not enough passengers on board.
5. Without completion of below items before shuttle start date, shuttle reservation will not be held!

*Quotation should be ready/ DRC must be clean/ SMIC IP merge case must be closed (related information need to be submitted at least 3 days before shuttle start date)
*GDSII and tape out forms all need to be Approved by mask shop/ PTOS should be Approved

6. SMIC dicing size limit: 1500um < X < 12000um, 1500um < Y < 12000um.
7. For 300mm shuttle, suggest use metal scheme condition: 6(M1-M6)+TM1(9kA)+TM2(9kA)+14.5kA ALPA+12mil BG.
8. Overdue MPW booked cases will be cancelled within 90 days after shuttle start.

Tech Node	IO Voltage/Tech Type/Char	RF	2020 MPW Booking Cut-Off Date											
			Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
14nm	IO=1.8V CMOS Logic (GE|GP)				10 Q67 (Fab8)			9 Q6P (Fab8)			8 Q6Z (Fab8)			8 Q7C (Fab8)
28nm	IO=1.8V | IO=2.5V CMOS Logic (HP)	Y			3 Q6D (Fab2)			2 Q6Q (Fab2)			1 Q6Y (Fab2)			
	IO=2.5V CMOS Logic (LL|UP)	Y												
40nm	IO=8/32V CMOS High Voltage (HV)			4 Q69 (Fab2)			5 Q6K (Fab2)		7 Q6T (Fab2)			13 Q73 (Fab2)		1 Q79 (Fab2)
	IO=1.8V| IO=2.5V Adv. Emb-Flash (Cu-BEOL with AL-TM2 + RDL process) (LL)							23 Q6R (Fab2)						15 Q7B (Fab2)
	IO=2.5/5V | IO=2.5V Adv. Emb-Flash (Cu-BEOL) (LL)						12 Q6M (Fab2)						10 Q77 (Fab2)	
55nm	IO=1.8/2.5V | IO=1.8V| IO=2.5V CMOS Logic (LL)	Y												
	IO=6/32V | IO=8/32V CMOS High Voltage (HV) Do not support 2XTM(STM)			11 Q6C (Fab2)		7 Q6G (Fab2)			14 Q6U (Fab2)			20 Q74 (Fab2)		
0.11um	IO=3.3V Adv. Emb-Super flash (AL-BEOL) (LL)										8 Q70 (Fab1)			
0.13um	IO=3.3/5V| IO=5V Adv. Emb-EEPROM (Cu-BEOL) (LL)									4 Q6V (Fab1)				
0.11/0.13um	IO=3.3V CMOS Logic (GE)|Mixed Signal (GE)	Y		4 Q6B (Fab1)		14 Q6H (Fab1)		30 Q6S (Fab1)		11 Q6W (Fab1)		27 Q75 (Fab1)		29 Q7D (Fab1)
0.153um	IO=3.3V CMOS Logic (GE)|Mixed Signal (GE)	Y								18 Q6X (Fab1)				
0.18um	IO=5/6/9/12/16/20/24/30/35/40 BCD V3E (EP)				3 Q6E (Fab1)						15 Q71 (Fab7)			
0.18um	IO=3.3V CMOS Logic (GE)|Mixed Signal (GE)	Y	1 Q68 (Fab1)				19 Q6N (Fab1)				15 Q72 (Fab1)			
	IO=3.3V CMOS Logic (GE)|Mixed Signal (GE) IO=5/10/12/20/35/40V BCDM (BCDM do not support RF)	Y			10 Q6F (Fab7)				21 Q6J (Fab7)				17 Q78 (Fab7)	
	IO=3.3/5V| IO=5V EEPROM Embedded (GE)					14 Q6L (Fab1)						27 Q76 (Fab7)		

* 2020 new offered feature: 40nm EF/0.11um EF

Version: 1.1 Update Date: 2019-10-15

Note: Please login SMIC-Now to find the most updated MPW schedule. (请登录Smic-Now以查阅最新MPW Schedule.)

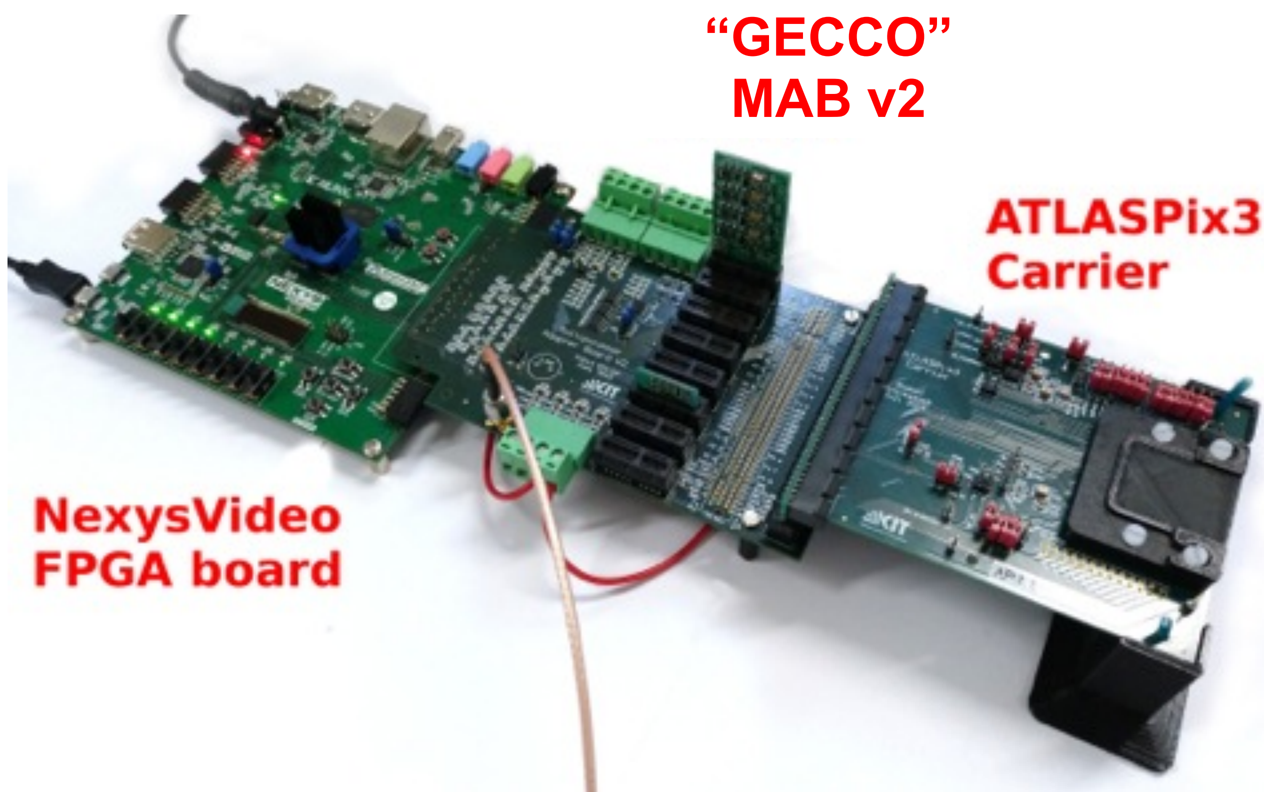
Module Flex

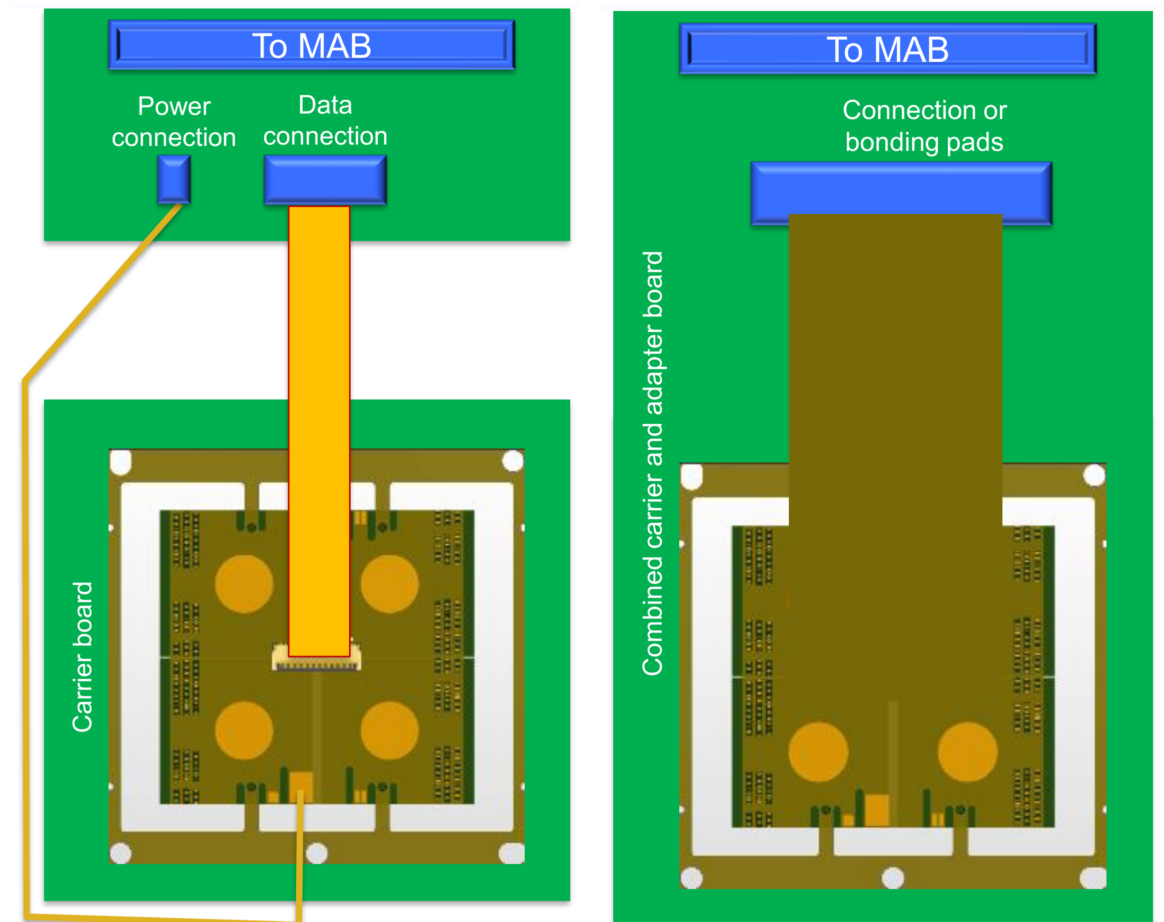
Università and INFN di Milano: Attilio Andreazza, Mauro Citterio, Fabrizio Sabatini

Purpose is to build a **pseudo-quad module** for ATLAS
Test system functionality for large size detectors

Starting point is the **ATLASPix3 single-chip card** produced by KIT and used for the tests

Two basic ideas:
- Connector
- Integrated Pigtail





DAQ: YARR
Yet Another Rapid Readout

https://iopscience.iop.org/article/10.1088/1742-6596/898/3/032053

YARR is a small **self-contained DAQ system**.

Linux PC with a x4 **PCIe slot for the FPGA card**

FPGA card: e.g. **Trenz TEF1001**, XpressK7,...

FMC cards for FE-I4 and RD53A

Up to **1.6GBit/s possible** with this setup.

We have used the YARR readout with a digital RD53A module in **Lancaster & Edinburgh**.

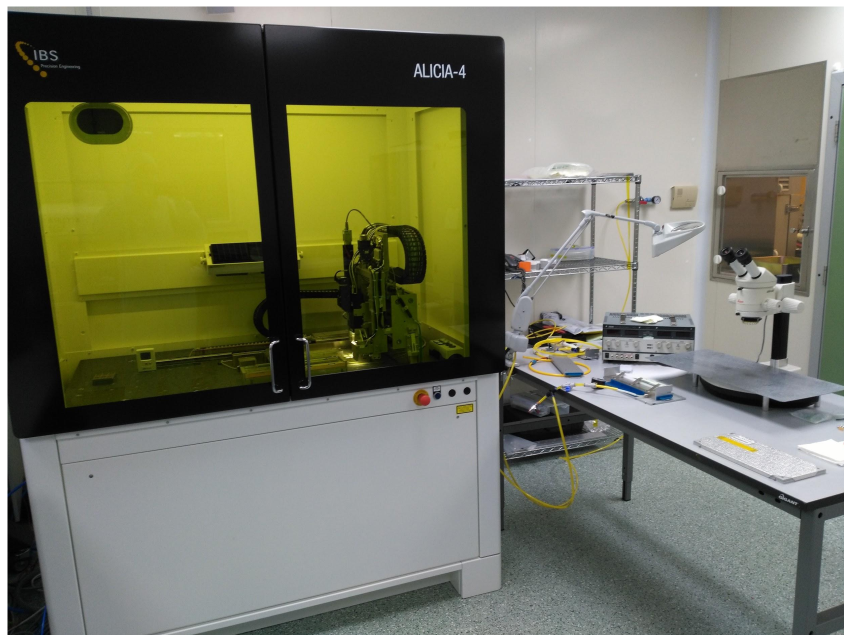
Todo: Adaptation to ATLASPix3 necessary:

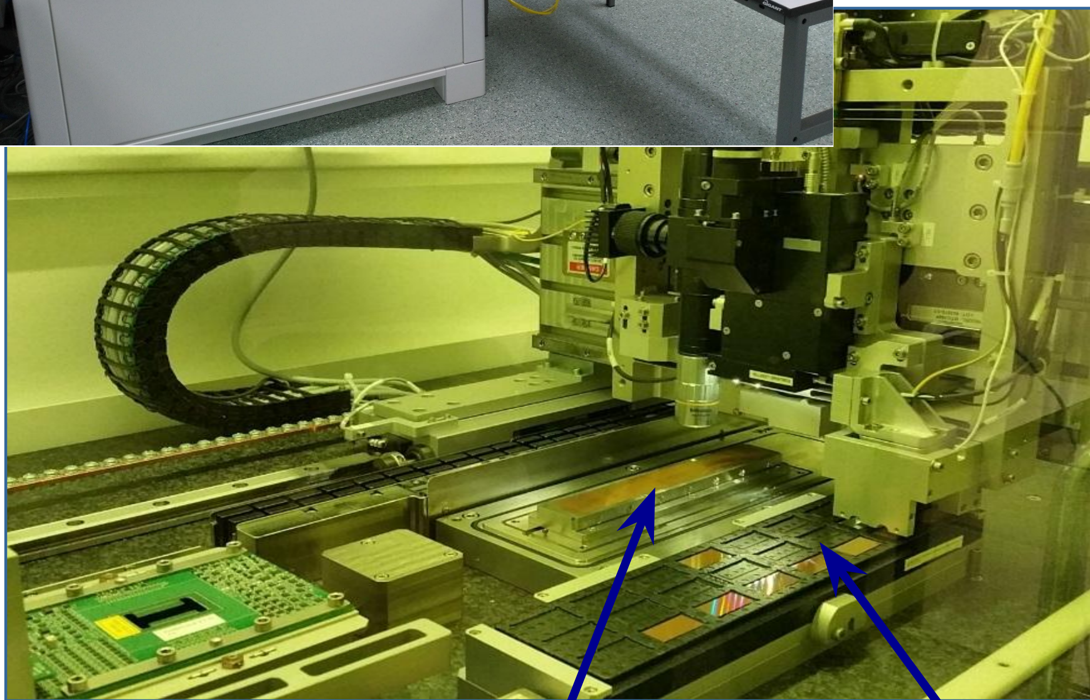
- **FMC**
- **Software**

ALICE: Outer Barrel Module Assembly

Liverpool (Prof. Marielle Chartier) with Daresbury are responsible for the **construction of 500 modules** (incl. spares) for the **Outer Layers** (until early 2019).

In partnership with Bari (IT), Strasbourg (FR), Pusan (KR), **Wuhan (CN)**.
Production in the Liverpool Semiconductor Detector Centre **finished**.

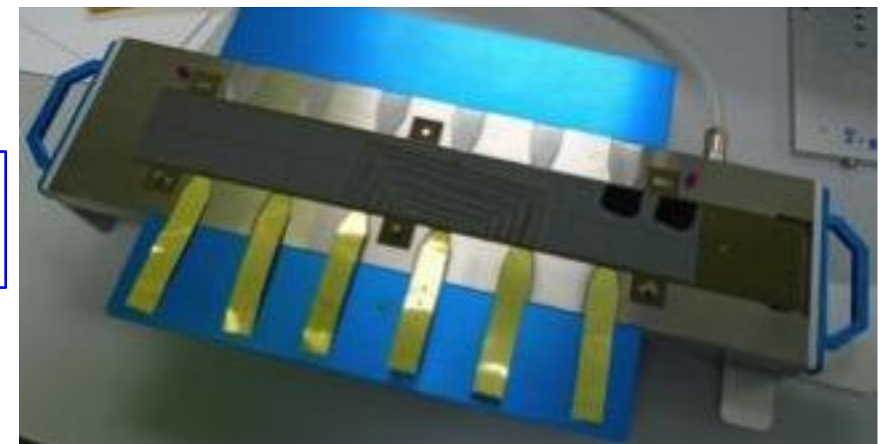




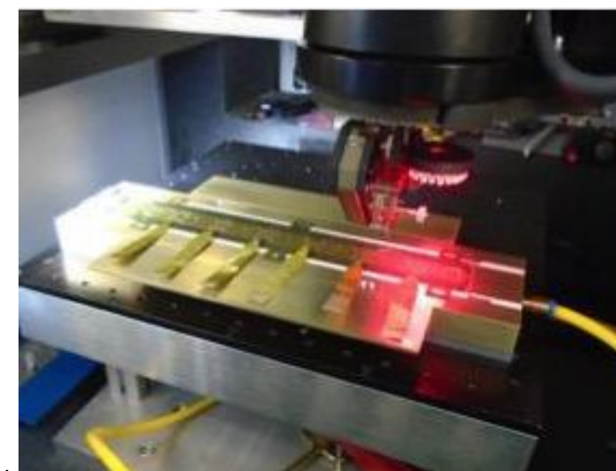
Assembly Table | Chip Tray

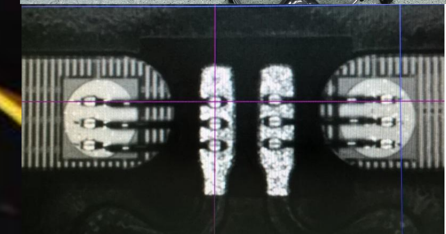
6 machines distributed to different construction sites

Sensor side (Outer Barrel)



Electrical Interconnection (wire bonding)



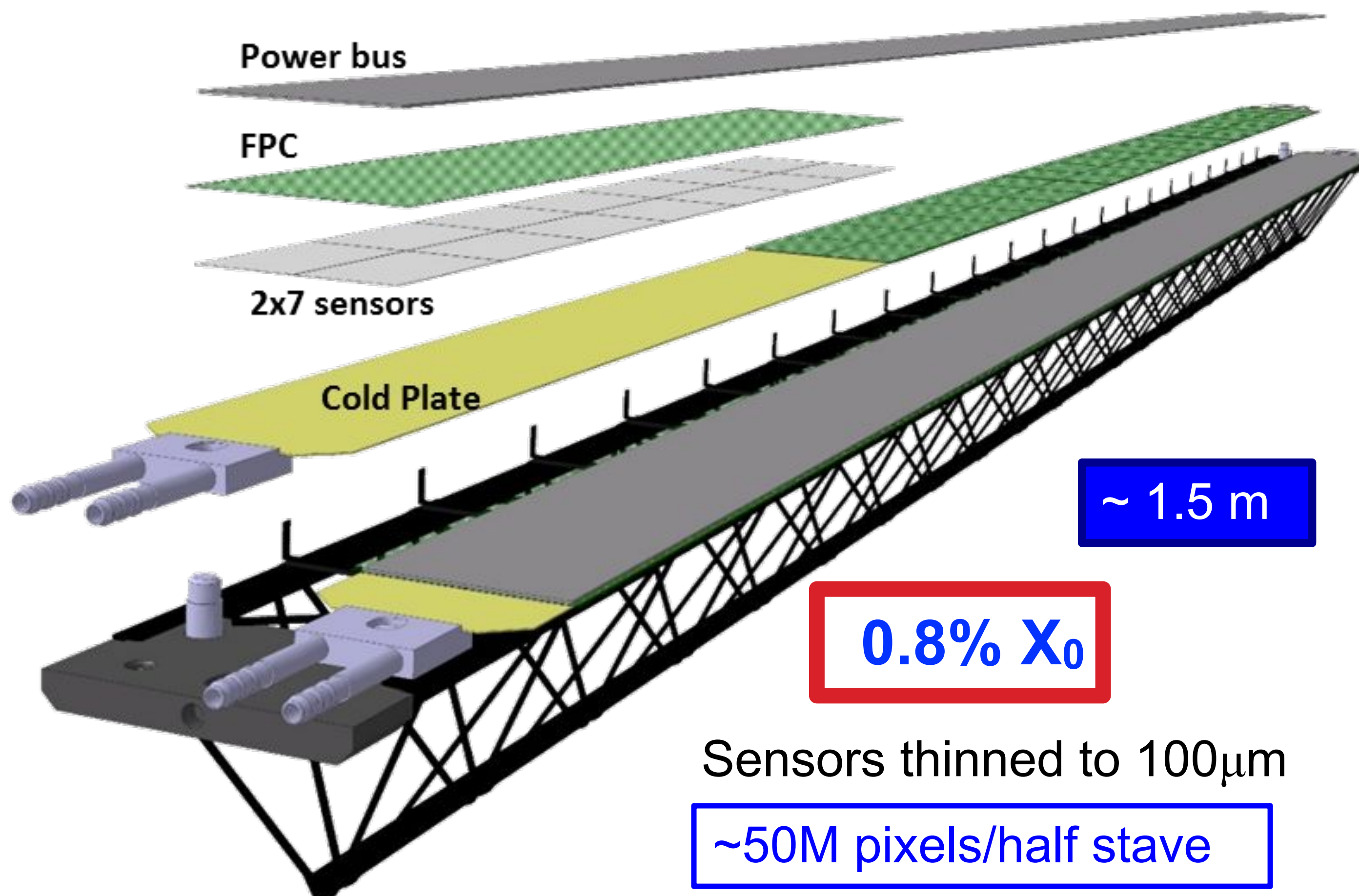


ALICE: Outer Barrel Stave Assembly

Physics | Lancaster University

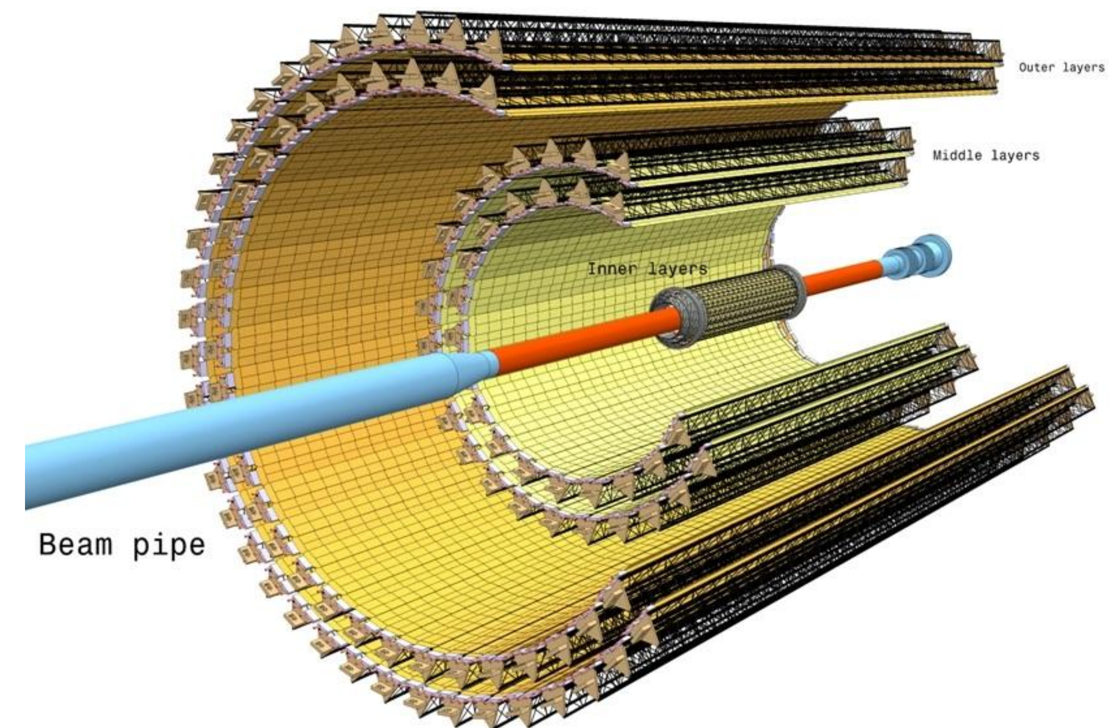
Daresbury is responsible for the **construction of 22 Staves for the Outer Layers**.

Production in the Engineering Technology Centre **finished** well within time this year.
In partnership with Torino & Frascati (IT), NIKHEF (NL), Berkeley (USA).



Sensors thinned to 100μm

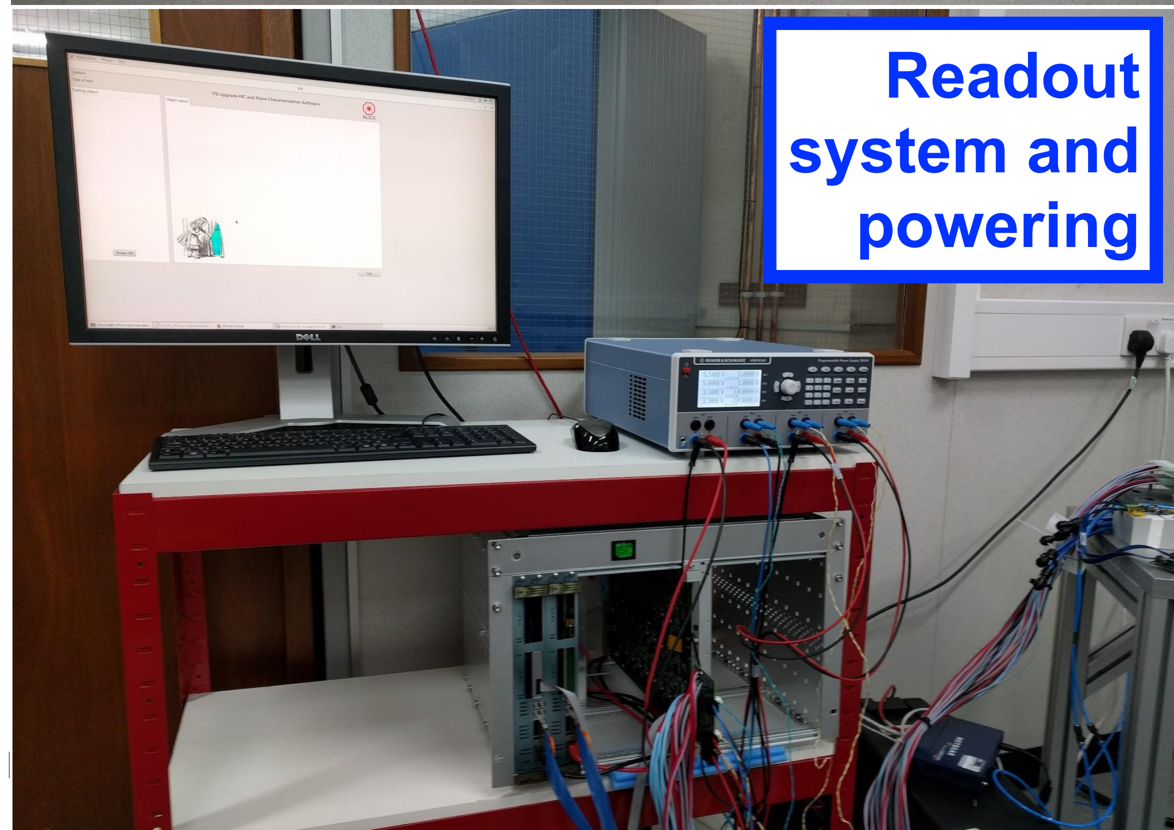
~50M pixels/half stave

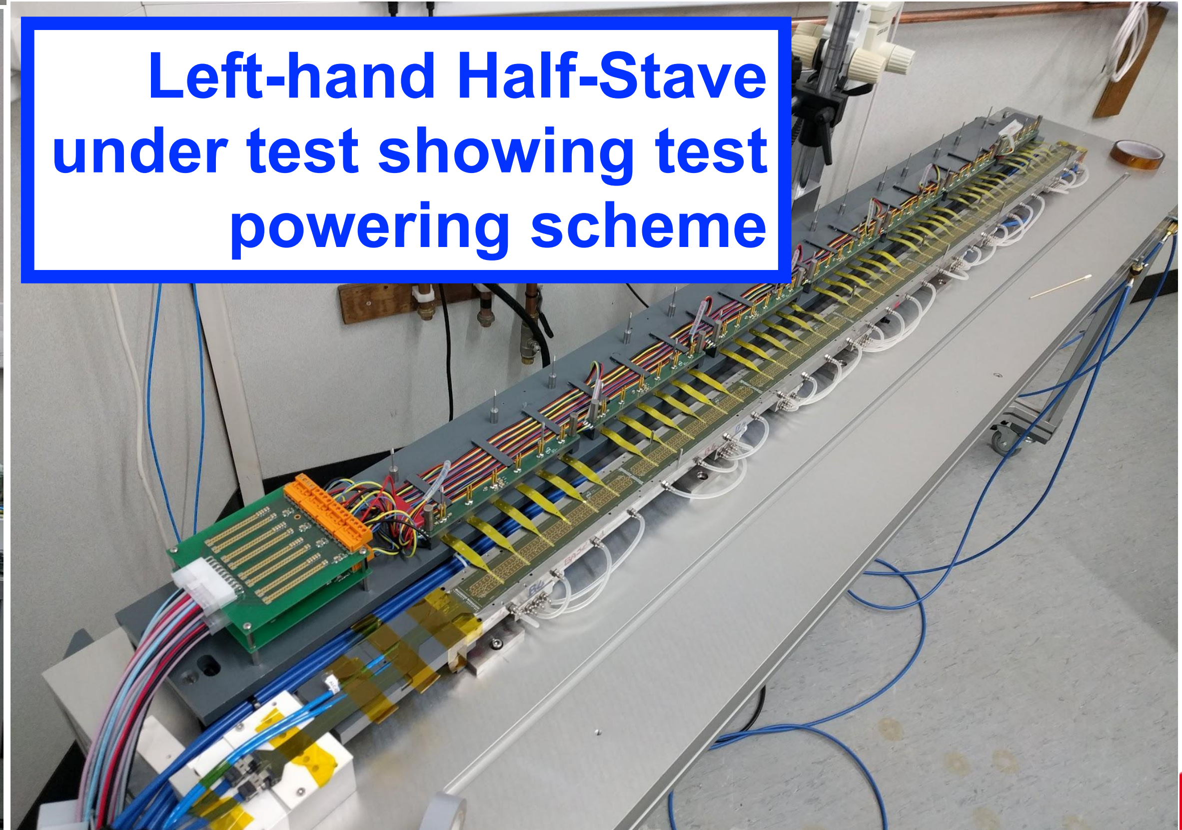


- 7 layers; 3 (IL), 2 (ML), 2(OL)
- 192 staves; 48 (IL), 54 (ML), 90 (OL)

ALICE: Stave Assembly and Testing at Daresbury

Daresbury Engineering Technology Centre





Interested Groups in China

Several Chinese institutions have expressed interests in the CMOS out tracker concept, including

- IHEP & Tsinghua – sensor/module assembly & tests, on-going activities on ATLAS ITk-Strip and LHCb UT, JadePix design & characterization for CEPC
- USTC – readout electronics, e.g. FELIX for the ATLAS Phase II upgrade and more
- SDU – ASIC design, e.g. SUPix, and test system
- CCNU – module assembly, delivery of ALICE ITS modules
- … more

Explore the synergy with LHCb – "mighty" tracker, on which Chinese groups have expressed strong interests

Interested Groups in the UK: Bristol

Made significant contribution to the **TimePix3 telescope**

- Online **Data Quality monitoring**
- **Slow control** (HV & motor stages)

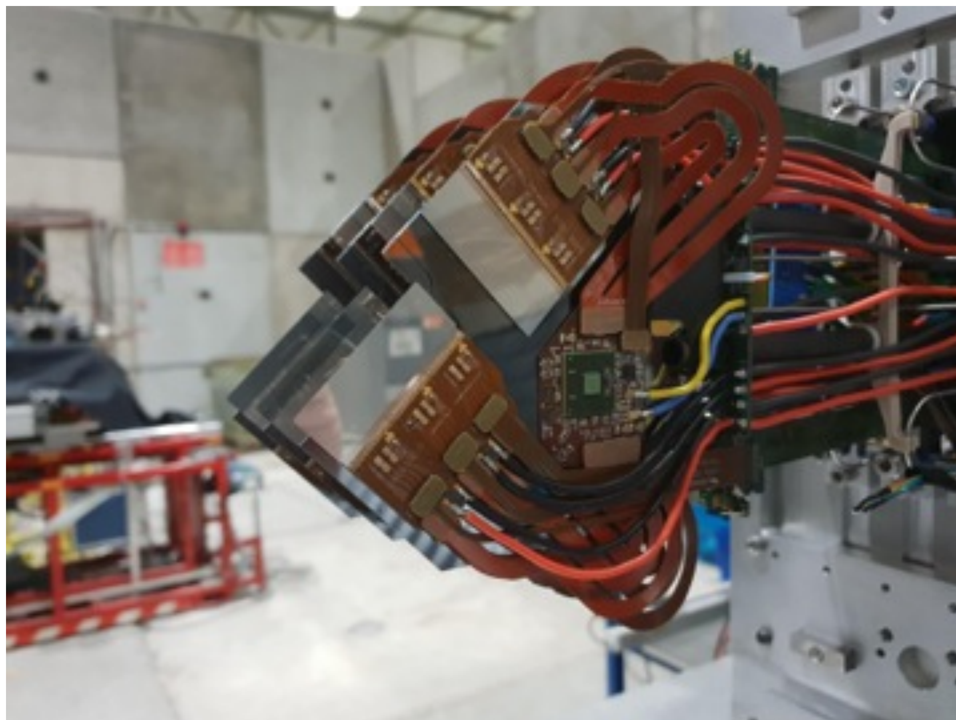
Did a large part of the **test beam** data analysis for the **Velo upgrade** modules

Did a large part of the **bench tests** for the **Velo upgrade modules**

Ran successful **test beam campaigns and bench tests** for **CMOS sensors** towards ILC (FORTIS, TPAC, ISIS, HEPAPS4)

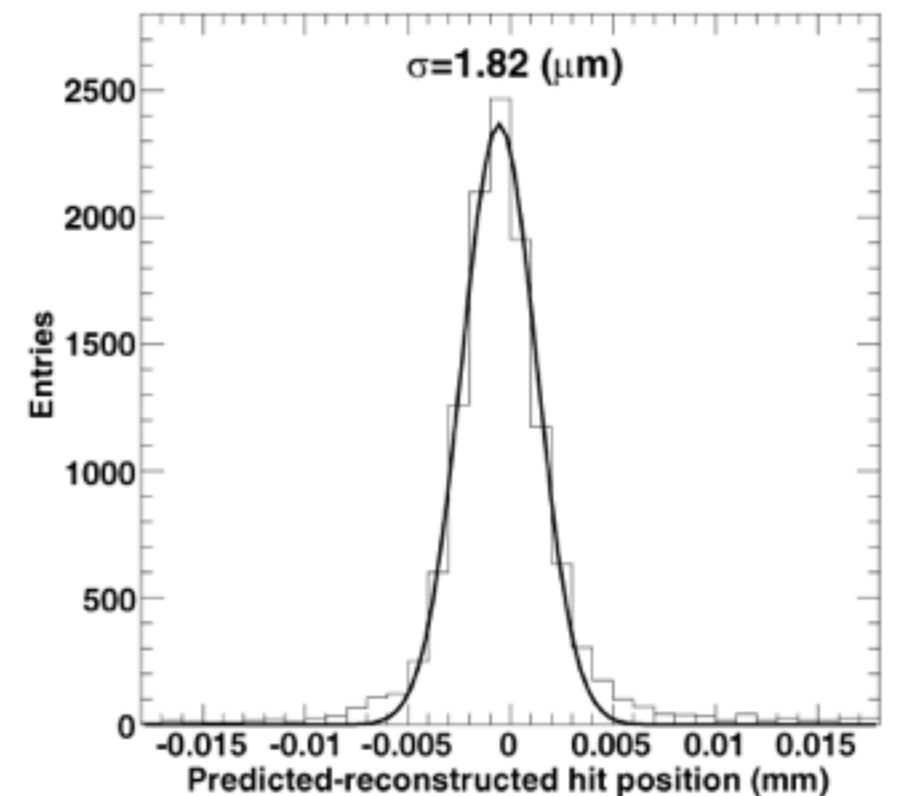
Built the **Aida Trigger Logic Unit**

Before performed testbeams with **DEPFET, ATLAS Diamond pixel sensors and 3D sensors**



VELO modules in a pre-commissioning testbed
LHCB, Oxford

Observed position resolution for DEPFET 4
J.J. Velthuis et al.,Trans. Nuc. Sc., 55, 2008

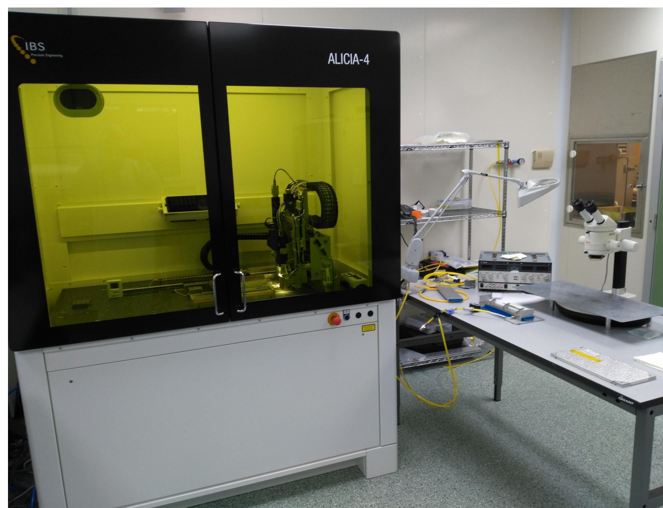


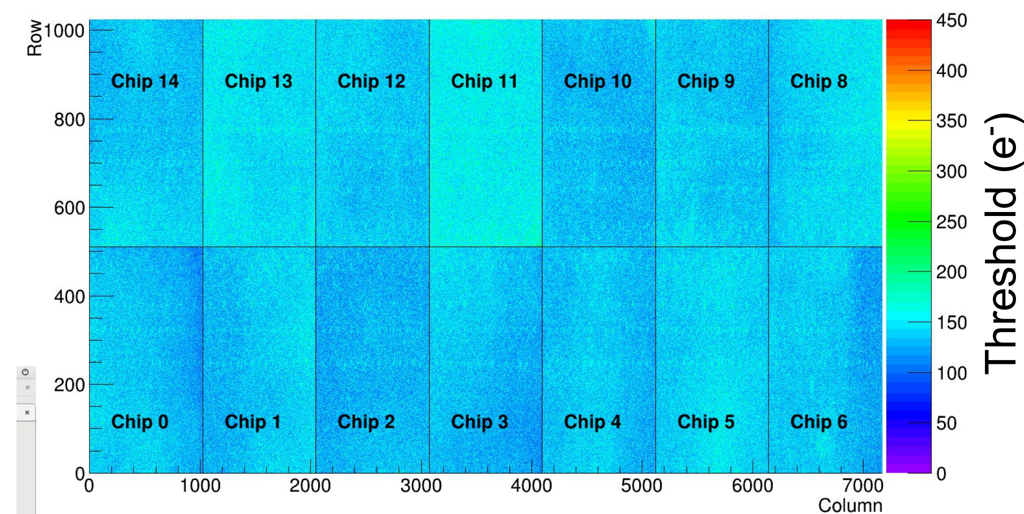
Interested Groups in the UK: Liverpool

The Liverpool **HV-CMOS work** includes generic development work for **RD50** as well as our involvement in the development of the **MuPix chips** for Mu3e and **AtlasPix** and work on HV-CMOS for medical applications. Currently, non of these have a particular focus on CEPC.

See **Tim Jones**' talk on **Light-weight Mechanics** in this session.

ALICE colleagues in Liverpool

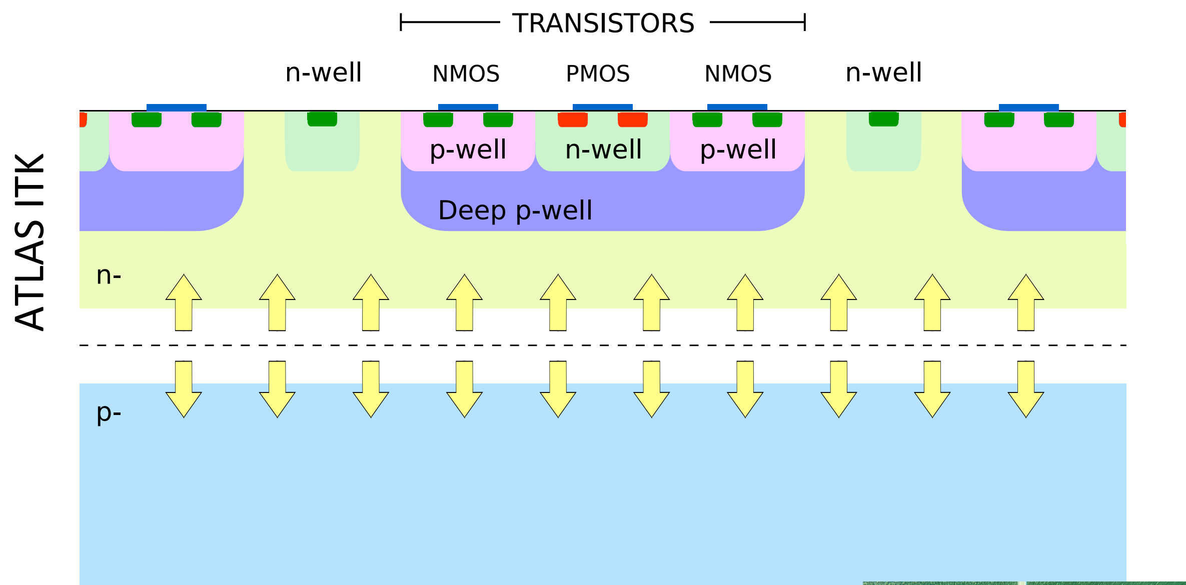




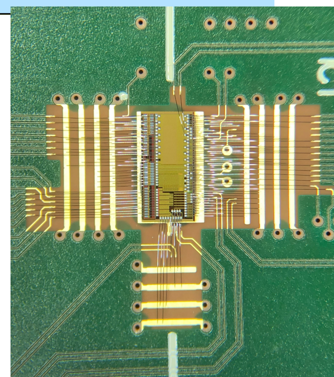
There is also **DAQ experience in the UK** with interest in **Bristol, RAL** (see **Jens Dopke's talk**) and **RHUL**.

TowerJazz 180 nm CMOS technology Oxford

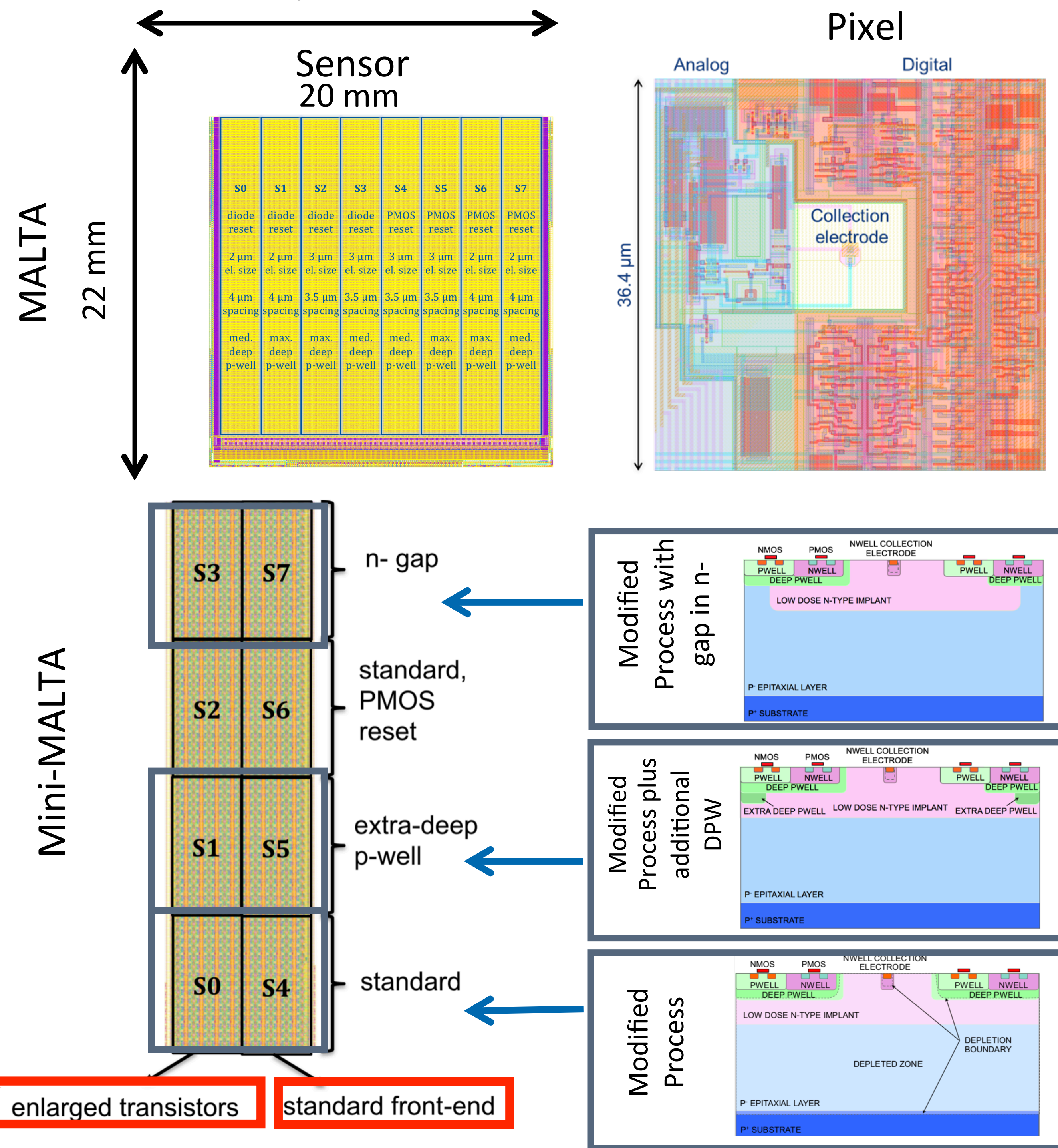
- Used in ALICE ITS
- Small collection electrode (3 μm^2) input capacitance (< 5 fF) ➠ high SNR
- Small depletion depth (~20 μm)
- Modified process to ensure full lateral depletion



- Mini-MALTA: Probing n-well gap and deeper p-well wafer process modifications



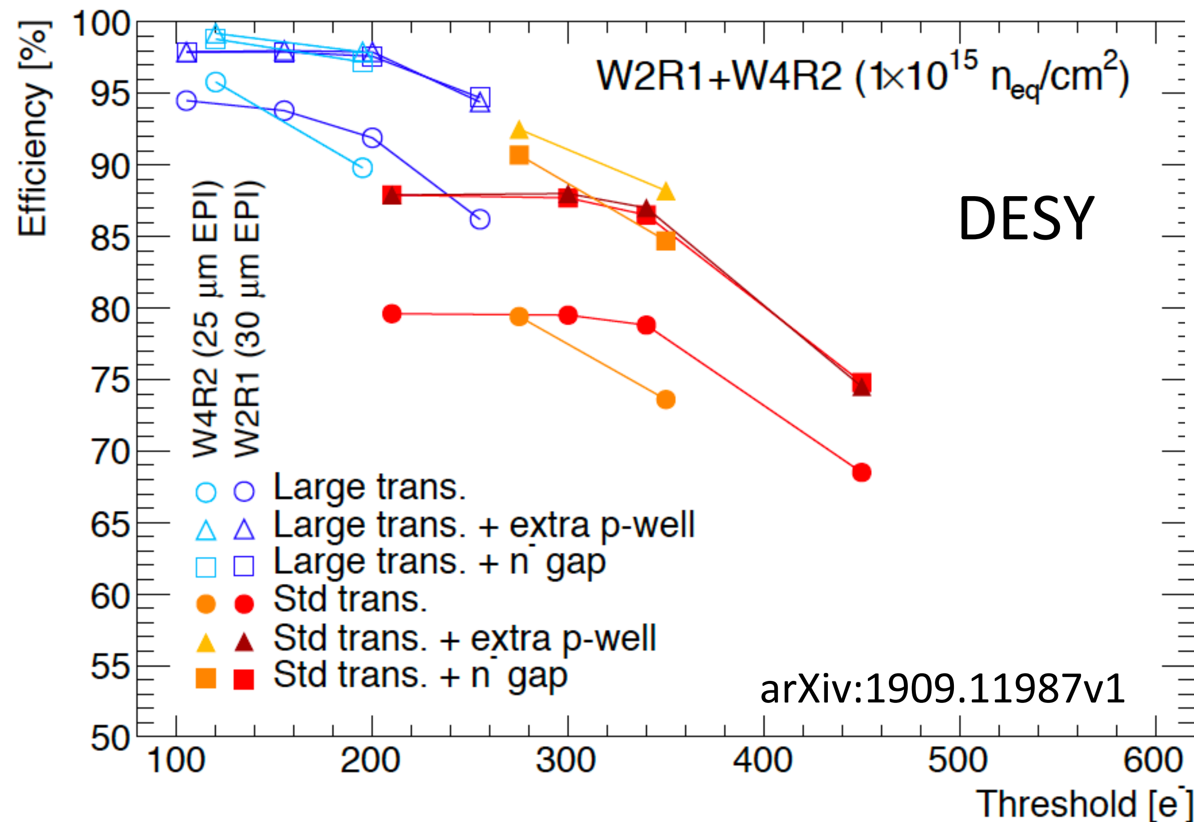
- MALTA: full demonstrator size sensor. Novel asynchronous readout architecture



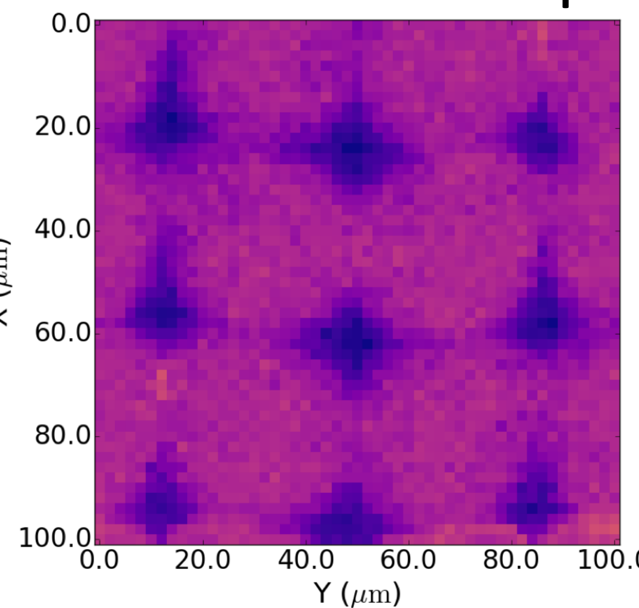
Sensor R&D and Future Plans Oxford

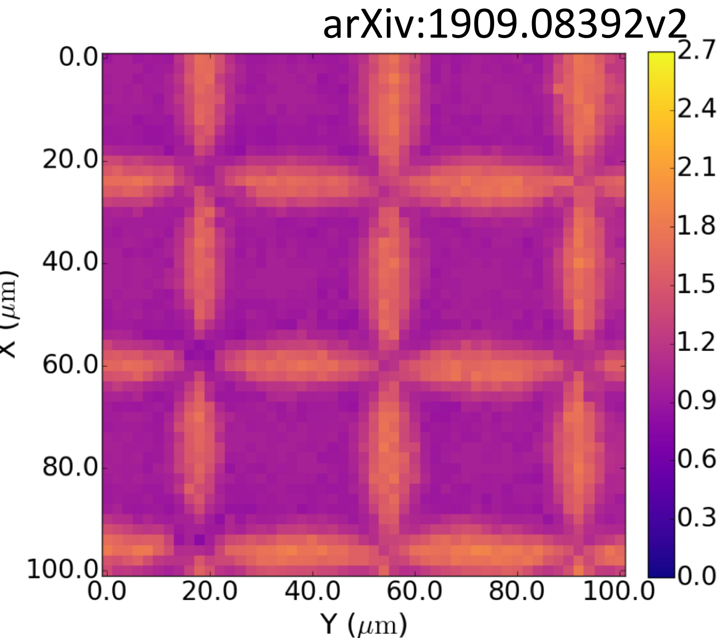
Characterisation measurements:
- I-V, Noise, Threshold, Gain, Source Response
- Test-beams at SPS, Diamond RAL, DESY & ELSA.

- X-Ray test beam measurements at Diamond Light Source with 2 µm beam spot



arXiv:1909.08392v2





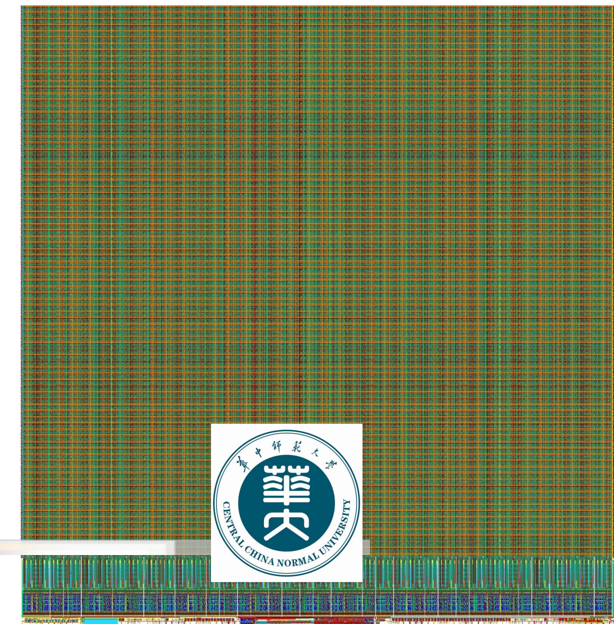
MALTA after 1e15 neq/cm²

miniMALTA n-gap after 1e15 neq/cm²

Plans:
- Engineering of new substrates (e.g.: Czochralski)
- new version of MALTA that will be aimed for testbeams, targeting the AIDA telescope framework

MALTA telescope in CERN SPS H6

Summary and Conclusion



Sensor:

Functional ATLASPix3 sensor available for prototyping

Optimisation for a (Chinese) e^+e^- collider

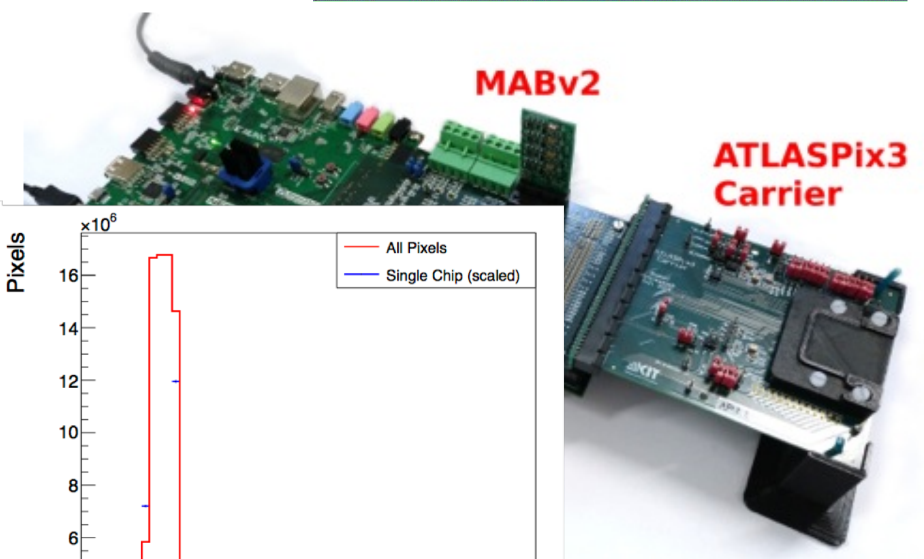
- Power consumption
- Investigate and work with Chinese foundry

Readout

Flex desi

New ada Pix3 needed

YARR (DA adapt



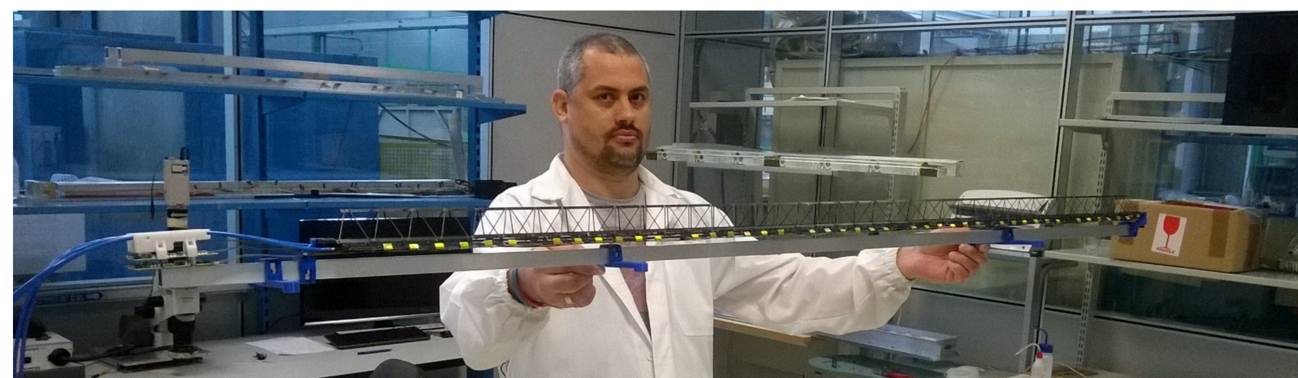
Staves:

Experien TLAS)

We need for th equirements

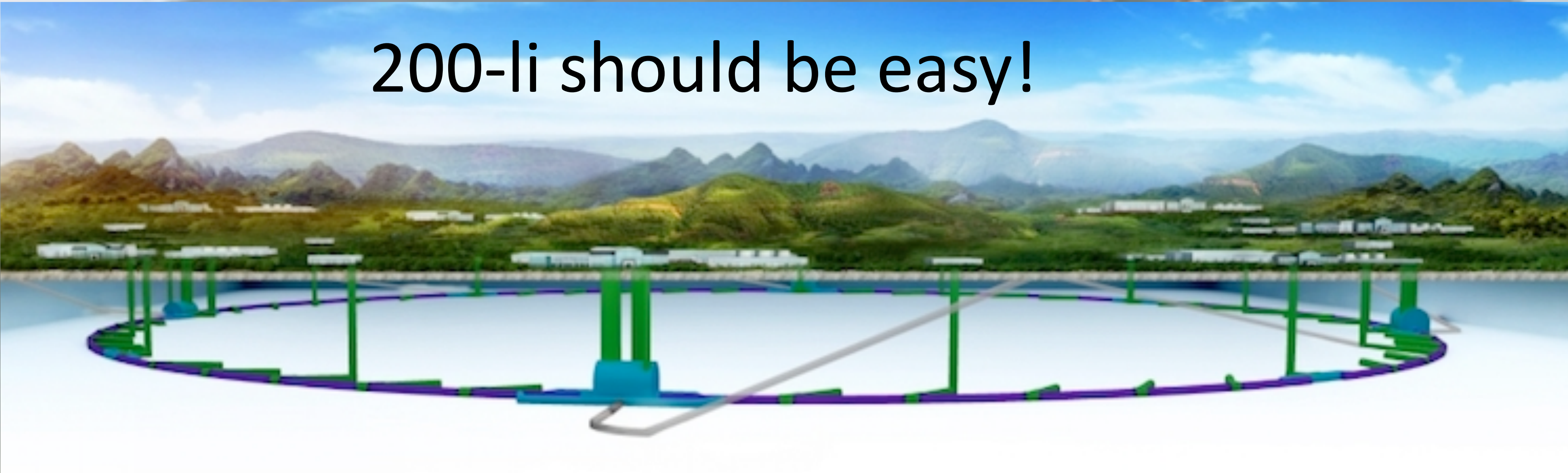
We have (Beiji supporting structure

ALICE stave at Daresbury



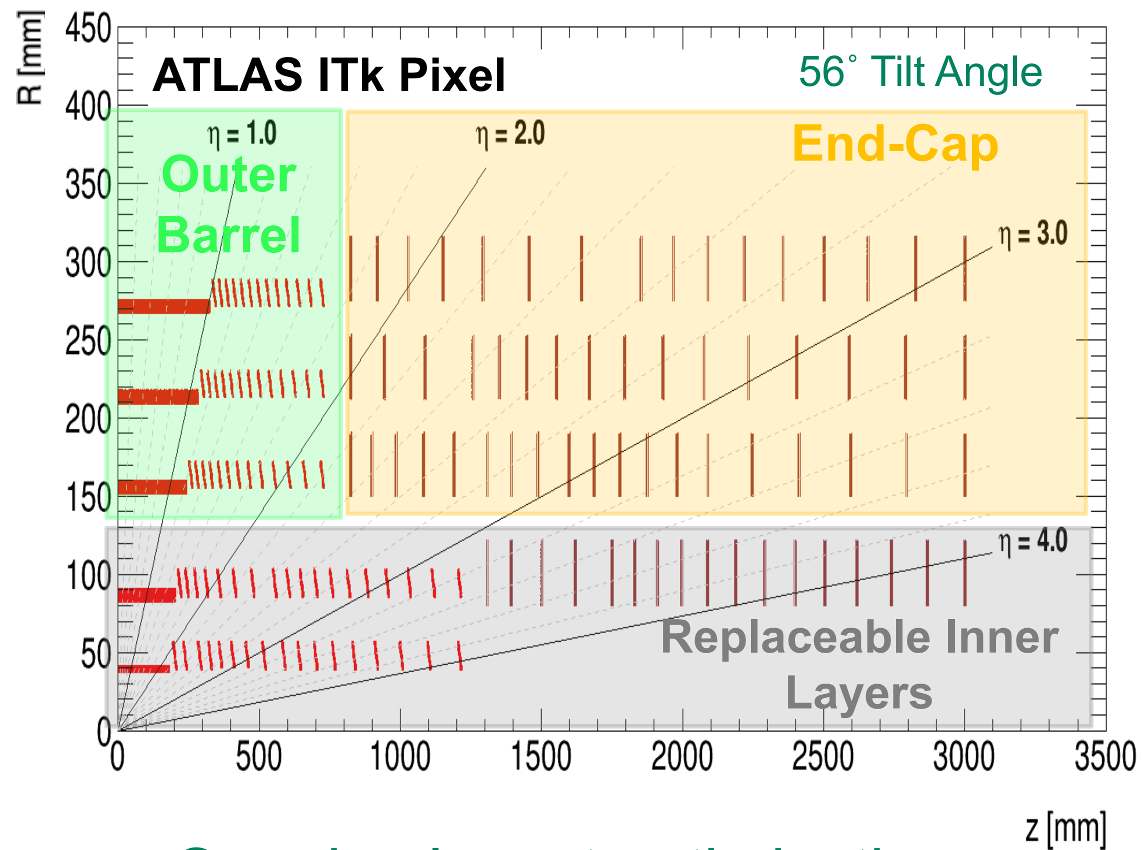
10000-li project

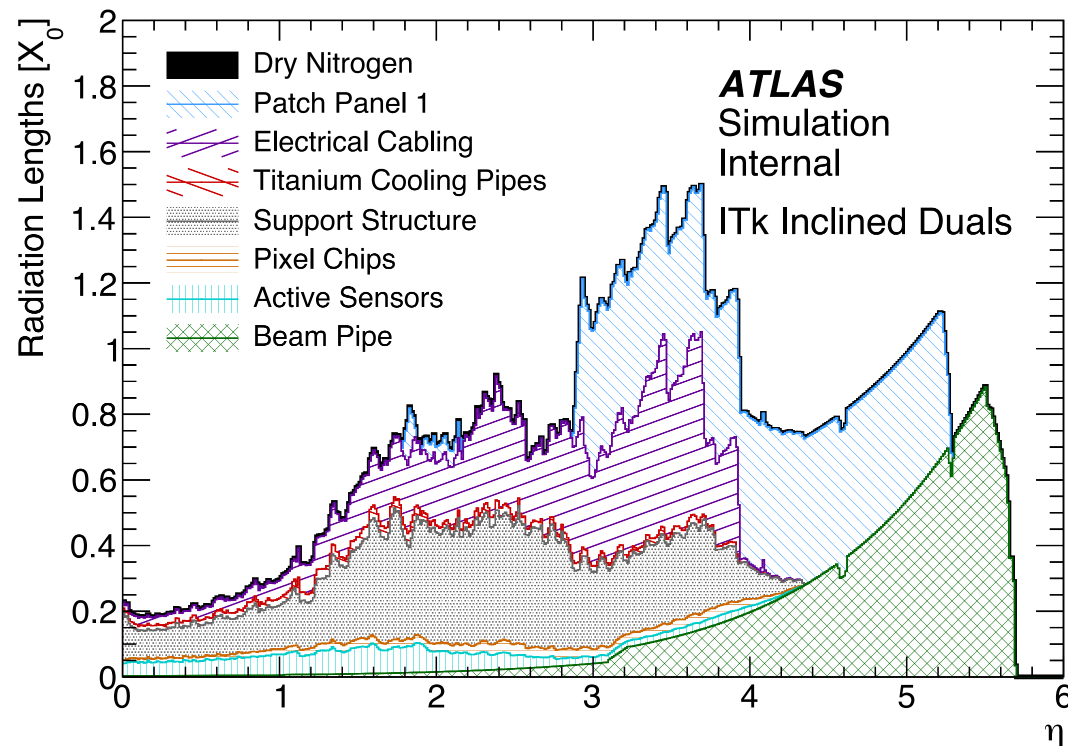
10000-li project



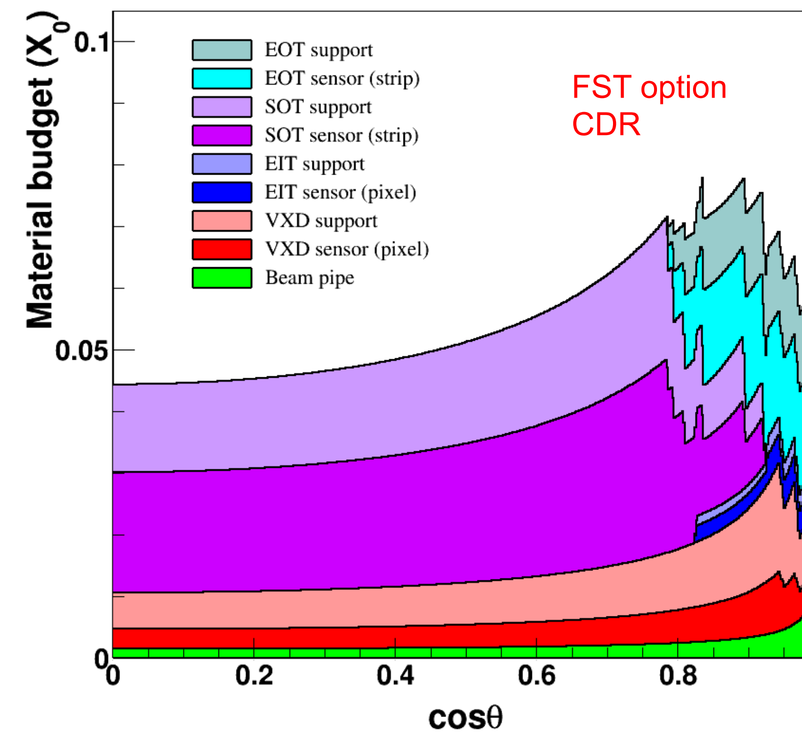
Backup

Backup: Radiation lengths X/X_0





CDR: FST: 5-7% FST2 7-10% X0



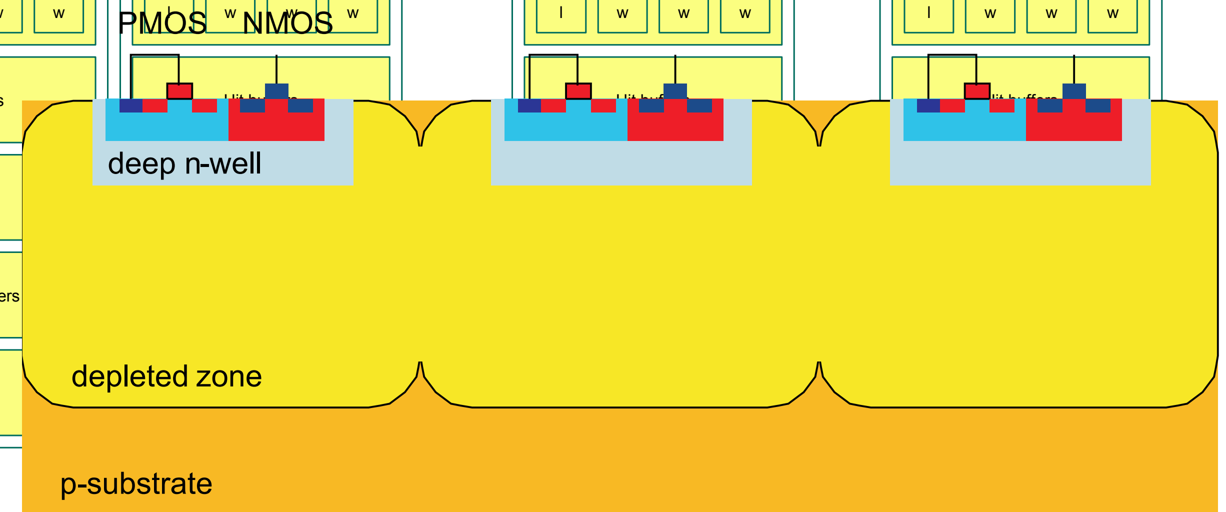
Alice: 0.8% X0/layer for outer barrel

Table 4.2: Estimated contributions of the Outer Layer Stave to the material budget.

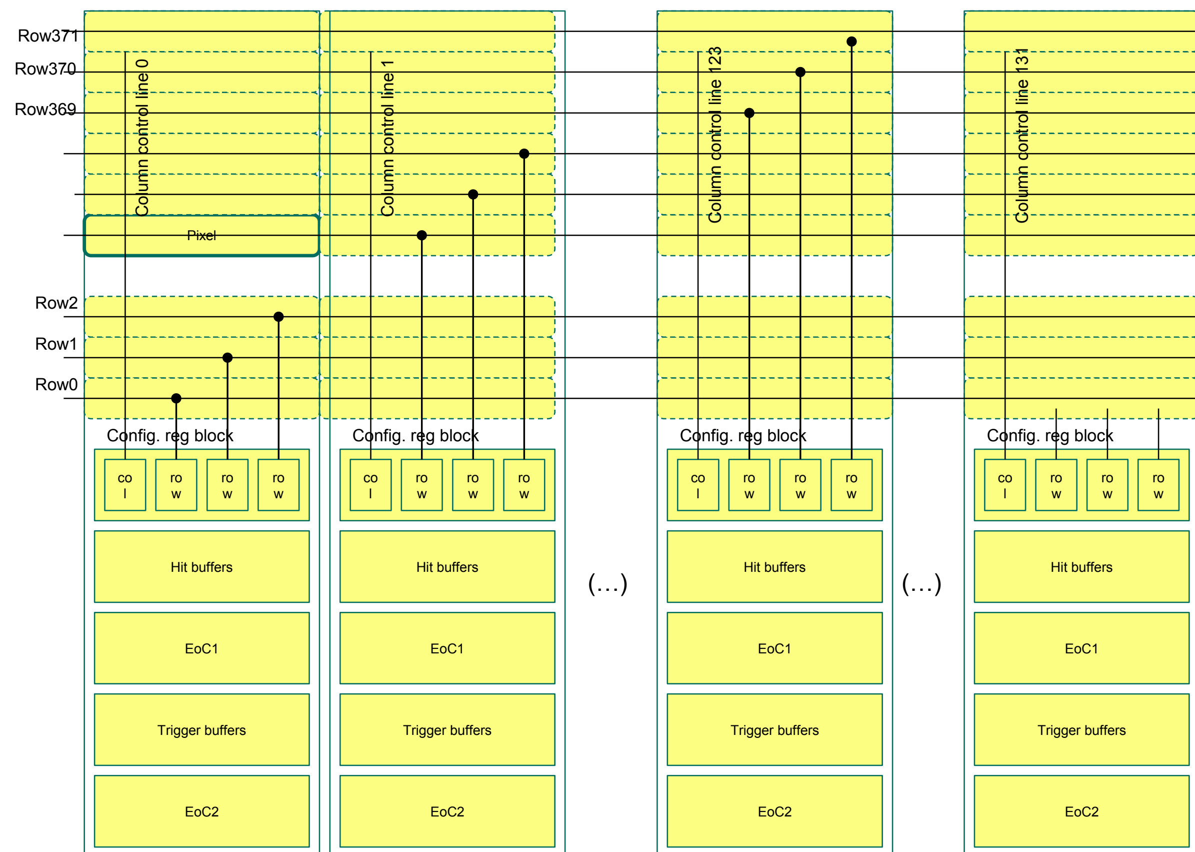
Stave element	Component	Material	Thickness (μm)	X_0 (cm)	X_0 (%)
Module	FPC Metal layers	Aluminium	50	8.896	0.056
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Module plate	Carbon fibre	120	26.08	0.046
	Pixel Chip	Silicon	50	9.369	0.053
	Glue	Eccobond 45	100	44.37	0.023
Power Bus	Metal layers	Aluminium	200	8.896	0.225
	Insulating layers	Polyimide	200	28.41	0.070
	Glue	Eccobond 45	100	44.37	0.023
Cold Plate		Carbon fleece	40	106.80	0.004
		Carbon paper	30	26.56	0.011
	Cooling tube wall	Polyimide	64	28.41	0.013
	Cooling fluid	Water		35.76	0.105
	Carbon plate	Carbon fibre	120	26.08	0.046
	Glue	Eccobond 45	100	44.37	0.023
Space Frame		Carbon rowing			0.080
Total					**0.813**

ATLASPix3: Column and Pixel S

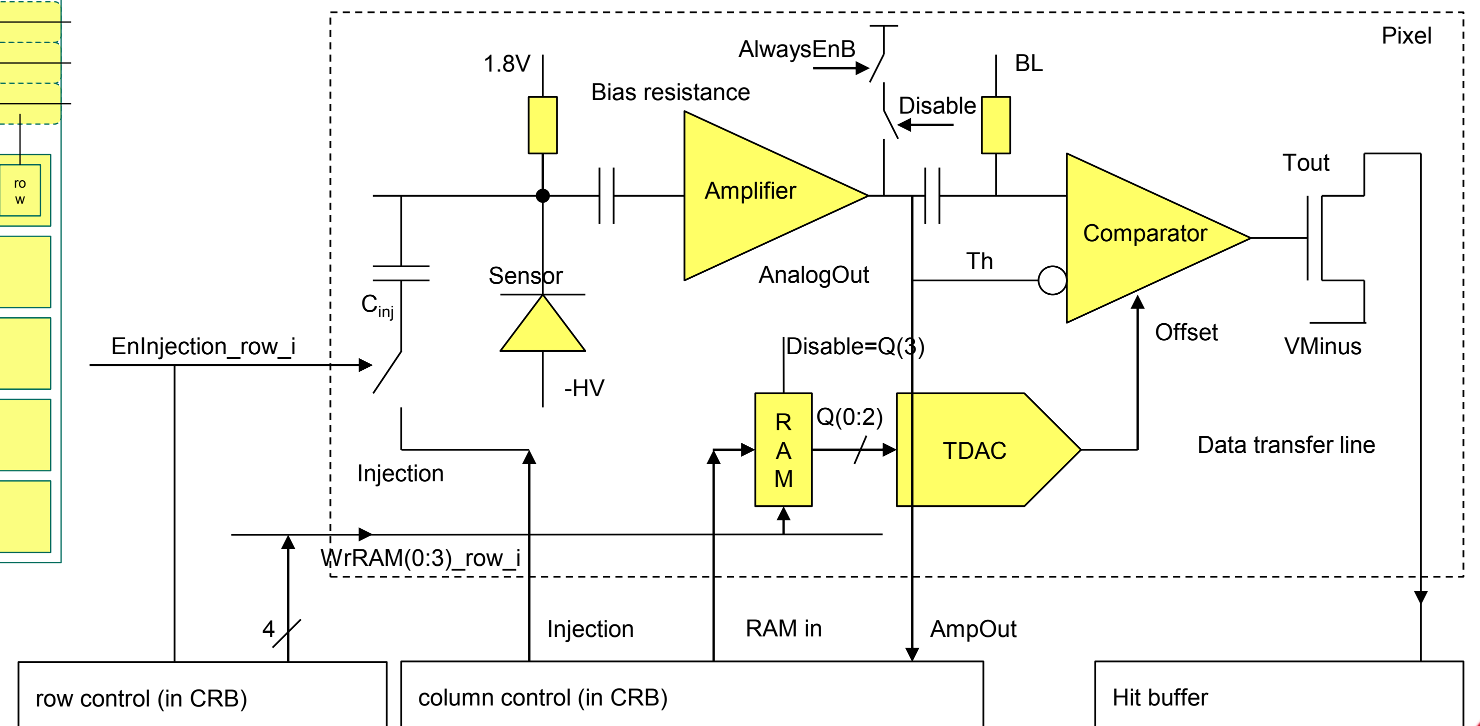
HV-CMOS structure



Block scheme of the pixel matrix and column circ



Pixel Schematics



ATLASPix3: Threshold and Noise Measurements

Physics | Lancaster University

Example Noise vs Threshold distribution: